Protection Design

Over Current Protection (OCP)

The IRS2092(S) features over current protection to protect the power MOSFETs during abnormal load conditions. The IRS2092(S) starts a sequence of events when it detects an over current condition during either high side or low side turn on of a pulse. As soon as either the high side or low side current sensing block detects over current:

1. The OC Latch (OCL) flips logic states and shutdowns the outputs LO and HO.
2. The CSD pin starts discharging the external capacitor Ct.
3. When V_{CSD}, the voltage across Ct, falls below the lower threshold Vth2, an output signal from COMP2 resets OCL.
4. The CSD pin starts charging the external capacitor Ct.
5. When V_{CSD} goes above the upper threshold Vth1, the logic on COMP1 flips and the IC resumes operation.

As long as the over current condition exists, the IC will repeat the over current protection sequence at a repetition rate dependent upon capacitance in CSD pin.

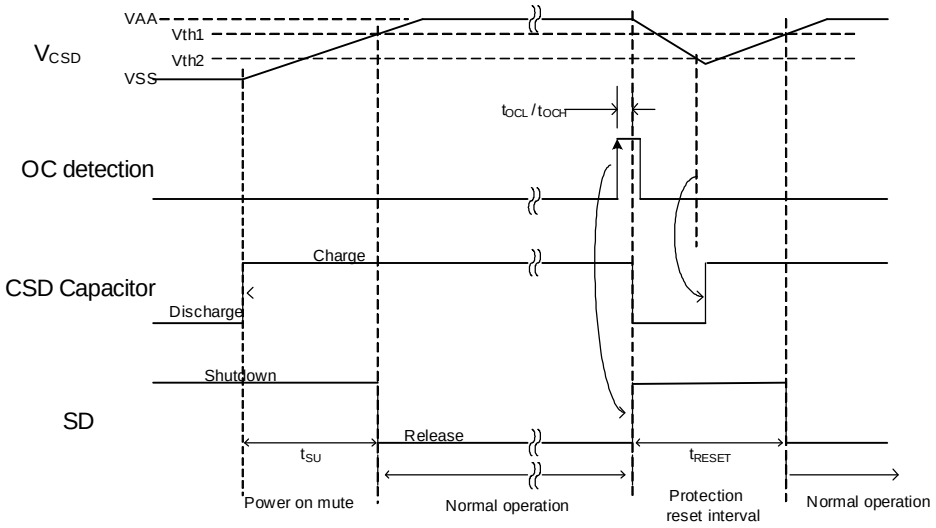

Figure 7 Over Current Protection Timing Chart

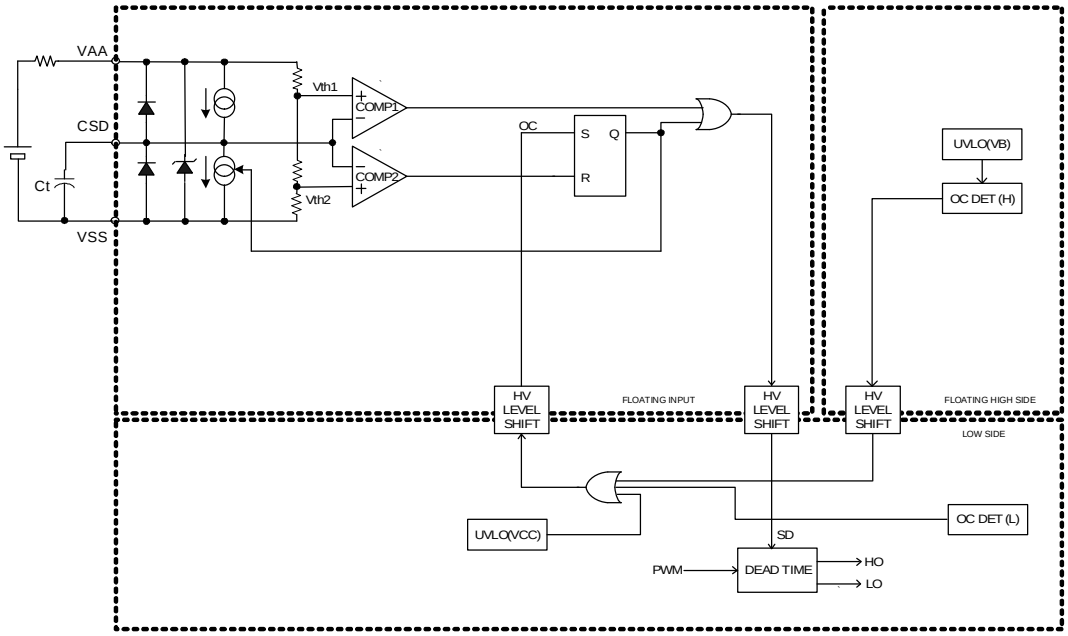

Figure 8 Shutdown Functional Block Diagram

Protection Control

The internal protection control block dictates the operational mode, normal or shutdown, using the input of the CSD pin. In shutdown mode, the IC forces LO and HO to output 0V with respect to COM and VS respectively to turn off the power MOSFETs.

The CSD pin provides five functions.

1. Power up delay timer
2. Self-reset timer
3. Shutdown input
4. Latched protection configuration
5. Shutdown status output (host I/F)

The CSD pin cannot be paralleled with other IRS2092(S).

Self Reset Protection

By putting a capacitor between CSD and V_{SS}, the IRS2092(S) resets itself after entering shutdown mode.

After the OCP event, CSD pin discharges Ct voltage V_{CSD} down to the lower threshold V_{th2} to reset the internal shutdown latch. Then, the IRS2092(S) begins to charge Ct in an attempt to resume operation. Once the voltage of the CSD pin rises above the upper threshold, V_{th1}, the IC resumes normal operation.

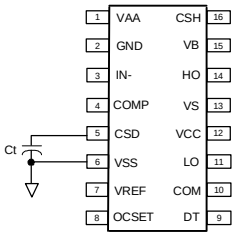

Figure 9 Self Reset Protection Configuration

Designing Ct

The timing capacitor, Ct, is used to program t_{RESET} and t_{SU}.

- t_{RESET} is the amount of time that elapses from when the IC enters shutdown mode to the time when the IC resumes operation. t_{RESET} should be long enough to avoid over heating the MOSFETs from the repetitive sequence of shutting down and resuming operation during over current conditions. In most of the applications, the minimum recommended time for t_{RESET} is 0.1 second.
- t_{SU} is the amount of time between powering up the IC in shutdown mode to the moment the IC releases shutdown to begin normal operation.

The Ct determines t_{RESET} and t_{SU} as following equations:

$$t_{RESET} = \frac{Ct \cdot V_{DD}}{1.1 \cdot I_{CSD}} \quad [s]$$

$$t_{SU} = \frac{Ct \cdot V_{DD}}{0.7 \cdot I_{CSD}} \quad [s]$$

where I_{CSD} = the charge/discharge current at the CSD pin

V_{DD} = the floating input supply voltage with respect to V_{SS}.

Shutdown Input

The IRS2092(S) can be shut down by an external shutdown signal SD. Figure 10 shows how to add an external discharging path to shutdown the PWM.

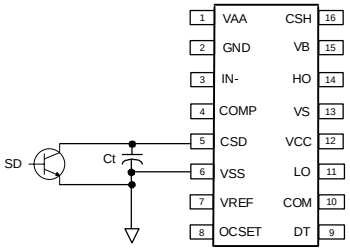

Figure 10 Shutdown Input

Latched Protection

Connecting CSD to V_{DD} through a 10k Ω or less resistor configures the over current protection latch. The latch locks the IC in shutdown mode after over current is detected. An external reset switch can be used to bring CSD below the lower threshold Vth2 for a minimum of 200ns to properly reset the latch. After the power up sequence, a reset signal to the CSD pin is required to release the IC from the latched shutdown mode.

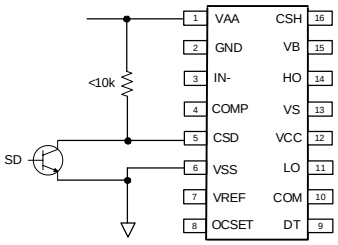

Figure 11 Latched Protection with Reset Input

Interfacing with System Controller

The IRS2092(S) can communicate with an external system controller through a simple interfacing circuit shown in Figure 12. A generic PNP transistor U1 detects the sink current at the CSD pin during an OCP event and outputs a shutdown signal to an external system controller. Another generic NPN transistor U2 can then reset the internal protection logic by pulling the CSD voltage below the lower threshold Vth2 for a minimum of 200ns. Note that the CSD pin is configured to operate in latched OCP. After the power up sequence, a reset signal to the CSD pin is required to release the IC from shutdown mode.

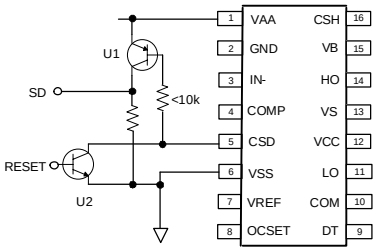

Figure 12 Interfacing with Host Controller

Programming OCP Trip Level

In a Class D audio amplifier, the direction of the load current alternates with the audio input signal. An over-current condition can therefore occur during either a positive current cycle or a negative current cycle. The IRS2092(S) uses the $R_{DS(on)}$ of the output MOSFETs as current sensing resistors. Due to the structural constraints of high voltage ICs, current sensing is implemented differently for the high side and low side. If the measured current exceeds a predetermined threshold, the OCP block outputs a signal to the protection block, forcing HO and LO low and protecting the MOSFETs.

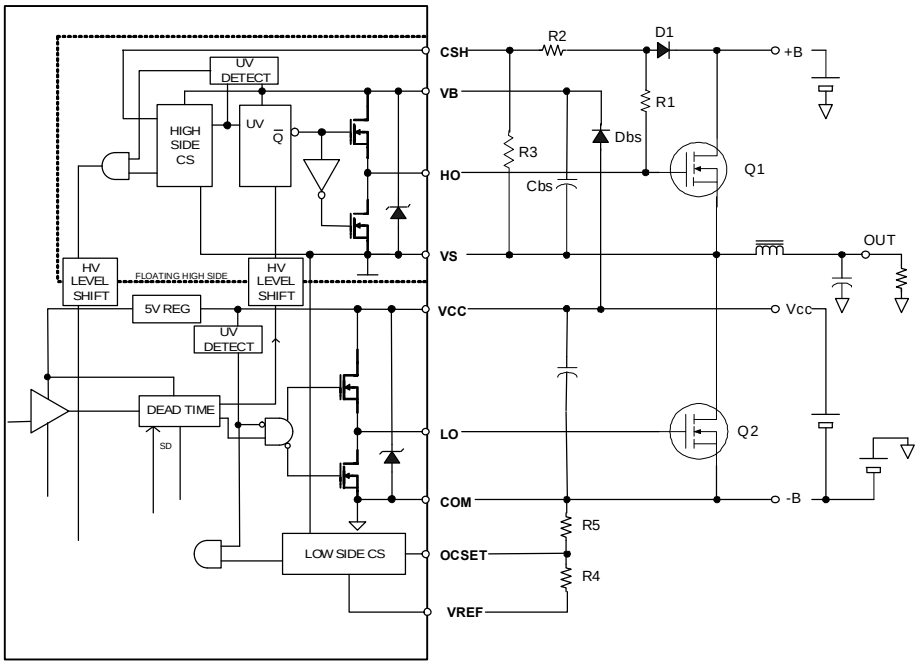

Figure 13 Bi-directional Over Current Protection

Low Side Over Current Sensing

For negative load currents, low side over current sensing monitors the load condition and shuts down switching operation if the load current exceeds the preset trip level.

Low side current sensing is based on the measurement of V_{DS} across the low side MOFET during low side on state. In order to avoid triggering OCP from overshoot, a blanking interval inserted after LO turn on disables over current detection for 450ns.

The OCSET pin is to program the threshold for low side over current sensing. When the V_{DS} measured of the low side MOSFET exceeds the voltage at the OCSET pin with respect COM, the IRS2092(S) begins the OCP sequence described earlier.

Note that programmable OCSET range is 0.5V to 5.0V. To disable low side OCP, connect OCSET to VCC directly.

To program the trip level for over current, the voltage at OCSET can be calculated using the equation below.

$$V_{OCSET} = V_{DS(LOW\ SIDE)} = I_{TRIP+} \times R_{DS(on)}$$

In order to minimize the effect of the input bias current at the OCSET pin, select resistor values for R4 and R5 such that the current through the voltage divider is 0.5mA or more.

* Note: Using V_{REF} to generate an input to OCSET through a resistive divider provides improved immunity from fluctuations in V_{CC}.

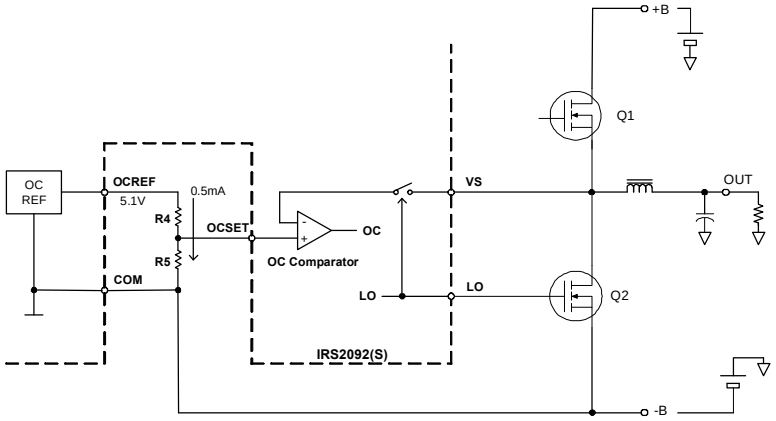

Figure 14 Low Side Over Current Sensing

Low Side Over Current Setting

Let the low side MOSFET has $R_{DS(on)}$ of 100mΩ. We wish to set the current trip level at 30A.
V_{OCSET} is given by:

$V_{OCSET} = I_{TRIP+} \times R_{DS(on)} = 30A \times 100m\Omega = 3.0V$

Choose R4+R5=10 kΩ to properly load the VREF pin.

$$R_5 = \frac{V_{OCSET}}{V_{REF}} \cdot 10k\Omega$$
$$= \frac{3.0V}{5.1V} \cdot 10k\Omega$$
$$= 5.8k\Omega$$

where $V_{REF} = 5.1V$

Based on the E-12 series of resistor values, choose R5 to be 5.6kΩ and R4 to be 3.9kΩ to complete the design.

In general, $R_{DS(on)}$ has a positive temperature coefficient that needs to be considered when setting the threshold level. Also, variations in $R_{DS(on)}$ will affect the selection of external or internal component values.

High Side Over-Current Sensing

For positive load currents, high side over current sensing also monitors the load condition and shuts down switching operation if the load current exceeds the preset trip level.

High side current sensing is based on the measurement of V_{DS} across the high side MOSFET during high side turn on through pins CSH and Vs. In order to avoid triggering OCP from overshoot, a blanking interval inserted after HO turn on disables over current detection for 450ns.

In contrast to low side current sensing, the threshold at which the CSH pin engages OC protection is internally fixed at 1.2V. An external resistive divider R2 and R3 can be used to program a higher threshold.

An external reverse blocking diode, D1, is required to block high voltages from feeding into the CSH pin while the high side is off. Due to a forward voltage drop of 0.6V across D1, the minimum threshold required for high side over current protection is 0.6V.

$$V_{CSH} = \frac{R3}{R2+R3} \cdot \left(V_{DS(HIGHSIDE)} + V_{F(D1)}\right)$$

where $V_{DS(HIGH\ SIDE)}$ = the drain to source voltage of the high side MOSFET during high side turn on
$V_{F(D1)}$ = the forward drop voltage of D1

Since $V_{DS(HIGH\ SIDE)}$ is determined by the product of drain current I_D and $R_{DS(on)}$ of the high side MOSFET. V_{CSH} can be rewritten as:

$$V_{CSH} = \frac{R3}{R2+R3} \cdot \left(R_{DS(ON)} \cdot I_D + V_{F(D1)}\right)$$

The reverse blocking diode D1 is forward biased by a 10kΩ resistor R1.

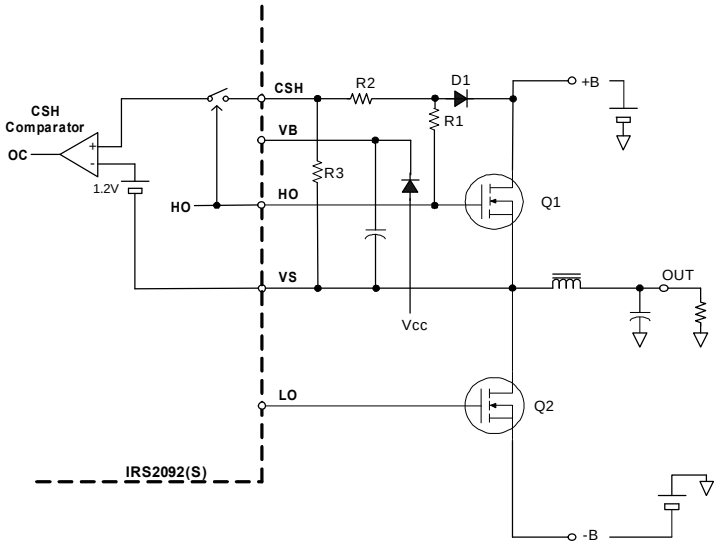

Figure 15 Programming High Side Over Current Threshold

High Side Over Current Setting

Figure 15 demonstrates the typical circuitry used for high side current sensing. In the following example, the over current protection level is set to trip at 30A using a MOSFET with an $R_{DS(on)}$ of 100mΩ. The component values of R2 and R3 can be calculated using the following formula:

Let R2 + R3=10 kΩ.

$$R_3 = 10k\Omega \cdot \frac{Vth_{OCH}}{V_{DS} + V_F}$$

where Vth_{OCL} = 1.2V

V_F = the forward voltage of reverse blocking diode D1 = 0.6V.

$V_{DS@ID=30A}$ = the voltage drop across the high side MOSFET when the MOSFET current is 30A.

Therefore, $V_{DS@ID=30A} = I_D \times R_{DS(on)}$ = 30A x 100mΩ = 3V

Based on the formulas above, R2 = 6.8kΩ and R3 = 3.3kΩ.

Choosing the Correct Right Reverse Blocking Diode

The selection of the appropriate reverse blocking diode D1 depends on its voltage rating and speed. To effectively block bus voltages, the reverse voltage must be higher than the voltage difference between +B and –B and the reverse recovery time must be as fast as the boot strap charging diode. A diode such as the Philips BAV21W, a 200V, 50ns high speed switching diode, is more than sufficient.

Dead-Time Generator

Dead-time is the blanking period inserted between either high-side Turn-OFF and low-side Turn-ON, or low-side Turn-OFF and high-side Turn-ON. Its purpose is to prevent shoot through, or a rush of current through both MOSFETs. In the IRS2092(S), an internal dead-time generation block allows the user to select the optimum dead time from a range of preset values. Selecting a preset dead-time through the DT/SD pin voltage can easily be done through an external voltage divider. This way of setting dead-time prevents outside noise from modulating the switching timing, which is critical to the audio performance.

How to Determine Optimal Dead-Time

The effective dead-time in an actual application differs from the dead-time specified in this datasheet due to the switching fall time, tf. The dead-time value in this datasheet is defined as the time period between the beginning of turn-off on one side of the switching stage and the beginning of turn-on on the other side as shown in Figure 16. The fall time of the MOSFET gate voltage must be subtracted from the dead-time value in the datasheet to determine the effective dead-time of a Class D audio amplifier.

(Effective dead-time) = (Dead-time in datasheet) – tf

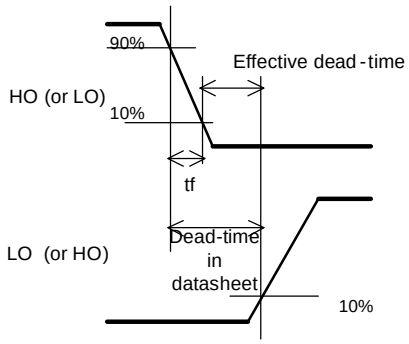

Figure 16 Effective Dead Time

A longer dead-time period is required for a MOSFET with a larger gate charge value because of the longer tf. Although a shorter effective dead-time setting is beneficial to achieving better linearity in Class D amplifiers, the likelihood of shoot-through current increases with narrower dead-time settings. Negative values of effective dead-time may cause excessive heat dissipation in the MOSFETs, leading to potentially serious damage.

To calculate the optimal dead-time in a given application, the fall time tf for both HO and LO in the actual circuit need to be taken into account. In addition, variations in temperature and device parameters could also affect the effective dead-time in the actual circuit. Therefore, a minimum effective dead-time of 10ns is recommended to avoid shoot-through current over the range of operating temperatures and supply voltages.

Programming Dead-Time

The IRS2092(S) selects the dead-time from a range of preset dead-time values based on the voltage applied at the DT pin. An internal comparator translates the DT input to a predetermined dead-time by comparing the input with internal reference voltages. These internal reference voltages are set in the IC through a resistive voltage divider using $V_{CC.}$ The relationship between the operation mode and the voltage at DT pin is illustrated in the Figure17 below.

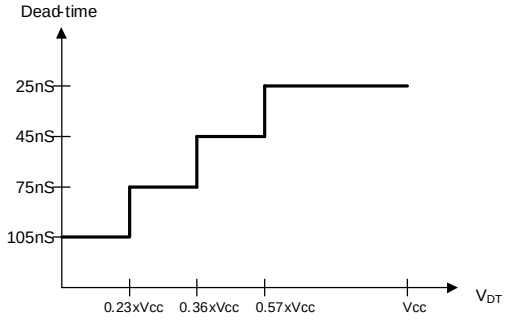

Figure 17 Dead Time vs. V_{DT}

Table 3 suggests pairs of resistor values used in the voltage divider for selecting dead-time. Resistors with up to 5% tolerance are acceptable when using these values.

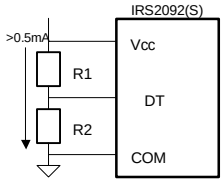

Figure 18 External Voltage Divider

Dead-time Mode	R1	R2	DT/SD Voltage
DT1	<10k	Open	Vcc
DT2	5.6kΩ	4.7kΩ	0.46 x Vcc
DT3	8.2kΩ	3.3kΩ	0.29 x Vcc
DT4	Open	<10k	COM

Table 3 Recommended Resistor Values for Dead Time Selection

Supplying V_{AA} and V_{SS}

There are two ways to implement power supplies V_{AA} and V_{SS}.

1. Supplying V_{AA} and V_{SS} with External Regulators

For best audio performance, it is preferred to produce V_{AA} and V_{SS} with external regulators, such as the three terminal regulators. To keep internal clamping zener diodes from conducting, the supply voltage should be $V_{AA} < V_{CLAMPM+}$ and $V_{SS} > V_{CLAMPM-}$. Standard 7805 and 7905 regulators are suitable.

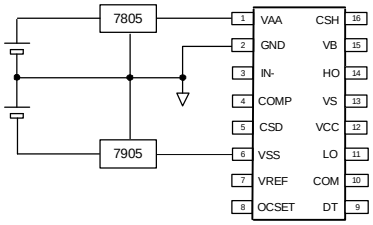

Figure 19 Supplying V_{AA} and V_{SS} with External Regulators

When switched mode regulators provide V_{AA} and V_{SS}, it is required to place a two stage noise filter in the supply lines as shown in Figure 20 to prevent noise from influencing the switching ripple voltage on +/-5V.

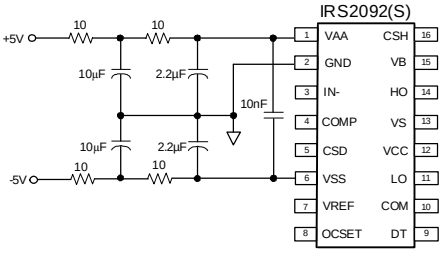

Figure 20 Supplying V_{AA} and V_{SS} from Switched Mode Power Supply

2. Regulating V_{AA} and V_{SS} Using Internal Zener Diodes

V_{AA} and V_{SS} can be supplied with an internal zener diode clamp as a shunt regulator. Recommended I_{AA} and I_{SS}, the supply current for V_{AA} and V_{SS}, is 10mA.
This implementation is suggested when the main bus voltages, +B and –B, are supplied from a regulated power supply.

Set R_{AA} and R_{SS} values in Figure 21 such that the supply currents feeding into V_{AA} and V_{SS} are each 10mA.

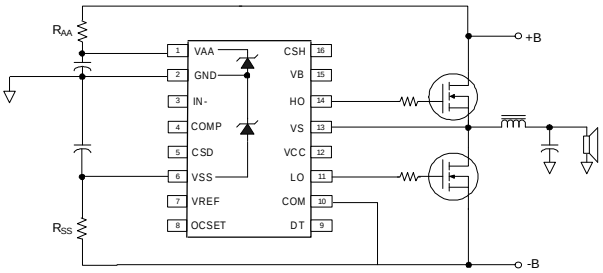

Figure 21 Regulating V_{AA} and V_{SS} with Internal Zener Diodes

Charging V_{BS} Prior to Start

For proper start-up, the high side bootstrap capacitor is required to be charged prior to PWM start-up through a resistor R_{CHARGE} from the positive supply bus to the V_B pin. By utilizing an internal 20.8V zener diode between V_B and V_S, this scheme eliminates the need to charge the boot strap capacitor through low side turn on during start up.

The value of this charging resistor is subject to several constraints:

- The minimum resistance of R_{CHARGE} is limited by the maximum PWM modulation index of the system. When HO is high, R_{CHARGE} drains bootstrap power supply so it reduces holding up time, hence maximum continuous HO on time.
- The maximum resistance of R_{CHARGE} is limited by the current charge capability of the resistor during startup:

$$I_{CHARGE} > I_{QBS}$$

where I_{CHARGE} = the current through R_{CHARGE}
I_{QBS} = the high side supply quiescent current.

I_{CHARGE} generates a DC offset at the speaker output prior to PWM start up. Check that the DC offset does not exceed a condition for click noise elimination. See Click Noise Elimination section for more detail.

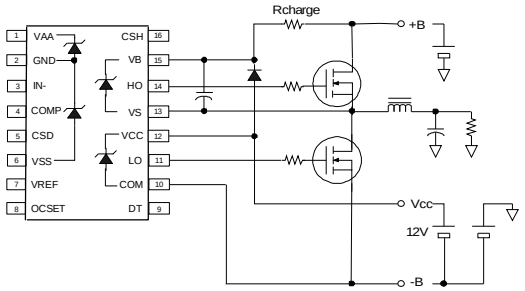

Figure 22 Boot Strap Supply Pre-charging

Start-up Sequence (UVLO)

The protection control block in the IRS2092(S) monitors the status of V_{AA} and V_{CC} to ensure that both voltage supplies are above their respective UVLO (Under Voltage Lock Out) thresholds before beginning normal operation. If either V_{AA} or V_{CC} is below the under voltage threshold, LO and HO are disabled in shutdown mode until both V_{AA} and V_{CC} rise above their voltage thresholds.

Power-down Sequence

As soon as V_{AA} or V_{CC} falls below its UVLO threshold, protection logic in the IRS2092(S) turns off LO and HO, shutting off the power MOSFETs.

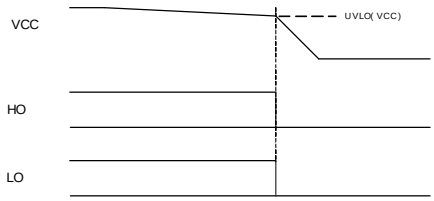

Figure 23 IRS2092(S) UVLO Timing Chart

Power Supply Decoupling

Careful attention must be given to decoupling the power supplies for proper operation of the IC. Ceramic capacitors of 0.1µF or more should be placed close to the power supply pins of the IC on the board.

Please refer to the application note AN-978 for general design considerations of a high voltage gate driver IC.

V_{SS} Negative Bias Clamping

An excessive negative Vss voltage with respect to COM could damage the IRS2092(S). V_{SS} can go below COM when a negative supply is missing in a dual supply configuration. To protect the IC from this possibility, a diode is recommended for clamping potential negative biases to V_{SS}. A standard recovery diode with a current rating of 1A such as the 1N4002 is sufficient for this purpose.

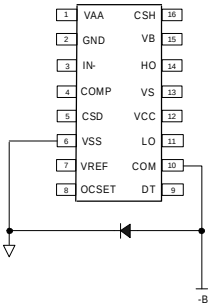

Figure 24 Negative V_{SS} Clamping

Junction Temperature Estimation

The power dissipation in the IRS2092(S) is dominated by the following items:

- P_{MID}: Power dissipation of the input floating logic and protection circuitry
- P_{LSM}: Power dissipation of the Input Level Shifter
- P_{LOW}: Power dissipation in low side
- P_{LSH}: Power dissipation of the High-side Level Shifter
- P_{HIGH}: Power dissipation in high side

The following equations are for your reference only. Because of the non-linear characteristics in gate drive stage, these assumptions may not be accurate.

1. P_{MID}: Power Dissipation of the Input Floating Logic and Protection Circuitry

The power dissipation of the input floating section is given by:

$$P_{MID} = P_{ZENER} + P_{OTA}$$

Where

P_{ZENER} = the power dissipation from the internal zener diodes clamping V_{AA} and V_{SS}

P_{OTA} = the power dissipation from the internal OTA

When V_{AA} and V_{SS} are regulated with internal zener diode clamping, P_{MID} can be simplified as:

$$P_{MID} \approx (V_{AA} - V_{SS}) \cdot \frac{(V_{+BUS} - V_{AA}) + (V_{SS} - V_{-BUS})}{R_{AA} + R_{SS}}$$

Where

V_{+BUS} = positive bus voltage feeding V_{AA}
V_{-BUS} = negative bus voltage feeding V_{SS}
R_{AA} = resistor feeding V_{AA} from V_{+BUS}
R_{SS} = resistor feeding V_{SS} from V_{-BUS}

See Figure 21.

2. P_{LSM}: Power Dissipation of the Input Level Shifter

$P_{LSM} = 1.5 \times 10^{-9} \times f_{SW} \times V_{SS\ BIAS}$

Where

f_{SW} = the PWM switching frequency
$V_{SS\ BIAS}$ = the bias voltage of V_{SS} with respect to COM

3. P_{LOW}: Power Dissipation of Low Side

The power dissipation of the low side comes from the losses of the logic circuitry and the losses of driving LO.

$$P_{LOW} = P_{LDD} + P_{LO}$$

$$= (I_{QCC} \cdot V_{CC}) + \left(Vcc \cdot Q_g \cdot f_{SW} \cdot \frac{R_O}{R_O + R_g + R_{g(\text{int})}} \right)$$

Where

P_{LDD} = power dissipation of the internal logic circuitry

P_{LO} = power dissipation from of gate drive stage for LO

R_O = output impedance of LO, typically 10 Ω for the IRS2092(S)

$R_{g(int)}$ = internal gate resistance of the low side MOSFET, typically 2Ω

R_g = external gate resistance of the low side MOSFET

Qg = total gate charge of the low side MOSFET

4. P_{LSH}: Power Dissipation of the High-side Level Shifter

$P_{LSH} = 0.4nC \times fsw \times V_{BUS}$

Where

f_{SW} = PWM switching frequency
V_{BUS} = difference between the positive bus voltage and negative bus voltage

5. P_{HIGH}: Power Dissipation of High Side

The power dissipation of the high side comes from the losses of the logic circuitry and the losses of driving HO.

$$P_{HIGH} = P_{LDD} + P_{HO}$$

$$= (I_{QBS} \cdot V_{BS}) + \left(V_{BS} \cdot Q_g \cdot f_{SW} \cdot \frac{R_O}{R_O + R_g + R_{g(\text{int})}} \right)$$

Where

P_{LDD} = power dissipation of the internal logic circuitry

P_{HO} = power dissipation of the gate drive stage for HO

R_O = equivalent output impedance of HO, typically 10 Ω for the IRS2092(S)

$R_{g(int)}$ = the internal gate resistance of the high side MOSFET, typically 2Ω

R_g = external gate resistance of the high side MOSFET

Qg = total gate charge of the high side MOSFET

6. **P_D: Total Power Dissipation**

Total power dissipation, P_D, is given by

$$P_D = P_{MID} + P_{LSM} + P_{LOW} + P_{HSM} + P_{HIGH}.$$

7. **Tj: Junction Temperature**

Given junction to ambient thermal resistance Rth_{JA}, the junction temperature Tj can be calculated from the formula provided below and must not exceed 150°C.

$$T_J = Rth_{JA} \cdot P_d + T_A < 150°C$$

Board Layout Considerations

The floating input section of the IRS2092(S) consists of a low noise OTA error amplifier and a PWM comparator along with CMOS logic circuitry. High frequency bypass capacitor $C_{VAA-VSS}$ should be placed closest to the IRS2092(S) to supply the logic circuitry. C_{VAA} and C_{VSS} are for stable operation of the OTA and should be placed close to the IC. Gate driver supply capacitors C_{VCC} and C_{VBS} provide gate charging current and should also be placed close to the IRS2092(S).

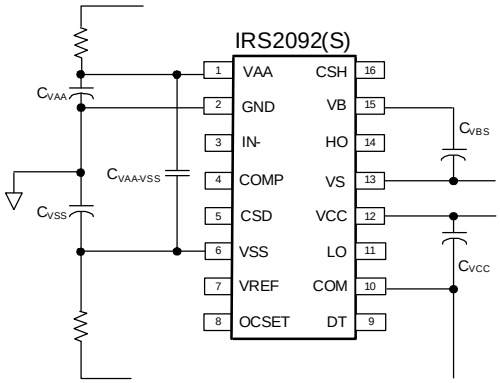

Figure 25 Placement Sensitive Bypass Capacitors

Ground Plane

In addition to the key component locations mentioned above, it is important to properly pour ground planes to obtain good audio performance. The IRS2092(S) does not accept single ground plane design because the integration of circuitries within the IC is referenced to different potentials. Proper application of the IRS2092(S) employs three reference potentials.

1. Analog Ground

The Input analog section around the OTA is referenced to the signal ground, or GND, which should be a quiet reference node for the audio input signal. The peripheral circuits in the floating input section such as CSD and COM pins refer to this ground. These nodes should all be separate from the switching stages of the system. In order to prevent potential capacitive coupling to the switching nodes, use a ground plane only in this part of the circuit. Do not share the ground plane with gate driver or power stages.

2. Gate Driver Reference

The gate driver stage of the IRS2092(S) is located between pins 10 and 15 and is referenced to the negative bus voltage, COM. This is the substrate of the IC and acts as ground. Although the negative bus is a noisy node in the system, both of the gate drivers refer to this node. Therefore, it is important to shield the gate drive stages with the negative bus voltage so that all the noise currents due to stray capacitances flow back to the power supply without degrading signal ground.

3. Power Ground

Power ground is the ground connection that closes the loops of the bus capacitors and inductor ripple current circuits. Separate the power ground and input signal grounds from each other as much as possible to avoid common stray impedances.

Figure 26 illustrates how to paint out reference planes. Power GND plane should include negative bus cap. Power reference plane should include Vcc. Also, Use distinctly different symbols for the different grounds.

For further board layout information, refer to AN-1135, PCB Layout with IR Class D Audio Gate Drivers

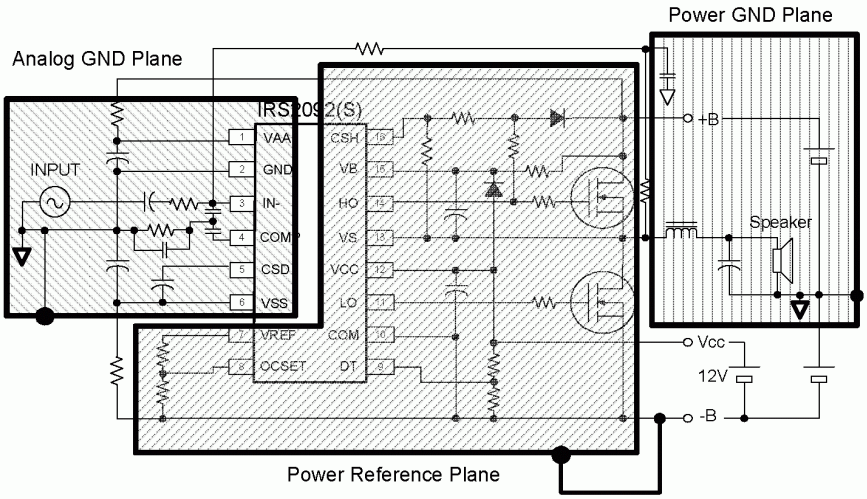

Figure 26 Applying Ground Planes