International
IOR Rectifier

APPLICATION NOTE

Application Note AN-1137

Power QFN® Technology Inspection Application Note

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The Discrete Power QFN is an efficient device with a wide range of input voltage in a small 5x6mm QFN package. This package is offered only as Lead-Free (PbF), identified by a PbF suffix after the part number (for example, IRFH7932TRPbF). The main text of this application note contains guidance applicable to Discrete Power QFN package. In Appendix A, there are device outlines, substrate layouts and stencil designs for Discrete Power QFN. To simplify board mounting and improve reliability, International Rectifier manufactures Power QFN devices to exacting standards. These high standards have evolved through evaluating many different materials and designs. Although such evaluations have yielded good results, the recommendations in this application note may need to be adjusted to suit specific production environments.

Introduction

Power QFN® is a surface mount semiconductor technology designed primarily for board-mounted power applications. It eliminates unnecessary elements of packaging that contribute to higher inductance and resistance, both thermal and electrical, so that its power capabilities exceed those of comparably sized packages.

*Figures **1*** and ***2*** show this construction.

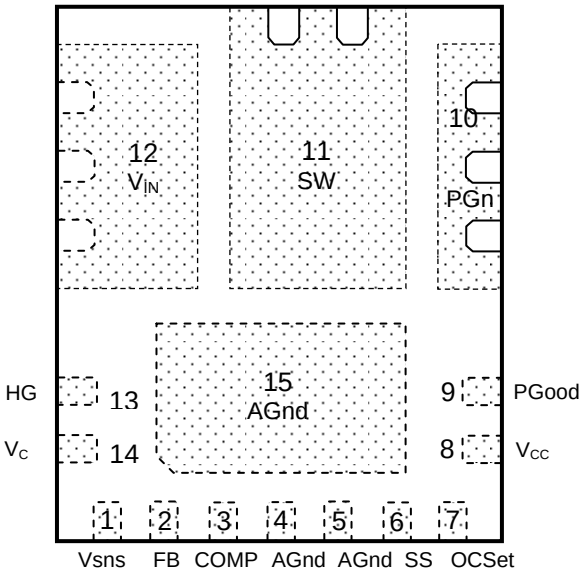

*Figure **1** Power QFN MCM contact configuration*

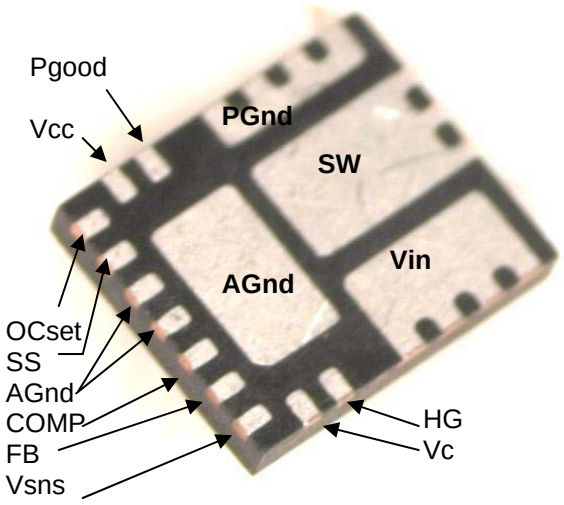

*Figure **2** Bottom view of Power QFN device*

This unique design means that inspection criteria for Power QFN devices may differ from more conventional surface mounted devices (SMDs). This application note explains the methods available for inspecting the quality of solder joints between device and PCB. Application note AN-1136 describes the methods and practices required to board-mount Power QFN devices, and the interactions that may occur with commonly used materials.

Inspection techniques

Background

Most of the connections on a Power QFN device are external, conventionally filleted solder joints (*Figure **3***). This means that they can be inspected visually, as with a conventional SMD, in accordance with industry standards (for example, IPC-A-610).

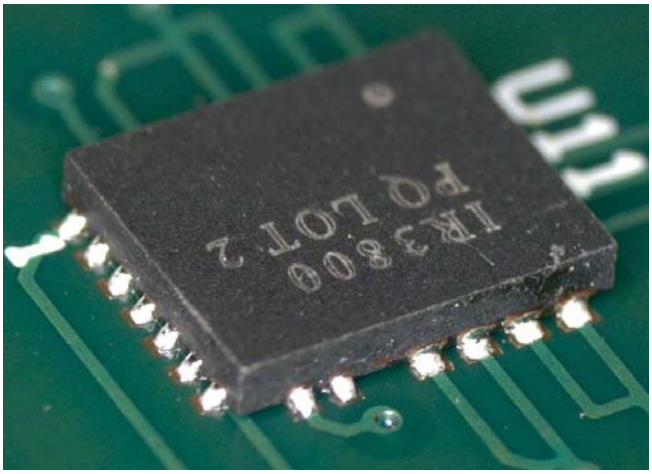

*Figure **3** External solder fillets on the drain*

Optical inspection can also detect several possible assembly issues, including devices that are twisted, rotated, tilted, and both twisted and tilted at once.

However, as the Switch Node and Analog Ground are within the outline of a Power QFN device, other inspection techniques are needed to inspect them with confidence. The most effective is X-ray microscopy.

An additional option to X-ray is endoscopes. This equipment, which is a small-scale camera primarily used for inspection of solder connections under Ball Grid Array (BGA) devices, can also be used to inspect the internal solder joints of a Power QFN device.

X-ray inspection

Many manufacturers offer X-ray equipment, which may be batch or in-line, 2D or 3D.

It is unusual to inspect a whole production run using X-ray. It is more common to use this technique when setting up a process or product, and on samples taken from production runs.

Examples of good assembly

*Figures **4*** to ***6*** show well-mounted Power QFN devices.

*Figure **4** Self-centered with good solder fillets*

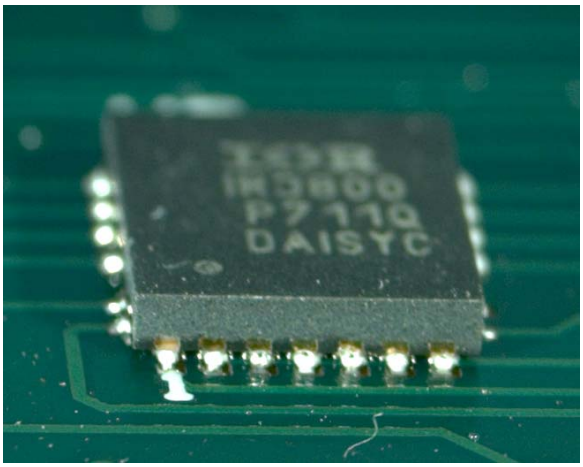

*Figure **5** Device mounted parallel to PCB*

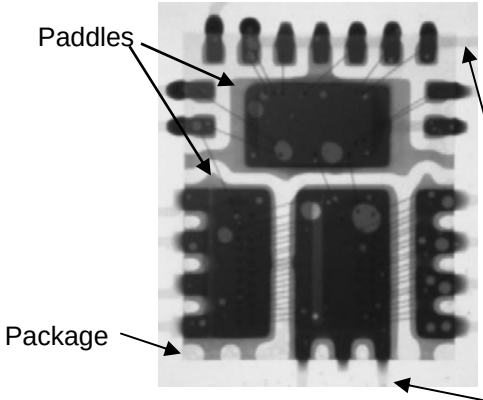

*Figure **6** Features revealed by an X-ray*

Summary of rejection criteria

The remaining sections of this application note explain the types of problems that can arise when board-mounting Power QFN devices. In each case, criteria are given on which to base the decision whether to accept or reject a device. The table below summarizes these criteria and gives the number of the page on which you will find more information. As with all solder joints, a major factor in the success of joints on a Power QFN device is the applied solder volume. Too little solder may result in voided joints (or open circuits, in extreme cases) and too much solder may result in solder balling (or short circuits, in extreme cases).

Observation	Reject any device that has:	Page
Twisted device	A gate or source pad with less than 75% solder coverage	4
	A drain pad with less than 50% solder coverage	
Rotated device	Been turned through 180^{o}	5
Tilted device	A gate or source pad with less than 75% solder coverage	5
	A drain pad with less than 50% solder coverage	
	Been tilted by more than 3^{o} relative to the PCB	
Twisted and tilted device	A gate or source pad with less than 75% solder coverage	5
	A drain pad with less than 50% solder coverage	
	Been tilted by more than 3^{o} relative to the PCB	
Solder voiding	A solder joint with less than 75% coverage of the pad on the PCB	6
Solder balling	A solder ball between the gate pad and the nearest drain pad	7
	A solder ball causing an electrical short	
Poorly formed joints	A solder joint with less than 75% coverage of the pad on the PCB	8
	A missing or open solder joint	8
	A solder bridge linking electrically isolated points of the circuit (for example, between gate and drain pads not two drain pads)	9

Note: Some of the problems shown in this document were deliberately created for illustrative purposes. They do not commonly arise in practice.

Types of faults

Twisted device

This describes a device that is mounted crookedly on the pads, as shown in *Figure **7***. The device is clearly twisted, but external solder fillets are still visible on all four contacts. The X-ray shows good solder joints on the switch and analog ground contacts.

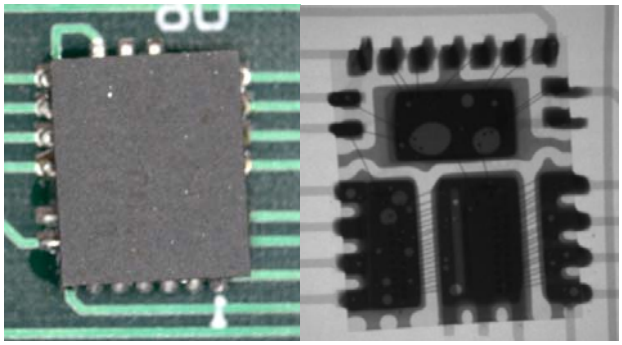

*Figure **7** Twisted device*

Reject twisted devices if one of the following is true:

- Any of pins 1-9 or 13,14 are shorted to the wrong land.
- There is less than 75% coverage on any pin 10-12 contact

Rotated device

This describes a device that is mounted the wrong way around, as shown in *Figure **8***. Although some external solder fillets on the drain contacts appear good, visual inspection and X-ray inspection reveals the problems with many of the contacts.

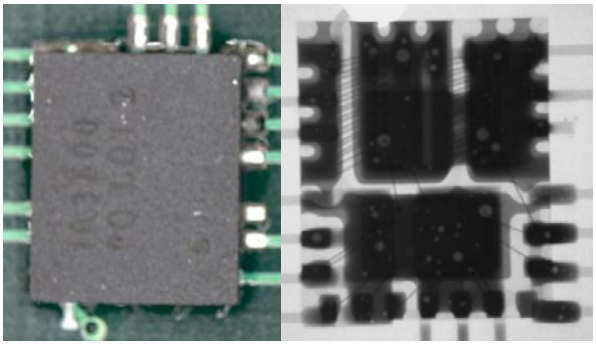

*Figure **8** Rotated device*

Reject all rotated devices.

Tilted device

This describes a device that is not parallel to the PCB. *Figure **9*** shows an example. Although the device is self-centered, visual inspection from above reveals more solder on the large contacts (top) than on the small contacts (bottom) in the photograph. This indicates a problem with the solder process: there is too much solder on the large lands versus the small lands. Visual inspection from the side reveals that the device is tilted by more than 3^{o} from the PCB. This again indicates a problem with solder under the device. The X-ray confirms the problem; it also reveals that there is very little solder on pins 1-7.

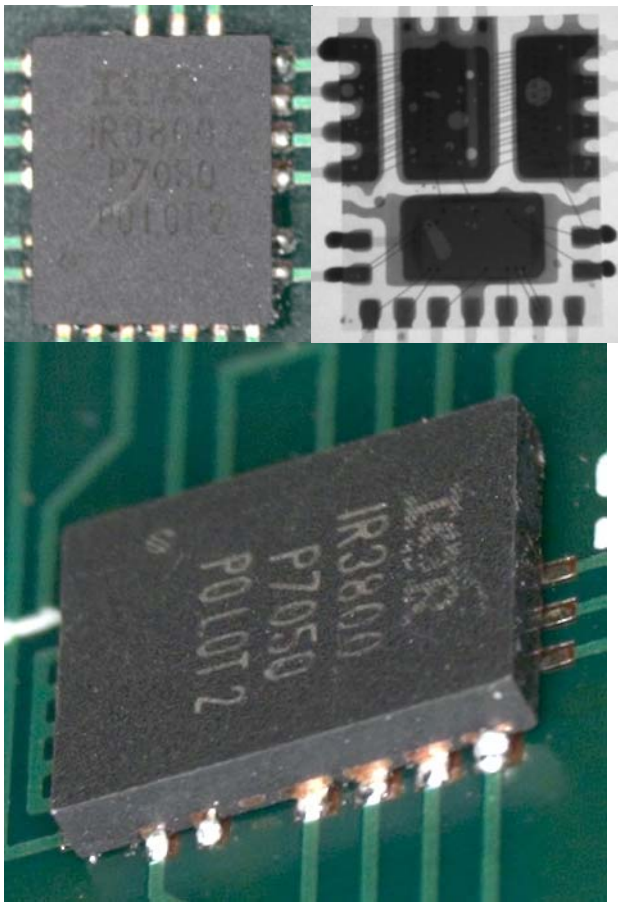

*Figure **9** Tilted device*

Reject tilted devices if one of the following is true:

- There is less than 75% coverage on large pads
- There is less than 50% coverage on small pads
- The angle of tilt exceeds 3^{o}. As a benchmark, *Figure **10*** shows a device that has a tilt of 1º

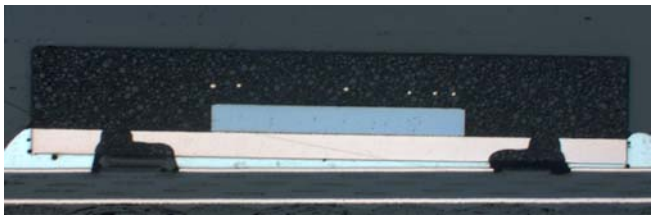

Figure 10: Cross-section of Power QFN with a tilt of 1º

Twisted and tilted device

This describes a device that is both crooked on the pads and not parallel to the PCB (*Figure **10***). Visual

inspection from above reveals the twist and from the side reveals the tilt. The X-ray shows the combined effects, with the contact area reduced by the twist and the pad definition impaired by the tilt.

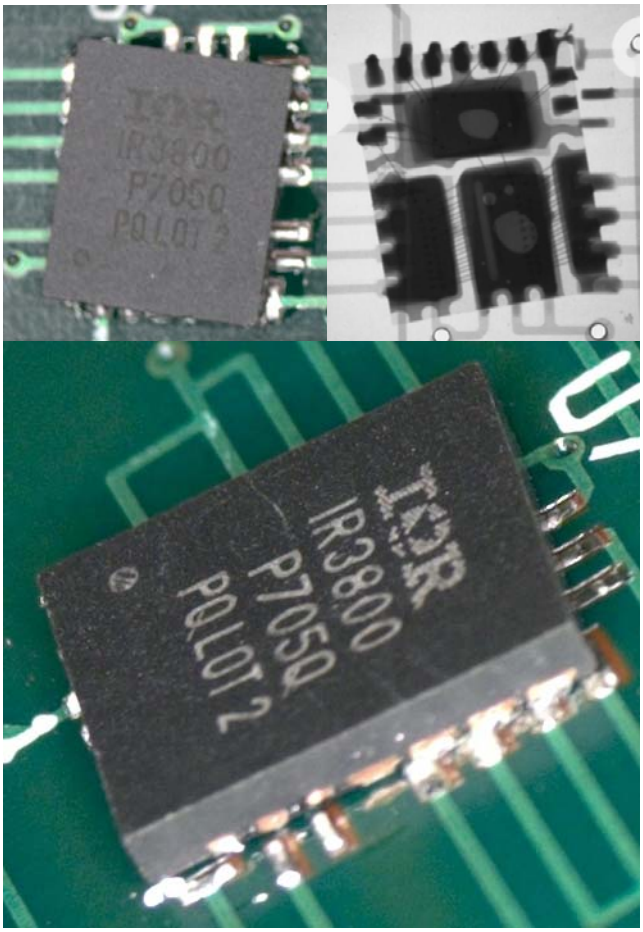

*Figure **10** Twisted and tilted device*

Reject twisted and tilted devices if:

- There is less than 75% coverage on the large contacts
- There is less than 50% coverage small contacts
- Any of pins 1-9 or 13,14 are shorted to the wrong land.
- The angle of tilt exceeds 3^{o}

Solder voiding

This describes joints in which some areas have no solder, as shown in *Figure **11***.

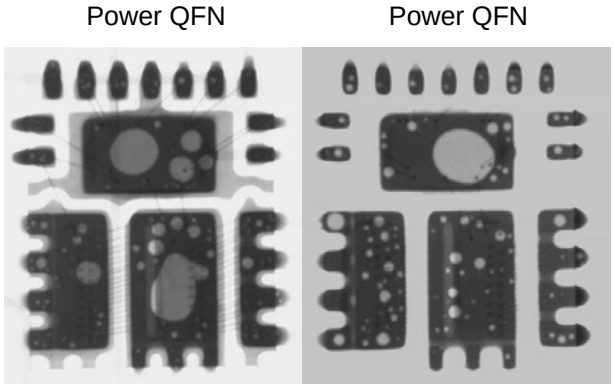

*Figure **11** Examples of solder voids*

Many industry standards (for example, IPC-A-610) accept voiding levels of up to 25% of the joint area. International Rectifier has carried out reliability tests on devices with 30% solder voiding that showed no deterioration in parametric or long-term reliability testing results.

To evaluate accurately the degree of solder voiding, it is important to use imaging and/or pixel-counting software. Estimating a percentage intuitively from an image invariably leads to inaccurate, usually exaggerated, results. Typically, people tend to judge the level of voiding to be about double the true amount. *Figure **12*** shows an example where viewers estimated about 10% of the contact area to be affected but imaging software revealed the true value to be only 4.7%. *Figure **13*** shows an example where viewers estimated about 40% of the contact area to be affected but imaging software revealed the true value to be only 27.5%. This demonstrates the importance of good image analysis software.

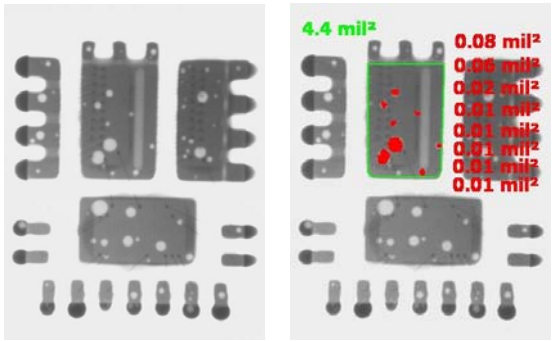

*Figure **12** Voids on the Switch Node contact. 4.4 mil^2 total pad area with 0.21 mil^2 void area. This*

represents 4.8% void area.

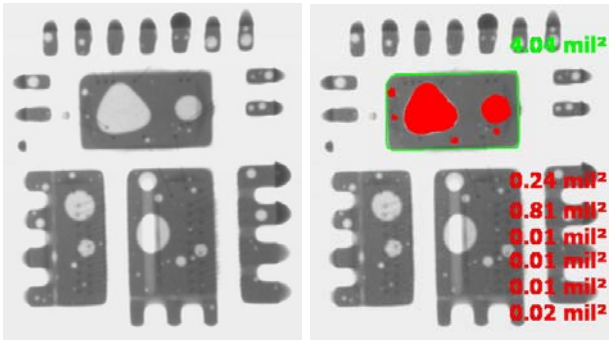

*Figure **13** Voids on the Analog Ground contact. 4.0 mil^2 total area with 1.1 mil^2 void area. This represents 27.5% voiding and is a fail according to IPC-A-610.*

Solder balling

This describes spheres of excess solder left after reflowing (*Figure **14***). In its most extreme form, it may result in short circuits.

As with any SMD, the aim in assembling Power QFN devices is to achieve good solder coverage of the joint area without solder balling. However, it is not always possible to achieve the ideal amount of solder, and solder balls sometimes form. In addition to solder quantity, an incorrect reflow profile (ramp rate too high) can cause solder balling; this happens because the solvent and/or flux boils, ejecting solder particles from the body of solder.

Although solder balling is not desirable, a few solder balls need not necessarily be an issue. For failure to occur, the solder balls must be of sufficient size to bridge across the pads. Solder balls of this diameter are extremely rare. In addition, solder balls tend to experience limited or no movement after assembly because of adhesion to flux residues or entrapment between the bottom of the Power QFN package and the printed circuit board. An example of an entrapped solder ball is shown in *Figure **14***.

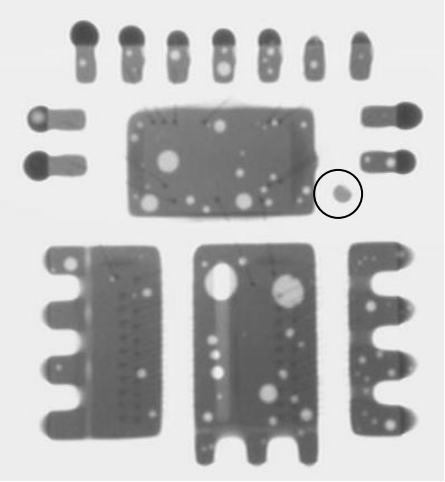

*Figure **14** Example of solder ball under the Power QFN*

Although solder balls rarely cause an electrical short, a smear of flux, solder particles or contaminant could lead to an electrical short or leakage in certain circumstances. This is very rare but can be exacerbated if the device shifts during reflow.

Use electrical tests to check for shorts. If there are no shorts when the device is mounted, it is unlikely that solder balls will cause shorting later.

The number and size of solder balls is not important. However, if solder balls occur often, perform a design of experiments (DOE) by varying solder paste, stencil thickness, stencil openings, squeegee pressure, bond pad dimensions, solder mask material, and reflow profiles. This activity should be able to identify and address the root-cause of solder balling.

Poorly formed joints

This describes joints in which excessive or insufficient amounts of solder are in contact with the bond pad and/or the Power QFN termination. In its most extreme form, it may result in opens or short circuits.

Excessive solder and short circuits

Poorly formed joints with excessive amounts of solder are acceptable unless it reduces spacing between adjacent bonds below distances acceptable per IPC-A-610 or induces a starved solder joint under the component. *Figure **15*** provides examples of both conditions. Note that the starved joint under the component can only be detected with X-ray or endoscope inspection. Poorly formed solder joints tend to appear on X-ray images as irregular patterns and shapes

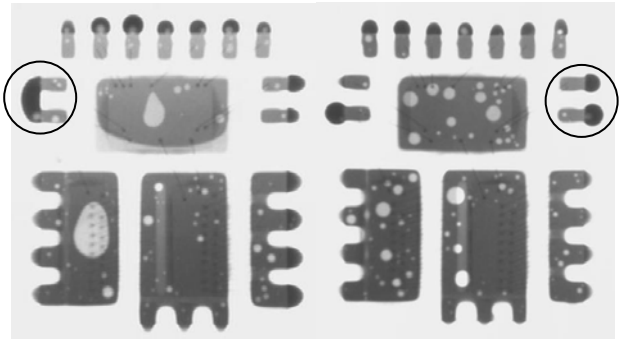

*Figure **15** Examples of poorly formed joints*

In extreme cases, excessive solder can also induce a short circuit, which describes accidental electrical connections between contacts that should be isolated. Figure 16 shows two examples of short circuits:

1. The image on the left shows a solder bridge between the source pads. Although this is undesirable, it is acceptable because the pads are electrically common.
2. The image on the right shows a solder bridge between the gate pad and a track on the PCB. This must be rejected or reworked. It might be detected in electrical testing if not by X-ray.

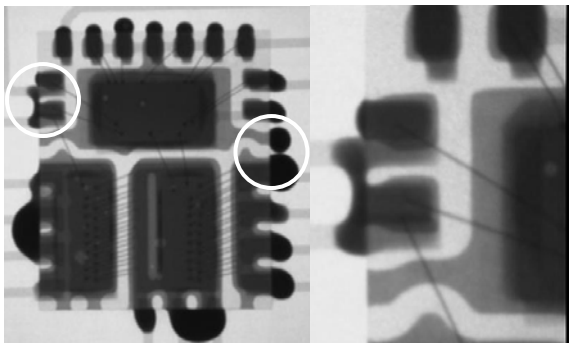

*Figure **16** Examples of short circuits*

Insufficient solder and open circuits

Poorly formed joints with insufficient amounts of solder are acceptable unless the area affected exceeds 25% of the joint. There is no need to rework or reject devices until this level is exceeded. However, if poor joints occur often, use process engineering or optimization and yield improvement exercises to rectify the situation.

As with voiding, use imaging or pixel-counting software to evaluate the extent of the affected area. Figures 17 shows an example.

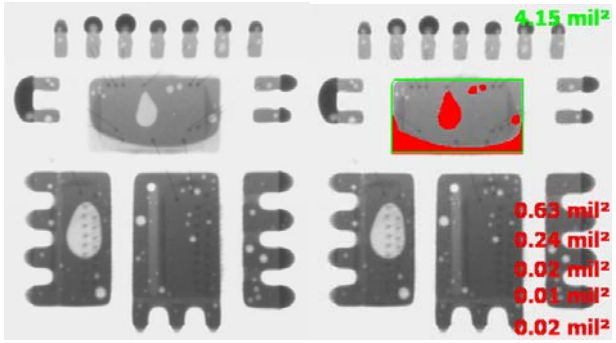

*Figure **17** Poorly formed Analog Ground joint – 22% missing*

In severe situations, insufficient solder will result in no electrical connection between the component and the board Open circuits appear on X-ray images as pads that are faint and/or poorly defined. Figure 18 shows an example of open circuits:

1. The image on the left shows an open connection on a pin 9. There is no electrical connection so this device would have to be rejected or reworked.
2. The image on the right shows a four pads with reduced contact area, pins 8, 9, 13, and 14. Pins 8 and 9 should be rejected because it has a maximum of 50% coverage, even if the other joints are perfect.

Figure 19 shows a visual observation of an open circuit (yellow arrow). When insufficient solder is present, the solder will tend to pull away from the component termination and pool on the bond pad.

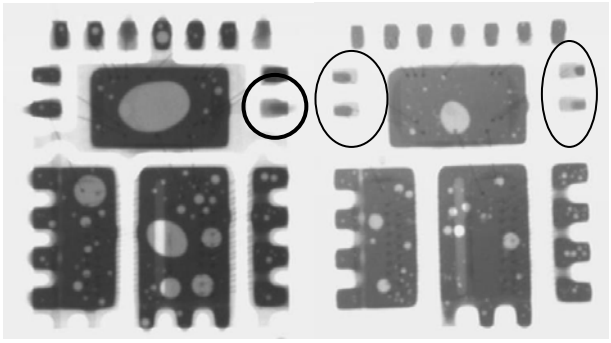

*Figure **18** Example of open circuits*

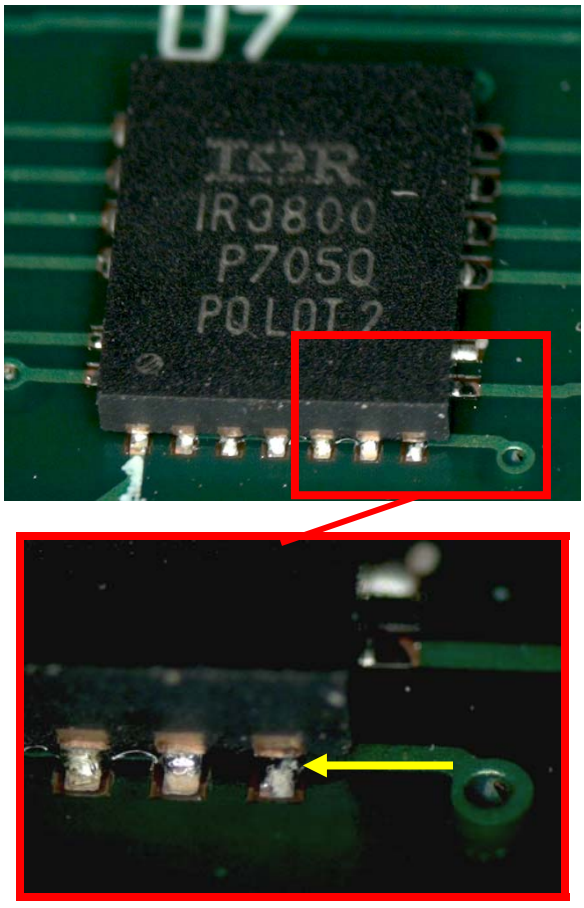

Figure 19: Example of open circuit

Design issues

In addition to their role in inspecting for processing faults, X-rays can reveal board design issues.