International
IOR Rectifier

APPLICATION NOTE

Application Note AN-1131

Universal Input (90 VAC – 265 VAC) LED Driver Using IRS2541

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1. Introduction

Explosive growth in emerging applications will drive demand for Light Emitting Diodes (LEDs). LEDs have proven a viable alternative to less efficient light sources. LED benefits include extremely long life, small size, design flexibility, architectural effects, significant maintenance cost savings, energy savings, and safe, low-voltage operation. With their cost decreasing and efficiency increasing over the long term, the industry is eagerly embracing LEDs.

This application note describes a universal input (90-265 VAC) LED driver using International Rectifier's IRS2541 LED driver IC. The IRS2541 is a high-voltage, high-frequency, buck control IC for constant LED current regulation. It incorporates a continuous-mode, time-delayed hysteretic buck regulator to directly control the average load current, using an accurate on-chip band-gap voltage reference. LEDs require drivers that have specific features such as constant current control over temperature, input voltage and manufacturing variations as well as dimming capability and appropriate fault protection. The IRS2541 is specifically designed to address these requirements.

This application note follows LED manufacturers' guidelines to connect LEDs in series because:

1) The typical LED I-V curve is very steep. A small change in the diode forward voltage translates into a large change in current. Since the LED brightness changes almost linearly with the current, the brightness of the LED can change drastically from small changes in voltage. Therefore, a much tighter control over the LED brightness is achieved if the driving circuit controls the current delivered to the LED as opposed to the voltage delivered across the LED. The IR2541 operates in this way.

2) Voltage tolerances, temperature dependence and the LEDs natural negative temperature coefficient provide challenges in current-sharing when LEDs are connected in parallel. When two diodes are connected in parallel but one has a slightly higher temperature, that diode will carry more current, making it hotter and thus contributing even more to the overall temperature. Eventually, the hotter diode reaches a point where it carries most of the current and fails prematurely. Moreover, the LEDs will differ in brightness because of temperature and voltage drop differences. Different voltage drops can also cause uneven current. Connecting the LEDs in series provides a possible solution since the legs of the LEDs connected in series share current more evenly than LEDs connected in parallel.

2. Circuit Description

This application note will describe a 90-265 VAC off-line LED driver designed with the IRS2541 LED IC. The circuit operates with a 220 VAC input, produces a 16 V to 35 V output voltage, and supplies a 350 mA programmable load current. This design can drive either six to 12 LEDs in series. For evaluation purposes, this design uses Luxeon Flood LEDs (LXHL-MMCA). Available through Future Electronics, these Lumileds flood boards have a maximum current rating of 700 mA with a breakdown voltage between 16 and 24 V.

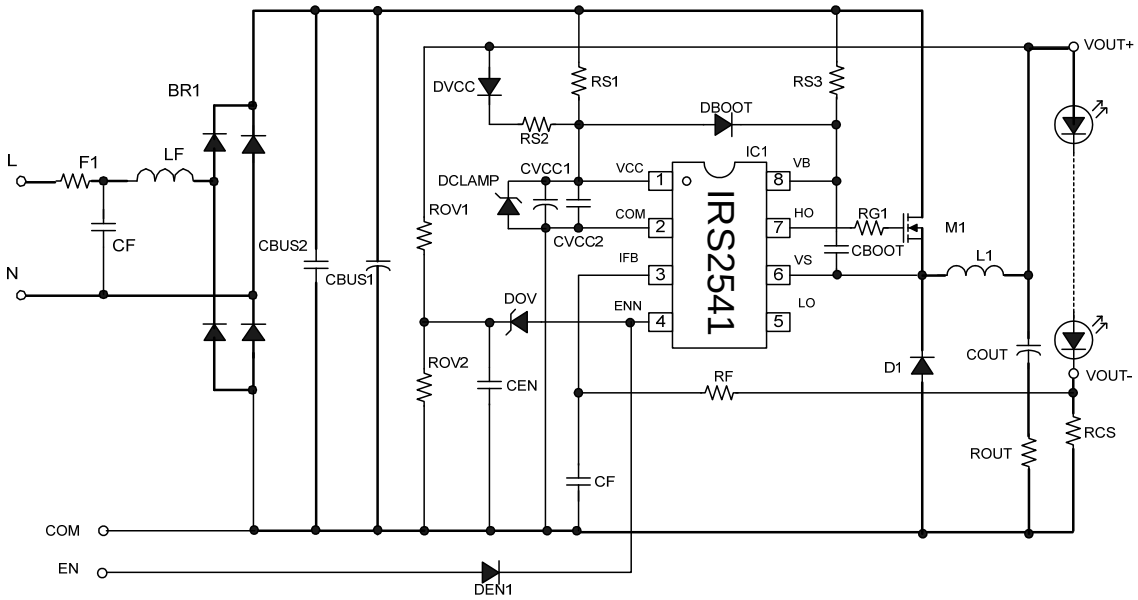

Fig. 2.1: IRS2541 LED Driver Schematic

Item	Description	Part #	Manufacturer	# of devices	Reference
1	Electrolytic Capacitor 10 µF, 25 V	UVZ1E100MDD	Nichicon	1	CVCC1
2	Capacitor, 100 nF, 400 V	MKP10	BC Components	1	CBUS2
3	Capacitor, 100 nF, 50 V	VJ0805Y104KXATW1BC	BC Components	3	CVCC2, CBOOT, CEN
4	Capacitor, 33 µF, 100 V	UVZ2A330MPD	Nichicon	1	COUT
5	Capacitor, 1 nF, 50 V, 0805	VJ0805Y102KXACW1BC	BC Components	1	CF
6	Electrolytic Cap, 47 µF, 450 V	EEU-EB2W470	Panasonic	1	CBUS1
7	Ultrafast Diode, 600 V, 1 A	MURS160DICT	Digi-key	1	DBOOT
8	4148 Diode	LL4148	Diodes Inc	2	DEN1, DVCC
9	Diode 400 V, 8 A, TO-220	8ETU04	IR	1	D1
10	Zener Diode 14 V, 0.5 W	ZMM5244B-7	Diodes Inc	1	DCLAMP
11	Zener Diode 7.5 V, 0.5 W	ZMM5236B-7	Diodes Inc	1	DOV
12	Inductor 470 µH	IL 050 321 31 01	VOGT	1	L1
13	Resistor 10 Ω, 1%	MCR10EZHF10R0	Rohm	1	RG1
14	Resistor 1.43 Ω, 1%	ERJ-8RQFR56V	Panasonic	1	RCS
15	Resistor 100 Ω, 1%, 0805	MCR10EZHF1000	Rohm	1	RF
16	Resistor 390 Ω, 5%, 1/2 W,2010	ERJ12ZYJ391	Panasonic	1	ROV2
17	Resistor 2 kΩ , 5%, 1/2 W,2010	ERJ12ZYJ202	Panasonic	1	ROV1
18	Resistor 1 kΩ, 5%, 1 W	5073NW1K000J12AFX	Phoenix Passive	1	RS2
19	Resistor 47 kΩ, 5%, 1 W	5073NW47K00J12AFX	Phoenix Passive	1	RS3
20	Resistor 56 kΩ, 5%, 1 W	5073NW56K00J12AFX	Phoenix Passive	1	RS1
21	Resistor 5Ω, 5%, 1 W	5073NW5R100J12AFX	Phoenix Passive	1	Rout
22	LED IC	IRS2541PBF	IR	1	IC1
23	500 V, 20 A, TO-220	IRFB20N50K	IR	1	M1
24	Heatsink	7-340-1PP-BA	IERC	1	
25	TO-220 Insulating Thermal Pad	SP600-54	Berquist	2	
26	Shoulder Washer	3049	Berquist	2	
27	Screw, 4-40, 0.5", Zinc	H346-ND	Building Fasteners	1	
28	Nut, 4-40, Hex, Zinc	H216-ND	Building Fasteners	1	
29	Fuse, 0.5 Ω, 1/2 W	CW 1/2	Dale	1	F1
30	Bridge Rectifier 1 A 1000 V	DF10S	IR	1	BR1
31	Capacitor, 0.33 µF, 275 VAC	F1772433-2200	Roederstein	1	CF
32	EMI Inductor, 470 µH	RFB1010-471	Coilcraft	1	LF

Table 2.2: Bill of Materials

This LED driver circuit precisely controls the current through the LED using IR's IRS2541 LED driver IC, a time-delayed hysteretic buck controller. Under normal operating conditions, the output current is regulated via the IFB pin voltage with a nominal value of 500 mV. This feedback is compared to an internal high-precision band-gap voltage reference. The chip toggles the HO output, as needed, to regulate the current.

Under normal operating conditions, if VIFB is below VIFBTH, HO is on and the load is receiving current from the bus voltage. This simultaneously stores energy in the output stage, L1 and COUT, while VIFB increases. Once VIFB crosses VIFBTH, HO switches off. Once HO is off, the inductor and output capacitor releases the stored energy into the load and VIFB decreases. When VIFB crosses VIFBTH again, HO switches on after the delay t_HO_on.

The switching continues to regulate the current at an average value determined as follows: when the output combination of L1 and COUT is large enough to maintain a low ripple on IFB (approximately less than 100 mV), the average of IOUT can be calculated with the equation below:

$$IOUT(avg) = VIFBTH / RCS$$

$$R_{350mA} = \frac{0.5V}{350mA} = 1.43\Omega$$

For more information on the IC or adapting the design for other inputs and outputs, please refer to the IRS2541 datasheet and IRPLLED1 reference design manual, respectively.

3. Components Selection

The frequency in the IRS2541 is free-running and maintains current regulation by quickly adapting to changes in input and output voltages. The device requires no additional external components to set the frequency. The frequency is determined by L1 and COUT, as well as the input/output voltages and load current.

Frequency selection becomes a trade-off between system efficiency, current control regulation, size, and cost. The higher the frequency, the smaller the size and lower the cost of L1 and COUT, the higher the ripple, the higher the FET switching losses, which becomes the driving factor as VBUS increases to higher voltages, the higher the component stresses and the harder it is to control the output current.

To maintain tight hysteretic current regulation, L1 and COUT need to be large enough to maintain the supply to the load during t_HO_on and avoid significant undershooting of the load current which in turn causes the average current to fall below the desired value. The input voltage has a great impact on the frequency and the inductor value has the greatest impact at reducing the frequency for smaller input voltages. The load current variation increases with lower inductance, either over the output voltage range or over the input voltage range.

The output capacitor can be used simultaneously to achieve the target frequency and current control accuracy. The capacitance reduces the frequency over the entire input voltage range. A small capacitance of 4.7 µF has a large effect on reducing the frequency. The current regulation is also improved with the output capacitance. The addition of the COUT is essentially increasing the amount of energy that can be stored in the output stage, which also means it can supply current for an increased period of time. Therefore, by slowing down the di/dt transients in the load, the frequency is effectively decreased. With the COUT capacitor, the inductor current is no longer identical to that seen in the load. The inductor current will still have a perfectly triangular shape, whereas the load will see the same basic trend in the current, but all sharp corners will be rounded with all peaks significantly reduced.

L1 and COUT need to be selected so that they store enough energy to supply the load during t_HO_on while maintaining current control accuracy. A lower L1 value will require a larger COUT value. With too small of an inductor (in the order of 100 µH or less), the COUT capacitor would need to be on the order of hundreds of microfarads to maintain good current regulation. Additionally, with a smaller inductance, the capacitor's ripple current would be quite large, shortening the life of the capacitor, if an electrolytic type is used.

Because of these considerations, a 470 µH inductor and a 33 µF output capacitor were selected. The current ripple associated with a 470 µH inductor is relatively small, so the board can be operated with or without output capacitance at lower current ratings.

4. Electrical Characteristics

Figure 4.1 and Table 4.2 show the resulting electrical performance when the circuit is used to drive six LEDs in series with 350 mA of current and variable input voltages across the universal input range, between 90 VAC and 265 VAC. For the test, one Luxeon flood board (25-0032) was used for the load.

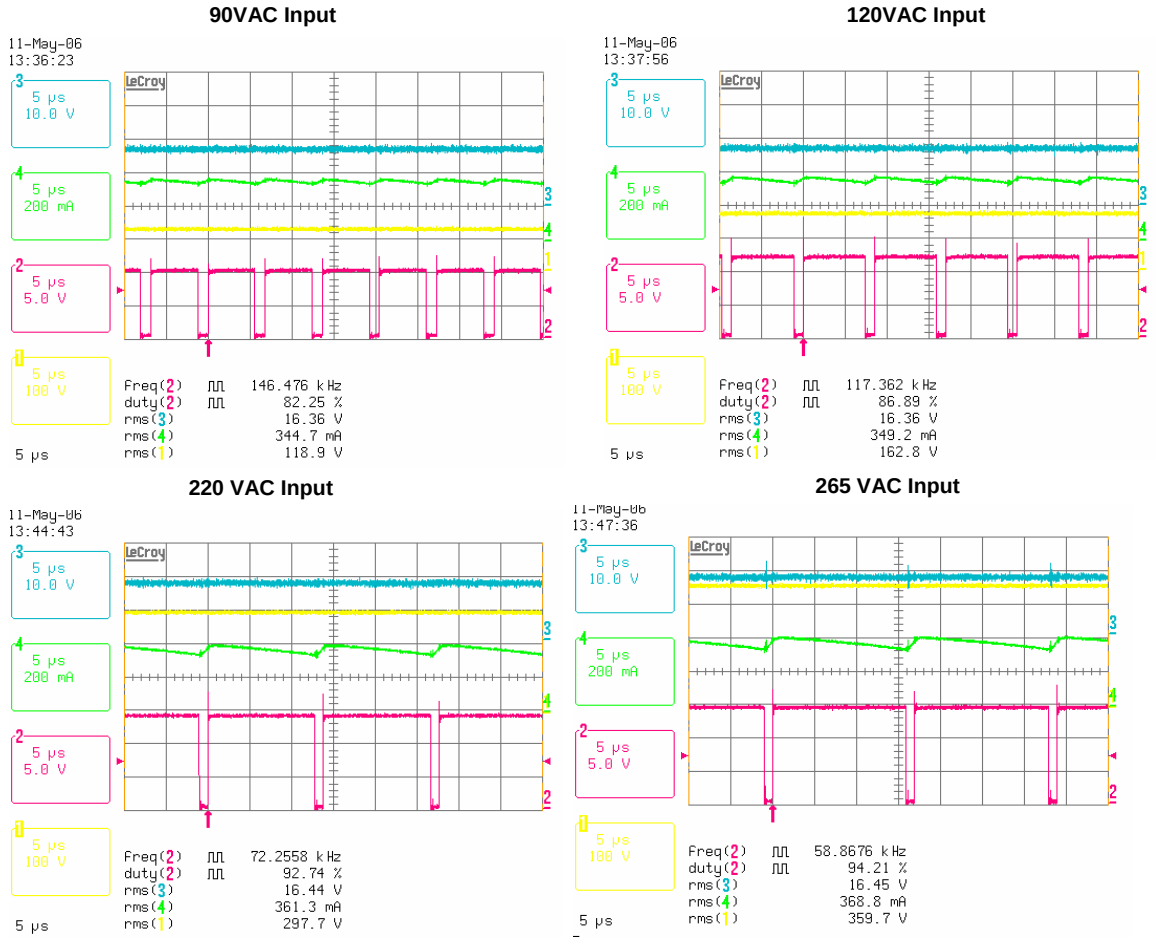

Fig. 4.1: Electrical Performance of Circuit Powering 6 LEDs
(Red: LO; Green: current through the LEDs; Blue: LED voltage; Yellow: bus voltage)

Results 6 LED in series @ 350 mA										
VAC Input	**Pin**	**Iin**	**Iled**	**Vled**	**Ipkpk**	**LO freq**	**LO duty**	**VBUS**	**T Diode**	**T Fet**
90 VAC	8.1 W	144 mA	344 mA	16.4 V	62 mA	146 kHz	82%	120 V	50.3 ºC	48.8 ºC
120 VAC	8.7 W	126 mA	351 mA	16.4 V	75 mA	120 kHz	87%	165 V	51.2 ºC	50.4 ºC
140 VAC	9.1 W	118 mA	352 mA	16.4 V	81 mA	105 kHz	88%	190 V	N/A	N/A
180 VAC	10.4 W	110 mA	356 mA	16.4 V	87 mA	86 kHz	91%	245 V	N/A	N/A
220 VAC	12 W	108 mA	365 mA	16.5 V	100 mA	72 kHz	92%	300 V	58.2 ºC	57.5 ºC
265 VAC	14 W	107 mA	369 mA	16.5 V	110 mA	58 kHz	94%	360 V	61 ºC	59 ºC

Table 4.2: Experimental Measurements
(Pin = input power; Iin = input current; Iled = current through the LEDs; Ipkpk = LED peak-to-peak ripple current; Vled = voltage across the LEDs; LO freq = frequency of the signal at pin LO; LO duty = duty cycle of the signal at pin LO; VBUS = bus voltage; T Diode = case temperature of the diode D1 when stable, after 30 minutes; T FET = case temperature of the FET M1 when stable, after thirty minutes)

Figure 4.3 and Table 4.4 show the resulting electrical performance when the circuit is used to drive twelve LEDs in series, with 350 mA of current, and variable input voltages across the universal input range, between 90 VAC and 265 VAC. For the test, two in-series Luxeon flood boards (25-0032) were used for load.

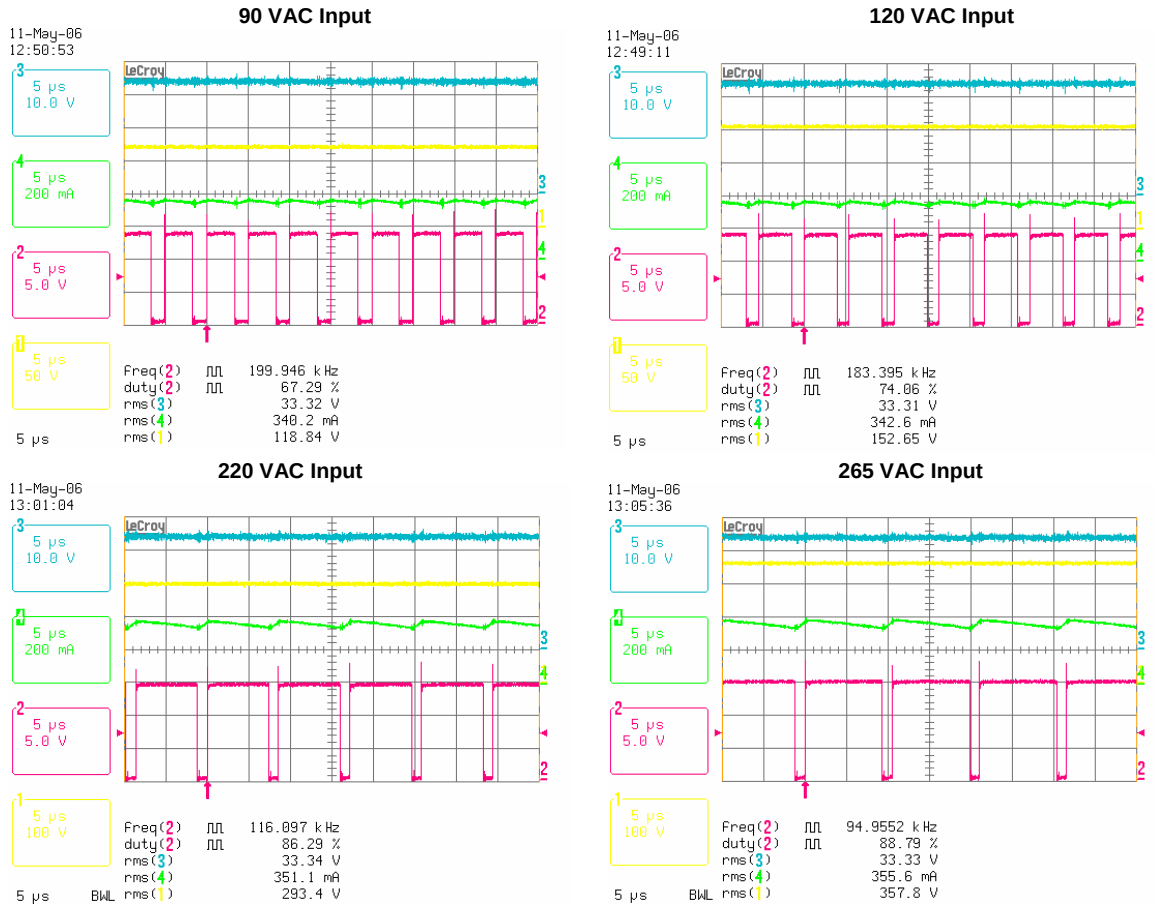

Fig. 4.3:
Electrical Performance of Circuit Powering 12 LEDs
(Red: LO; Green: current through the LEDs; Blue: LED voltage; Yellow: bus voltage)

Results 12 LED in series @ 350 mA										
VAC Input	**Pin**	**Iin**	**Iled**	**Vled**	**Ipkpk**	**LO freq**	**LO duty**	**VBUS**	**T Diode**	**T Fet**
90 VAC	14.8 W	241 mA	340 mA	33.4 V	81 mA	200 kHz	68%	120 V	56.5 ºC	54.5 ºC
120 VAC	15.5 W	207 mA	342 mA	33.4 V	76 mA	180 kHz	75%	165 V	N/A	N/A
140 VAC	16.1 W	190 mA	345 mA	33.4 V	76 mA	160 kHz	78%	190 V	N/A	N/A
180 VAC	17.4 W	168 mA	348 mA	33.4 V	85 mA	137 kHz	83%	245 V	N/A	N/A
220 VAC	19 W	157 mA	356 mA	33.4 V	87 mA	115 kHz	86%	300 V	71 ºC	69.7 ºC
265 VAC	20.8 W	150 mA	362 mA	33.4 V	95 mA	95 kHz	88%	360 V	72.2 ºC	71.2 ºC

Table 4.4:
Experimental Measurements
(Pin = input power; Iin = input current; Iled = current through the LEDs; Ipkpk = LED peak-to-peak ripple current; Vled = voltage across the LEDs; LO freq = frequency of the signal at pin LO; LO duty = duty cycle of the signal at pin LO; VBUS = bus voltage; T Diode = case temperature of the diode D1 when stable, after 30 minutes; T FET = case temperature of the FET M1 when stable, after thirty minutes)

For this design, an extremely tight current regulation was achieved with a worst-case result of ± 3.7% as the AC input voltage was swept from 90 VAC to 265 VAC. Likewise, a precise regulation of ± 1.3% was maintained for a varying load voltage from 16.4 V to 33.4 V.

5. Dimming

The enable pin can be used for dimming and open-circuit protection. When the ENN pin is held low, the chip remains in a fully functional state with no alterations to the operating environment. To disable the control feedback and regulation, a voltage greater than VENTH (approximately 2.5 V) needs to be applied to the ENN pin. With the chip in a disabled state, HO output will remain low, whereas the LO output will remain high to prevent VS from floating, in addition to maintaining charge on the bootstrap capacitor. The threshold for disabling the IRS2541 has been set to 2.5 V to enhance immunity to any externally generated noise, or application ground noise. This 2.5 V threshold also makes it ideal to receive a drive signal from a local microcontroller.

To achieve dimming, a signal with constant frequency and a set duty cycle can be fed into the ENN pin. There is a direct linear relationship between the average load current and duty cycle. If the ratio is 50%, 50% of the maximum set light output will be realized. Likewise, if the ratio is 30%, 70% of the maximum set light output will be realized. A sufficiently high frequency of the dimming signal must be chosen to avoid flashing or the "strobe light" effect. A signal on the order of a few kHz should be sufficient. Please refer to the IRPLLED1 reference design manual for information on how to design a fully-adjustable (0% to 100% duty cycle) PWM wave generator to connect to the enable signal as well as the modifications required for a dimming LED driver. These modifications include using a large enough capacitor on VCC, about 10 µF, and connecting a resistor ROUT in series with the output capacitor to limit the in-rush current.

6. Efficiency, Power Losses and Temperature Considerations

Efficiency, power losses and temperature considerations play an important role in choosing the switching devices, the output inductor value and capacitor value. The circuit described in this application note is optimized for cost (only one diode and one FET used as switching devices) and for performance (precise current regulation) but not for efficiency. Certain modifications to the schematics improve efficiency.

System efficiency can be calculated with the results in table 4.2 and 4.4 using the equation below:

$$Efficiency = \frac{Pin}{Vled \bullet Iled}$$

Efficiency increases as the difference between the bus voltage and the output voltage decreases, and therefore, will increase by decreasing the bus voltage (AC input voltage) and by increasing the output voltage (the number of LED in series). Considering the results for twelve LEDs in series, the efficiency is around 63% at 220 VAC input and around 67% for 120 VAC input. The efficiency can be improved further by increasing the output voltage. For example, considering a 3 V-voltage drop per LED, one can drive 16 LEDs in series to set the output voltage 48 VDC (maximum output voltage suggested from the safety regulations) and obtain a better efficiency.

To improve efficiency, one can also modify the circuit to reduce the losses on the switching devices. Especially for higher input voltages, the difference between the bus voltage (300 V for the 220 VAC input in Europe), and the output voltage across the LED is very great and the frequency, the duty cycle and the current over-shoot are critical parameters that influence losses. One can modify the values of the output capacitor COUT and the output inductor L1 to reduce the losses on the switching devices. For example, a

bigger value of COUT will decrease the frequency and decrease the switching losses. The resistor ROUT can be eliminated from the circuit as well. This resistor is required only for dimming applications to limit the in-rush current.

A very effective way to improve efficiency is to choose switching components with lower losses or use a different configuration, such as two FETs or two FETs and one diode instead of one FET and one diode as switching devices. The configuration with a single FET may yield a system with a lower cost, but a configuration using a FET (or even a FET with a diode in parallel) instead of the diode in the low-side position will yield better efficiency, particularly for higher load currents and higher input voltages. Generally, the IRS2541 has been designed so that it can drive either a high-side FET to be used together with a freewheeling diode (as the discussed schematics in Fig. 2.1) or a low-side FET and a high-side FET. The circuit for this configuration is shown in Fig. 6.2. Please refer to the IRPLLED1 reference design manual for additional information on this circuit.

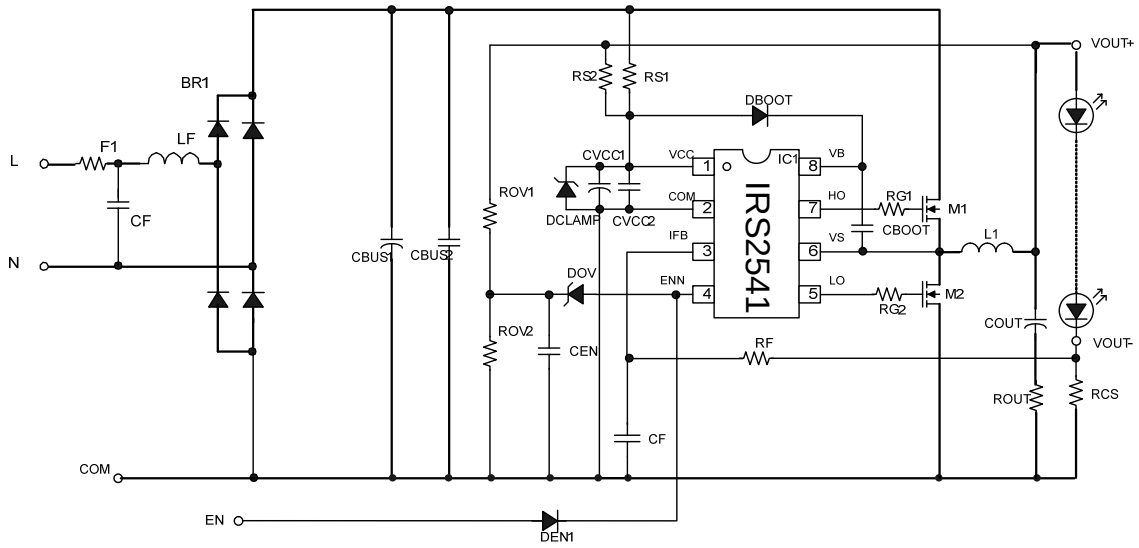

Fig. 6.2: IRS2541 Circuits Using Two FETs

The system efficiency is directly influenced by several system parameters including operating frequency, load current, and input voltage. A major parameter to consider is the reverse recovery time of the diode in comparison to the body diode of the FET it replaces. The diode intrinsically has a much shorter reverse recovery time since the device is specifically designed for this, whereas the body diode is a parasitic element that originates from basic processing technology and typically has inferior characteristics, in terms of forward drop, reverse recovery, and power handling capabilities. The reverse recovery problem is incurred during the deadtime after the low-side FET has been on and conducting current. During this deadtime, the low-side FET is off, but the body diode is freewheeling and providing current to the load. Since the body diode is conducting current, carriers are present and will eventually need to be recombined, leading to reverse recovery. When the high-side FET turns on, the VS node is almost instantly pulled from COM to VBUS and the low-side FET or the freewheeling diode conducts current from VS to ground due to the reverse recovery effect, potentially resulting in large power losses, overheating of the low-side switching component and causing component stress. Since the power diode has a much shorter reverse recovery time, the diode will conduct current for a significantly shorter period with lower power losses. At lower frequency and lower load current, the long recovery time associated with the FET body diode may not be an issue. For higher frequency higher current applications, a diode could provide lower power losses with respect to a FET.

The bus voltage is also important since it will determine how long the low-side FET, or the freewheeling diode, will be conducting. If the bus voltage is very large in comparison to the output, the low-side FET or

diode will be conducting for the majority of the switching period. A FET has much lower on-state losses due to the low RDS-on, whereas high voltage diodes rarely have forward drops less than 1 V. For system efficiency, a diode's forward conduction losses can also be compared to the low-side FET's reverse recovery losses.

The most efficient solution would be to place the FET in parallel with the diode in the low-side position. In this case, during the deadtime, instead of the body diode freewheeling, the additional diode would be conducting. This will always be the case as long as the forward drop of the external diode is less than that of the body diode. If costs permit, a diode in parallel with an IGBT could also be an option.

System needs and cost should be evaluated prior to choosing a FET or diode for the low side. Although a diode is cheaper, in certain cases, the associated power losses may require a heatsink, nullifying any cost savings. Likewise, there are conditions where a FET may prove less efficient, increasing the cost to keep it cool.

The best FET for the circuit is the one that provides the lowest power dissipation. It is best to use a FET with the lowest rating needed in the application. FET parameters degrade as the voltage ratings increase. If using two FETs, the next parameter to think about is the reverse recovery time. While FETs will not have reverse recovery times comparable to diodes, a good reverse recovery time for a FET is 150 ns to 200 ns. The two remaining parameters to consider, on-state resistance and gate charge, present direct trade-offs. If the FET has low gate capacitance, the die size will be small, but this will result in a larger on-state resistance which could potentially be a problem for high current applications. On the other hand, if the FET has a large gate capacitance, the die will be large and the FET will have a low on resistance, but it will be more difficult to turn on the FET which will also stress the IC. There has to be a direct compromise between the two. Typically, the best solution is a FET with a relatively low RDS-on and a medium-sized gate capacitance, much like the device chosen for this application

To estimate the power losses, one can use the following considerations. During the time HO is high, the high-side FET will conduct and the load will receive current from the bus voltage and simultaneously store energy in the output stage. During the time LO is high, the diode D1 or the low side FET will conduct and the inductor and the output capacitor release the stored energy into the load.

The total power dissipation in the diode is determined by the power dissipation due to the on-state voltage drop and the reverse recovery blocking leakage current and can be calculated using the following equation:

$$P_D = I_F V_F \frac{t_{ON}}{T} + I_L V_R \frac{(T - t_{ON})}{T}$$

Where:

t_{ON} is the time the diode is in the on-state

T is the total period

I_F is the forward conduction current

V_F is the forward voltage drop

I_L is the reverse leakage current

V_R is the applied voltage

In this case $\frac{t_{ON}}{T}$ is the LO duty cycle and $\frac{(T - t_{ON})}{T}$ is the (1- LO duty cycle)

V_R is the bus voltage

Generally, the second term can be neglected and the forward conduction current can be considered equal to Iled. The total power dissipation in the diode can be simplified by this equation:

$$P_D = I_{led} V_F (LOduty)$$

The power dissipation in the FET can be considered (with some approximation) the sum of the power losses during the on-state and the power loss during switching, and can be calculated using the following equation:

$$P_F = I_F V_F \frac{t_{ON}}{T} + \frac{1}{2} I_F V_S \frac{t_F}{T}$$

Where:

t_{ON} is the time the FET is in the on-state

T is the total period

I_F is the conduction current

V_F is the forward voltage drop at a current I_F

V_S is the blocking voltage

t_F is the time the current is assumed to fall to zero from the on-state to the off-state (we assumed the turn-off time much longer than the turn-on time)

In this case $\frac{t_{ON}}{T}$ is (1- the LO duty cycle) and $\frac{1}{T}$ is the LO frequency

V_S is the bus voltage and the forward conduction current can be considered equal to Iled. The calculation can be simplified using this equation:

$$P_F = I_{led}{}^2 RDSon(1 - LOduty) + \frac{1}{2} I_{LED} V_S \frac{t_F}{T}$$

To this term we should add the turn-on losses and the power dissipation incurred in the body diode (same equation for a common diode, but the second term becomes predominant)

7. Other Design Considerations

7.1 Open-Circuit / Over-Voltage Protection

By using the suggested voltage divider, capacitor, and zener diode (ROV1, ROV2, CEN and DOV), the designer can virtually clamp the output voltage at any desired value. If there is no load and the output clamp is not utilized, the positive output terminal will float at the high-side input voltage. The open load clamp is recommended if the load is disconnected and then reconnected without shutting down the driver. When the load is reconnected with power on, the load would see the entire bus voltage for a short period of time. The open circuit clamp minimizes the amount of stress seen by the load under such circumstances by clamping the voltage much lower than VBUS.

In an open-circuit condition, switching will still occur between the HO and LO outputs, whether due to the output voltage clamp or to the watchdog timer. In this state, rather than regulating the current with the feedback pin, the output voltage will be loosely regulated via the enable pin. Transients and switching will

be observed at the positive output terminal as seen in Fig. 30. The difference in signal shape, between the output voltage and the IFB, is due to the capacitor CEN used to form the voltage clamp. The repetition of the spikes can be reduced by simply increasing the capacitor size. If VBUS is significantly larger than the desired output voltage clamp, the output voltage will become a function of VBUS. This is because of the intrinsic delays of the chip (t_LO_on, t_LO_off, t_HO_on, and t_HO_off) along with the minimum HO on time. If the load is removed, the output will clamp at the desired voltage. Then if the bus voltage is increased, there could be a proportional change in the clamped voltage. This is not seen as an issue since the open circuit clamp is strictly a safety feature to reduce the stress seen by the load, if disconnected and reconnected without a power down.

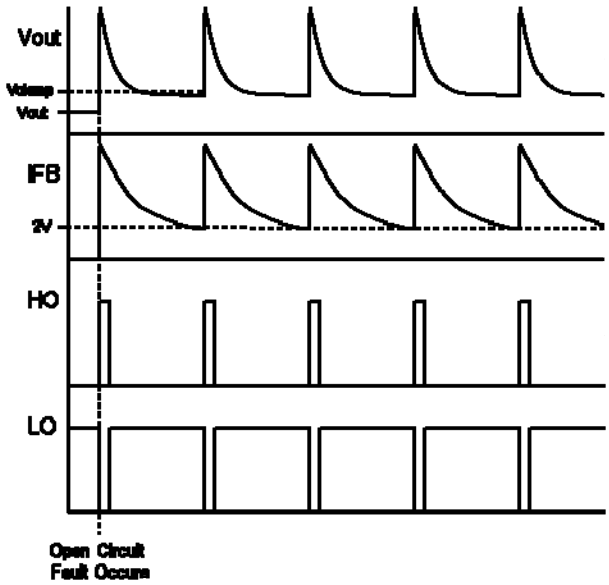

Fig. 7.1: Open-Circuit Fault Signals with Clamp

The two resistors ROV1 and ROV2 form a voltage divider for the output, which is then fed into the cathode of the zener diode DOZ. The diode will only conduct, flooding the enable pin, when its nominal voltage is exceeded. The chip will enter a disabled state once the divider network produces a voltage at least 2.5 V greater than the zener rating. The capacitor CEN serves only to filter and slow the transients/switching at the positive output terminal. The clamped output voltage can be determined by the following analysis.

$$V_{out} = \frac{(2.5V + DZ)(R_1 + R_2)}{R_2}$$

$$DZ = \text{Zener Diode Nominal Rated Voltage}$$

DOV has been chosen to be a 7.5 V zener diode. ROV2 has also been set to 390 Ω to help provide a low resistive charging path for CBOOT as previously discussed. It was also decided to clamp the output voltage at 60 V, this is sufficiently larger than the predefined maximum load voltage as to not cause any erroneous shut-down, while it is also well within the specifications of the 100 V-rated output stage. Having arbitrarily chosen these parameters, ROV1 was calculated as follows:

$$V_{out} = \frac{(2.5V + DZ)(R_{OV1} + R_{OV2})}{R_{OV2}}$$

$$R_{OV1} = \frac{V_{out} R_{OV2}}{(2.5V + DZ)} - R_{OV2} = \frac{60V \cdot 390\Omega}{(2.5V + 7.5V)} - 390\Omega \approx 2K\Omega$$

7.2 Filtering/ EMC issues

The IRS2541 was specifically designed to handle low frequency ripples on VBUS. Its capability to handle such ripple makes it ideal for an offline rectified waveform. If high voltage (on the order of 5 V to 10 V) high frequency oscillations (greater than or close to the operating frequency) are present on VBUS, however, it is recommended to implement an input filter. If these high frequency signals are present on VBUS, the IRS2541 will still continue to regulate the current through the load, but abnormal switching of LO and HO may be observed. This poses a problem in terms of switching losses. As previously noted, one may need or want to control the operating frequency to control the systems efficiency, but if LO and HO randomly switch, it may negate all attempts to control the frequency. Of course the root of this problem can be the PCB layout, but it is also a function of the load current. To alleviate the problem, a designer may implement an input filter (CF, LF, and CBUS1 in Figure 2.1). The input filter will also greatly improve the circuits EMC performance.

The IRS2541 demo board has not been EMC tested. Input and output filters can be used to reduce the conducted emissions to below the limits of the applicable EMC standard, as needed. All inductors may require a powdered iron core rather than ferrite. It can handle a much larger current before saturating; needs are dependent upon the load current. If EMC is of critical importance, one may prefer to use one FET and one diode, in contrast to a half-bridge driver. The reverse recovery time for a diode is inherently shorter than that of a FET. This will help in reducing transients observed in the switching elements resulting in better EMC performance.

7.3 Layout Considerations

It is very important when laying out the PCB for the IRS2541 to consider the following points:

1. CVCC2 and CF must be as close to IC1 as possible.
2. The feedback path should be kept to a minimum without crossing any high frequency lines.
3. COUT should be as close to the main inductor as possible.
4. All traces that form the nodes VS and VB should be kept as short as possible.
5. All signal and power grounds should be kept isolated from each other to prevent noise from entering the control environment. It's a general rule of thumb that all components associated with the IC should be connected to the IC ground with the shortest path possible.
6. All traces carrying the load current need to be adjusted accordingly.
7. Gate drive traces should also be kept to a minimum.

8. Design Procedure Summary

1. Determine the systems requirements: input/output voltage and current needed.
2. Calculate current-sense resistor.
3. Determine the operating frequency required.
4. Select L1 and COUT so that they maintain supply into the load during t_HO_on.
5. Select switching components (FET/freewheeling diode) to minimize power losses.
6. Determine VCC and VBS supply components.
7. Add filtering on the input, IFB and ENN as needed.
8. Fine tune components to achieve desired system performance.

Careful selection of the components will significantly increase the reliability of the product, particularly for the capacitors. These need to be rated for at least 100 ºC and a proper voltage. As in most electronic power applications, capacitors and resistors are the components most likely to fail due to stress over time and high operating temperatures.

For every design, start testing at low voltage and gradually increase the input voltage while performing the following check:

- Check the temperatures of the switching devices.
- Check the frequency at LO to make sure it is stable and it is not excessive (a high frequency will cause high switching losses on the FET).
- Check the duty cycle at LO.
- Check the current at pin IFB of the IRS2541 for over-shoot. This current is more representative of the current through the output inductor than the current through the LED because of the presence of COUT. The over-shoot needs to be limited.