Application Note AN-1125

IRS212(7,8,71) and IR212(7,8,71) Comparison

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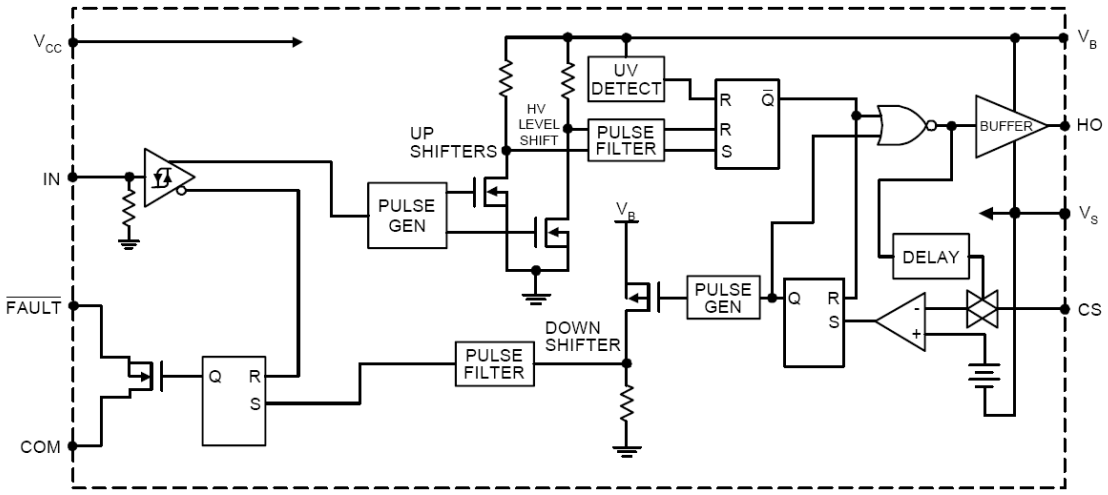
Introduction

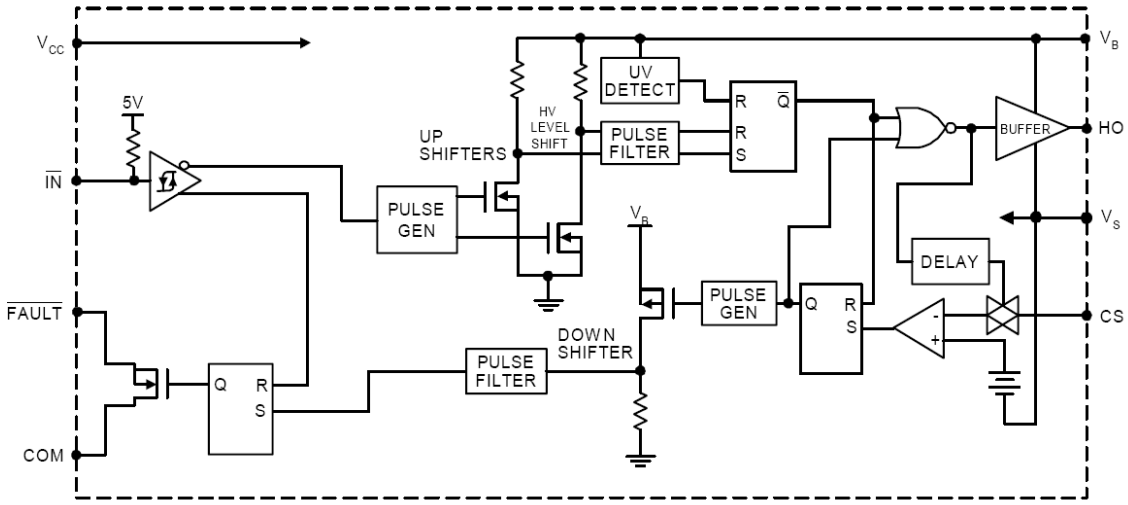
The IRS212(7,8,71) are new HVIC products that replace the IR212(7,8,71) and are pin-to-pin compatible with their corresponding predecessors. In many cases, little or no change is necessary to use the new products. This application note describes the various differences between the IRS212(7,8,71) and the IR212(7,8,71) HVICs.

The IRS212(7,8,71) are high voltage, high speed power MOSFET and IGBT drivers. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The logic input is compatible with standard CMOS or LSTTL outputs, down to 3.3 V. The protection circuitry detects over-current in the driven power transistor and terminates the gate drive voltage. An open drain FAULT signal is provided to indicate that an over-current shutdown has occurred. The output driver features a high pulse current buffer stage designed for minimum cross-conduction. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high-side or low-side configuration which operates up to 600 V.

Block Diagram



212(7,71)



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The IRS212(7,8,71) and IR212(7,8,71) share the same block diagram. The functionality of the two ICs is the same.

Electrical Characteristic Differences

All measurement conditions remain unchanged unless noted. Parameters not mentioned have not changed.

Absolute Maximum Ratings

There are no changes to the Absolute Maximum Ratings

Recommended Operating Conditions

There are no changes to the Recommended Operating Conditions.

Dynamic Electrical Characteristics

Parameter		IR212(7,8,71)			IRS212(7,8,71)			Units
Symbol	Definition	min	typ	max	min	typ	max	
t_{on}	Turn-on propagation delay	-	200	250	-	150	200	ns
t_{off}	Turn-off propagation delay	-	150	200	-	150	200	
t_{bl}	Start-up blanking time	500	700	900	550	750	950	
t_{cs}	CS shutdown propagation delay	-	240	360	-	65	360	
t_{flt}	CS to FAULT pull-up propagation delay	-	340	510	-	270	510	

The IRS212(7,8,71) has reduced in propagation delays and increased blanking time when compared to the IR212(7,8,71).

Static Electrical Characteristics

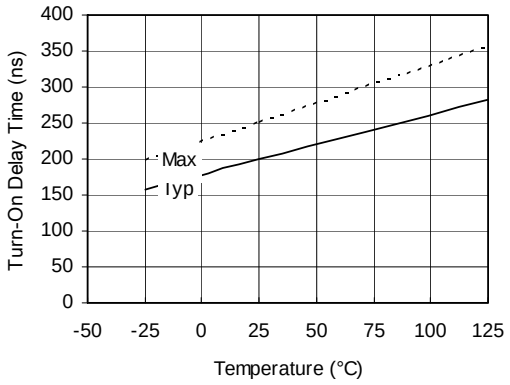
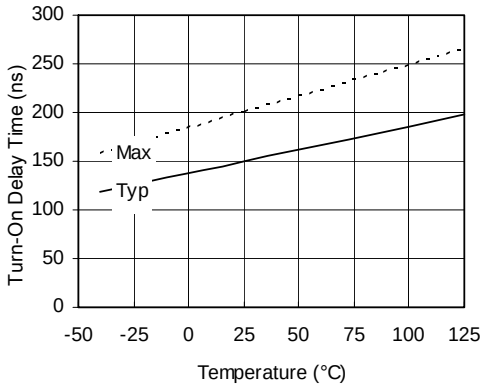
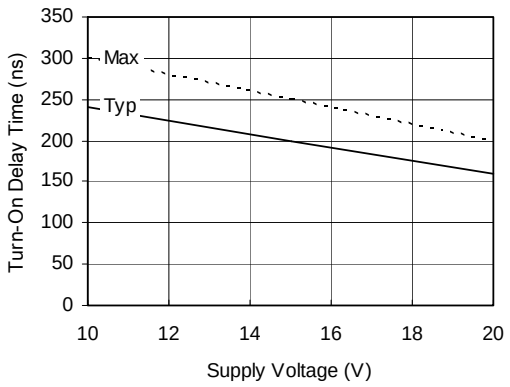
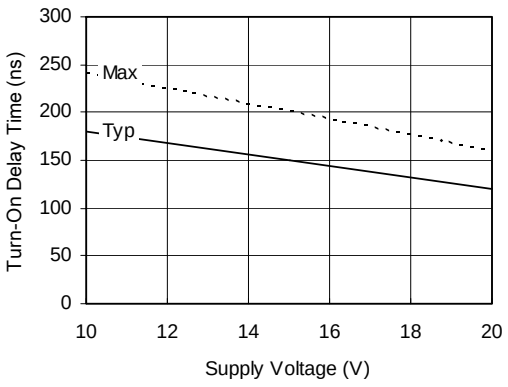
Parameter		IR212(7,8,71)			IRS212(7,8,71)			Units
Symbol	Definition	min	typ	max	min	typ	max	
V_{IH}	Logic "1" input voltage (V_{CC} = 10 V to 20 V)	3.0	-	-	2.5	-	-	V
V_{IL}	Logic "0" input voltage (V_{CC} = 10 V to 20 V)	-	-	0.8	-	-	0.8	
V_{OH}	High level output voltage, V_{BIAS} - V_O	-	-	0.1	-	0.05	0.2	
		Io = 0 mA			Io = 2 mA			
V_{OL}	Low level output voltage, V_O	-	-	0.1	-	0.02	0.1	
		Io = 0 mA			Io = 2 mA			
I_{QBS}	Quiescent V_{BS} supply current (V_{IN} = 0 V or 5 V)	-	200	400	-	250	500	uA
I_{IN}+	Logic “1” input bias current	-	7.0	15	-	7.0	15	
I_{IN}-	Logic “0” input bias current	-	-	1.0	-	-	5.0	
I_{CS}+	"High" CS Bias Current	-	-	1.0	-	-	5.0	
I_{CS}-	"Low" CS Bias Current	-	-	1.0	-	-	5.0	

With the IRS212(7,8,71),

1. V_{IH} is decreased to 2.5 V for better 3.3 V logic compatibility.
2. I_{QBS} has increase slightly.
3. The I_{IN-}, I_{CS+}, and I_{CS-} has increased to better reflect tester capabilities.
4. The V_{OL} and V_{OH} are tested using a new standardized test condition of I_O= 2 mA.

Figures

This figures shown in this section compare figures shown in the IR212(7,8,71) (left column) and IRS212(7,8,71) (right column) datasheets. Illustrations that have not changed between the two datasheets have not been included in this section.

IR212(7,8,71)	IRS212(7,8,71)
 **Figure 6A. Turn-On Delay Time vs. Temperature**	 **Figure 6A. Turn-On Delay Time vs. Temperature**
 **Figure 6B. Turn-On Delay Time vs. Voltage**	 **Figure 6B. Turn-On Delay Time vs. Voltage**

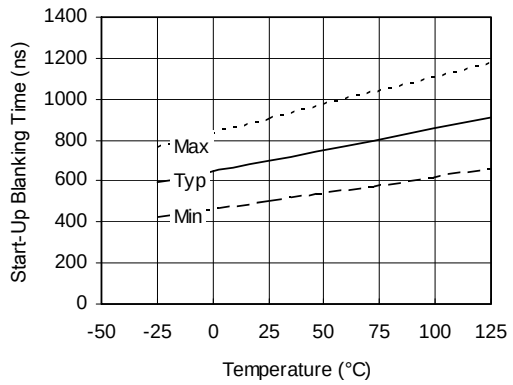
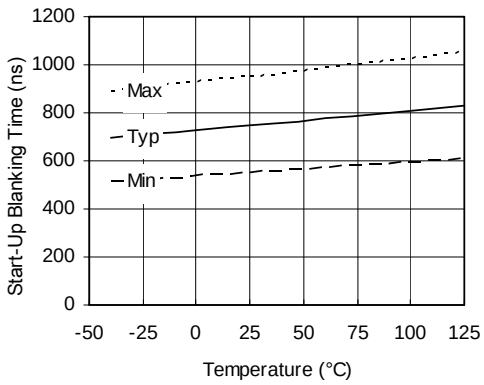


Figure 10A. Start-Up Blanking Time vs. Temperature



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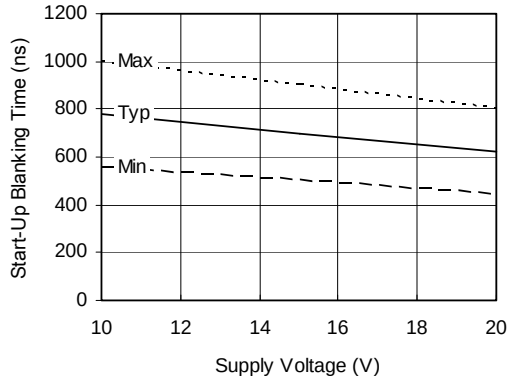


Figure 10B. Start-Up Blanking Time vs. Voltage

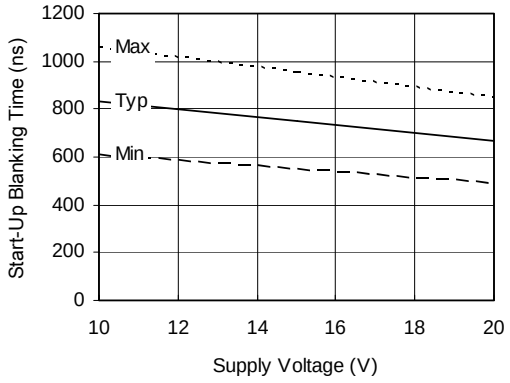


Figure 10B. Start-Up Blanking Time vs. Voltage

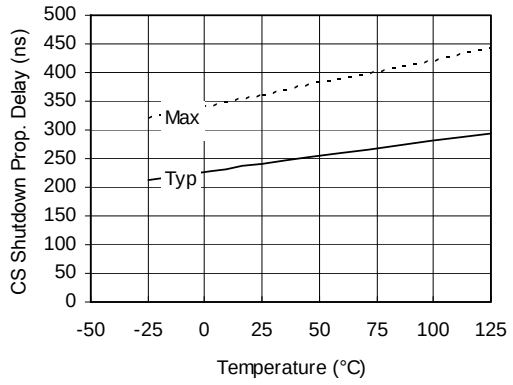
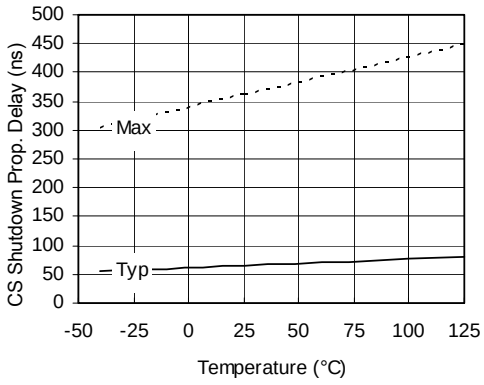


Figure 11A. CS Shutdown Prop. Delay vs. Temperature



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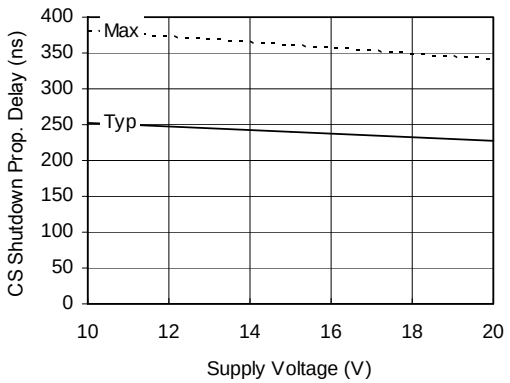


Figure 11B. CS Shutdown Prop. Delay vs. Voltage

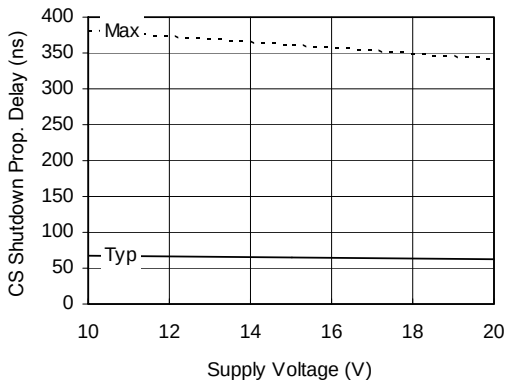


Figure 11B. CS Shutdown Prop. Delay vs. Voltage

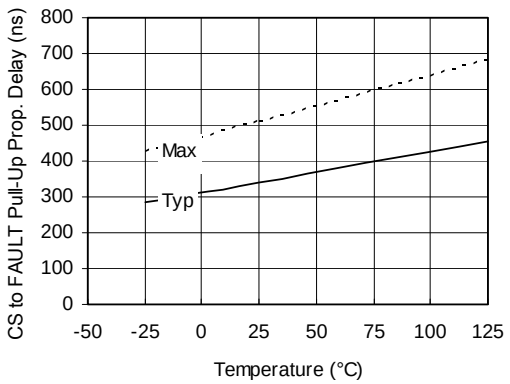
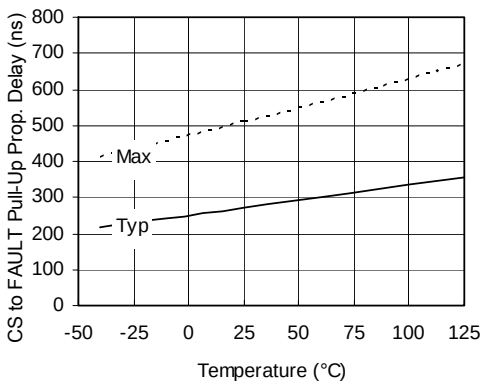


Figure 12A. CS to FAULT Pull-Up Prop. Delay vs. Temperature



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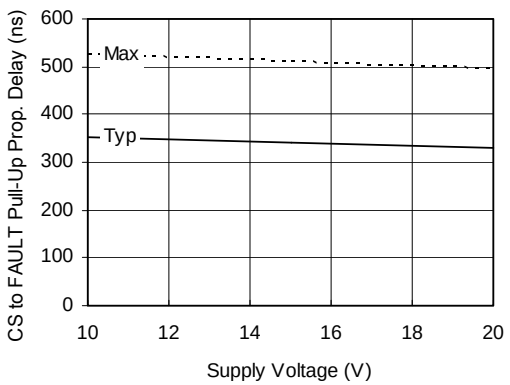


Figure 12B. CS to FAULT Pull-Up Prop. Delay vs. Voltage

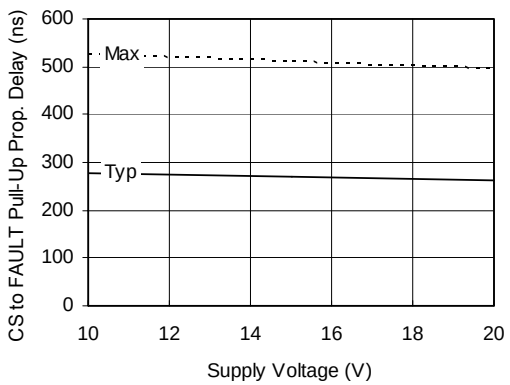


Figure 12B. CS to FAULT Pull-Up Prop. Delay vs. Voltage

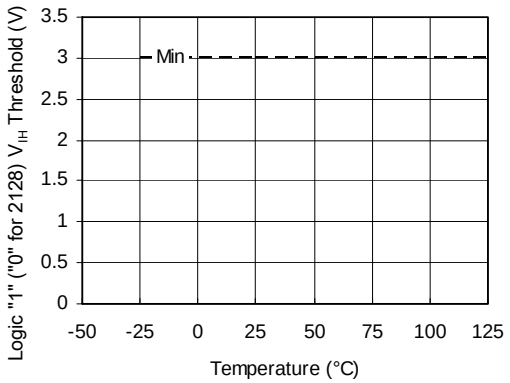
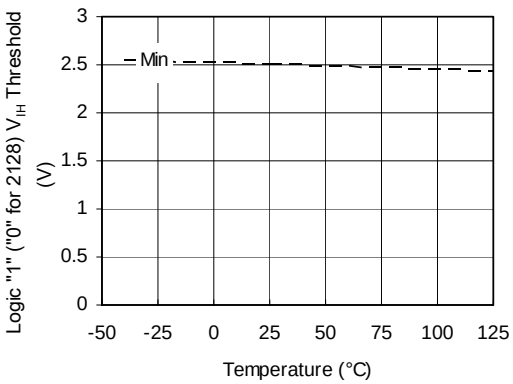


Figure 13A. Logic "1" ("0" for 2128) V_{IH} Threshold vs. Temperature



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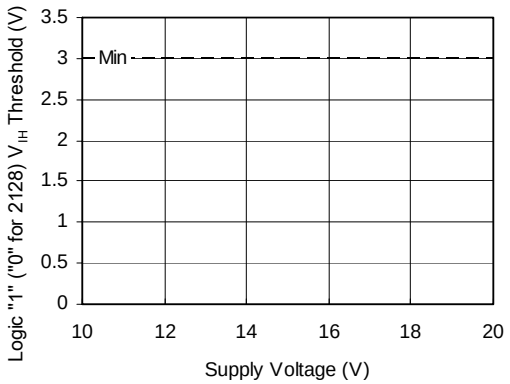

Figure 13B. Logic "1" ("0" for 2128) V_{IH} Threshold vs. Voltage

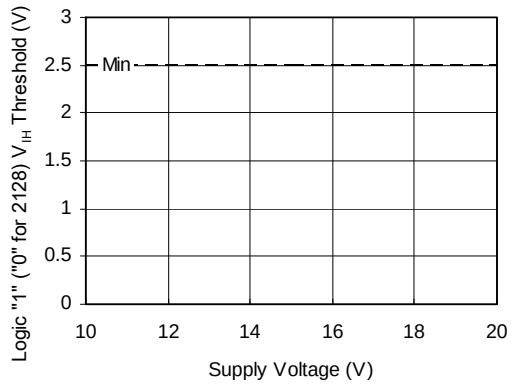

Figure 13B. Logic "1" ("0" for 2128) V_{IH} Threshold vs. Voltage

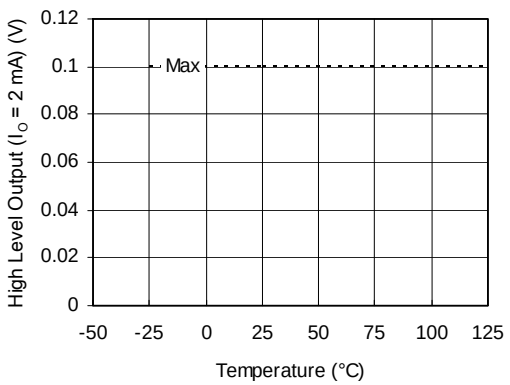

Figure 16A. High Level Output (I_O = 2 mA) vs. Temperature

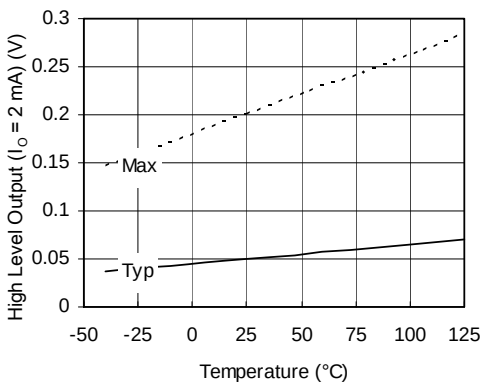

Figure 16A. High Level Output (I_O = 2 mA) vs. Temperature

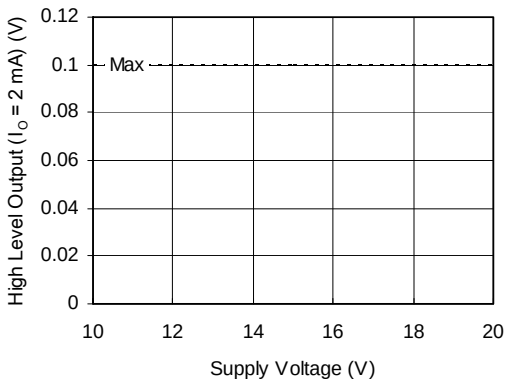

Figure 16B. High Level Output (I_O = 2 mA) vs. Voltage

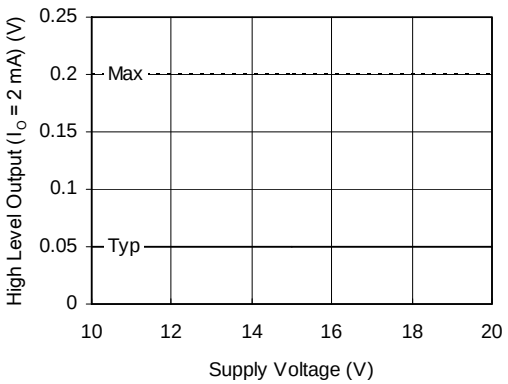

Figure 16B. High Level Output (I_O = 2 mA) vs. Voltage

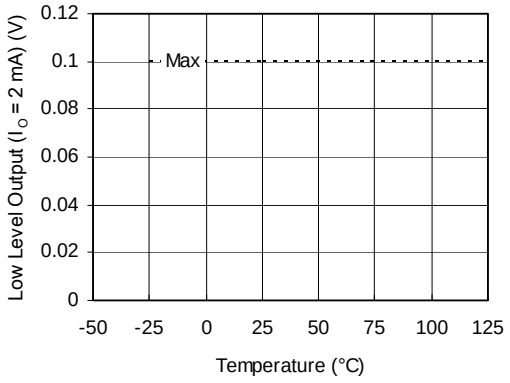

Figure 17A. Low Level Output (I_O = 2 mA) vs. Temperature

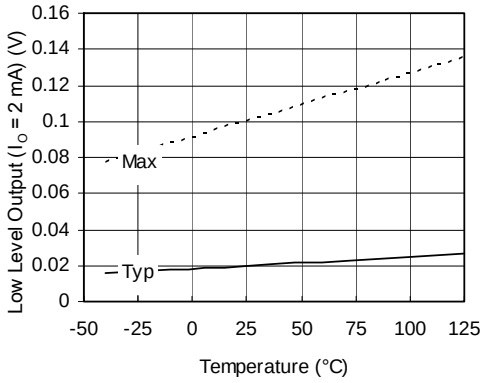

Figure 17A. Low Level Output (I_O = 2 mA) vs. Temperature

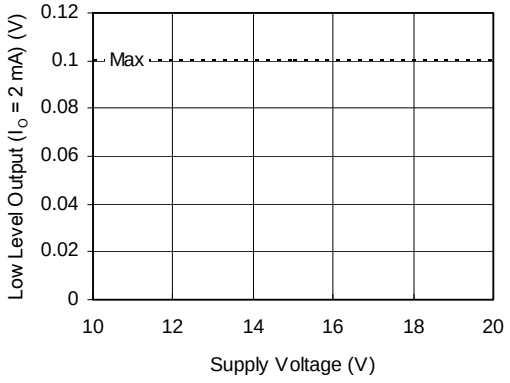

Figure 17B. Low Level Output (I_O = 2 mA) vs. Voltage

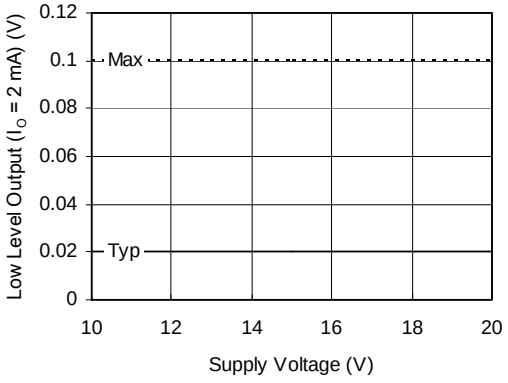

Figure 17B. Low Level Output (I_O = 2 mA) vs. Voltage

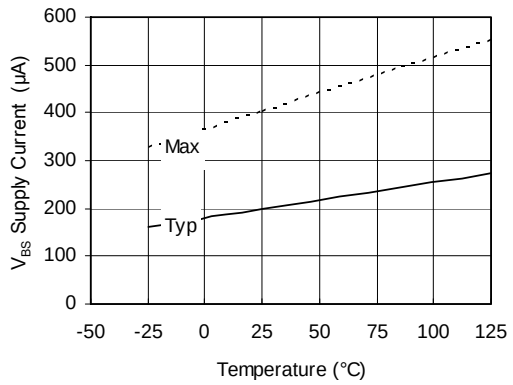

Figure 19A. V_{BS} Supply Current vs. Temperature

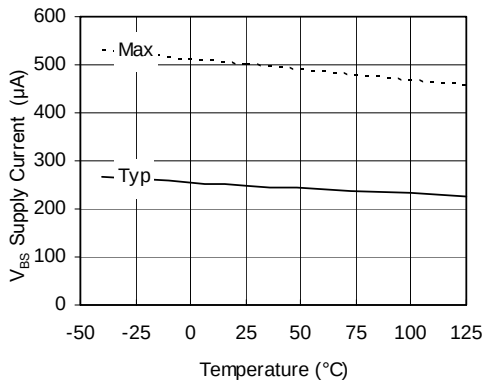

Figure 19A. V_{BS} Supply Current vs. Temperature

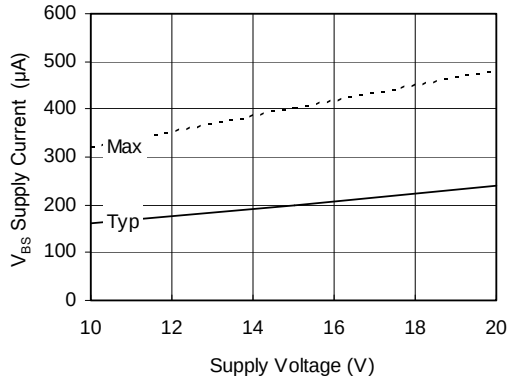

Figure 19B. V_{BS} Supply Current vs. Voltage

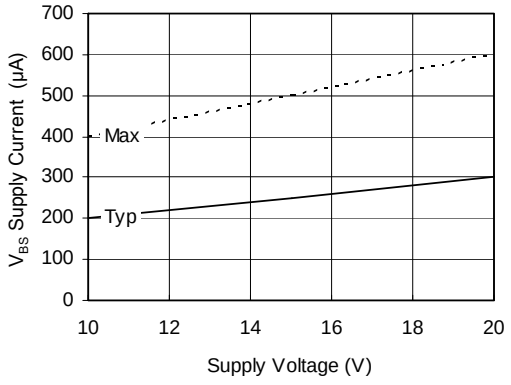

Figure 19B. V_{BS} Supply Current vs. Voltage

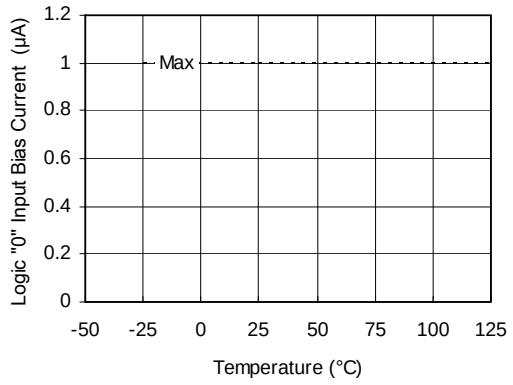

Figure 22A. Logic "0" Input Bias Current vs. Temperature

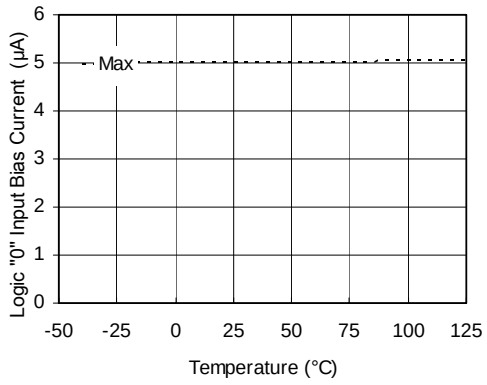

Figure 22A. Logic "0" Input Bias Current vs. Temperature

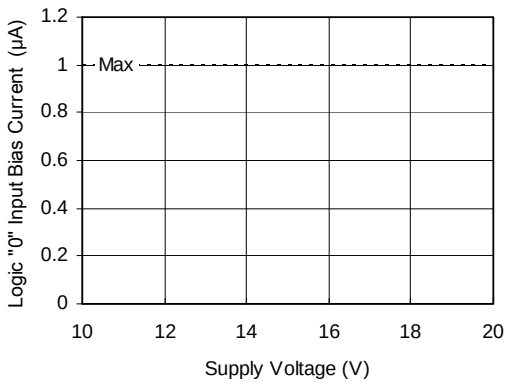

Figure 22B. Logic "0" Input Bias Current vs. Voltage

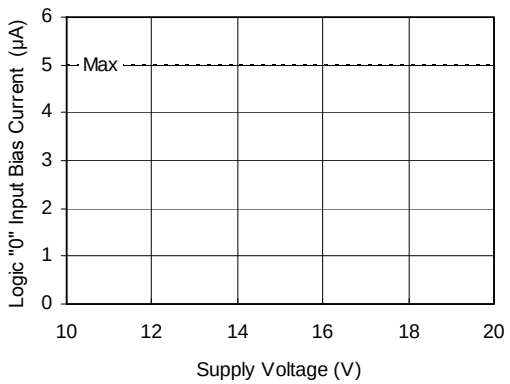

Figure 22B. Logic "0" Input Bias Current vs. Voltage

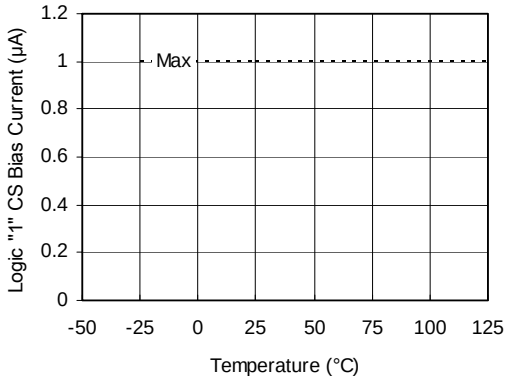

Figure 23A. Logic "1" CS Bias Current vs. Temperature

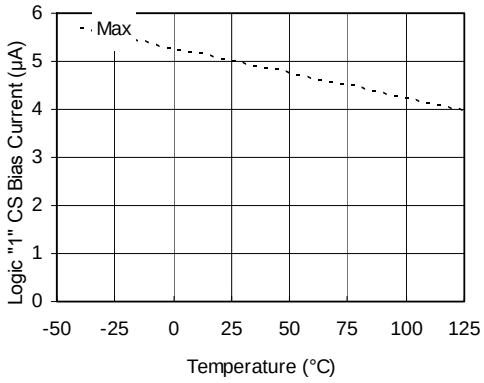

Figure 23A. Logic "1" CS Bias Current vs. Temperature

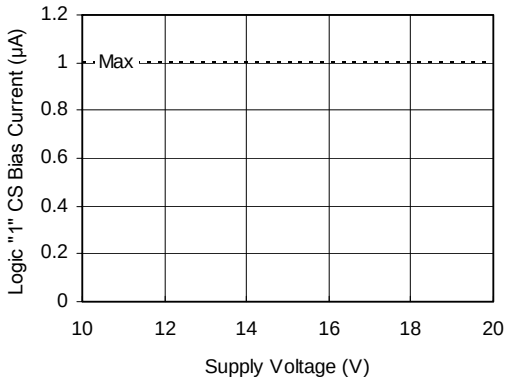

Figure 23B. Logic "1" CS Bias Current vs. Voltage

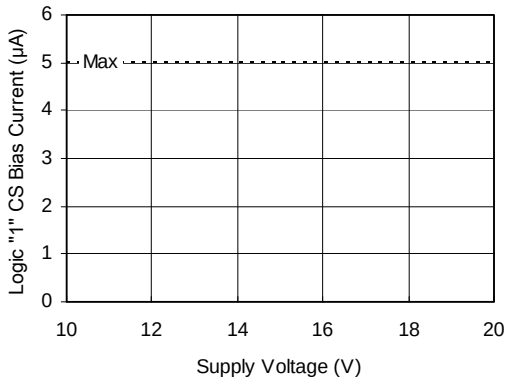

Figure 23B. Logic "1" CS Bias Current vs. Voltage

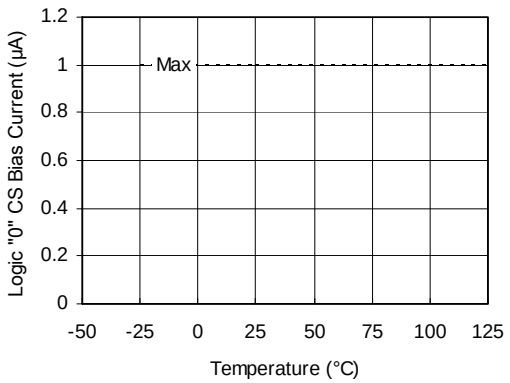

Figure 24A. Logic "0" CS Bias Current vs. Temperature

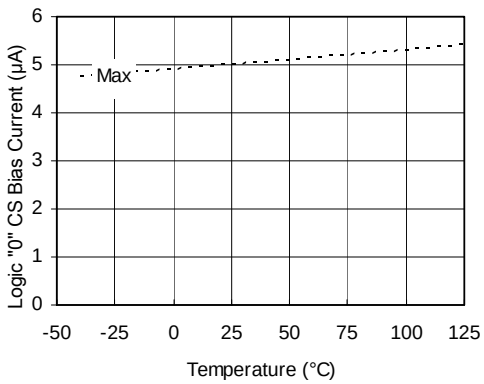

Figure 24A. Logic "0" CS Bias Current vs. Temperature

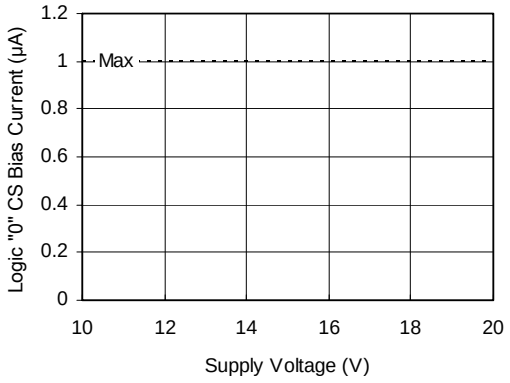

Figure 24B. Logic "0" CS Bias Current vs. Voltage

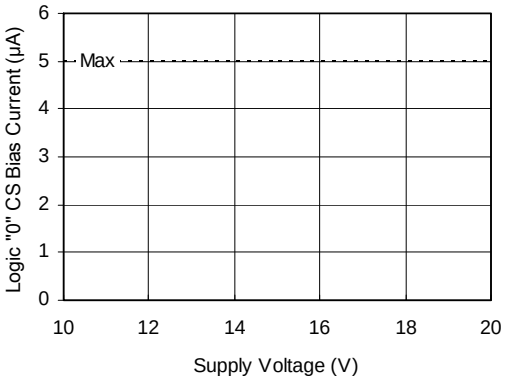

Figure 24B. Logic "0" CS Bias Current vs. Voltage

Summary

This document highlights the differences between the IRS212(7,8,71) and the IR212(7,8,71) HVICs.