Application Note AN-1124

IRS2166D & IR2166 Comparison

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Introduction

The new IRS2166D replaces the existing IR2166 HVIC advantageously with the following enhancements:

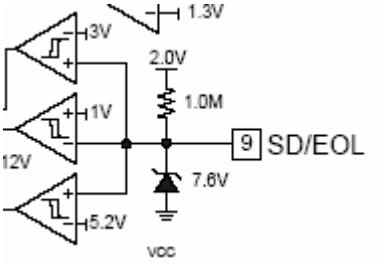
- Improved V_{BUS} regulation voltage tolerance
- Improved frequency tolerance
- Increased SD pin shutdown voltage threshold hysteresis
- Changed EOL pin internal 2 V bias to a +/-10 µA OTA
- Internal bootstrap MOSFET
- Undervoltage lockout on the floating supply
- Improved EOL pin shutdown threshold tolerance

It is based on the same core design (but with the addition of the integrated bootstrap functionality) and is pin-to-pin compatible, allowing minimum changes to the previous design. This application note describes the differences between the existing IR2166 HVIC and the new IRS2166D.

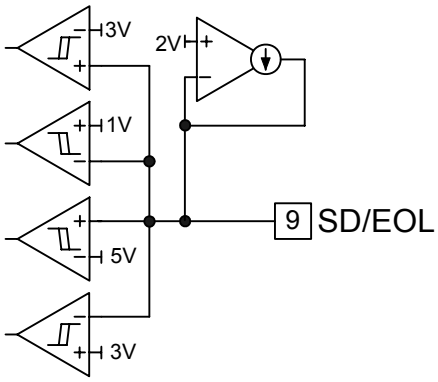
BLOCK DIAGRAM

Beside the integration of the internal bootstrap MOSFET, the main change in the block diagram relates to the SD/EOL pin.

IR2166



IRS2166D



As can be observed in the diagrams, there are two important changes:

1) The 2 V bias at the SD/EOL pin is maintained with a 10 µA OTA in the IRS2166D compared to a Zener/current source combination in the IR2166. The robustness of the IRS2166D is therefore increased, while there should not be any impact on the application.
2) A 5 V comparator, not shown in IR2166, is now included in the block diagram of the IRS2166D to clarify the functionality of the SD/EOL pin. The IC is shutdown when SD/EOL goes over the 3 V (V_{EOLTH+}) threshold; to restart the IC either V_{CC} should be recycled below 10.5 V (V_{CCUV-}) or SD/EOL should be increased over 5 V (V_{SDTH+}) and then below 3 V (V_{SDTH-}); this functionality exists already in the IR2166 HVIC but is not illustrated in the block diagram.

ELECTRICAL CHARACTERISTICS

The following tables and comments highlight the differences between the IR2166 and the IRS2166D:

Absolute Maximum Ratings

Parameter			IR2166		IRS2166D		
Symbol	Definition		Min.	Max.	Min.	Max.	Units
V_B	High-side floating supply voltage		-0.3	625	-0.3	625	V
V_S	High-side floating supply offset voltage		V_B – 25	V_B + 0.3	V_B – 25	V_B + 0.3	
V_{HO}	High-side floating output voltage		V_S - 0.3	V_B + 0.3	V_S - 0.3	V_B + 0.3	
V_{LO}	Low-side output voltage		-0.3	V_{CC} + 0.3	-0.3	V_{CC} + 0.3	
V_{PFC}	PFC gate driver output voltage		-0.3	V_{CC} + 0.3	-0.3	V_{CC} + 0.3	
$I_{O,MAX}$	Maximum allowable output current (HO, LO, PFC) due to external power transistor miller effect		-500	500	-500	500	mA
V_{VBUS}	VBUS pin voltage		-0.3	V_{CC} + 0.3	-0.3	V_{CC} + 0.3	V
V_{CPH}	CPH pin voltage		Not specified	Not specified	-0.3	V_{CC} + 0.3	
V_{RT}	RT pin voltage		-0.3	V_{CC} + 0.3	-0.3	V_{CC} + 0.3	
V_{RPH}	RPH pin voltage		-0.3	V_{CC} + 0.3	-0.3	V_{CC} + 0.3	
I_{RT}	RT pin current		-5	5	-5	5	mA
I_{RPH}	RPH pin current		-5	5	-5	5	
V_{CT}	CT pin voltage		-0.3	V_{CC} + 0.3	-0.3	V_{CC} + 0.3	V
I_{COMP}	COM pin current		-5	5	-5	5	mA
I_{ZX}	ZX pin current		-5	5	-5	5	
I_{CC}	VCC pin current (see Note 1)		-25	25	-25	25	
$V_{SD/EOL}$	SD/EOL pin voltage		-0.3	V_{CC} + 0.3	-0.3	V_{CC} + 0.3	V
$I_{SD/EOL}$	SD/EOL pin current		-5	5	-5	5	mA
V_{CS}	CS pin voltage		-0.3	V_{CC} + 0.3	-0.3	V_{CC} + 0.3	V
I_{CS}	CS pin current		-5	5	-5	5	mA
dV/dt	Allowable V_S offset voltage slew rate		-50	50	-50	50	V/ns
P_D	Package power dissipation @ $T_A \leq +25$ °C $P_D = (T_{JMAX}-T_A)/R_{\theta JA}$	(16-Pin DIP)	---	---	1.8	1.8	W
		(16-Pin SOIC)	---	---	1.4	1.4	
$R_{\Theta,JA}$	Thermal resistance, junction to ambient	(16-Pin DIP)	---	---	70	70	°C/W
		(16-Pin SOIC)	---	---	82	82	
T_J	Junction temperature		-55	150	-55	150	°C
T_S	Storage temperature		-55	150	-55	150	
T_L	Lead temperature (soldering, 10 seconds)		---	300	---	300	

Comments:

All absolute maximum ratings are the same except for the thermal resistance junction to ambient for the SO package which as been slightly reduced (this will give lower temperatures on the package surface).

Recommended Operating Conditions

Parameter		IR2166		IRS2166D		
Symbol	Definition	Min.	Max.	Min.	Max.	Units
V_B-V_S	High-side floating supply voltage	V_{CC}-0.7	V_{CLAMP}	V_{BSUV+}	V_{CLAMP}	V
V_S	Steady state high-side floating supply offset voltage	-1	600	-1	600	
V_{CC}	Supply voltage	V_{CCUV+}	V_{CLAMP}	V_{CCUV+}	V_{CLAMP}	
I_{CC}	V_{CC} supply current (see Note 2)	Note 2	10	Note 2	20	mA
C_T	CT pin capacitance	220	---	220	---	pF
$I_{SD/EOL}$	SD/EOL pin current	-1	1	-1	1	mA
I_{CS}	CS pin current					
I_{ZX}	ZX pin current					
T_J	Junction temperature	-25	125	-25	125	°C

Comments:
Most of the parameters are the same; the high-side floating supply voltage (V_B-V_S) is recommended to exceed V_{BSUV+} as it incorporates the undervoltage lockout protection.

Electrical Characteristics

Parameters		IR2166			IRS2166D			
Symbol	Definition	Min	Typ	Max	Min	Typ	Max	Units
Supply Characteristics								
V_{CCUV+}	V_{CC} supply undervoltage positive going threshold	10.0	11.5	12.5	11.5	12.5	13.5	V
V_{CCUV-}	V_{CC} supply undervoltage negative going threshold	8.5	9.5	10.7	9.5	10.5	11.5	
V_{UVHYS}	V_{CC} supply undervoltage lockout hysteresis	1.5	2.0	3.0	1.5	2.0	3.0	
I_{QCCUV}	UVLO mode V_{CC} quiescent current	145	170	290	---	250	500	µA
I_{QCC}	Quiescent V_{CC} supply current	---	2.3	4.0	---	4.3	5.1	mA
I_{QCCFLT}	Fault quiescent V_{CC} supply current	Not Specified			---	600	900	µA
$I_{CC,RUN}$	V_{CC} current at RUN frequency	Not Specified			---	5.0	---	mA
V_{CLAMP}	V_{CC} zener clamp voltage	14.3	15.6	17	14.6	15.6	16.6	V
Floating Supply Characteristics								
I_{QBS0}	Quiescent V_{BS} supply current	-1	0	5	---	30	70	µA
I_{QBS1}	Quiescent V_{BS} supply current	5	30	70	---	50	90	
V_{BSMIN}	Minimum required V_{BS} voltage for proper HO functionality	---	2.5	---	Replaced by V_{BSUV}			V
V_{BSUV+}	V_{BS} supply undervoltage positive going threshold	Functionality not included in IR2166			8.0	9.0	10.0	
V_{BSUV-}	V_{BS} supply undervoltage negative going threshold				7.0	8.0	9.0	
I_{LKVS}	V_S offset supply leakage current	---	---	50	---	---	50	µA

Comments:

- **V_{CCUV}:** V_{CC} supply undervoltage thresholds have been increased for the IRS2166D compared to the IR2166 for proper operation of the integrated bootstrap functionality; increasing the thresholds might require an adjustment of the start-up resistor (R_{VCC}). It should also be noticed that a slightly tighter tolerance has been achieved.
- **I_{QCCUV}** and **I_{QCC}** are slightly higher for the IRS2166D compared to the IR2166 due to the use of a high-accuracy and lower temperature coefficient voltage reference that also consumes a little more current; this however should not impact the application.
- **I_{CC_RUN}:** although this parameter was not specified in IR2166, it is higher for the IRS2166D when compared to the IR2166, consequently the charge pump may need to be resized.
- **V_{CLAMP}:** the tolerance has been slightly improved for the IRS2166D when compared to the IR2166
- In the IRS2166D, (**V_{BSUV+}, V_{BSUV-}**) an undervoltage lockout function (UVLO) has been added for proper operation of the internal bootstrap MOSFET. The UVLO circuit guarantees that V_B is high enough before turning on HO and prevents the internal bootstrap MOSFET from being driven in the linear region (should V_B decrease too much).

Electrical Characteristics (cont'd)

Parameters		IR2166			IRS2166D			
PFC Error Amplifier Characteristics								
$I_{COMP,SOURCE}$	OTA error amplifier output current sourcing	5	30	55	20	30	40	µA
$I_{COMP,SINK}$	OTA error amplifier output current sinking	-62	-30	-12	-45	-35	-25	
V_{COMPOH}	OTA error amplifier output voltage swing (high state)	10.5	13.5	14.5	12.0	12.5	13.0	V
V_{COMPOL}	OTA error amplifier output voltage swing (low state)	---	0.25	4.0	0.2	0.3	0.4	
PFC Control Characteristics								
$V_{VBUSREG}$	V_{BUS} internal reference voltage (guaranteed by design)	3.7	4.0	4.2	3.9	4.0	4.1	V
$V_{VBUSOV+}$	V_{BUS} over-voltage comparator positive going threshold	Not specified in IR2166			4.1	4.3	4.5	
$V_{VBUSOV-}$	V_{BUS} over-voltage comparator negative going threshold	Not specified in IR2166			4.0	4.15	4.3	
V_{VBUSOV}	Overvoltage comparator threshold	3.8	4.3	4.7	Replaced by $V_{BUSOV+/-}$			V
$V_{VBUS\ HYS}$	Overvoltage comparator hysteresis	150	300	400	Replaced by $V_{BUSOV+/-}$			mV
V_{ZX}	ZX pin positive edge triggered threshold voltage	1.1	1.65	2	1.5	2	2.5	V
V_{ZXHYS}	ZX pin comparator hysteresis	75	300	800	100	300	500	mV
$V_{ZXclamp}$	ZX pin clamp voltage (high state)	6.3	7.5	9.1	5.7	6.7	7.7	V
t_{WD}	PFC watch-dog pulse interval	90	400	824	150	400	500	µs

PFC Protection Circuitry Characteristics								
$V_{VBUSUV-}$	V_{BUS} pin undervoltage reset threshold	2.6	3.0	3.3	2.7	3.0	3.3	V

Comments:

The IRS2166D contains a floating supply undervoltage lockout circuit. This is necessary because of the additional integrated bootstrap MOSFET. This circuit will guarantee that V_{BS} is high enough before turning on HO and will protect the external MOSFET from being driven in the linear region should V_{BS} decrease too much. Regarding the PFC control characteristics, $V_{VBUSREG}$ has tighter tolerances for the IRS2166D when compared to the IR2166 and allows more accurate V_{BUS} regulation.

Electrical Characteristics (cont'd)

Parameters		IR2166			IRS2166D			
Symbol	Definition	Min	Typ	Max	Min	Typ	Max	Units
Ballast Control Oscillator Characteristics								
f_{PH}	Preheat half-bridge oscillator frequency	73	78	84	73	76	81	kHz
f_{RUN}	Run half-bridge oscillator frequency	39	43	50	40	43	46	
D	Oscillator duty cycle	---	50	---	---	50	---	%
$t_{d,LO}$	LO output deadtime	0.7	1.0	1.5	0.7	1.0	1.5	µs
$t_{d,HO}$	HO output deadtime	0.7	1.0	1.5	0.7	1.0	1.5	
V_{CT+}	CT pin rising threshold voltage	6.8	8.4	10.7	7.8	8.4	9.0	V
V_{CT-}	CT pin falling threshold voltage	1.8	4.6	5.6	4.1	4.6	5.1	
Ballast Control Preheat Characteristics								
V_{CPHEOP}	CPH pin end of preheat threshold voltage	---	10	----	---	10.8	---	V
V_{CPHRUN}	CPH pin run mode threshold voltage	---	12	---	---	12.0	---	
I_{RPHLK}	RPH pin leakage current	---	0.1	---	---	0.1	---	µA
I_{CPH}	CPH pin charging current	2.6	3.2	4.6	2.6	3.6	4.6	
V_{CPHFLT}	CPH pin voltage in fault mode	---	0	---	---	0	---	V
Ballast Control Protection Circuitry Characteristics								
V_{CSTH+}	CS pin over-current sense threshold	0.91	1.2	1.3	1.125	1.25	1.375	V
n_{EVENTS}	CS pin fault counter number of events	25	75	90	70	100	140	
V_{SDTH+}	SD pin rising non-latched shutdown threshold voltage	4.5	5.2	5.6	4.5	5.0	5.5	V
V_{SDHYS}	SD pin 5.0 V threshold hysteresis	100	150	350	Replaced by V_{SDTH-}			mV
V_{SDTH-}	SD pin falling reset threshold voltage	Not specified for IR2166			2.7	3.0	3.3	V
$V_{SD,delay}$	Delay from V_{SDTH+} until LO goes low	Not specified				450		ns
$V_{EOLBIAS}$	EOL pin bias voltage	Not specified			1.8	2.0	2.2	V
$I_{EOL,SRC}$	EOL pin internal OTA source current	Different functionality in IR2166			---	10	---	µA
$I_{EOL,SNK}$	EOL pin internal OTA sink current				---	10	---	
V_{EOLTH+}	EOL pin rising latched shutdown threshold (active during RUN MODE)	2.4	3	3.6	2.7	3.0	3.3	V
V_{EOLTH-}	EOL pin falling latched shutdown threshold (active during RUN MODE)	0.7	1	1.3	0.9	1.0	1.1	V
V_{EOL_delay}	Delay from VEOLTH+ until LO goes low	Not specified			---	1	---	µs
V_{CTFLT}	CT pin fault mode voltage	---	0	---	---	0	---	V

V_{CPHFLT}	CPH pin fault mode voltage	---	0	---	---	0	---	

Comments:
Most of the parameters are the same with tighter tolerances (f_{RUN}, V_{CT+}, V_{CT-}, V_{CSTH+}, $V_{EOLTH+/-}$), while a few of them have slightly changed (f_{PH}, t_{dLO}, t_{dHO}); overall these small differences should have little (if any) impact on the application. For the IRS2166D, the V_{SDTH-} specification replaces the V_{SDHYS} of the IR2166 as the hysteresis of 150 mV typical at SD is replaced by 2 comparators with an equivalent hysteresis of 2 V and achieves consequently better noise immunity. Additional functionality has been included in the IRS2166D, like I_{EOL_SRC} and $I_{EOL-SNK}$ to increase the robustness of the bias without having an impact on the application.

Electrical Characteristics (cont'd)

Gate Driver Output Characteristics (HO, LO and PFC)								
V_{OL}	Low-level output voltage, LO, HO, PFC	---	0	100	---	COM	---	V
V_{OH}	High-level output voltage, LO, HO, PFC	---	0	100	---	V_{CC}	---	
t_r	Turn-on rise time	---	110	210	---	120	220	ns
t_f	Turn-off fall time	---	55	160	---	50	100	
I_{0+}	Source current	---	300	---	---	180	---	mA
I_{0-}	Sink current	---	400	---	---	260	---	
Bootstrap FET Characteristics								
$V_{B,ON}$	V_B when the bootstrap FET is on	Functionality not included in IR2166			13.2	13.7	---	V
$I_{B,CAP}$	V_B source current when FET is on				40	55	---	mA
$I_{B,10V}$	V_B source current when FET is on				9	12	---	

Comments:
Output rise and fall times are slightly longer due to a small decrease in the output source and sink currents.

STATE DIAGRAM

This diagram is updated to reflect the changes described above. The state diagram clearly shows that the SD function is disabled during ignition for the IRS2166D while it was active during ignition of the IR2166. This is to improve transient immunity during ignition.

CONCLUSIONS

In most cases the IR2166 will be easily and advantageously be replaced by the new leadfree IRS2166D. The application will benefit from a monolithic solution with integrating bootstrap functionality, an improved V_{BUS} regulation voltage tolerance, and an improved SD/EOL functionality.