Application Note AN-1091

Recommended PCB Via Design for International Rectifier's BGA and LGA Packages

By Kevin Hu, International Rectifier

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This application note discusses the Via-In-Pad PCB designs for mounting IR's BGA and LGA devices. Topics discussed include thermal performance advantage and reliability assesment when employing Via-In-Pad technology.

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Introduction

IR Ball Grid Array (BGA) and Land Grid Array (LGA) devices are high performance microelectronic devices designed to provide efficient and reliable operation. To ensure their high performance, Printed Circuit Board (PCB) via design is important. IR Application Notes AN-1028[1] and AN-1029[2] discuss PCB via recommendations for using IR BGA and LGA devices. To help remove heat from the device, in those two App Notes, it is recommended to have as many vias as possible underneath and in the immediate vicinity of the device. And the recommendations are focused on designs that vias are not in land pads. But to further improve thermal performance it is often desired to place vias in PCB land pads (Via-In-Pad). This will be discussed in this App Note.

1.0 Test Card Designs

Theoretically, the thermal performance gets better as more vias are added to the PCB. But in a study done by Lang and Wu [3], it is shown that placing vias in the solder pad gives a negligible thermal performance advantage. In order to evaluate the thermal advantage of adding vias to solder pad for IR power devices, four test cards were designed. Table 1 lists the four designs. All the vias in test cards are through-hole vias. All the test cards are 4 layer 1oz cards with the same overall thickness and dimensions.

Design	Via-In-Pad	Via Drill Hole	Via Wall	Via Capture Land	Via Pitch
1	No	13 mil	1 mil	25 mil	36 mil
2	Yes	10 mil	1 mil	18 mil	25 mil
3	Yes	15 mil	1 mil	27 mil	60 mil
4	Yes	20 mil	1 mil	32 mil	72 mil

Table 1 Test card designs

The test cards were designed based on the layout of IR's iP2003. Figure 1 shows the design with no vias in the solder pad. The vias in this design have a 13mil drill hole and a via capture land of 25mil diameter. Figure 2 shows the design with maximum amount of 10mil vias in the solder pad. The design in Figure 2 is used to check the thermal advantage of having maximum amount of vias in the solder pad area.

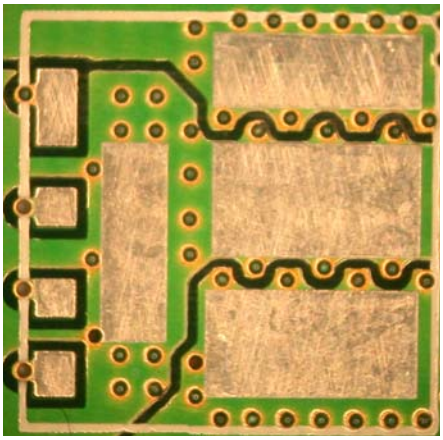

Figure 1. Test card design with no Via-In-Pad.

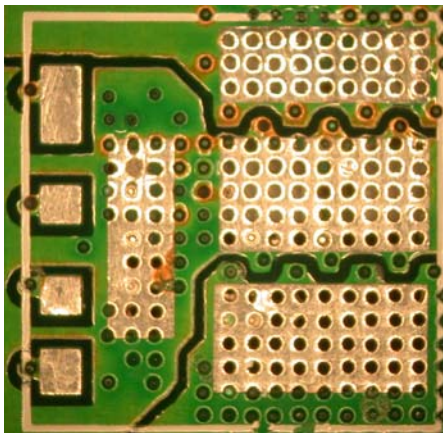

Figure 2. Test card design with 10mil Via-In-Pad.

2.0 Thermal Experiment

IR's iP2003 devices were mounted on the test cards for thermal experiment. Thermal test was done under nature convection condition with the room temperature at 23°C. All the devices were run at the same condition of f_{SW} = 1MHz, V_{IN} = 12V and I_{OUT} = 20A. Table 2 lists the steady state thermal test results of the four test card designs. The results show that having Via-In-Pad helps to drop the junction temperature about 3 to 5°C. The results, however, vary little with the size of vias in the solder pad area.

Design	Via-In-Pad	P_{loss} (W)	$T_{junction}$ [°C]	$(T_{junction}-T_{ambient})/P_{loss}$ [°C/W]
1	No Vias	5.80	104.8	14.1
2	Yes, 10mil	5.65	100.1	13.6
3	Yes, 15mil	5.79	102.7	13.8
4	Yes, 20mil	5.61	99.7	13.7

Table 2 Thermal test results

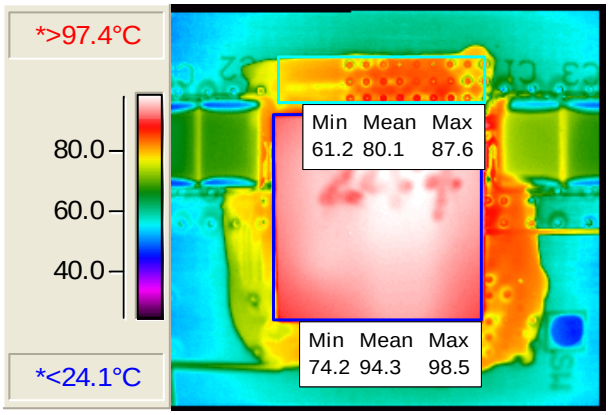

Figure 3. Infra-Red (IR) image of test card with no Via-In-Pad.

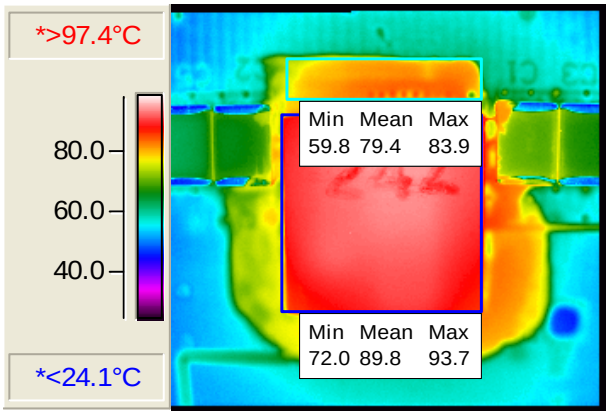

Figure 4. IR image of test card with 10mil Via-In-Pad.

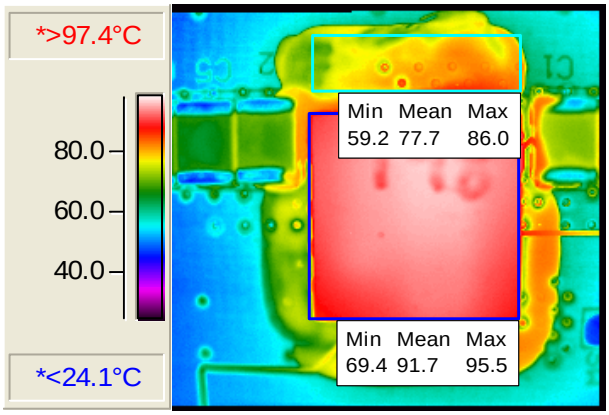

Figure 5. IR image of test card with 15mil Via-In-Pad.

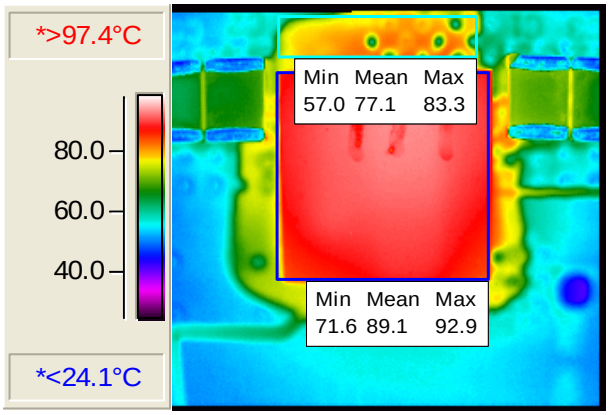

Figure 6. IR image of test card with 20 mil Via-In-Pad.

3.0 Reliability Test and Failure Analysis

In order to check if Via-In-Pad design will cause any reliability issues, the test cards of all four designs with iP2003 devices mounted were tested in temperature cycle (T/C) chamber. The test condition was -40 °C to 125 °C. Generally, the device power loss is sensitive to the quality of the solder joint between the device and the test card. So after 1000 cycles of T/C test the electrical test was done to check the device power loss. The results show that there are no noticeable performance differences among the four designs. Table 3 lists the average device power loss and the power loss shift percentage of each design after 1000 cycles of T/C test. After the 1000 cycles T/C test, the device condition represents the end of life condition. At this condition data shows that differences among these four designs are within error margin.

Design	Via-In-Pad	P_{loss} after T/C Test (W)	P_{loss} Shift [%]
1	No Vias	9.18	1.76
2	Yes, 10mil	9.10	1.34
3	Yes, 15mil	9.05	1.25
4	Yes, 20mil	9.03	1.51

Table 3 Power loss results after temperature cycle test.

After the T/C tests were extended to 2000 cycles, the test cards with devices mounted on were submitted for X-Ray and cross-section to check the solder joint quality of the different test cards designs. X-Ray shows that the solder void percentage of the solder joint between the device and the test card is nearly the same regardless there is Via-In-Pad or not. Cross-section study doesn't find much difference either. No solder joint fracturing or voiding was observed in any of the four designs. And the solder joints of the four designs are quite uniform as seen in Figure 7 - Figure 9. The solder joint thickness of the designs with Via-In-Pad is only slightly thinner than that of the design without Via-In-Pad. Figure 7 and Figure 8 show the cross-sections of the solder joints with 20mil vias in the solder pad and 10mil vias in the solder pad respectively. The solder joint appears very uniform with very little solder being wicked into the vias. Figure 9 is a typical cross-section of the solder joint that is observed in all the four different test card designs.

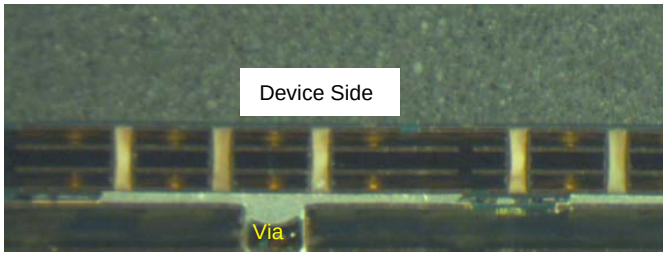

Figure 7 20-mil Via-In-Pad solder joint

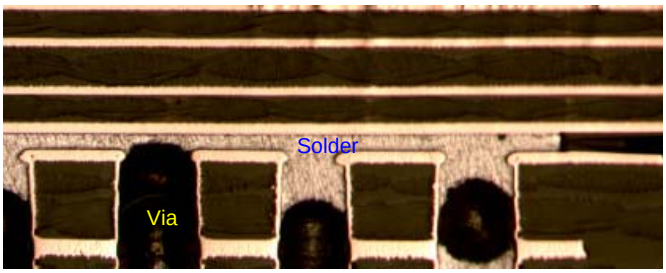

Figure 8 10-mil Via-In-Pad solder joint

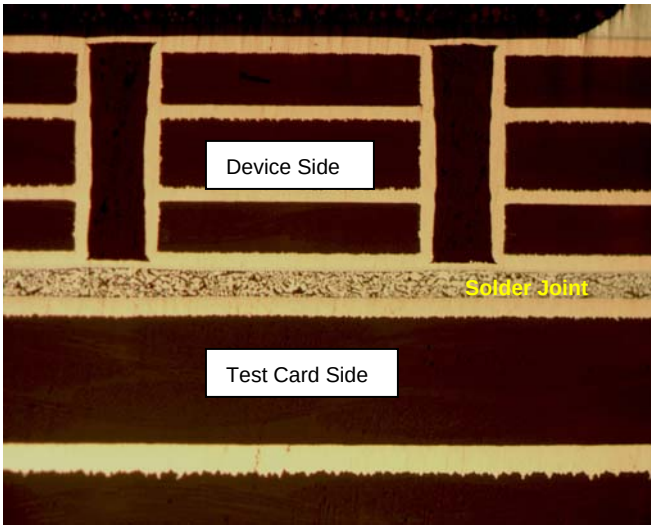

Figure 9 Via-In-Pad solder joint

4.0 Summary

This application note discusses the Via-In-Pad PCB designs for mounting IR's BGA and LGA devices. For BGA devices, it is not recommended to have through via right under solder balls. For LGA devices, given natural convection condition, the Via-In-Pad design is slightly better thermally than the design without vias in the solder pad. More thermal advantage is expected if the device is under forced convection condition. There is not much thermal performance difference among Via-In-Pad designs with different via sizes. If heat dissipation is not a concern it is recommended not to use Via-In-Pad design. If the Via-In-Pad design is strongly desired it is recommended to use the capped vias in pad. And, employ the through-hole Via-In-Pad only if capped vias are not feasible. The experimental results don't show any electrical or reliability performance difference between the through-hole Via-In-Pad design and the no Via-In-Pad design.

Even though very little solder loss down the vias was observed it is still recommended to use a minimum thickness of 6 mils stencil to prevent a possible starved solder joint if the through vias are desired in the solder pad.

References

[1] Kevin Hu, Recommended Design, Integration and Rework Guidelines for International Rectifier's BGA and LGA Packages, *International Rectifier Application Note AN-1028.*

[2] David Jauregui, Optimizing a PCB Layout for an iPowIR Technology Design, *International Rectifier Application Note AN-1029.*

[3] Dennis Lang and Chung-Lin Wu, Impact of Vias on Printed Circuit Board Thermal Performance, *IMAPS*, Nov. 2004.