

Application Note AN-1086

BV_{CES} Testing Considerations for Ultra-thin wafer Depletion Stop Trench IGBTs

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1. Abstract

The 600V Depletion Stop Trench IGBTs from IR utilize benefits of ultra-thin wafer technology to improve the conduction (V_{CEON}) and switching (E_{OFF}) performance. When the wafer thickness is reduced below 85 μm , looping is observed during the static break down voltage measurements. This looping characteristic is a result of the high gain of the PNP transistor part of the IGBT structure. Though the looping behavior can potentially harm the IGBT during the measurements, they do not have harmful effects on the performance of the IGBT in the application. This application note discusses the physics of the phenomenon, safe measurements methods, and the application considerations.

2. IGBT performance improvements with Depletion Stop Trench structure

IR has demonstrated that the ultra-thin wafer technology improves the performance of the NPT IGBTs. IR has a mature, high performance ultra-thin wafer NPT IGBT technology. Based on the extensive experience in processing ultra-thin wafers, IR has developed a new 600V Depletion Stop IGBT with trench cell targeted for Appliance Motion Control and other inverter applications. See Figure 1 for the NPT & Trench IGBT cell structures. Ultra-thin wafer Depletion Stop technology offers improved efficiency while maintaining the smooth turn-off characteristics and has robust SOA required for Hard-switching applications. The trench cell design has very low V_{CEON} because it increases the channel density and minimizes the JFET resistance inherent of the planar structure. Compared to the planar NPT device, the trench Depletion Stop IGBT has much lower conduction loss with lower total switching loss. By thinning the wafer to 70 μm and optimizing the N Depletion layer, the trench IGBT provides superior performance tradeoff in V_{ce} (on) and E_{TS} . See figure 2 for the V_{CEON} vs. E_{OFF} trade off values for Planar NPT & DS Trench ultra-thin wafer IGBTs.

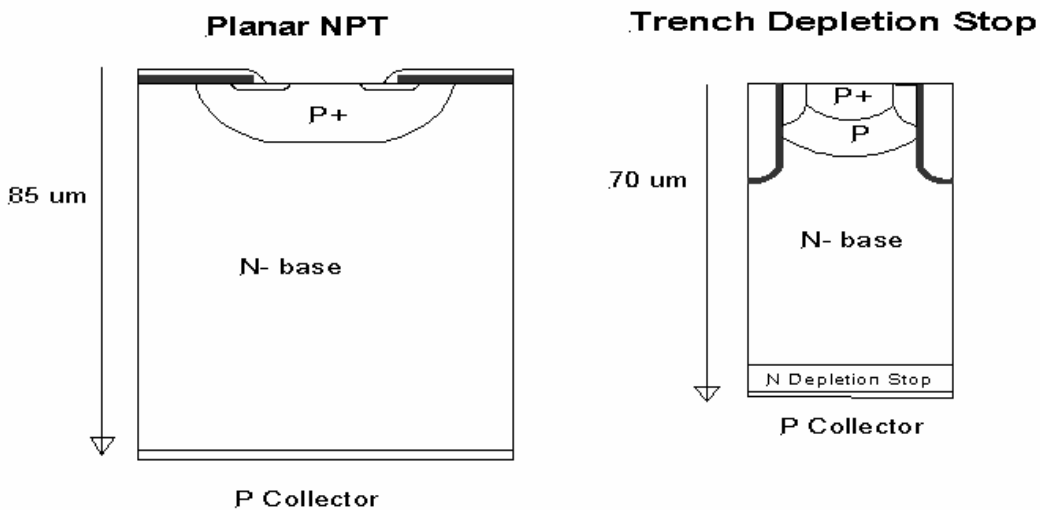


Fig 1. NPT & Depletion Stop Trench IGBT cell cross sections

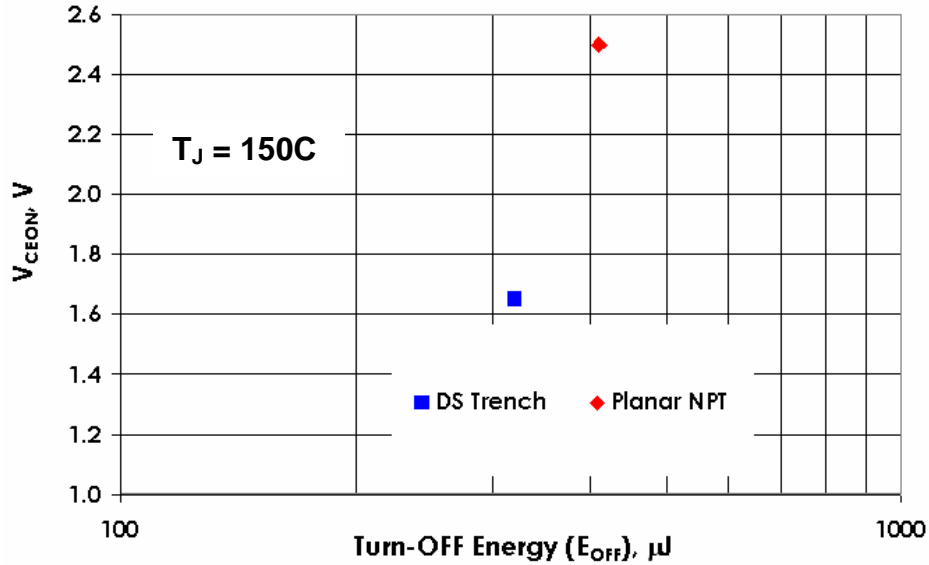


Figure 2. V_{CE0} vs. E_{OFF} Trade-OFF for Planar NPT IGBTs and DS Trench IGBTs

3. Breakdown Voltage of ultra-thin wafer Depletion Stop IGBTs

During the breakdown voltage measurement, a positive voltage is applied to the collector with respect to the Emitter with the Gate shorted to the Emitter. The forward breakdown voltage of Depletion Stop IGBT is limited by punch-through mechanism. See figure 3 for the electric field distribution in the DS trench IGBT cell cross section.

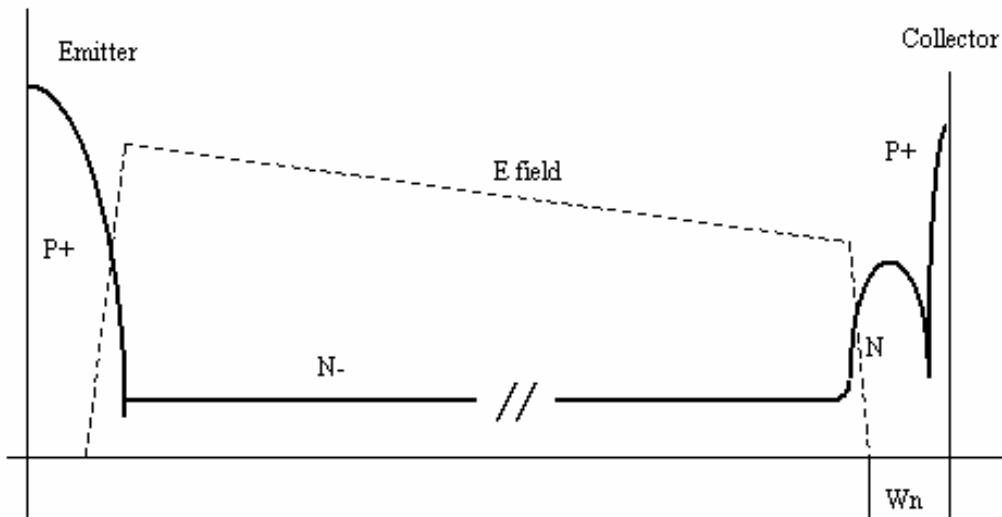


Figure 3. Filed Distribution within the Depletion Stop Trench IGBT structure

When the edge of depletion layer width of the reverse biased P+/N- junction approaches the P+ collector of the IGBT, injection of holes will occur causing and results in breakdown when the undepleted drift region portion (W_n) is less than one hole diffusion length. In this case open base transistor BV_{ceo} occurs when the product of electron multiplication coefficient and base transport factor becomes equal to unity. It can be demonstrated (Ref 1, pg 352) that

$$BV_{ceo} = V_B (1 - \alpha_T)^{1/6}$$

Where V_B = Avalanche Breakdown Voltage of the P⁺N⁻ junction,

$$\alpha_T = \text{Base Transport Factor} = 1 / \cosh [(W_n / \text{Sqrt} (D_p \tau_p))]$$

W_n = Undepleted Base Width, D_p = Hole Diffusion Coefficient, τ_p = Hole Carrier Lifetime.

In order to reduce conduction and switching losses, short N⁻ base and N Depletion Stop are required, along with high carrier lifetime to insure sufficient conductivity modulation of the N- base. As a result high base transport factor is achieved. The short N- base could also result in BV_{ceo} -type of characteristics, which cause looping behavior in static BV. The looping phenomenon is non destructive as long as the current is limited within the SOA capability of the device. If the current source used in an automatic tester (typically used in final probe and assembly) to perform the BV test has a high Voltage compliant, the variable load will result in uncontrolled repetitive current spikes that can damage the device. See Figure 4 for normal and loopy static BV waveforms as seen on a curve tracer.

When the loopy BV phenomenon occurs, it can be seen that the leakage current is low (40~60nA at 25C) up to the onset of avalanche breakdown, approx 700V. As soon as the impact ionization process starts, the secondary holes are injected into the base triggering the PNP transistor into BV_{ceo} mode. After the open base transistor breakdown the current through the N-drift region increases and this can result in depletion extension and further reduction of undepleted portion of the base (W_n). The depletion extension can be estimated by comparing the leakage current to the Kirk current density (Ref 2 p 224). Overall impact of this is increase in α_T and further reduction in voltage across the IGBT. This leads to device exhibiting negative resistance where voltage decreases with increasing current.

Due to the constant power provided by the curve tracer, the negative resistance developed as the avalanche current increases results in Current / Voltage looping. This looping will result in inconsistent break down voltage readings. Repetitive measurements can potentially damage the IGBT under test.

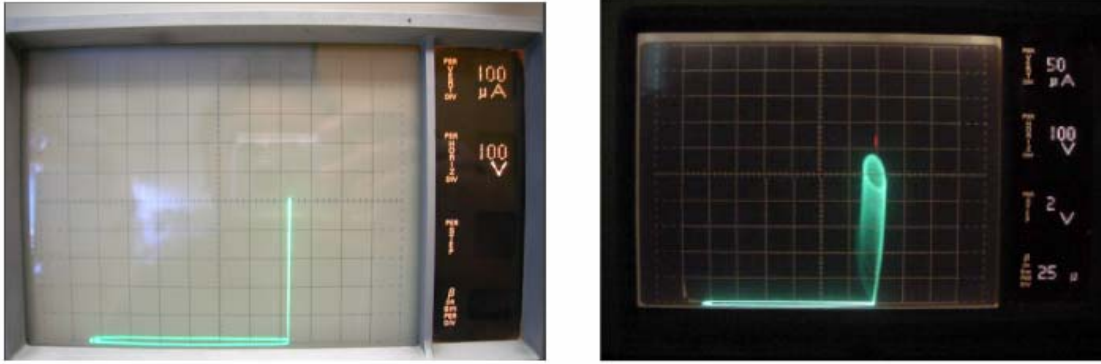


Figure 4. Normal & Loopy BV_{CES} waveforms

4. Performance of ultra-Thin wafer DS Trench IGBTs in the motion control Applications

The looping BV characteristic is not a concern in dynamic switching application. In a normal switching application, the bus voltage is typically well below the break down voltage of the IGBT and the switching waveforms do not show any looping behavior (Fig. 5). In the uncommon event where the IGBT is in dynamic avalanche, BV waveform remains stable (Fig 6) and does not show any oscillations. The device would not be damaged as long as the current is within SOA limits.

The DS trench IGBTs have Peak Current rating, I_{CM} & clamped inductive current rating, I_{LM} which are 4 times the continuous DC current rating at 100C case temperature. The DS trench IGBTs also have 5 μ s SCSOA at $T_J < 150C$, $V_{DC} = 400V$. Overall, the DS trench IGBTs is very rugged with excellent RBSOA capability.

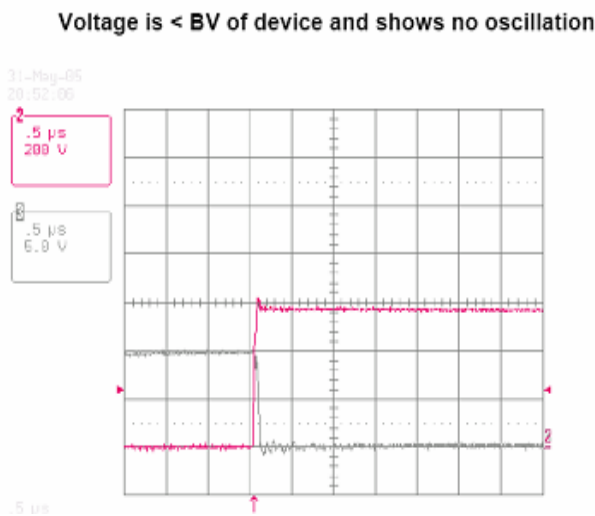


Figure 5 Inductive Load Current Turn-OFF Waveform ($V < 600V$) at $T_J = 150C$

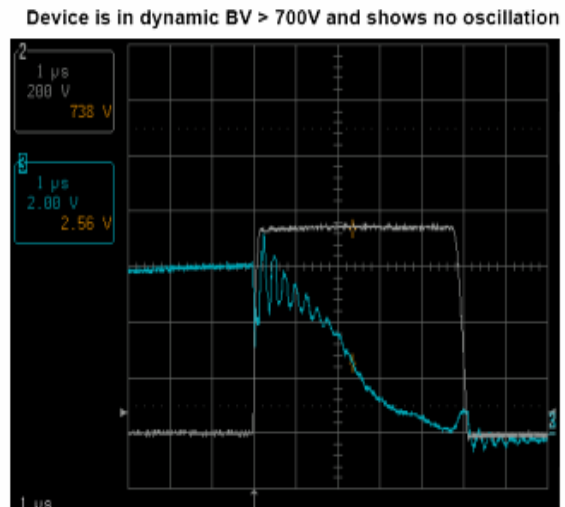


Figure 6 Unclamped Inductive Load Turn-OFF at $T_J = 150C$

5. Safe BV_{CES} Measurement methods

A filter was developed to enable a more reliable BV measurement without damaging the device. See figure 7 for the schematic of the typical filter circuit. An inductor was placed in series with the Collector Force to control the current spikes that the devices are subjected to when the BV starts to loop. An air-core inductor was selected for this set-up. The low pass RC filter enables consistent BV measurement. The RC filter averages the variations of the voltage signal. The effect of using a filter was validated using a Tektronix 370A curve tracer. The TEK 370A digitized waveform is an indication of what an automated tester would likely see. The analog waveform shown earlier is a real time display of the BV waveform. The current-voltage waveforms shown are for non-filter (Fig. 8) and filtered (Fig. 9) traces.

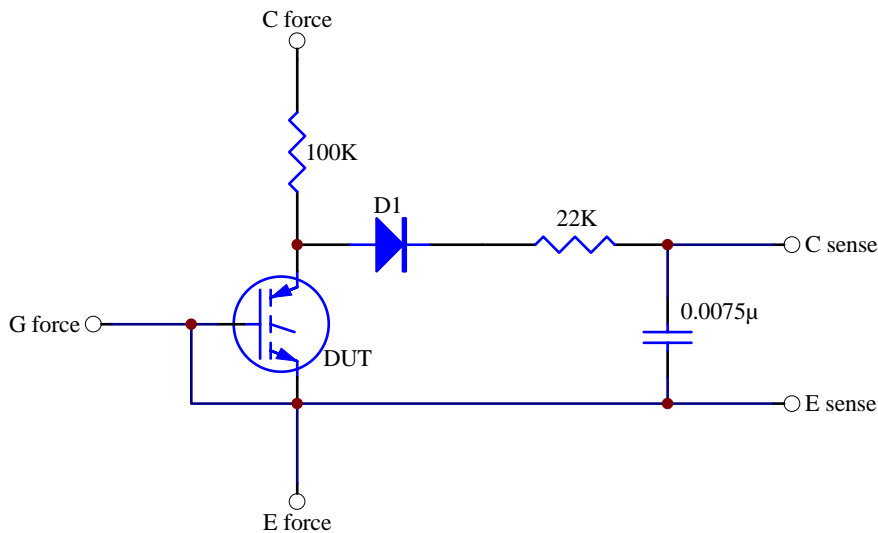


Figure 7. Typical Filter circuit schematic for the safe BV_{CES} measurement

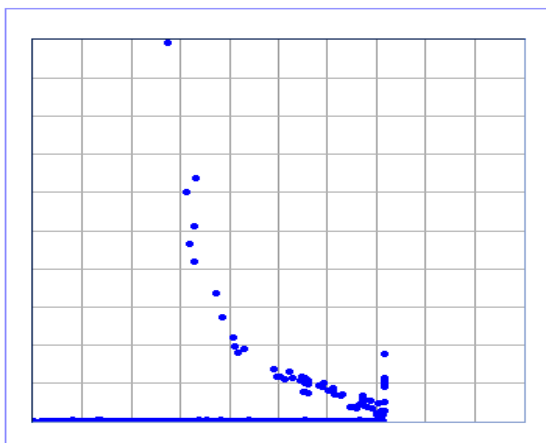


Figure 8. BV waveforms from the Tek 370A without the filter

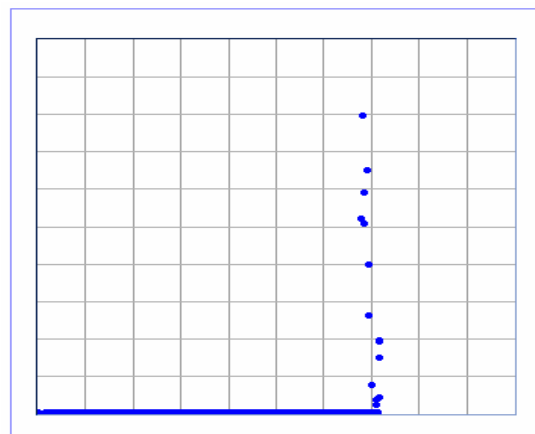


Figure 9. BV waveforms from the Tek 370A with the filter

For the automated testers (TESEC in particular), the test time was set to ensure a stable, repeatable and valid BV reading without compromising the device. The oscillograms below show (Fig.10 & 11) the BV waveforms without the filter.

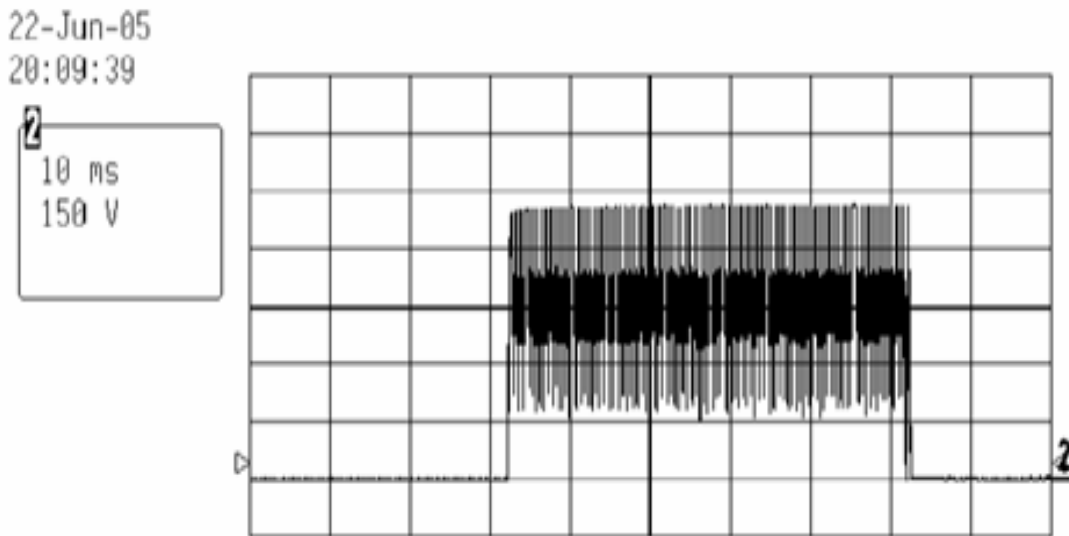


Figure 10 Compressed view of the BV as seen by TESEC w/o FILTER

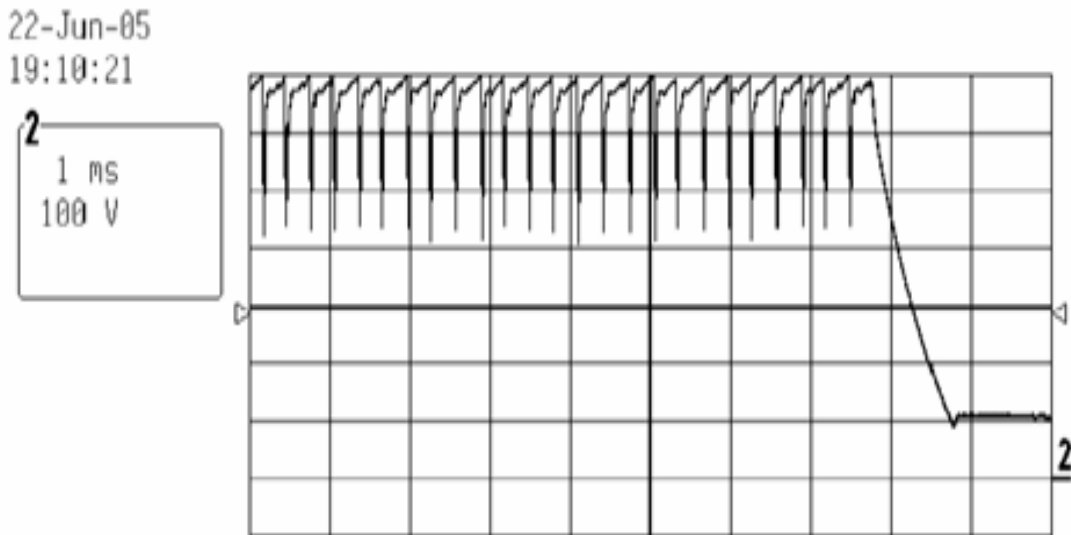


Figure 11 Expanded view of the BV as seen by the TESEC w/o FILTER

The oscillograms in Fig.12 and 13 show the same BV test condition with the filter installed. The optimum test time was determined for the given test BV current for various die sizes. The tester will

record the value seen 50 to 60 us before the end of test signal. Without the FILTER the number seen by the tester will depend on what the value it sees 50us before END of TEST.

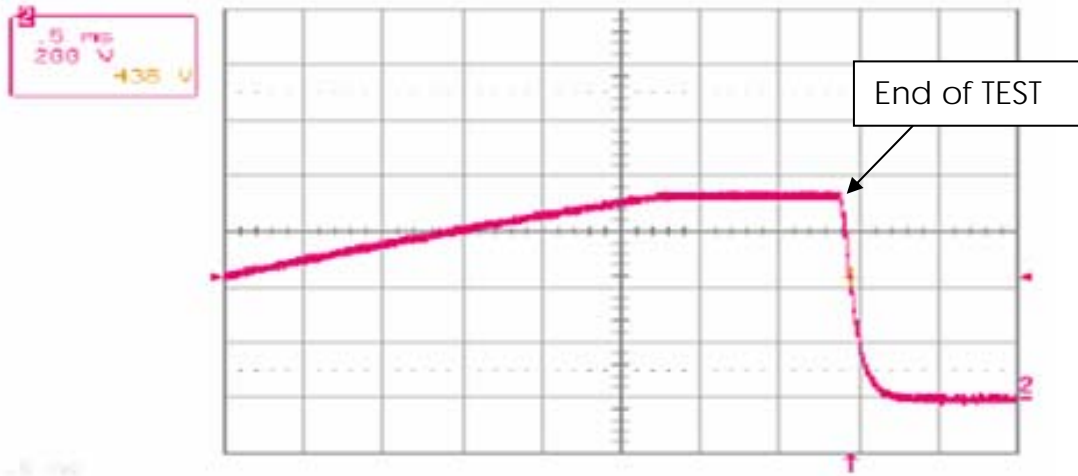


Figure 12. BV waveform as seen by TESEC w/ FILTER installed

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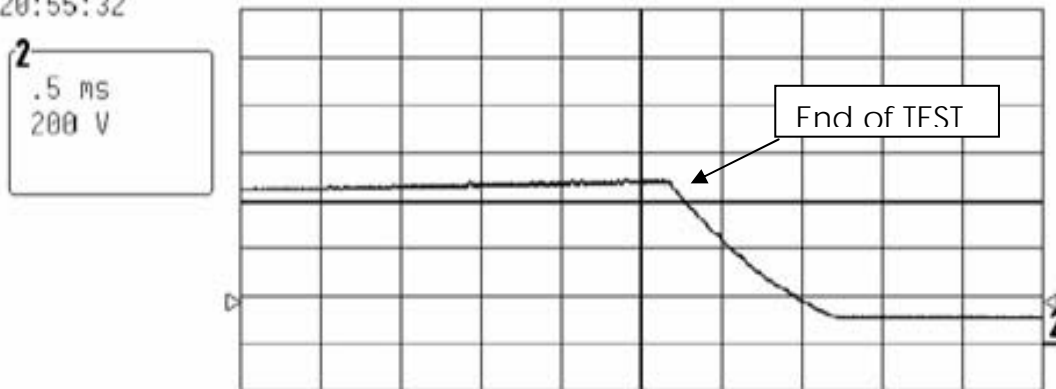


Figure 13. Minimum test time to ensure stable reading

6. Conclusions

The reduced V_{CEON} , E_{TS} , excellent ruggedness of the IGBTs and 5.0 uS SCSOA makes the ultra-thin wafer Depletion Stop Trench IGBTs the ideal switches for the motion control and other hard switched inverter applications.

Due to the high gain of the internal bipolar PNP, the current/voltage characteristic will exhibit a negative resistance behavior (usually 100uA to 1mA) when BV is measured in static mode. This behavior is typical for ultra-thin wafer bipolar transistors and IGBTs. The resulting current/voltage

looping can result in inconsistent break down voltage measurement and can potentially damage the device due to uncontrolled current spikes generated by the test equipment.

The BV looping characteristic is seen only during the static BV_{CES} measurements. The IGBT does not exhibit the looping BV characteristic under inductive load switching or dynamic avalanche conditions.

For safe BV_{CES} measurement, a filter was developed to protect the DUT and ensure consistent BV measurements for a wide range of die sizes and test current conditions. The effectiveness of the filter is validated on analog and digital curve tracers as well as automatic TESEC tester.

A guard-banded leakage test is recommended for incoming inspections to verify the parts will meet nominal voltage capability. If static BV_{ces} measurement is required, IR recommends the use of a BV filter described in this document. The actual component values for the filter, test time and the test sequence should be determined to suit the needs of the test equipment and the test methods employed.

References

- [1] V. K. Khanna: "IGBT, Theory and Design" – Wiley Inter Science, 2003, p.352
- [2] B.J. Baliga: "Power Semiconductor Device" – PWS Publishing Company, p. 224
- [3] M. Bairanzade: "Understanding Power Transistors Breakdown Parameter", ON-Semi AN 1628/D.