International
IOR Rectifier

Application Note AN-1075

Obtaining Low THD and high PF without A PFC

By Cecilia Contenti and Peter Green

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In some applications it can be desirable to have a regulated and boosted DC bus voltage and a high power factor, but the classical solution using an additional PFC inductor, an additional MOSFET and additional PFC IC (or the additional PFC control circuitry) can be too expensive for the cost range of the product. A typical case is low cost CFL (below 25W power). In these applications PFC is often not used because of cost but this causes very high harmonics and does not provide regulation when the AC line varies and the light level varies with the AC line. This application note shows a method of obtaining a boosted bus voltage with a high PF and reduced THD, requiring only an additional inductor without the PFC control IC.

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Obtaining low THD and high PF without a PFC IC

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I. Introduction

In some applications it can be desirable to have a regulated and boosted DC bus voltage and a high power factor, but the classical solution using an additional PFC inductor, an additional MOSFET and additional PFC IC (or the additional PFC control circuitry) can be too expensive for the cost range of the product. A typical case is low cost CFL (below 25W power). In these applications PFC is often not used because of cost but this causes very high harmonics and does not provide regulation when the AC line varies and the light level varies with the AC line.

This application note shows a method of obtaining a boosted bus voltage with a high PF and reduced THD, requiring only an additional inductor without the PFC control IC.

II. Test Results

A circuit using the new IR2520D 8 pin ballast control IC has been built and tested for performances. With 26W input power and 110VAC supply we measured PF=0.99, bus voltage = 350V and THD about 12%.

Figure 1 shows HB voltage, lamp voltage and DC bus voltage.

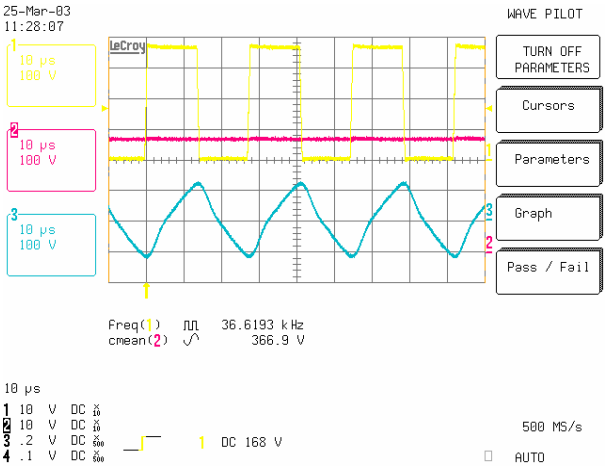


Fig.1: HB Voltage (yellow), DC bus voltage (red) and lamp voltage (blue).

III. Electrical Circuit

The control circuit proposed is shown in fig.2

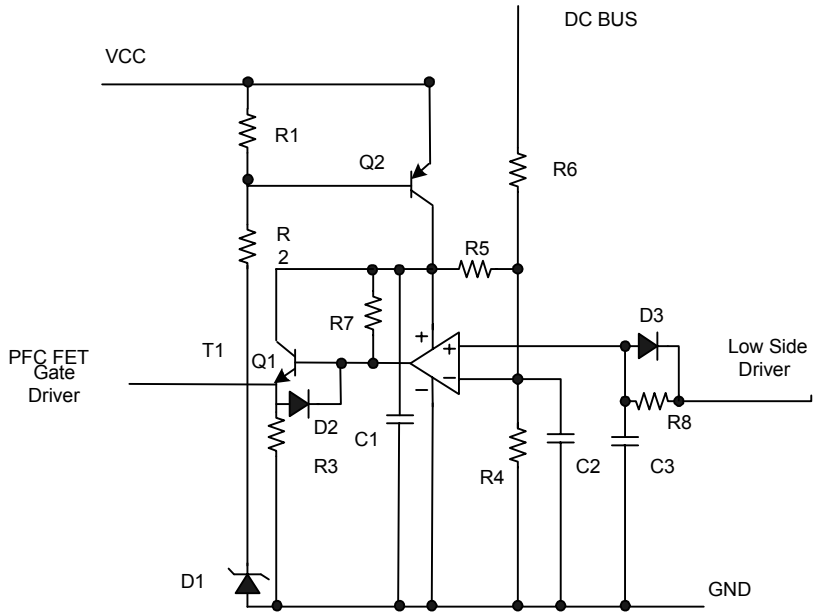


Fig.2: Boost regulation circuit

The circuit includes:
1) UVLO circuit for the comparator: R1, R2, D1, Q2 and C1. This is to prevent the PFC MOSFET from being switched on at any time before the IR2520D is out of UVLO and running normally. The additional circuit supplies the comparator only when the VCC voltage reaches 14V and the current is enough to switch on the zener diode that consequentially switch on Q2. Without this circuit the comparator could start to draw current before the supply voltage reaches the UVLO threshold of the IR2520D.

2) Boost regulation circuit: Comparator, R6, R4, C2, R5, D3, R8, R7 and C3. This circuit adjusts the on time of the PFC MOSFET. As the DC bus increases, the on time is reduced.

3) Driving stage for the PFC mosfet: Q1, D2 and R3. This is needed as the comparator output is open collector in order to produce sufficient gate drive current to switch on the FET with fast transition 0-15V.

The complete circuit tested in the lab is showed in fig. 3

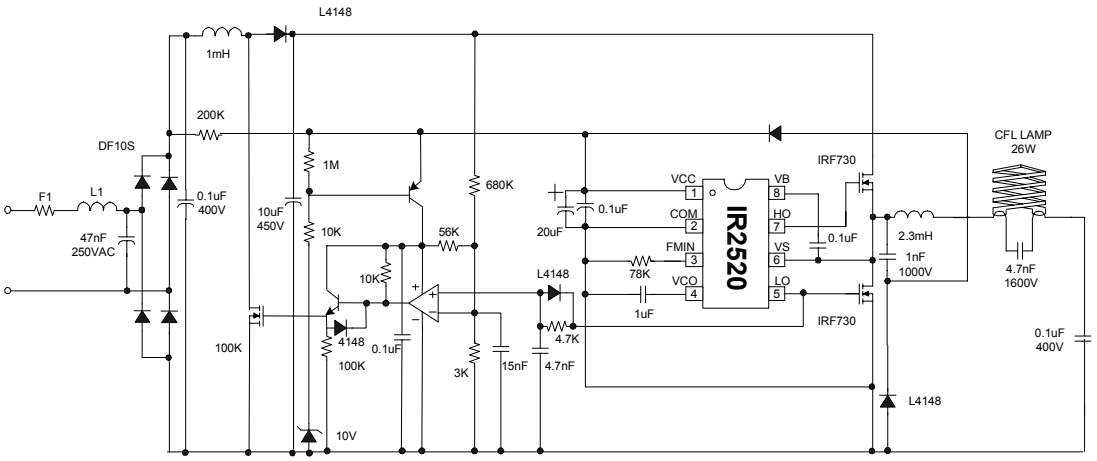


Fig. 3: Complete circuit.

IV. Circuit Functionality and method concept

The circuit is similar to a boost type PFC circuit working in critical conduction mode. When the PFC mosfet is turned on, the PFC inductor (1 mH) is connected between the rectified line input (+) and (-) causing the current in the PFC inductor to rise linearly. When the PFC mosfet is turned off, the PFC inductor is connected between the rectified line input (+) and the DC bus capacitor (10 uF) (through the PFC diode) and the stored energy in the PFC inductor causes current to flow into the bus capacitor. As the PFC Mosfet is turned on and off at a high frequency, the voltage on CBUS charges up to a specified voltage.

The feedback loop adjusts the bus voltage by continuously monitoring the DC voltage and adjusting the on-time of the PFC mosfet accordingly. In this way the maximum DC bus voltage is limited to a level where the feedback voltage is greater than the maximum point of the saw tooth waveform, which is approximately 5V. The duty cycle will be greater when the DC bus is low allowing it to increase more rapidly to the desired level. This system allows some degree of line and load compensation but does not produce true regulation of the DC bus. Consequently this approach is suitable for a limited range of supply voltage only and works very well for a typical 120VAC line US application.

The load compensation is sufficient to prevent excessive voltage existing on the DC bus during preheat when the load is relatively light. For an increasing DC bus the on-time is decreased, and for a decreasing DC bus the on-time is increased.

The duty cycle of the signal driving the PFC mosfet is determined by comparing a fraction of the DC Bus voltage with a reference saw tooth wave generated using the signal in the LO pin used to drive the Low Side fet of the half bridge. The comparator produces a positive output whenever the voltage in the 0-5V saw tooth-wave generated with the signal in the LO pin exceeds the fraction of the DC bus voltage.

In this way the on time of the PFC mosfet can be adjusted between 0 (0% duty cycle), when the DC bus voltage is high, and a maximum (50% duty cycle) when the bus voltage is low.

Figure 4 shows the saw tooth- wave generated with the signal in the LO pin, the bus voltage reference and the PFC mosfet gate driver voltage.

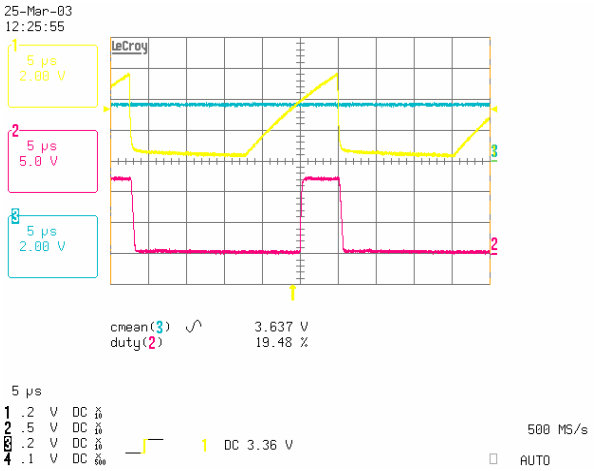
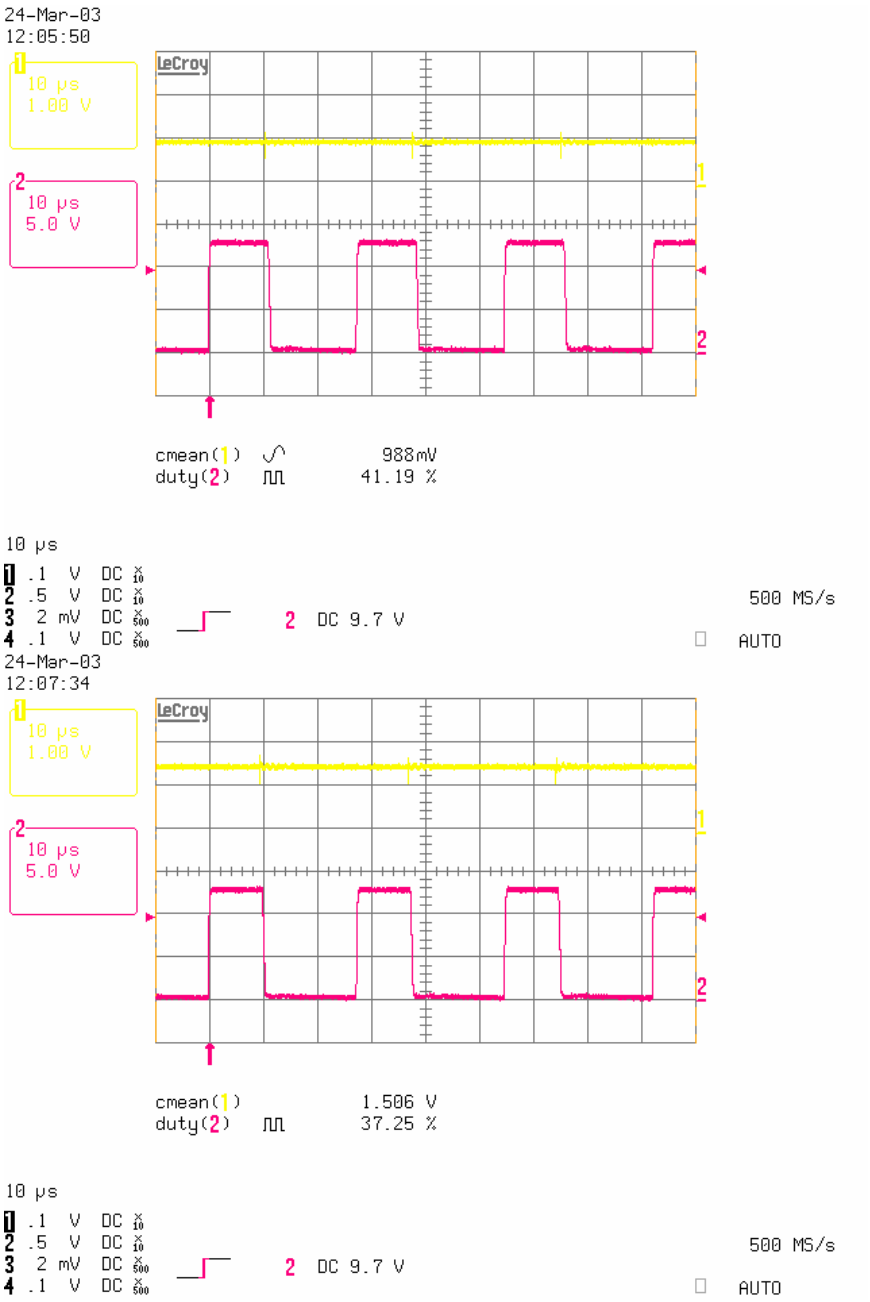
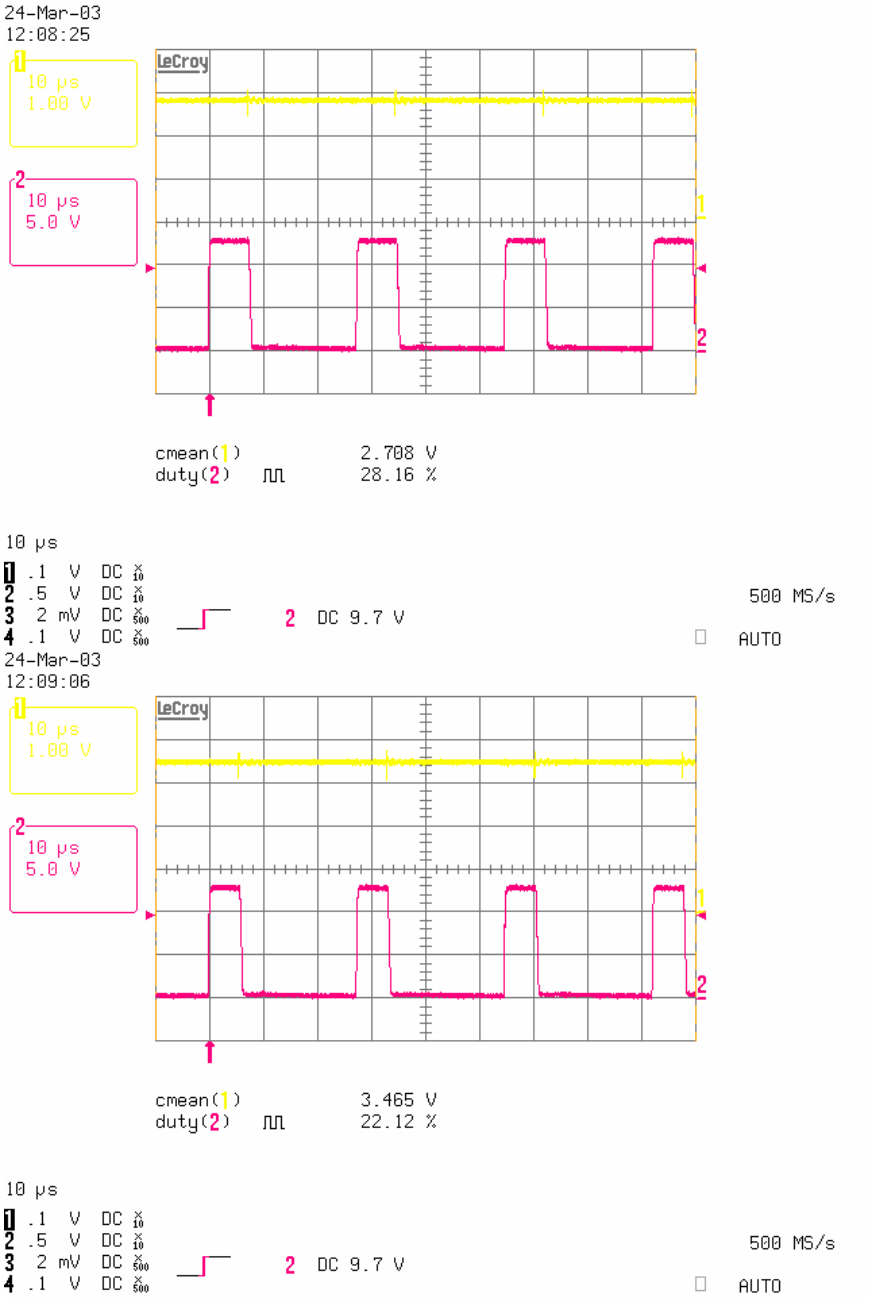


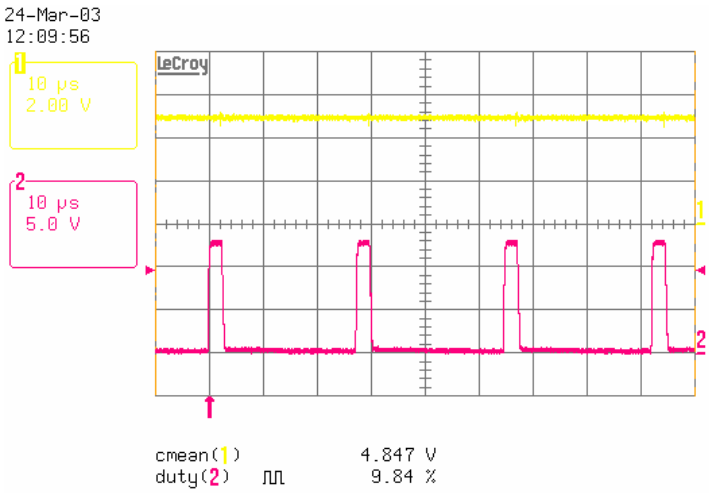
Fig. 4: Saw tooth- wave generated with the signal in the LO pin (yellow), bus voltage reference (blue) and PFC mosfet gate driver signal (red).

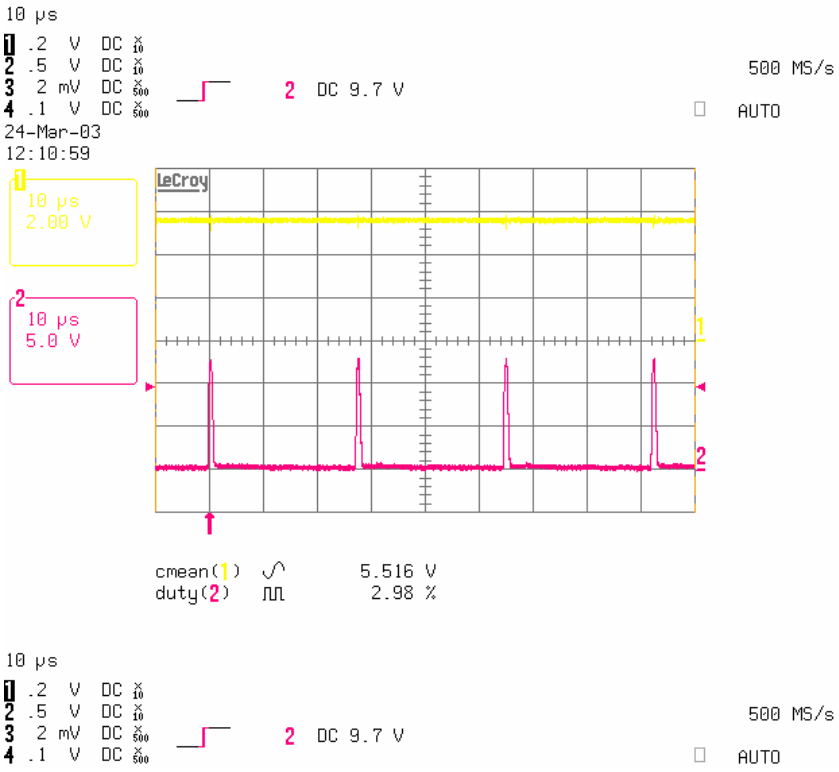
The DC bus regulation resulting from this technique is 350Vdc with an input range of 90-130 VAC. The bus value or the AC range can be regulated changing the value of the fraction of DC bus used as negative threshold. To set 320V with 90-130VAC we used R4= 3.9K resistor, to get the same bus voltage with 220V input you need R4=6.8K resistor.
The following figures (Fig. 5) show the waveform in the PFC mosfet gate driver for different values of the voltage in the – pin of the comparator (bus voltage derivate).

As you can see, in case of over voltage the duty cycle is zero and the PFC MOSFET is always off.


24-Mar-03
12:05:50
10 µs
1.00 V
2
10 µs
5.0 V
LeCroy
1
2
cmean(1) 988mV
duty(2) 41.19 %
10 µs
1 .1 V DC
2 .5 V DC
3 2 mV DC
4 .1 V DC
2 DC 9.7 V
500 MS/s
AUTO
24-Mar-03
12:07:34
10 µs
1.00 V
2
10 µs
5.0 V
LeCroy
1
2
cmean(1) 1.506 V
duty(2) 37.25 %
10 µs
1 .1 V DC
2 .5 V DC
3 2 mV DC
4 .1 V DC
2 DC 9.7 V
500 MS/s
AUTO


24-Mar-03
12:08:25
LeCroy
10 µs
1.00 V
10 µs
5.0 V
cmean(1) 2.708 V
duty(2) 28.16 %
10 µs
1 .1 V DC
2 .5 V DC
3 2 mV DC
4 .1 V DC
2 DC 9.7 V
500 MS/s
AUTO
24-Mar-03
12:09:06
LeCroy
10 µs
1.00 V
10 µs
5.0 V
cmean(1) 3.465 V
duty(2) 22.12 %
10 µs
1 .1 V DC
2 .5 V DC
3 2 mV DC
4 .1 V DC
2 DC 9.7 V
500 MS/s
AUTO


24-Mar-03
12:09:56
LeCroy
1
10 µs
2.00 V
2
10 µs
5.0 V
cmean(1) 4.847 V
duty(2) 9.84 %


10 µs
1 .2 V DC
2 .5 V DC
3 2 mV DC
4 .1 V DC
2 DC 9.7 V
500 MS/s
AUTO
24-Mar-03
12:10:59
LeCroy
1
10 µs
2.00 V
2
10 µs
5.0 V
cmean(1) 5.516 V
duty(2) 2.98 %
10 µs
1 .2 V DC
2 .5 V DC
3 2 mV DC
4 .1 V DC
2 DC 9.7 V
500 MS/s
AUTO

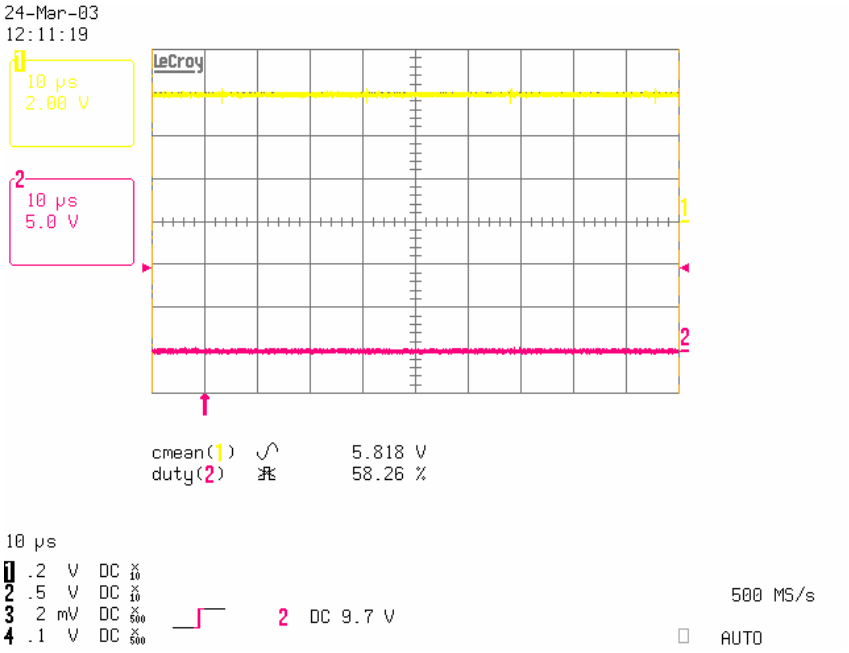


Fig. 5: waveform in the PFC mosfet gate driver for different values of the voltage in the – pin of the comparator (bus voltage derivate).

V. Comparison with Traditional Method

Figure 7 shows the block diagram of a traditional PFC circuit and figure 8 shows the equivalent circuit with a standard PFC IC.

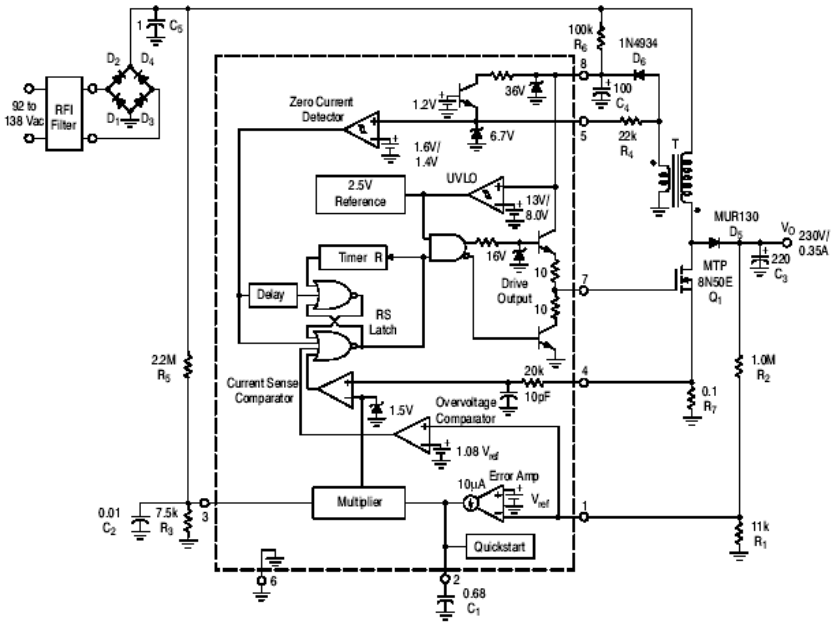


Fig. 7: Traditional PFC circuit

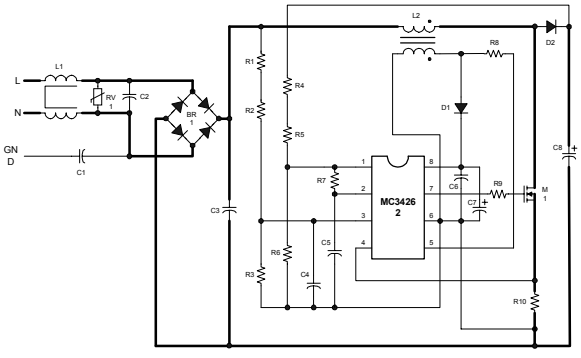


Fig. 8: PFC control section

Main advantages:

Reduced cost and component count and only 3 control pins (instead than 6 like other PFC control method). The components saved are:

1) No AC line sensing, this saves 5 components.
2) No PFC MOSFET current sensing (this saves a high precision resistor and simplifies the layout)
3) No zero crossing of current sensing (this saves 1 component and a secondary winding in the PFC inductor)
4) Saves a multiplier to sense the power
5) Saves the error amplifier
6) Saves a comparator for the over voltage detection
7) Saves a comparator for the zero current detection
8) Saves the additional circuitry for the PFC control: multiplier, latch, PWM, timer & Logic Multiplier

Disadvantage:

1) The range of VAC in which we obtain low THD and good PFC is narrow (about 40 VAC)
2) The method realizes a bus compensation, not a bus regulation.
3) No protections against continuous mode.

VI. CONCLUSIONS

This application note shows a new method to obtain a boosted bus voltage regulation that is cheaper than the standard active power factor correction. This method allows high PF and reduced THD, requiring only an additional inductor without the PFC control IC. A circuit using the new IR2520D ballast control IC has been built and tested for performance. With 26W input power and 110VAC supply we measured PF=0.99, bus voltage = 350V and THD about 12%. This system allows some degree of line and load compensation but does not produce true regulation of the DC bus. Consequently this approach is suitable for a limited range of supply voltage only. Main advantages: reduced cost and components count. Disadvantages: the range of VAC in which we obtain low THD and good PFC is narrow (about 40 VAC), the method realizes a bus compensation, not a bus regulation and does not offer protection against continuous mode.