International
IOR Rectifier

APPLICATION NOTE

Application Note 1072 revA

CFL Ballast with Passive Valley Fill & Crest Factor Control

by
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I. INTRODUCTION

In some applications it is desirable to have a regulated and boosted DC bus voltage and a high power factor, but the classical solution using an additional inductor, an additional FET and an additional IC can be too expensive for the cost range of the product. The goal is a tradeoff between performance and cost. A typical case is low cost CFL (below 25W power). In these applications PFC is often not used because of cost but this causes very high harmonics and does not provide regulation when the AC line varies and the light level varies with the AC line.

In this application note we will try to find a trade off between high PF and low THD and costs. The goal of this design is to implement a 14W CFL ballast which conform to these specs:

1) Total Harmonic distortion (THD) < 30 %
2) Power Factor (PF) > 0.85
3) Lamp Current Crest Factor Ipk/Irms (CF) < 1.7
4) Input: 220-240VAC
5) Cheaper than an active PF solution.

II. Functional Description

A 14W CFL ballast has been designed and tested for performance. The circuit is based on a resonant topology driven by a MOSFET half bridge. The circuit is controlled by the IR2520D Ballast Control IC from IR that provides lamp preheat, lamp ignition, running mode and fault protection (lamp fault, open filaments, failure to strike, deactivated lamp and low AC line).

To achieve high PF a Passive Valley Fill configuration has been used on the input stage, a diode and resistor has been added at the standard Passive Valley Fill configuration to reduce THD.

High Crest Factor of the lamp current is intrinsic in a Passive Valley Fill Configuration because of the bus shape. The crest factor is very high because the bus voltage changes between 2 different values, very different between each other: about VACpk and 1/2VAC pk. The current associated at the minimum bus voltage will be more than the double of the current associated to the maximum bus voltage and the intrinsic crest factor will be higher than 2. This is valid in case of constant frequency. Using a resistor to limit the harmonics increases the crest factor even further because the minimum bus voltage decreases. Figure 1 shows the bus voltage shape (in yellow) and the lamp current shape in blue) in a circuit with Passive Valley Fill configuration using a 1K resistor to reduce the harmonics.

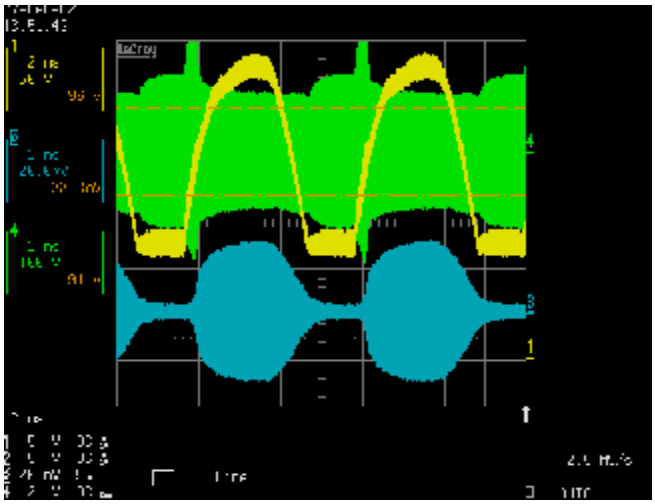

Fig. 1: Bus voltage shape (in yellow) and the lamp current shape (in blue) in a circuit with Passive Valley Fill configuration. In green the lamp voltage.

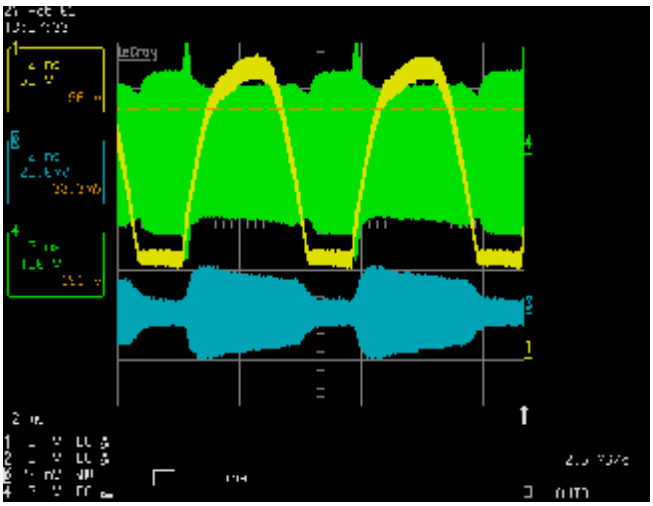

Fig. 2: Bus voltage shape (in yellow) and the lamp current shape (in blue) in a circuit with Passive Valley Fill configuration and frequency modulation. In green the lamp voltage.

To limit the crest factor an additional circuit has been used to modulate the frequency of the Half Bridge versus the DC Bus Voltage value. The circuit increases the frequency when the DC bus increases above a threshold, limiting the crest factor of the current.

Figure 2 shows the effect of the frequency modulation on the lamp current.

III. Electrical circuit

Figure 4 shows the complete electrical circuit and Table 1 shows the Bill Of Materials.

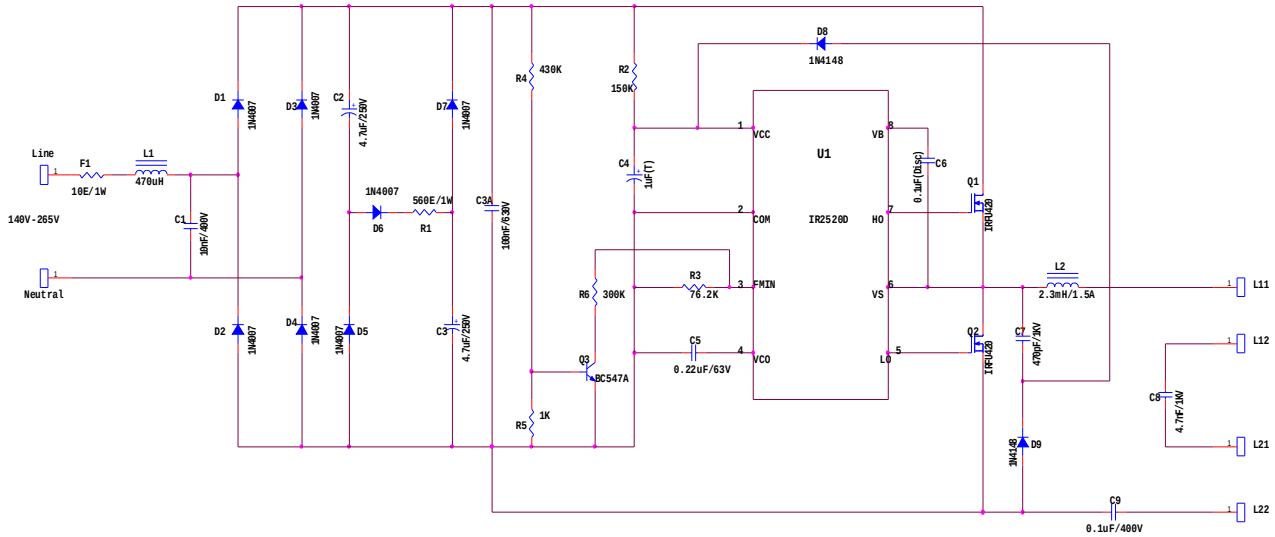

Fig. 4: Electrical Circuit - 14W CFL Ballast

Sl No	Reference	Description	Qty	Type	Make
1	R1	560E/1W	1	CFR	
2	R2	150K	1	CFR	
3	R3	75K,1%	1	MFR	
4	R4	430K	1	CFR	
5	R5	1K	1	CFR	
6	R6	300K	1	CFR	
7	C1	10nF/250V(X2)	1	X2 Type	Box type ,Philips
8	C2,C3	4.7uF/250V	2	Electr	Keltron
9	C3A	0.1uF/630V	1	PPC	Philips
10	C4	1uF(T) bead	1	Tantulum	Keltron
11	C5	0.1uF/63V	1	MP	Usha
12	C6	0.1uF(Disc)	1	Disc	
13	C7	470pF/1KV	1	Ceramic	
14	C8	4.7nF/1KV	1	PPC	Philips
15	C9	0.1uF/400V	1	PPC	Philips
16	D1-D7	1N4007	7	1A,1000V	
17	D8,D9	1N4148	2	0.15A,75V	
18	**Q1,Q2**	**IRF820**	**2**	**TO-220**	**IR**
19	Q3	BC547	1		
20	**U1**	**IR2520D**	**1**	**DIP8**	**IR**
21	L1	470uH	1	Beads	
22	L2	2.3mH/1.5A	1	EE13	#30swg, 185T
23	Bare PCB		1	39mm Dia	
24	F1	10E/1W(Optional)	1		

Table 1: Bill Of Materials for 14W CFL, 220V-240V Input. Different lamp types will require component changes.

The circuit includes resonant output stage (C8, L2), rectification (D1, D2, D3, D4), standard EMI filter and input stage (L1, C1, C3A, F1), half bridge (Q1, Q2), ballast control IC IR2520D (U1) and circuitry needed around the IC (C6, C4, R3, C5), charge pump to supply the IR2520D (R2, D9), snubber cap (C7), Passive Valley Fill low THD configuration (C2, C3, D6, R1, D5, D7) and crest factor control circuit (R4, R5, Q3, R6).
R3 programs the minimum frequency of the IR2520D. During steady state the IR2520D will oscillate at the minimum frequency in case of zero voltage switching condition. If non- zero voltage switching is detected, the IR2520D will increase automatically the frequency until reaching zero-voltage switching operation. C5 programs the startup time, setting the preheat time.
The idea of the crest factor control method is to avoid constant frequency operation and to use 2 different frequencies: minimum frequency for minimum bus voltage and an higher frequency for maximum bus voltage. An higher frequency will cause a lower voltage and current on the lamp, decreasing the maximum value the current will reach at the maximum bus voltage.

The crest factor control circuit generates 2 different frequencies adding a resistor R6 in parallel to the resistor R3 when the transistor Q3 is on. The new working frequency of the IR2520D will depend on the parallel between R6 and R3 and will be bigger than the frequency determined by R3 alone. The transistor Q3 will turn on when the voltage between base and emitter, which is determined by R5, will exceed the conduction threshold of the transistor Q3.

Summarizing, when the bus is low the IR2520D will oscillate at the minimum frequency, determined by R3 and when instead the bus voltage exceeds a certain value (determined by R5 and R4), the IR2520D will oscillate at an higher frequency, determined by the parallel of R3 and R6.

IV. Design Procedure

The design procedure is:

1) Select C8 and L2 to have the right preheat on the lamp in the preheat time and the right lamp power at about 40KHz (refer to AN-1066 for IR2520D for design procedure)
2) Select C5 to have the right preheat time
   Increase C5 to increase the preheat time (refer to AN-1066 for IR2520D design procedure)
3) Select R3 to have the right minimu frequency (fmin), Input Power slightly higher than the input power needed (14W + 4W)
   Increase R3 to decrease fmin and increase Input Power

Key point on the design:

4) R1 reduces the THD and the harmonics related to Passive Valley Fill configuration:

Start with R1=0 and increase R1 until THD is inside the spec. Higher R1 will cause lower minimum bus voltage and so higher crest factor of the current and can cause multiple ignition on the lamp, so R1 should be selected as low as possible.

5) R5 set the bus voltage threshold value. When the bus voltage exceed this threshold, the Half Bridge frequency will start to increase above fmin

   Adjust the value of R5 so that the Vbus threshold is selected around (Vbus max – Vbus min) / 2

6) R6 set the maximum frequency when the bus voltage is maximum, determined by R3 parallel R6

   For bus voltage < Bus voltage threshold f(R5)
   f = f min= f(R3)
   For bus Voltage > Bus voltage threshold f(R5)
   f = fmax (R3 parallel R6)

   In reality, above the Bus Voltage threshold, we will have a range in witch the frequency will be between fmin and fmax. Start with R6 = 300K and decrease the frequency to decrease the crest factor. This operation will increase the maximum frequency fmax.
   To decrease the crest factor you can either decrease R6 to increase fmax and so the amount of frequency modulation, either adjust the value of R5. Decreasing the crest factor you will decrease the input power (because you will work more time at fmax if changing R1 or the same time at a higher fmax by changing R6), if the power decreases

too much you can increase the value of R3 to decrease fmin.

7) Adjust (Increase) again the value of R3 to guarantee the right input power. This operation will increase the minimum frequency fmin.

In reality fmin depends also on C8 if non-zero voltage switching occurs because the IR2520D will work above fmin in case of non-zero voltage switching. To avoid this we could increase C8.

8) Increase C8 in case of non- zero voltage switching or to increase the preheat on the lamp if a longer lamp life is needed.

V. Test Results

Table 2 shows the electrical parameters measured in our lab.

Vrms	220.5V	240.2V
Irms	59.62mA	60.85mA
Pin	12.604W	0.95
PF	0.951	13.895W
THD	28.20%	29.10%
Lamp CF	1.7	1.75
3rd	15.86%	16.84%
5th	6.68%	7.75%
7th	16.92%	16.99%
9th	6.79%	5.96%

Table 2: Electrical parameters.

Figure 5 shows the lamp current.

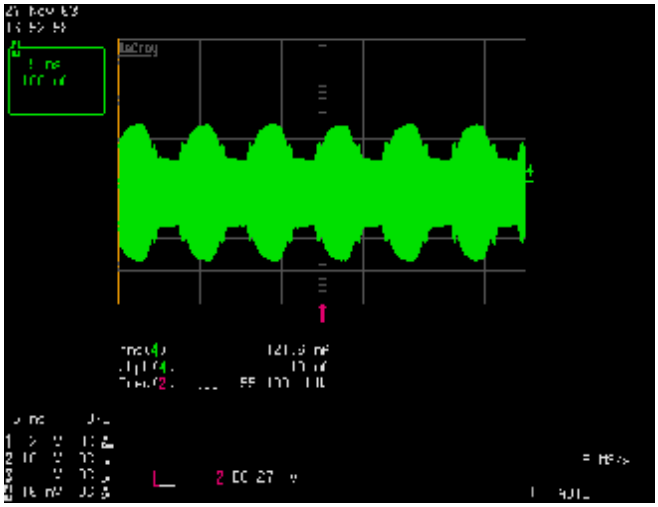

Fig. 5: Lamp current.

The Crest Factor can be calculated as peak value divided average value of current,

Crest Factor = 419/121.6 = 0.7

Figure 6 shows the frequency modulation. You can see the 2 different frequencies: fmin for minimum bus voltage and fmax for maximum bus voltage.

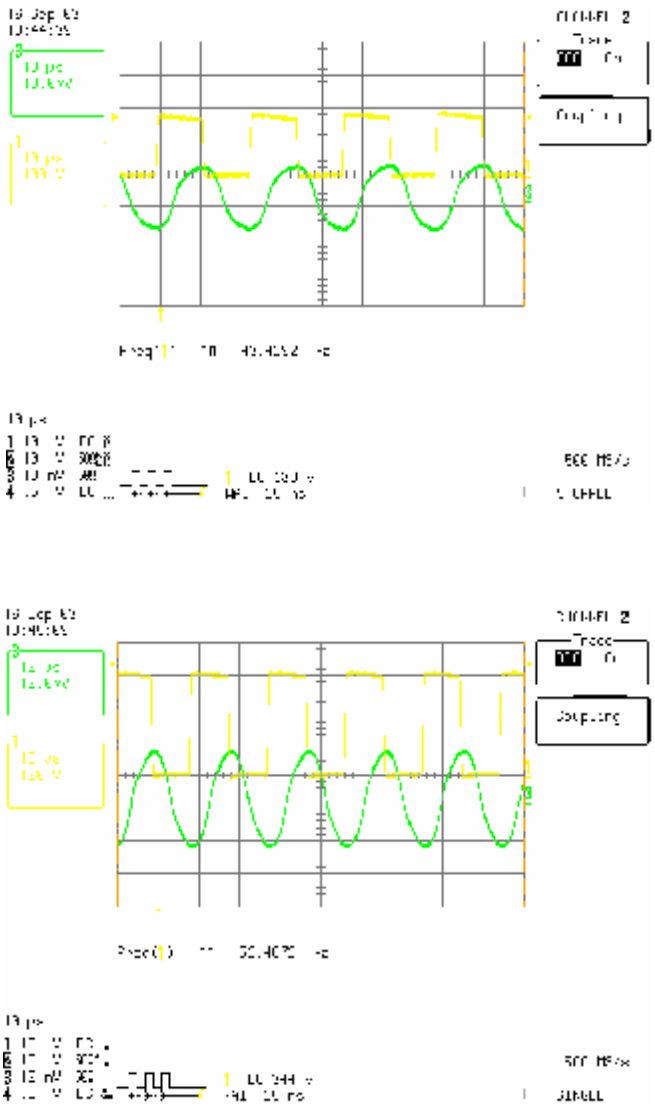

Fig. 6: VS pin of the IR2520D in yellow and lamp current in green.

Figure 7 shows the bus voltage and the lamp current.

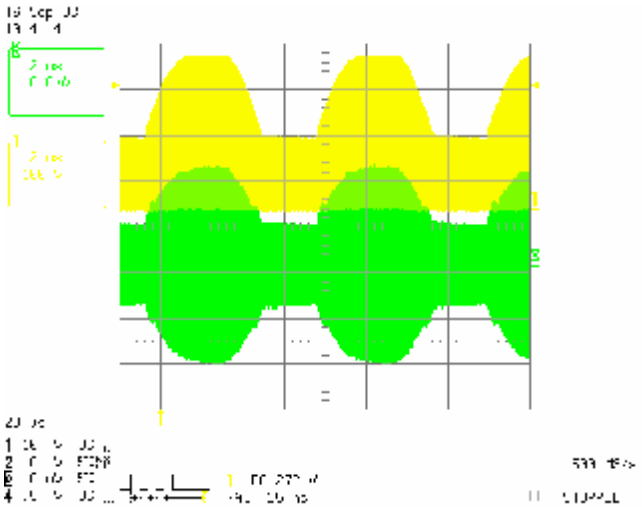

Fig. 7: Bus voltage (yellow waveform) and lamp current (green waveform).

The best trade of for the circuit is:
R5=1K, R3 = 76.2K, R6 = 300K, R1 = 560 ohm
Crest factor is 1.7 with these values.
To improve further the crest factor
Step 1) reduce R1 to 500 ohm (this will slightly increase THD)
Step 2) Decrease R6 up to when crest factor is OK
With 250K crest factor is <1.7 and power is still acceptable (12.3W)
Step 3) Increase R3 to increase the Input power if power becomes too low. If this does not increase power because of non zero voltage switching (fmin does not decreases), increase C8 (this will also improve the preheat).

VI. Conclusion:

The IR2520D is a very versatile and flexible building block to design the typical functions of electronic ballast in a cheap and easy way. In this application note we discussed a solution to obtain high power factor in a cheaper way than using an active PF configuration. To achieve high PF a Passive Valley Fill configuration has been used on the input stage, a diode and resistor has been added at the standard Passive Valley Fill configuration to reduce THD. To limit the crest factor an additional circuit has been used to modulate the frequency of the Half Bridge versus the DC Bus Voltage value.
The resulting circuit allows:
1) Total Harmonic distortion (THD) < 30 %
2) Power Factor (PF) > 0.85
3) Lamp Current Crest Factor Ipk/Irms (CF) < 1.7
4) Input: 220-240VAC and input power 14W.
The Same circuit, (R6, Q3, R5 and R4) could be used in a circuit with IR2520D in also in a standard configuration with bus capacitor and rectification for:

1) Stabilize the lamp power (or current or voltage) versus bus voltage changes due to AC line changes
2) Allow a smaller bus capacitor in every type of CFL circuit
3) Reduce EMI through frequency wobble (peach of EMI spread in a frequency range instead than at a constant frequency).

NOTE: Please be advised that anyone making, using or selling a ballast that uses the circuit shown in this application note may need to obtain a license under U.S. patent no. 6141230.