International
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Application Note AN-1053

Power-up Sequencing Techniques Using *i*P1201 & *i*P1202

by David Jauregui, International Rectifier

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Many of today's high performance DSPs and ASICs require two well regulated voltage supplies. Furthermore, these ICs require special care of its voltage rails during the power-up sequence. Violating the power-up sequence required by the IC can cause a latch-up condition and/or degrade the long-term reliability of the IC.

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Introduction

Many of today's high performance DSPs and ASICs require two well regulated voltage supplies. Furthermore, these ICs require special care of its voltage rails during the power-up sequence. Violating the power-up sequence required by the IC can cause a latch-up condition and/or degrade the long-term reliability of the IC.

There are three types of power-up sequencing: Sequential, Ratiometric, and Simultaneous (see Figure 1). This application note will address how to implement these types of power-up sequencing with iP1201/2 designs. In all three cases, the input supply (V_{IN}) is held constant and the ENABLE pin is used to initiate the power-up sequence.

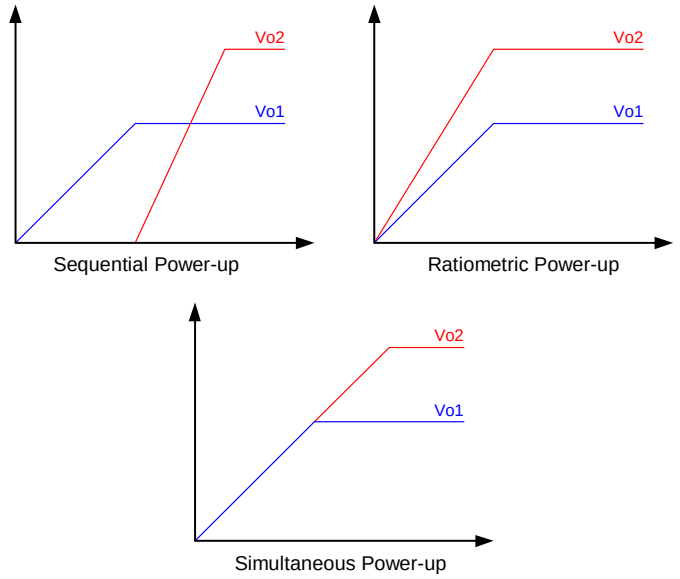

Figure 1 power-up sequencing types

Power-up Sequencing Approaches

Sequential Power-up

Sequential power-up energizes each rail in sequence, meaning that typically, the second rail will be enabled after the first rail reaches its normal operation point.

Sequential power-up can be easily implemented in iP1201/2 designs by tuning the soft start capacitors. Use the following formula for setting the value of the soft start capacitors:

$$C_{SS2} = 2.25 \times C_{SS1}$$

Where C_{SS2} = Soft start capacitor for output 2

C_{SS1} = Soft start capacitor for output 1

Figure 2 is an example of sequential power-up using iP1201/2. Output 1 is set to 1.5V and has a soft start capacitor value of 0.1µF. Output 2 is set to 2.5V and has a soft start capacitor value of 0.22µF.

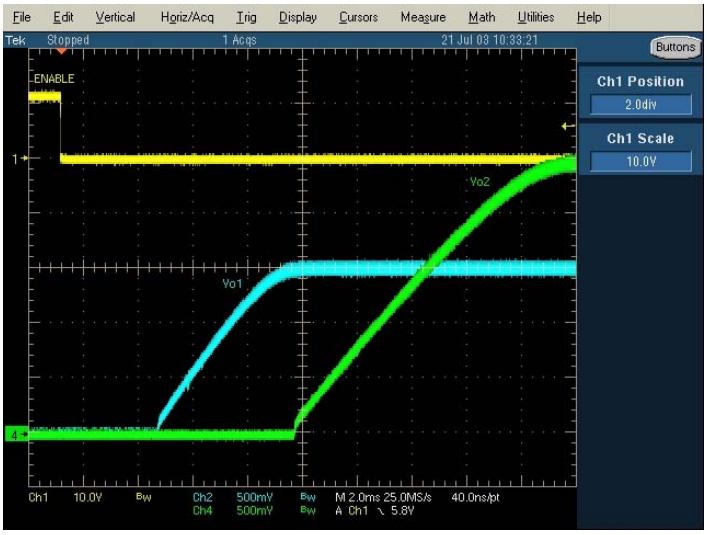

Figure 2 Sequential power-up

Ratiometric Power-up

Ratiometric power-up energizes both rails at the same time. In addition, both rails reach regulation at the same time. The ratio of differential voltage is held constant throughout the power-up sequence. This requires the higher voltage rail to have a higher slew rate.

Ratiometric power-up can be easily implemented in iP1201/2 designs through two methods.

1. Tying SS1 and SS2 pins together to one common soft start capacitor creates a precise power-up sequence (see Figure 3). In this configuration, the over current protection (OCP) needs to be set to latch mode. To due so, the HICCUP pin needs to be tied to ground (see Figure 4).
2. Tying SS1 and SS2 pins to individual soft start capacitors creates the same power-up sequence. The capacitance tolerance will dictate the precision during power-up. A 0.1µF, 16V, X7R, 10% capacitor was used in this experiment (see Figure 5). In this configuration, OCP can be set to either latch mode or hiccup mode (see Figure 6).

The output voltage slew rate in method 1 will be approximately twice that of method 2 if the same value soft start capacitor is used because there are two soft start current sources feeding one capacitor in method 1. This is

evident in figures 3 & 5 by comparing the time scales of each graph (1.0ms/div versus 2.0ms/div).

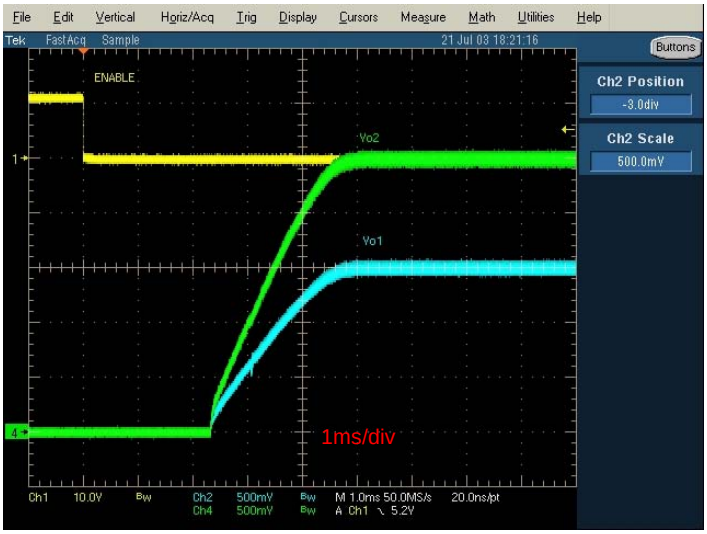

Figure 3 Ratiometric power-up using one soft start cap

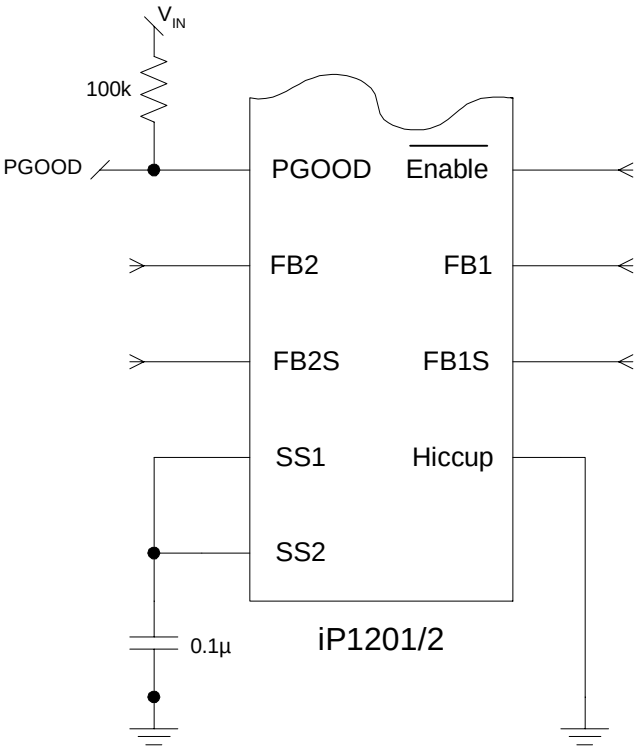

Figure 4 Ratiometric configuration using one soft start cap

Figure 5 Ratiometric power-up using two soft start caps

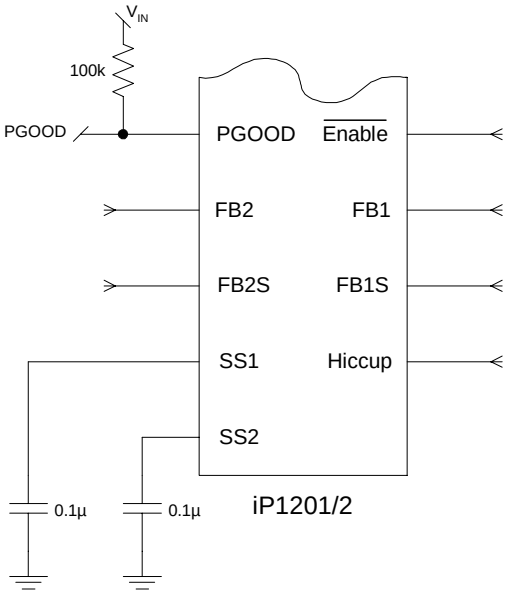

Figure 6 Ratiometric configuration using two soft start caps

Simultaneous Power-up

Simultaneous power-up energizes both rails at the same time. In addition, the differential voltage between rails during power-up is minimized until the lower of the two rails reaches its normal operating point. This requires both rails to have the same slew rate.

Simultaneous power-up can be implemented in iP1201/2 designs through the aid of two external MOSFETs (see Figure 7). At power up, both rails regulate to the lower of the two required output voltages and slew at the same rate (both SS pins tied to one capacitor). Upon reaching their nominal operating point, the PGOOD pin will drive the two

FETs (Q1 & Q2) and concurrently introduce a parallel impedance to RA and RB. This will cause the second rail to regulate to a higher level (see Figure 8).

The small delay before the two rails separate is caused by the time it takes to reach the turn on threshold of the external FETs. Tying both soft start pins to one capacitor can precisely control the difference in voltage rails during power-up (see Figure 9). In this configuration, OCP must be set to latch mode.

Simultaneous power-up can also be achieved by using two separate soft start capacitors, one for each soft start pin (see Figure 10). The capacitance tolerance will dictate the differential voltage precision during power-up (see Figure 11). A 0.1uF, 16V, X7R, 10% capacitor was used in this experiment. In this configuration, over current protection can be set to either latch mode or hiccup mode.

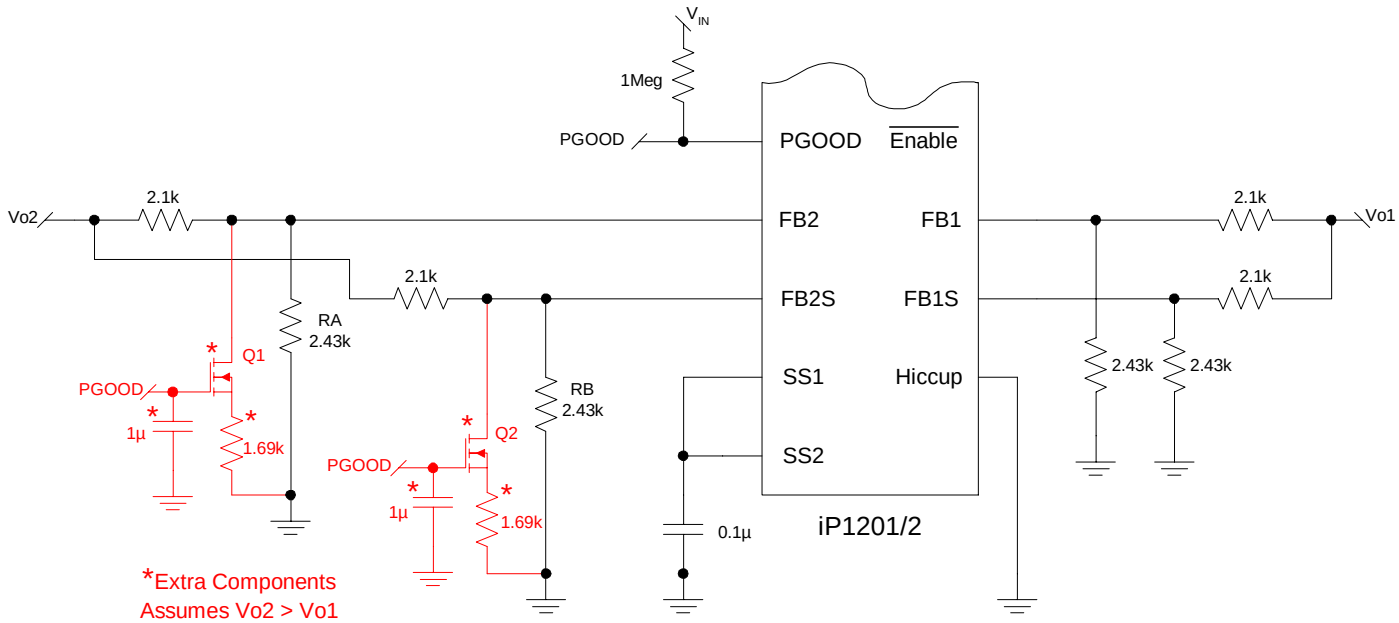

Figure 7 Simultaneous configuration using one soft start capacitor

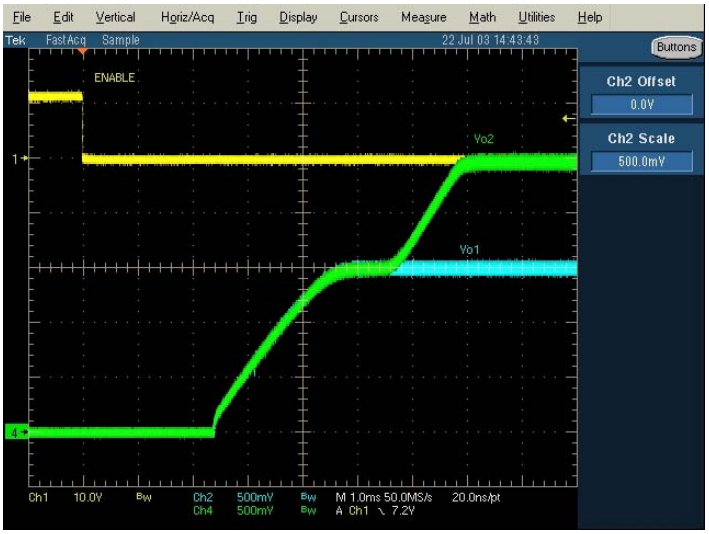

Figure 8 Simultaneous power-up using one soft start cap

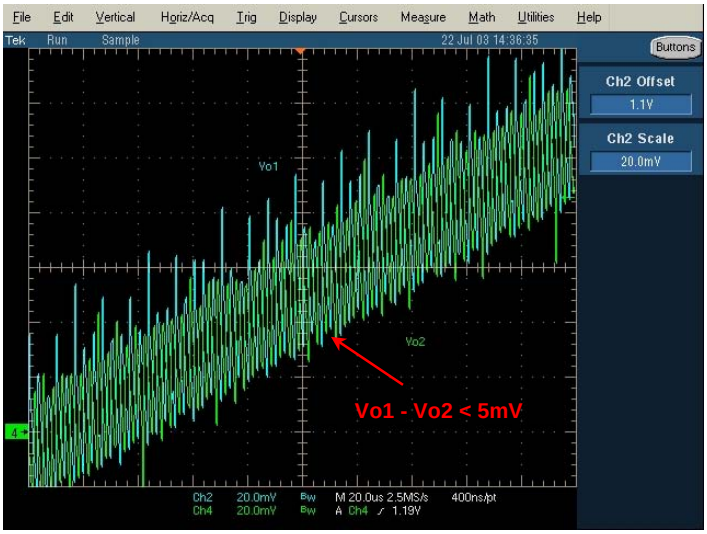

Figure 9 Differential voltage during simultaneous power-up

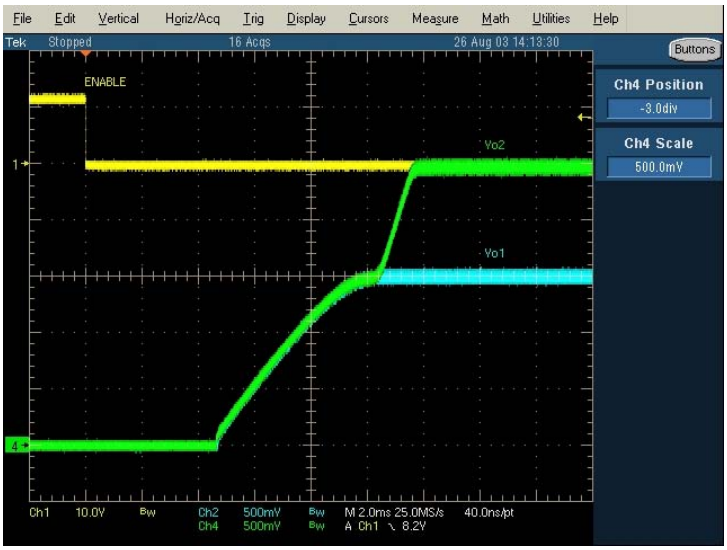

Figure 10 Simultaneous power-up using two soft start cap

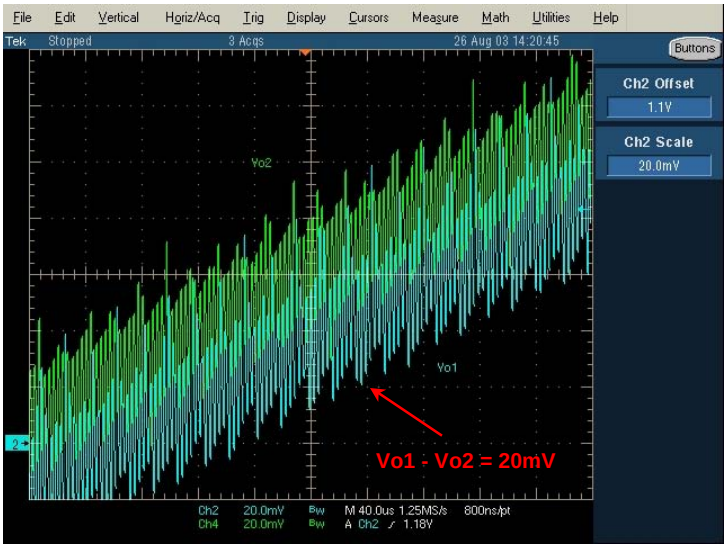

Figure 11 Differential voltage during simultaneous power-up

Conclusion

It is important to properly sequence the voltage rails during power-up on dual supply ASICs and DSPs. iP1201/2 designs can easily implement all three types of power-up sequencing through the aide of simple and low cost external components.