

Application Note AN-1014

Using The Current Sensing IR212X Gate Drive ICs

By Jonathan Adams

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There are four single channel devices which incorporate current sensing. The IR2121 and IR2125 are low and high side drivers respectively, which have a high output drive (1A source /2A sink). The current sensing circuit for these two devices uses a timing circuit via the ERR pin to program the time between over-current detection and latched shutdown. The IR2127 and IR2128 are both high side drivers (IR2127-active high input/ IR2128 active low input), with a lower output drive (200mA source/420mA sink), and a more basic current sensing scheme. For applications where the output needs to be ON for long periods of time, or if the load has a reasonable impedance (>500Ω) the bootstrap capacitor voltage (V_{bs}) may start to droop. In this case a charge pump circuit may be needed.

APPLICATION NOTE

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TOPICS COVERED

Introduction to the Devices
Current Sense Operation
Current Sensing Circuit Configurations
Layout Considerations

1) INTRODUCTION TO THE DEVICES

There are four single channel devices which incorporate current sensing. The IR2121 and IR2125 are low and high side drivers respectively, which have a high output drive (1A source /2A sink). The current sensing circuit for these two devices uses a timing circuit via the ERR pin to program the time between over-current detection and latched shutdown. The IR2127 and IR2128 are both high side drivers (IR2127-active high input/ IR2128 active low input), with a lower output drive (200mA source/420mA sink), and a more basic current sensing scheme.

For applications where the output needs to be ON for long periods of time, or if the load has a reasonable impedance (>500Ω) the bootstrap capacitor voltage (V_{bs}) may start to droop. In this case a charge pump circuit may be needed (see application note **AN978**). For help with selecting the Bootstrap components see **DT98-2 "Bootstrap Component Selection For Control IC's"**.

2) CURRENT SENSE OPERATION

IR2127/IR2128 Current Sensing Function

A typical connection for the IR2127/IR2128 is shown in fig 1). The CS pin is the pin used for sensing the current. The sensing circuit includes a blanking time to ensure there is no nuisance tripping during device switch on (the IC initially ignores the voltage at the CS pin, immediately after the output has turned on for a time equal to the blanking time, nominally 750ns). After the blanking time has elapsed if a CS voltage above the threshold is still present, then the IC turns off the output, and sets the FAULT pin low (NOTE: The fault pin is an open drain output, and is thus set to active low).

When the input is turned off the fault signal is cleared and the IC is reset. On the next active input signal the IC will repeat the operation described above if the overcurrent condition remains. Hence the overcurrent control is on a cycle-by-cycle basis.

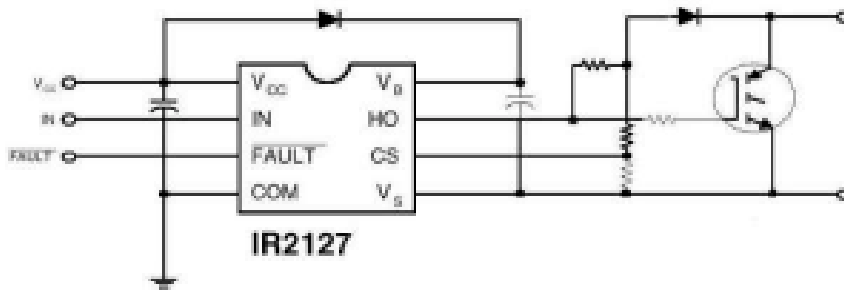


Fig 1) IR2127 Typical Connection Diagram

IR2121/IR2125 Current Sensing Function

A typical connection for the IR2125 is shown in fig 2). The typical connection for the IR2121 is similar, but this time its a low side drive and no bootstrap diode is needed (pin 1 & pin 8 are connected internally) . Again the CS pin is the pin used for sensing the current. Again there is a blanking time to ensure there is no nuisance tripping, but the operation is slightly different. When the voltage at the CS pin reaches the threshold (230mV nominal), the IC will detect the overcurrent condition. At this point the IC will wait for a time equal to the blanking time (500ns nominal) to filter out the noise spike caused by the switching action of the power device. After the blanking time has elapsed if a CS voltage above the threshold is still present, the output driver is switched into a linear mode with a feedback amplifier controlling the output gate drive voltage. The amplifier and the output power switch form a negative feedback loop which controls and settles the gate drive voltage to a lower value in order to keep the switch current limited to the preset value determined by the sensing resistor between the CS pin and VS(IR2125) or COM(IR2121). For example if the sensing resistor is 0.23W then the current would be limited to 1A.

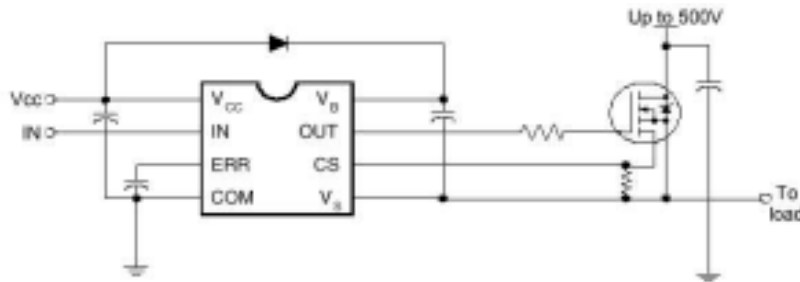


Fig 2) IR2125 Typical Connection Diagram

The ERR pin is multifunctional, providing status reporting, linear mode timing, and cycle-by-cycle control. When the IN signal is low the ERR pin is pulled low with 30mA of pull-down current. After the IN signal is switched high the ERR pin is switched to a high impedance state with 1M Ω pull-down. When the output stage switches to linear mode due to an overcurrent signal at CS, the ERR pin is set to drive a 100 μ A charging current into the capacitor connected between ERR and COM. Hence the ERR pin voltage rises at a rate determined by the capacitor ($dt=C*(dv/I_{err})$). This charging current will be terminated if the CS voltage disappears, and the driver returns to the normal switching mode. However if the fault condition remains and the ERR capacitor is charged to above 1.8V, then the ERR trip comparator will be triggered and the output is turned off for the remainder of the cycle. The ERR trip comparator also activates a 15mA pull-up current, which pulls up the ERR pin to V_{CC} indicating a fault (reporting function). The ERR trip comparator can also be triggered by

external pulses for a cycle-by-cycle shutdown function. These pulses must only occur when the output is on to prevent high current consumption (remember when input is low, Err pin is pulled down by 30mA of pull-down current).

The current sensing function is designed to handle both “Hard” and pulsed short circuit conditions as shown in fig 3). In the case of a “hard” short (fig 3a) the ERR capacitor value will determine the duration of the linear mode gate drive, before shutdown occurs. In the case of a pulsed short (fig 3b) The ERR capacitor acts as an

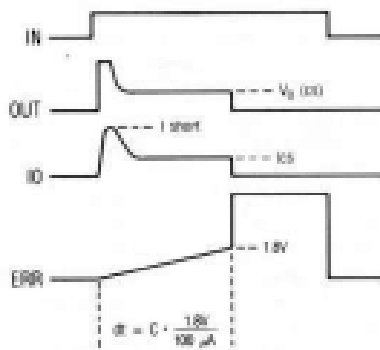
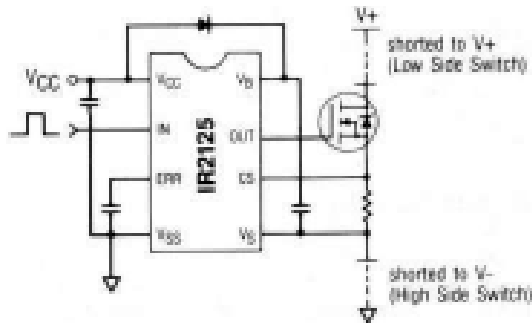


Fig. 3a — Protection Logic Scheme with Current Sensing in “hard” Short Condition

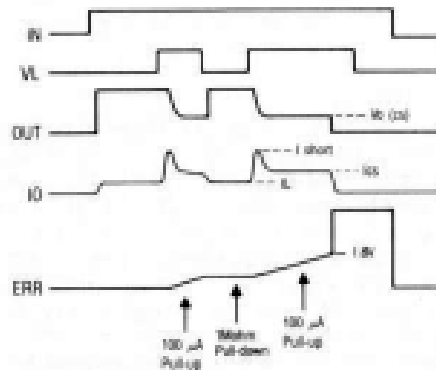
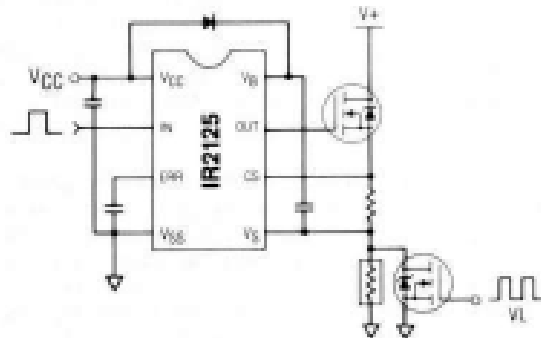


Fig. 3b. — Protection Logic Scheme with Current Sensing in pulsed Short Condition

integrator, determining the number of pulsed shorts before shutdown for the remaining cycle.

3) CURRENT SENSE CIRCUIT CONFIGURATIONS

Basic Source/Emitter Sense Resistor Configuration

The configuration shown in fig 4 shows the use of a basic source/emitter sense resistor. The resistor value is chosen so that, at the desired trip current level the voltage across the resistor, and therefore applied to the CS pin is above the $V_{CS\text{TH}+}$ threshold. There are two drawbacks to this method:-

- 1) The entire load current passes through the sensing resistor, causing power dissipation and reduced efficiency.
- 2) The reverse current passing through the antiparallel diode of the main switch causes a negative voltage to be applied to the CS pin. This must be limited to 300mV.

The major advantage of this circuit is that is very simple to implement for both MOSFETs and IGBTs.

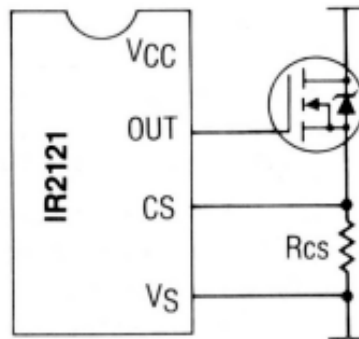


Fig 4) Current Sense Circuit Configuration With A Source/Emitter Resistor

Hexsense MOSFET Configuration

The circuit shown in Fig 5) shows the circuit configuration if you are using a Hexsense current sensing MOSFET. In this circuit a fraction of the drain current flows out of the Hexsense MOSFET current sense pin through the current sense resistor to the Kelvin source lead. The current sense resistor value is chosen based on the fraction of current that flows out of the Hexsense current source pin corresponding to the overload current in the main part of the MOSFET.

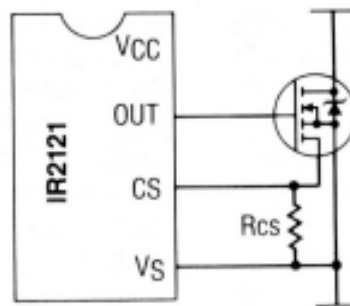


Fig 5) Current Sensing Using a Hexsense MOSFET

This circuit is better than the source/emitter sense resistor configuration in that only a very small fraction of the drain current flows through the sensing resistor, therefore dissipation is significantly lower for this configuration. One possible drawback is that there are not as many variations of Hexsense MOSFETs to choose from in terms of voltage ratings and $R_{ds(on)}$ as there are conventional MOSFETs.

Desaturation Detection Circuit

The current sensing circuit configuration shown in fig 6) is known as a desaturation (or desat) detection circuit. It was originally intended for use with IGBTs to detect the situation where the IGBT comes out of saturation due to an overcurrent condition. This being said, it is also possible to use this circuit configuration with MOSFETs. With MOSFETs the principle is similar, as the voltage across the FET will increase significantly during an overload condition.

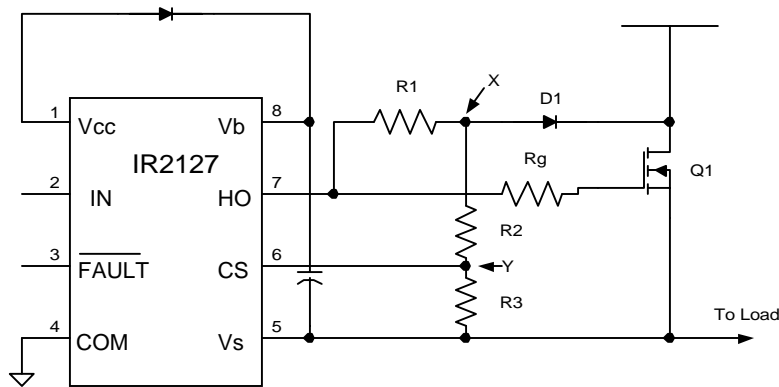


Fig 6) Desat Detection Circuit Configuration

To Calculate the resistor values use the following guidelines.

Rg is the gate resistor, and the value is chosen to optimize switching speed and switching losses.

R1 is typically chosen to be 10k (12V Vbs)/22k (15V Vbs)/33k (18V Vbs); this high value helps to minimize the increased miller capacitance effect from diode D1, and makes sure there is not significant current being drawn from the HO output. Note diode D1 must have the same characteristics as the bootstrap diode.

When the HO output goes high MOSFET (or it could be an IGBT) Q1 turns on. Now point X in fig 6) will be pulled down to a voltage which equals the voltage across the FET (V_{DS}) plus the voltage across diode D1. Therefore in an overload condition we want to shut down the driver output when the voltage across the FET (or IGBT) Q1 equals a set limit that indicates an overload condition has occurred (for example 8V).

Therefore with a 8V Vds on Q1. V_{D1} is typically 1.2V for a small 1A ultra fast recovery diode.

$$V_x = V_{D1} + V_{DS}$$

$$V_x = 1.2 + 8$$

$$V_x = 9.2V$$

For an IR2127 the CS pin threshold is 250mV, therefore we need to divide V_x so that when $V_x=11.2V$, then $V_y=250mV$.

$$V_y = V_x \cdot R3 / (R2+R3)$$

$$\text{let } R2 = 33k$$

$$R3 = 922\Omega$$

4) Layout Considerations

The following is a guideline list for PCB layout when using the IR212X current sensing gate drive IC' s.

- 1) Keep the track between the output of the IC and the gate of the MOSFET or IGBT as short as possible (preferably < 1 inch).

- 2) Keep the current sense circuit components as close as possible to the IC to minimize the possibility of false triggering due to noise coupling in the circuit.
- 3) Make all high current tracks as large as possible to minimize inductance.
- 4) Further layout guidelines can be found in Design Tip **97-3 “Managing Transients in Control IC Driven Power Stages”**