SIEMENS

Microcomputer Components
Technical Support Group Munich
HL DC PD MC

Errata Sheet

December 16, 1997 / Release 1.3

Device : SAB-C501G

Marking : AC

These parts of the SAB-C501G can be identified by the letters "AC" below the part number. The parts are mounted in a Plastic Dual-Inline package (P-DIP-40), in a Plastic Leaded Chip Carrier package (P-LCC-44) or in a Plastic Metric Quad Flat Package (P-MQFP-44).

This errata sheet describes both the *functional problems* (see part 1) and the *deviations from the electrical and timing specifications* (see part 2) known in this step.

If a problem was already introduced with an errata sheet of an earlier step, its initial number is still retained in this errata sheet. Thus, the numerical order of the problems described in the following may contain gaps.

At the end of this document, you will find two history tables showing the problems found in the SAB-C501G up to now. Changes to the last revision are shaded light grey in the history tables.

1) Functional Problems

The following malfunctions are known in this step:

Problem 1: Wrong destination address at AJMP and ACALL instructions

If an opcode byte of an AJMP or ACALL instruction is located at the last but one address location of a 2K code memory page, a wrong destination address is calculated and the program execution will continue at a wrong address, which is 2K (800H) below the correct destination address. There are 32 2K code memory pages available with critical address locations where an AJMP or ACALL instruction can be located: 7FEH, FFEH, 17FEH, 1FFE, 27FEH, ... F7FEH, and FFFEH. At all of these 32 address locations AJMP or ACALL instructions show a malfunction.

Workaround:

There are only software workarounds possible:

- Avoiding ACALL and AJMP instructions in the program code and using LCALL and LJMP instructions only. Typically, compilers have built-in switches which disable the usage of ACALL and AJMP instructions and force the usage of LCALL and LJMP instructions.
- Existing programs (HEX-files) must be checked whether the opcode of an AJMP or ACALL instruction is located at a critical address location. If yes, the instruction has to be moved to an uncritical address location or it has to be replaced by a LJMP or LCALL instruction.

Problem 2 : Timer 2 - Concurrent Access on T2CON

A problem might occur when Timer 2 is used together with the functionality of the P1.1/ T2EX pin in the following operating modes :

- Timer 2 as baud rate generator
- Timer 2 in 16-bit capture
- Timer 2 in 16-bit auto-reload with DCEN=0

When a falling edge on P1.1/T2EX occurs during the execution of a read-modify-write instruction on SFR T2CON, the interrupt flag EXF2 is not set and and the related interrupt, if enabled, is not executed.

Workaround :

When using a read-modify-write instruction on T2CON, it must be checked (e.g. by software) whether a high-to-low signal transition occured at pin P1.1/T2EX during the execution of the read-modify-write instruction. This can be achieved by polling the level on P1.1/T2EX before and after the read-modify-write instruction. The timer 2 interrupt has to be disabled during the polling sequence. If a high-to-low signal transition is detected at P1.1/T2EX, the interrupt EXF2 flag can be set by software.

The following assembly program demonstrates a possible software workaround:

```
workaround:
        clr     et2             ; disable t2 interrupt
        jnb     p1.1, rmw1      ; normal rmw if pin is already low
rmw2:   orl     t2con, #xxh     ; rmw on t2con
        jnb     p1.1, force_t2int ; force t2int if p1.1 low now
        setb    et2             ; enable t2 int again
        sjmp    go_on           ; go_on, no falling p1.1-edge occured
force_t2int:
        setb    exf2            ; set request flag
        setb    et2             ; enable t2 int again, force interrupt exf2
        sjmp    go_on           ; go_on, falling edge occured within rmw
rmw1:   orl     t2con, #xxh     ; rmw on t2con
        setb    et2             ; ena t2 int again & go_on
go_on:
        ::::
```

Note :
If the external signal on P1.1/T2EX is a short pulse, the pulse width has to be 3 instruction cycles long at least. Otherwise the polling sequence of the pin cannot recognize the high-to-low signal transition.

Problem 3 : Port 2 behaviour during MOVX @Ri instructions

During normal program execution a problem occurs at the port 2 lines if the following conditions are met :

- Program execution from internal program memory (pin EA# tied to Vss)
- MOVX instrcution with 8-bit address (@Ri) is executed

If an 8-bit address (MOVX @Ri instruction) is executed by an internal program, port 2 pins which contain a ‘1’ in the port latch are driving a strong ‘1’ (instead of a weak ‘1’) during the external memory cycle. This behaviour may cause problems with an external hardware which is connected to the port 2 lines.

Workaround:

none

2) Electrical- and Timing-Spec. Deviations

The following deviations of electrical and timing parameters from the specification are known in this step:

Problem 1: Test condition for Icc in power down mode

The test condition for I_{cc} in power down mode is V_{cc} = 5 V (instead of V_{cc} = 2 ... 5.5V)

Functional Problem No.	Marking	Description	Remarks
1	AC	Wrong destination address at AJMP and ACALL instructions	
2	AC	Timer 2 - Concurrent Access on T2CON	
3	AC	Port 2 behaviour during MOVX @Ri instructions	

Table 1: History of Functional Problems

Electrical- / Timing-Problem No.	Marking	Description	Remarks
1	AC	Test condition for Icc in power down mode	

Table 2: History of Electrical- and Timing-Spec. Deviations