XC878 series

8-bit microcontrollers with 64K Flash and CAN connectivity

New member to cost-effective
XC800 8-bit Family

July 2008

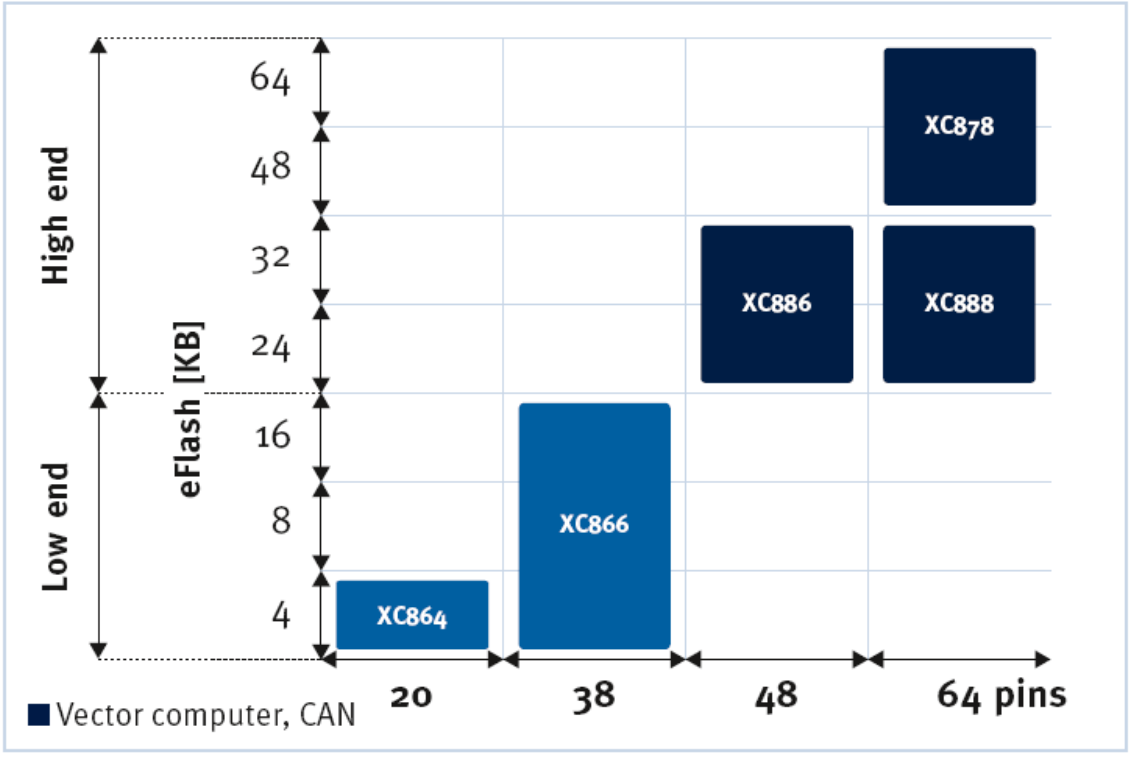
Never stop thinking

Agenda

- XC878 Product Presentation (Technical Overview)
  - Family Overview
  - System & Core
  - Embedded Memories
  - Standard Peripherals
    - GPIO
    - Timers & WDT
    - UART & LIN
    - SSC
  - Special Peripherals
    - ADC
    - CAPCOM6E
    - T2CCU
    - MultiCAN
    - MDU & Cordic
  - Debug Support & Toolchain

Roadmap for XC800 Family

Family of cost-effective 8-bit MCUs



Key Features

- High-performance 8051 core
- 4 KB up to 64 KB Flash
- EEPROM support
- 20-pin up to 64-pin packages
- Flexible PWM unit
- Fast 10-bit ADC
- On-chip OSC
- LIN, CAN connectivity

New XC878 Series on a Glance

Applications	☒ **Automotive Body:** Power Closure Systems, Steering lock , Immobilizers ☒ **Motor Control:** Air conditioners, White goods, Forklifts, Automation ☒ **Building control:** Compressors, pumps, Fans, LED lighting

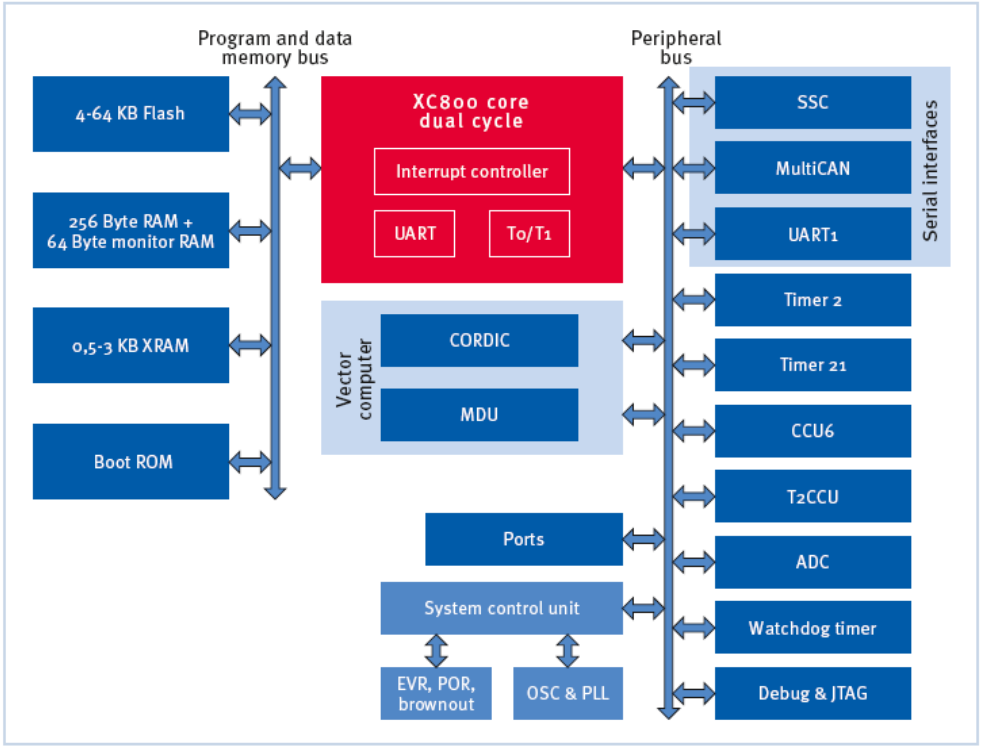



Advantage	Advanced peripheral integration for motor control performance FOC + PFC on a single MCU together with CAN connectivity

Key Benefits to Customers	☒ 64KB Flash, 3KB RAM and CAN connectivity ☒ Powerful motor control features: Vector Computer, ADC ,CCU6E ☒ 2 PWM timers with 8 PWM channels and 4 independent time bases ☒ Integrated safety features: Voltage &Clock supervisory, ECC

Eval Boards	XC878 Easy Kit €99

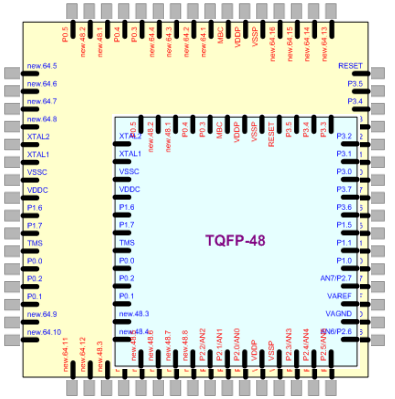
XC878 Product Block Diagram



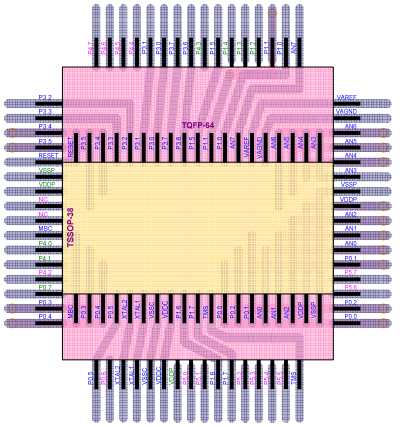
- 64KB Flash, 3KB RAM and CAN connectivity
- Powerful motor control features: Vector Computer, ADC ,CCU6E
  - Enables Field Oriented Control at lowest system cost
- 2 PWM Modules with 10 PWM channels and 4 independent time bases
- Enables PFC + FOC motor control on a single MCU
- Integrated safety features: Voltage & Clock supervisory, ECC
- Supporting Documentation www.infineon.com/XC878
  - AppNotes
  - Data Sheets
  - Users Manual
  - Hands On Training

Pin-Out Compatibility within XC800 Family

- LQFP64 and LQFP48

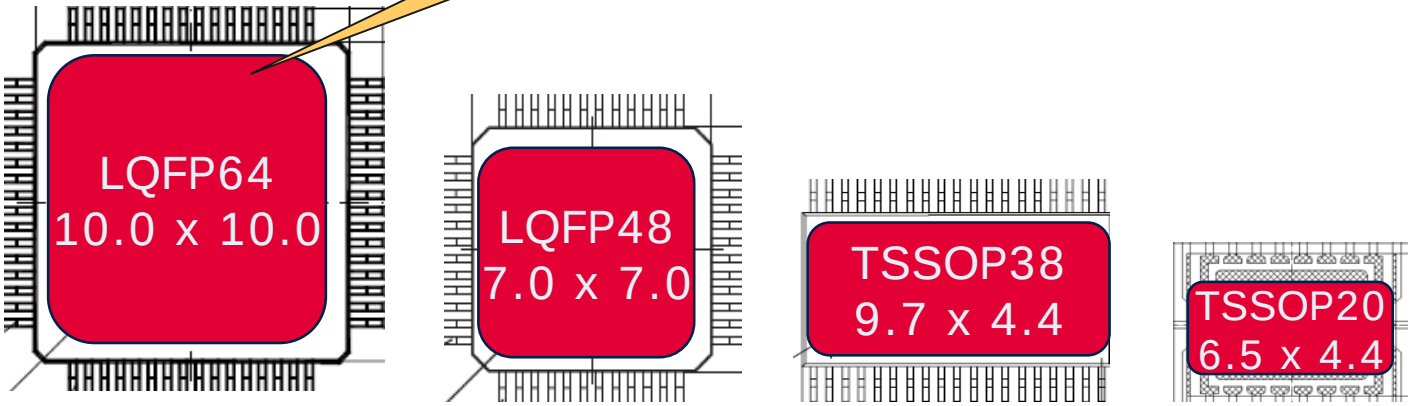


- LQFP64 and TSSOP38



- Body Size

XC878 and XC888



- Pin Pitch

Migration from XC886/888 to XC878

- Migration guide is available → Starterkit CD
- List of differences:
  - Memory Extension
  - Flash Architecture
  - Clock System
  - EVR and Interrupts
  - Bootstrap Loader
  - Pinout

- Note: Actual Starter Kit CD contents is available on
  www.infineon.com\xc878

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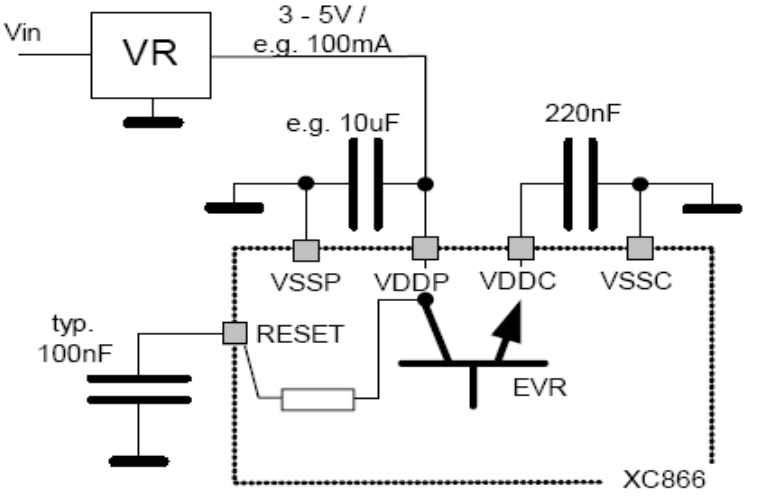
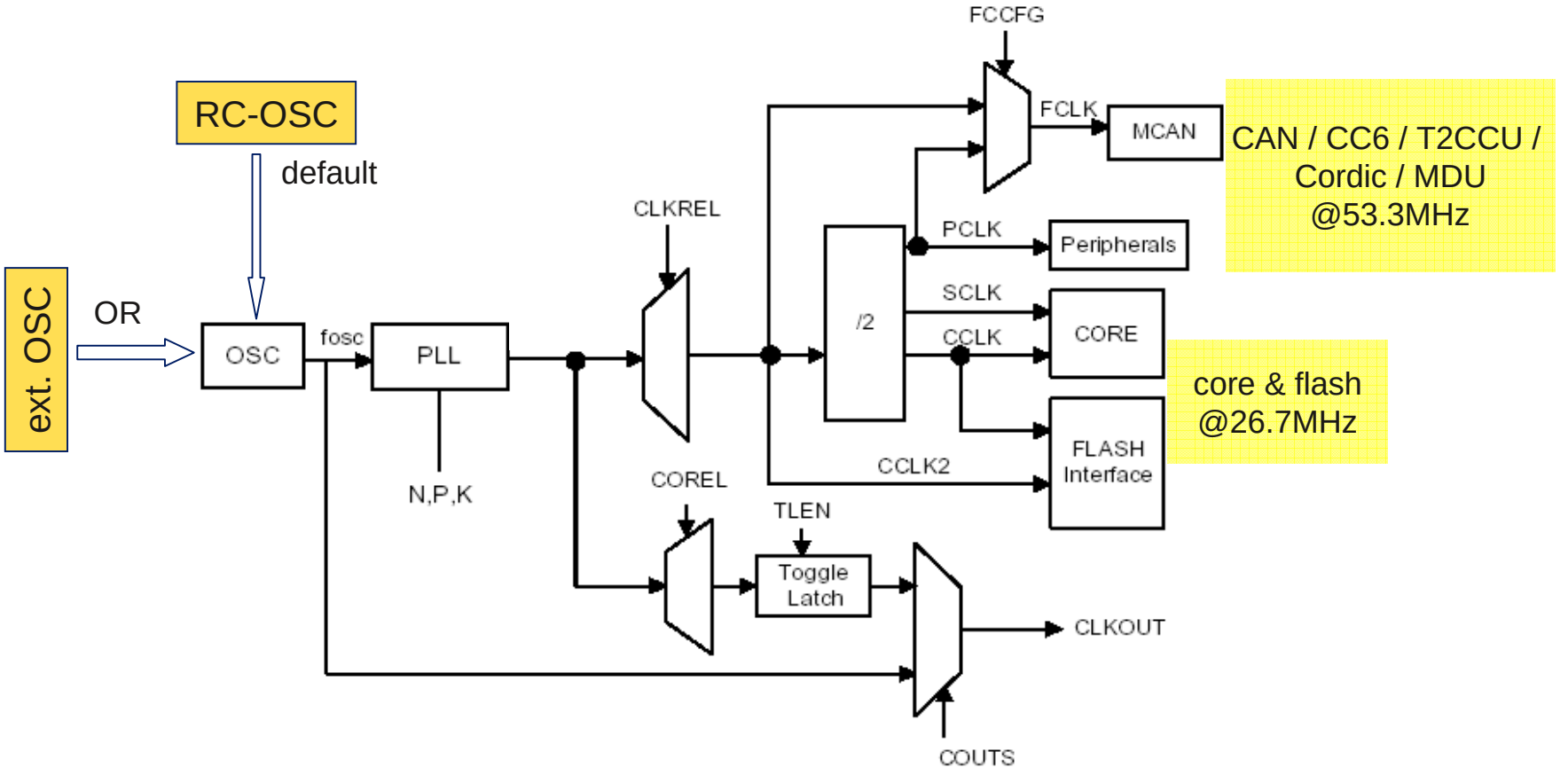
  - Debug Support & Toolchain

System Control Unit – EVR & Powerup

- Dual voltage supply concept
- Embedded Voltage Regulator (EVR)
- Features:
  - Input voltage
    – pad supply **VDDP**: 3V / 5V
  - Output voltage
    – core supply **VDDC**: 2.5V
  - **Main EVR** can be turned off (power down mode)
  - **Auxiliary EVR** maintains RAM and wake-up logic (power down mode)
  - EVR needs external **buffer capacitor** on pins VDDC / VSSC
  - CPU and all peripherals (including flash & ADC) are running at VDDC
    - all modules are widely indepent on pad supply VDDP
  - Power On RESET and Brownout RESET generation

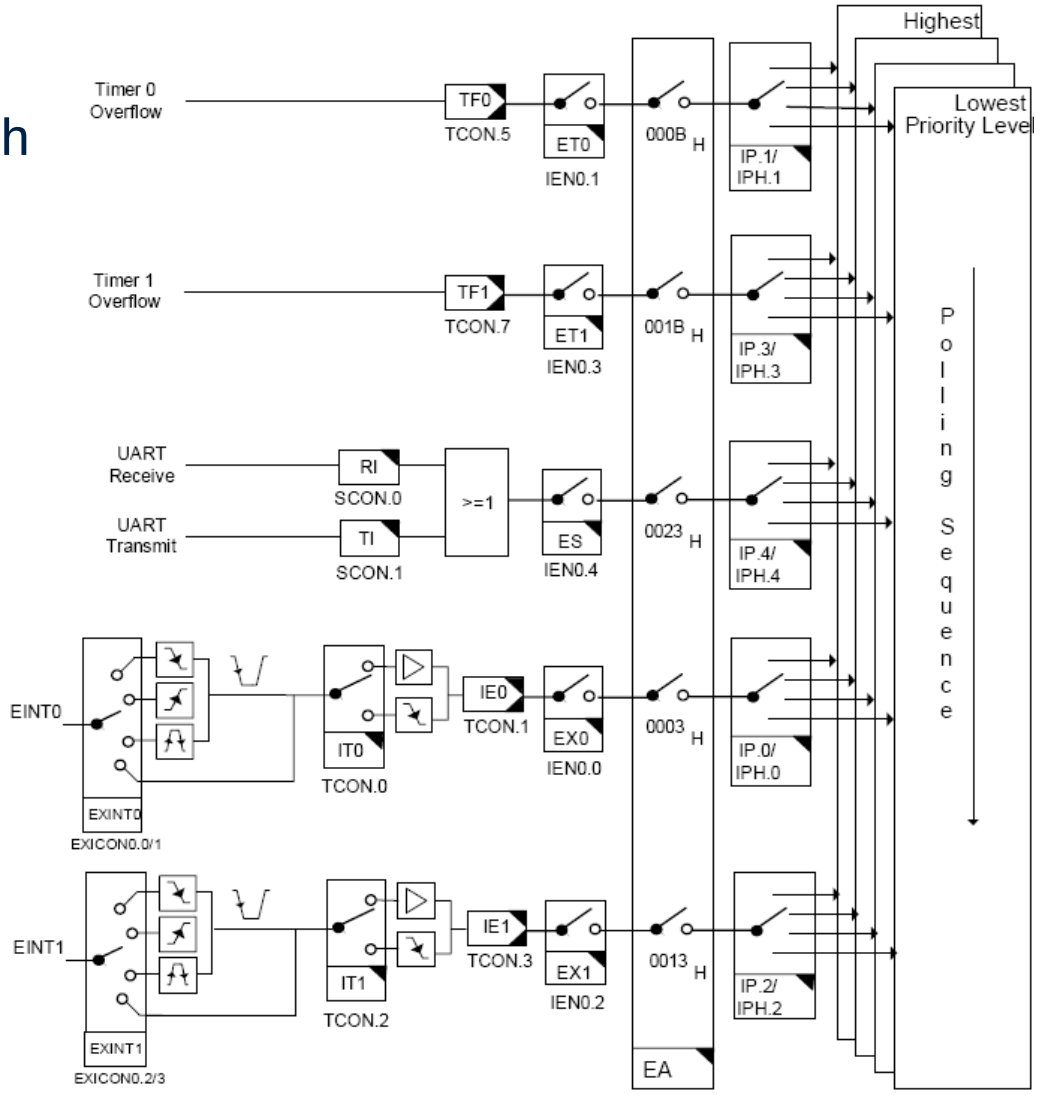


System Control Unit – Clock System



System Control Unit – Interrupt Controller

- Interrupt Controller
  - 14 interrupt vectors with four priority levels
    - up to 15 external interrupts
  - Non-Maskable interrupt (NMI); highest priority



System Control Unit – Power Management

- Four Power Management Modes
  - Active Mode
    - peripherals can be individually enabled/disabled
  - Idle Mode
    - CPU is off and wakes up on any interrupt
  - Slowdown Mode
    - CPU and all modules are clocked down
    - prescaler /1, /2, /3, /4, /5, /8, etc...
  - Powerdown Mode
    - CPU and all peripherals are clockless
    - main EVR is off
    - wakeuplogic active
    - RAM/SFRs keep value
    - wakeup thru EXINT0 or RESET

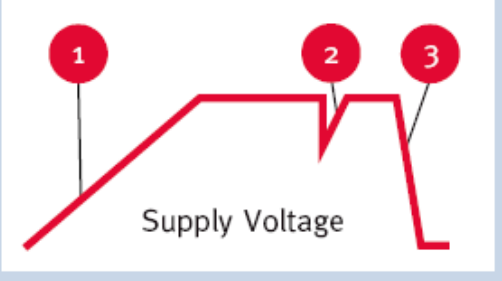
Mode	Typical current consumption
Active	~37mA
Idle	~29mA
Slow Down (fsys/2048)	~9mA
Power Down	~10uA@25°C

System Control Unit – Fail Safe

- XC878 provides Hardware functions to meet Safety standards:
  - Class B, Class C, IEC 60730

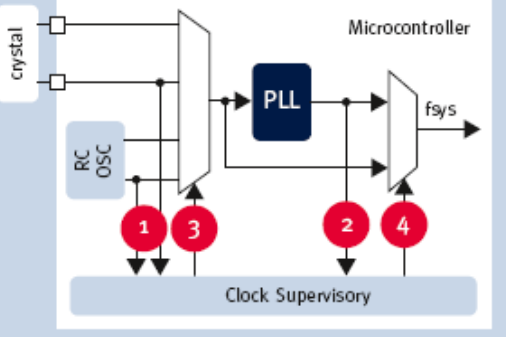
Voltage Supervisory

- Power On Reset (1)
- Early Warning (2)
- Brownout Reset (3)



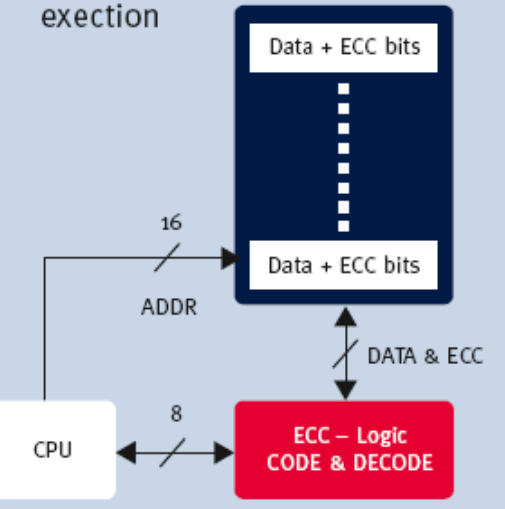
Clock Supervisory

- Run Detection (1)
- Lock Detection (2)
- Automated Clock Selection (s3)
- Automated Bypass (4)



Memory Error Correction – ECC

- Single Bit Error Correction
- Double Bit Error Detection
- Protect against Invalid code exection



Ensures a SAFE STATE

Boot-Concept

Bootstrap Loader Options	
UART	download to XRAM or Flash
LIN	
CAN	download to XRAM
ALTERNATE	jumps to user defined Flash address

Mark / Boot	„C“	„L“	„CM“	„ - “
UART	x	-	x	x
LIN	-	x		-
CAN	x	-	x	-

- BSL is entered
  - with MBC = 0 (always)
  - with MBC = 1 (if flash @0x0000 is zero)
- Booting only on pins
  - P1.0/RXD/RXDC0_0
  - P1.1/TXD/TXDC0_0
- Booting always supports autobaudrate detection
- MultiCan Booting
  - point-to-point connection
  - external clock required
    - default 8MHz (initial programming)

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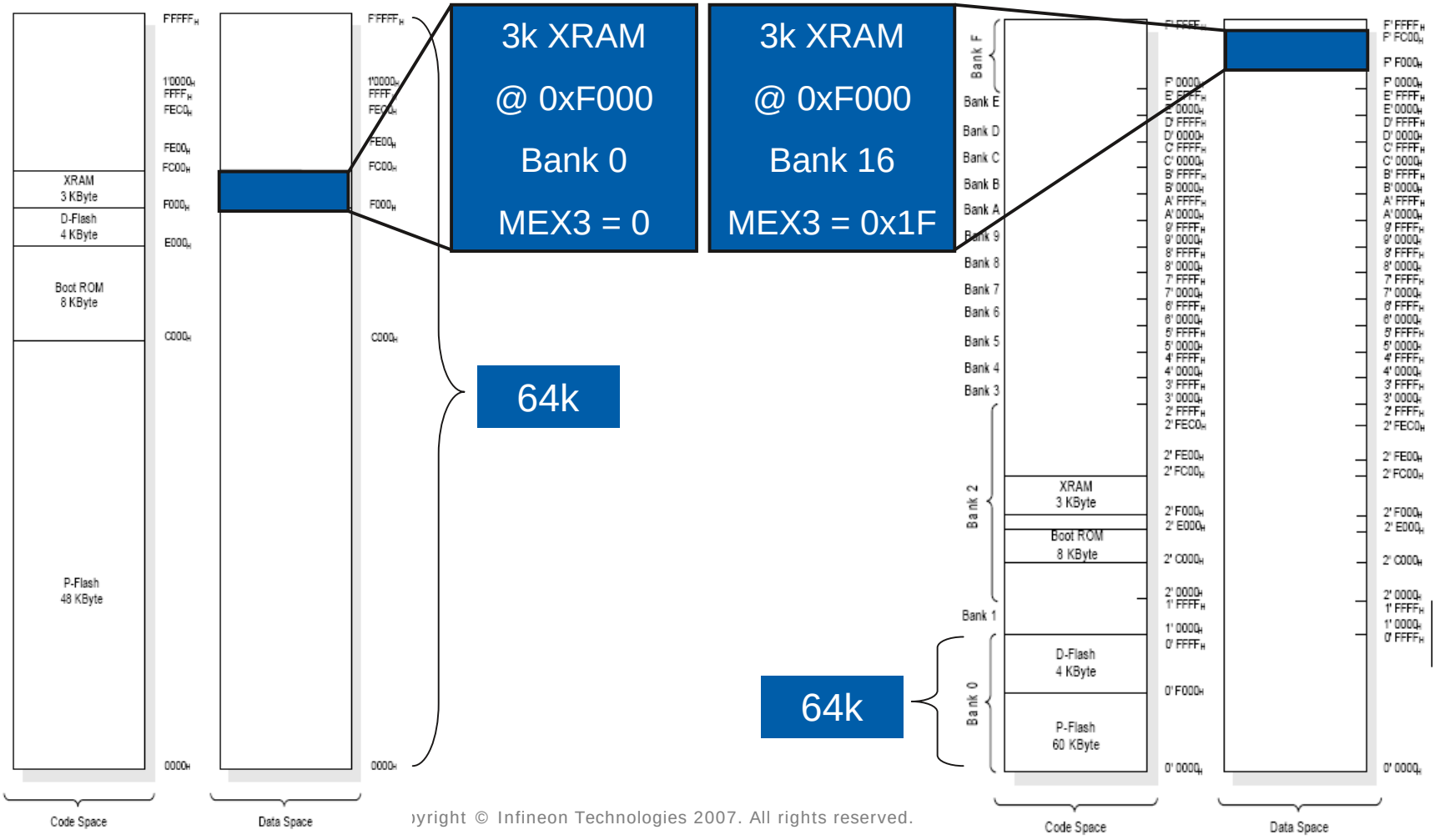
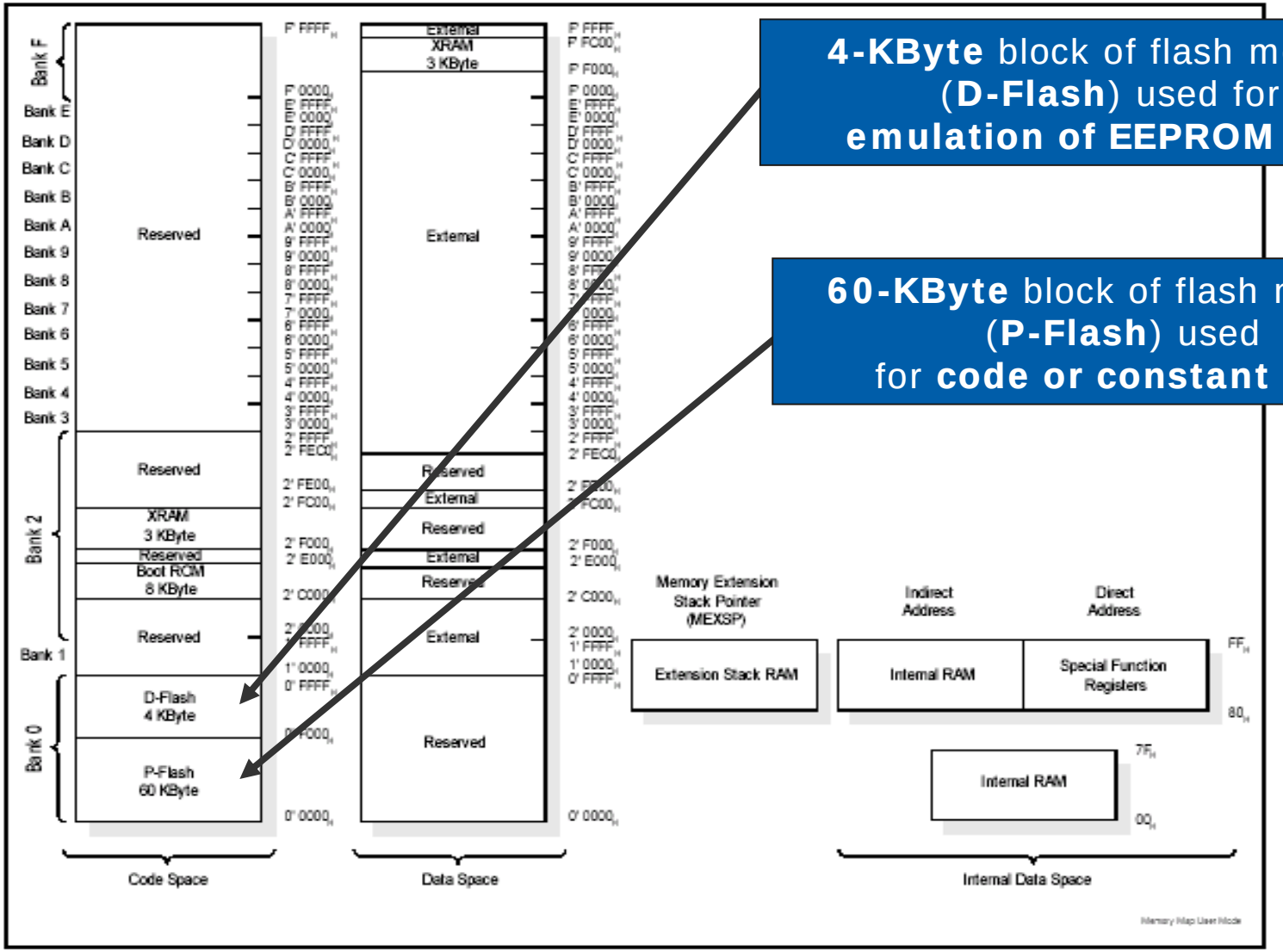
Memory Layout

- XC878 – 13FF (52K flash)
  - compatible to XC886
- XC878 – 16FF (64K flash)
  - banking for XRAM



Memory Layout – Flash



Flash Architecture

- XC878 has two independent Flash-Blocks:
  - PFLASH (48/60k) & DFLASH (4k)
    - both can be used for CODE and DATA
    - but DFLASH is capable for „background EEPROM emulation“
  - for data integrity a hardware error correction (ECC) is provided
  - Flash Readout- and Write-Protection mechanism

- Characteristics for Programming & Erase:

	PFLASH	DFLASH
Programming Time	20-40us	
Page Erase Time	20ms	
Mass Erase Time	200ms	
Min Programming Width	1 Byte	
Max Programming Width	64 Bytes	32 Bytes
Min Erase Width	512 Bytes	64 Bytes
Max Erase Width	60k	4k

Flash Retention & Endurance

- Characteristics for Retention & Endurance for DFLASH:

	Endurance [cycles]	Retention [years]	Size [bytes]	Remark
Automotive	1k	15	4096	non-emulated
	10k	5	1024	
	30k	2	512	
		1	2048	
	120k	2	512	emulation mode using dataset size of 128bytes

	Endurance [cycles]	Retention [years]	Size [bytes]	Remark
Industrial	1k	15	4096	non-emulated
	10k	10	4096	
	30k	5	4096	
	100k	1	4096	

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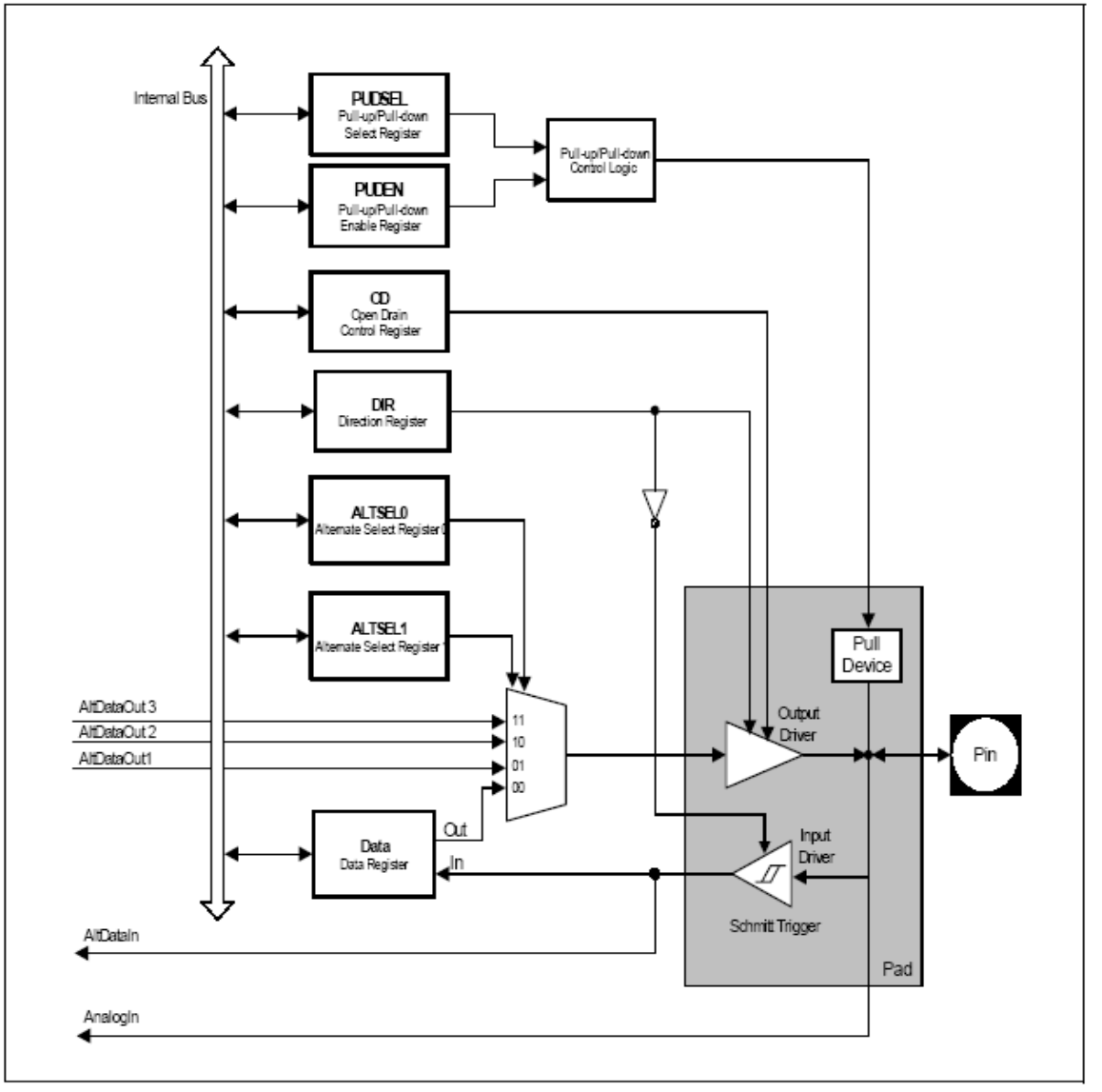
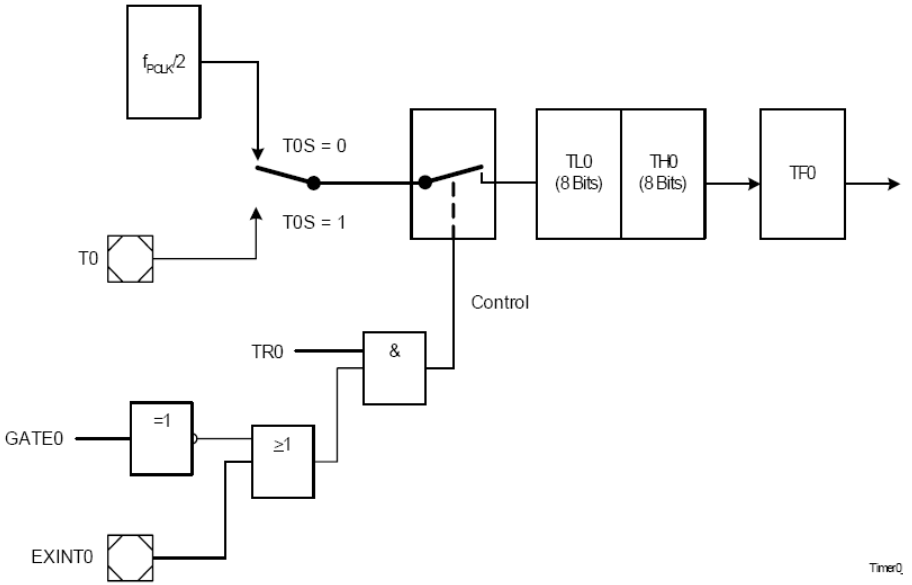
GPIO

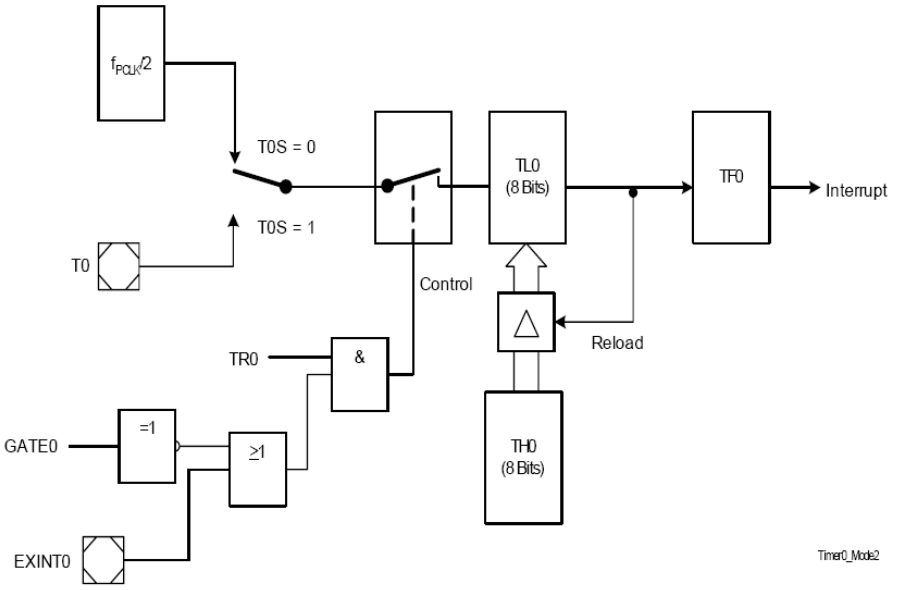
- Flexible IO configuration
- Two driver strength
- Open drain mode
- Selectable pullup/down devices
- Up to 4 alternate output functions on each I/O
- Up to 15 external interrupts on different nodes



Timers T0, T1

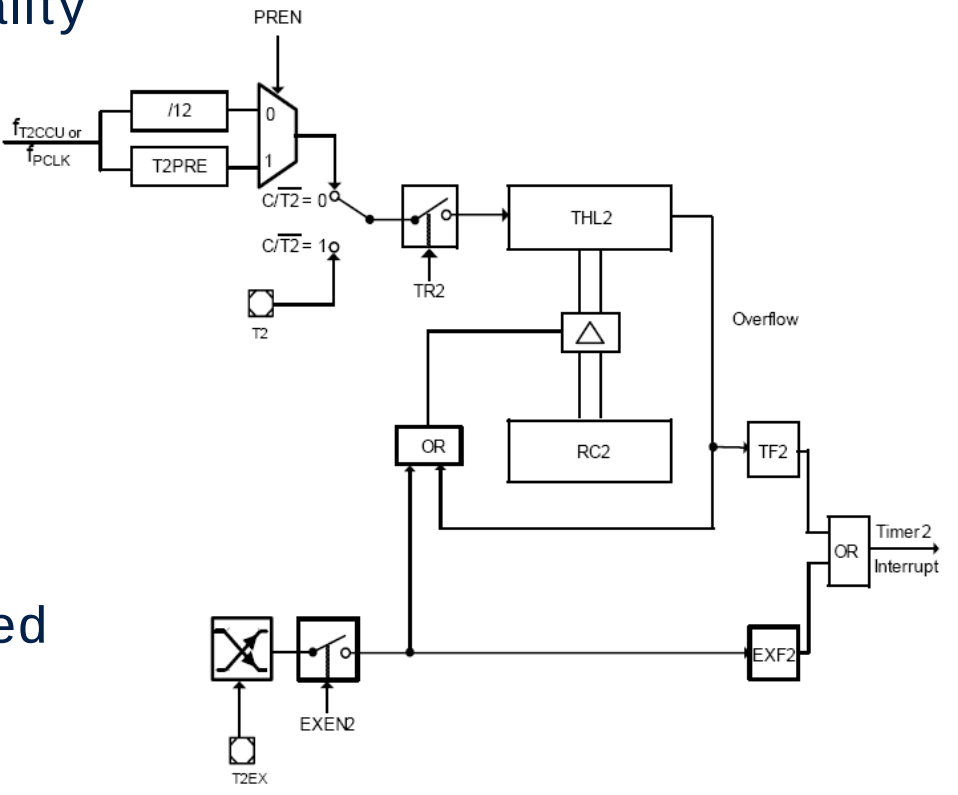
- Incremented once every fsys / 2
- Timer Modes
  - Mode 0: 13-bit timer
  - Mode 1: 16-bit timer
  - Mode 2: 8-bit timer with auto-reload
  - Mode 3; T0 is configured as two 8-bit timers. T1 holds the count.
  - external counter mode
  - two interrupt vectors for T0 / T1





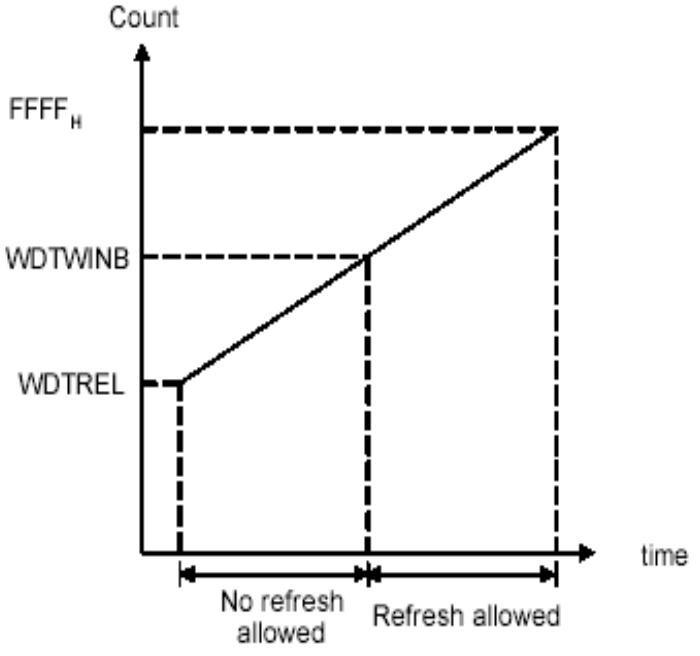
Timers T2, T21

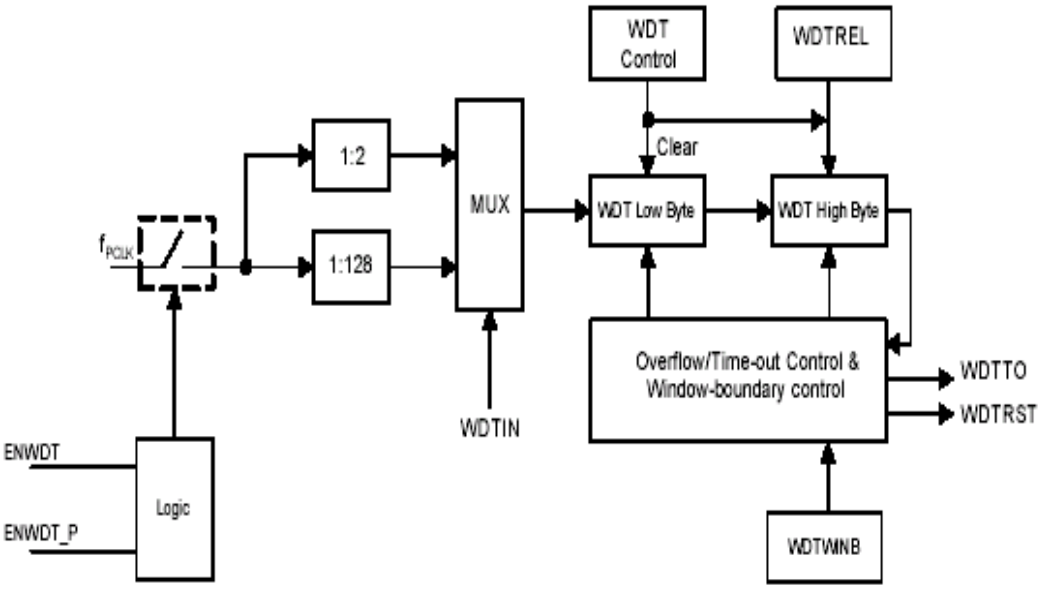
- T2 / T21 have same functionality
  - 16bit up/down-count with autoreload
  - capture – *T2EX*
  - external start – *T2EX*
  - output toggle – *EXF2*
  - external count input – *T2*
- large prescaler arrangement
- supports automatic baudrate capture for UART/UART1
- two interrupt vectors on shared nodes



Watchdog Timer

- Window Watchog Timer
  - Provides a reliable and secure way to detect and recover from SW or HW failures
- If the WDT is not serviced (refreshed) within the allowed window a system malfunction is assumed and an internal RESET is performed
- The window can be freely programmed

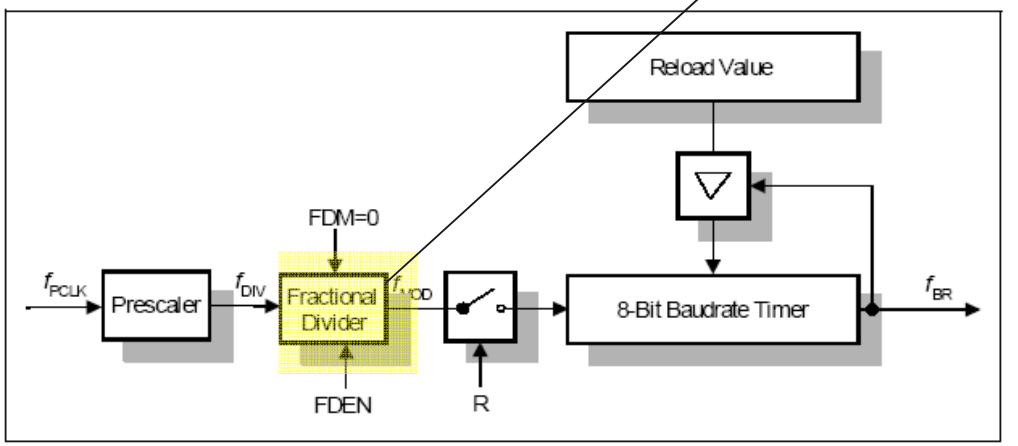




UART / UART1

- Two independent UART modules
- Full Duplex
- Receive Double Buffered
- 8/9-bit UART with a variable baud rate
- Integrated Baudrate Generator
- Integrated Fractional Divider for accurate baudrate adjustment
- Autobaudrate capture feature for LIN2.0 header
- Two interrupt vectors for UART/UART1

$$\text{baud rate} = \frac{f_{PCLK}}{16\text{x PRE x (BG+1)}} \text{ x } \frac{n}{256}$$



SSC

- High Speed Synchronous Serial Interface
  - Supports both **full-duplex** and **half-duplex** serial synchronous communication up to **13.3 MBaud**
  - Serial clock signal can be generated by the SSC (in Master mode) or can be received from an external master (Slave mode).
  - Transmission and reception is **double-buffered.**
  - A **16-bit baud-rate generator** provides a separate clock signal.
  - Communication with SPI compatible devices is supported
  - Flexible data format
    - Programmable number of data bits: **2 to 8 bits**
    - Programmable shift direction: **LSB or MSB** shift first
    - Programmable clock **polarity**: idle low or high state for the shift clock
    - Programmable **clock / data phase**: data shift with leading or trailing edge of the shift clock.
  - **Interrupt generation**
    - On a transmitter empty condition
    - On a receiver full condition
    - On an error condition (receive, phase, baud rate, transmit error)

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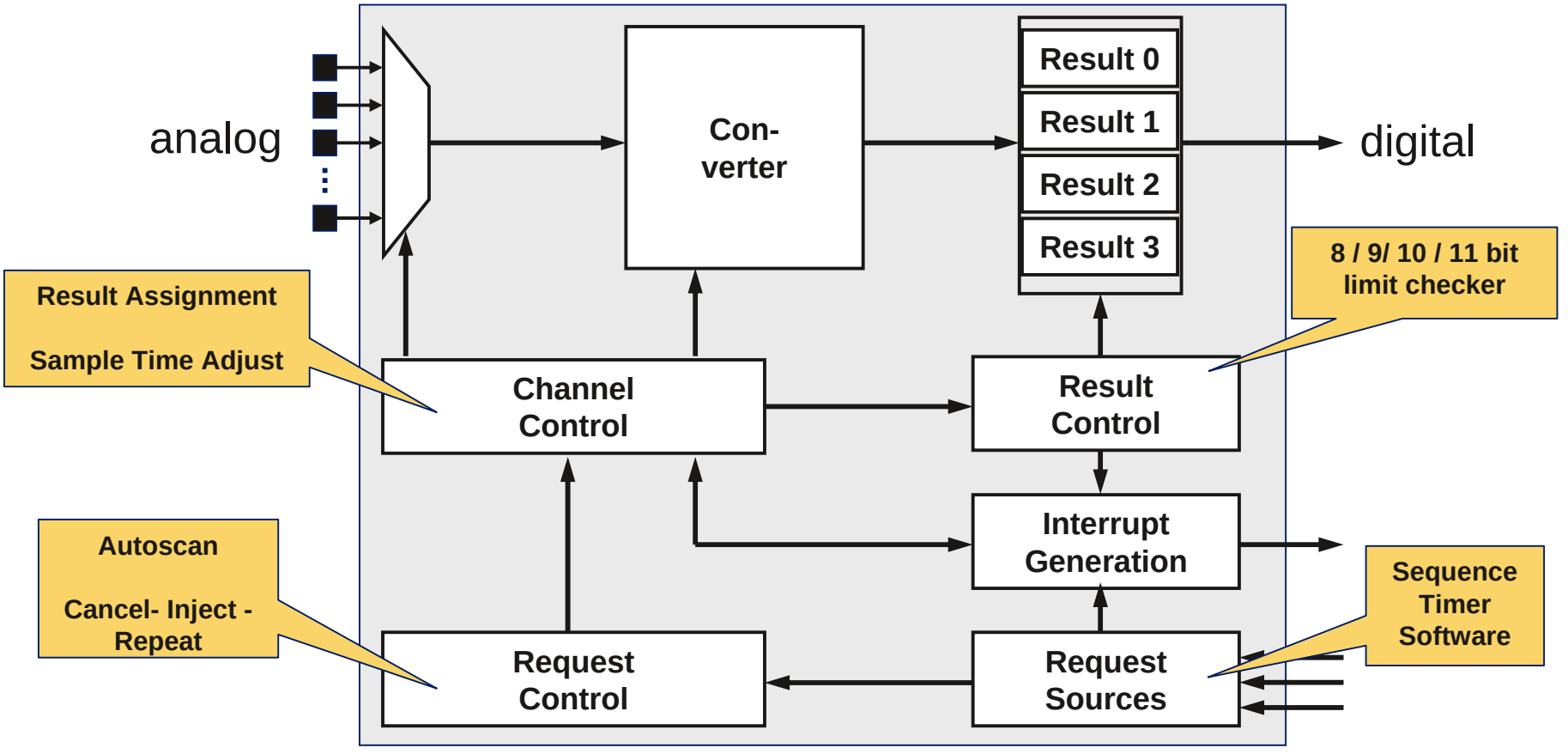
ADC – Block Diagram



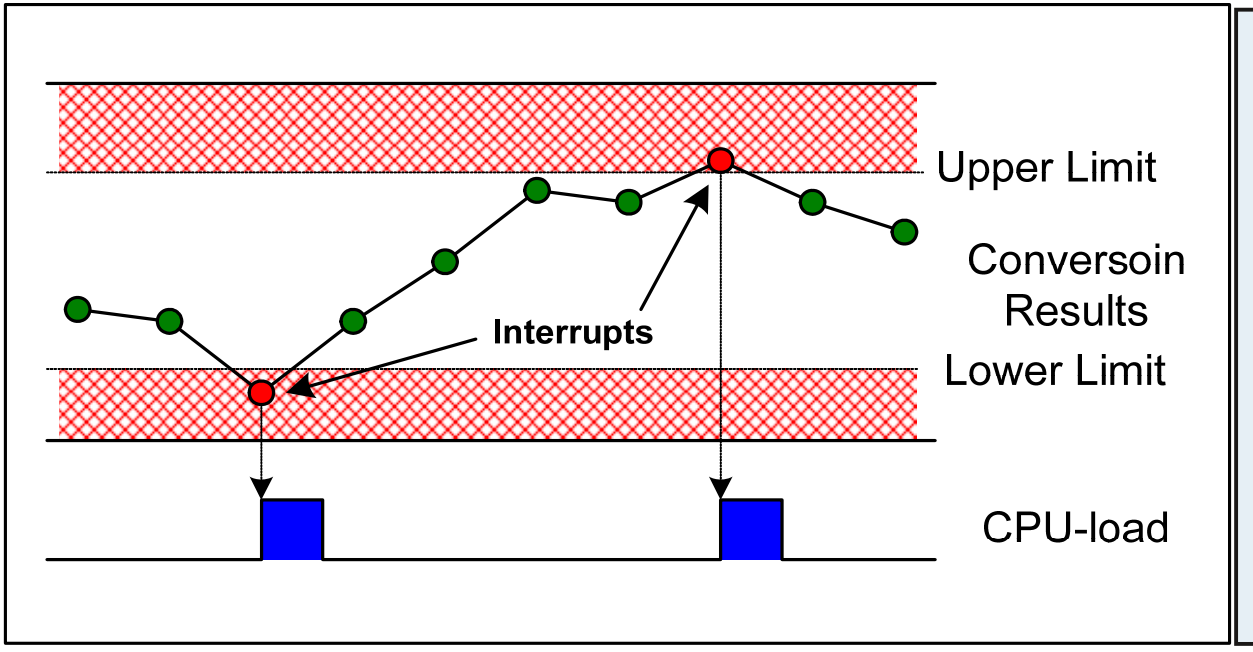
ADC – Features

- ADC Characteristics
  - 8 channels with 10bit resolution
  - TUE = +/- 3 lsb, DNLE = +/- 2 lsb, INLE = +/- 2 lsb
  - sample time down to 75ns
  - conversion time down to 0.85us@8bit and 1us@10bit

- ADC Features
  - Fully autonomous peripheral which off loads CPU while converting
    - ADC triggering and result storage is solved in hardware
    - background conversions in a defined sequence are possible
    - limit & boundary checking with interrupt (comparator mode)
    - autoscan and queued conversion on several channels
    - result accumulator & data reduction filter (median filter)
    - timetriggered and injected conversions (hardware arbitration)
    - 8, 9, 10, 11 bits result

ADC– Limit and Boundary Checking

Comparator Mode

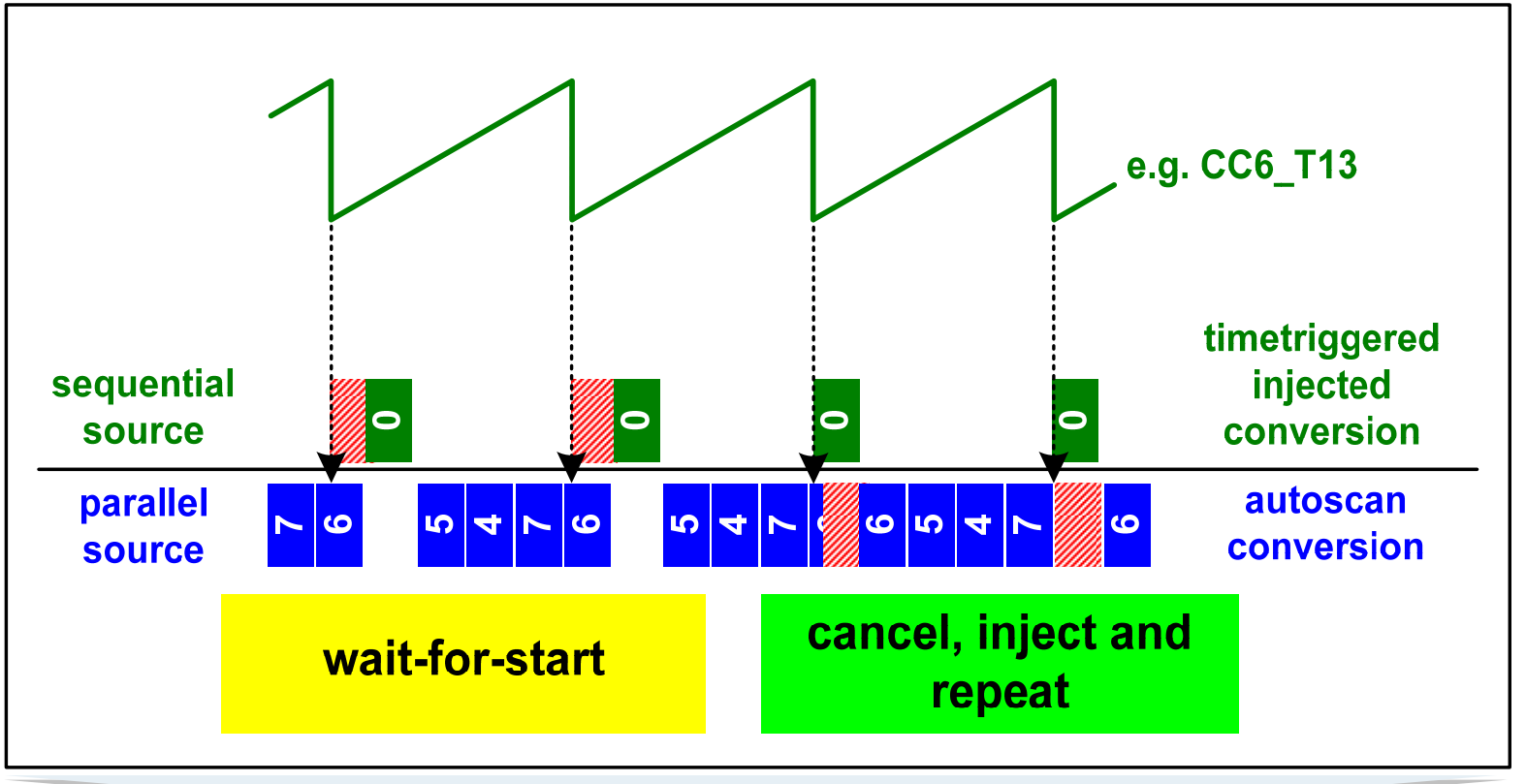


- comparator mode is selective per channel
- limit is global for all channels
- 4bits for upper & lower limit
- 8 combinations with 3 areas

Reduced CPU load
Software interaction for interesting results only

ADC – Arbitration on Trigger Sources

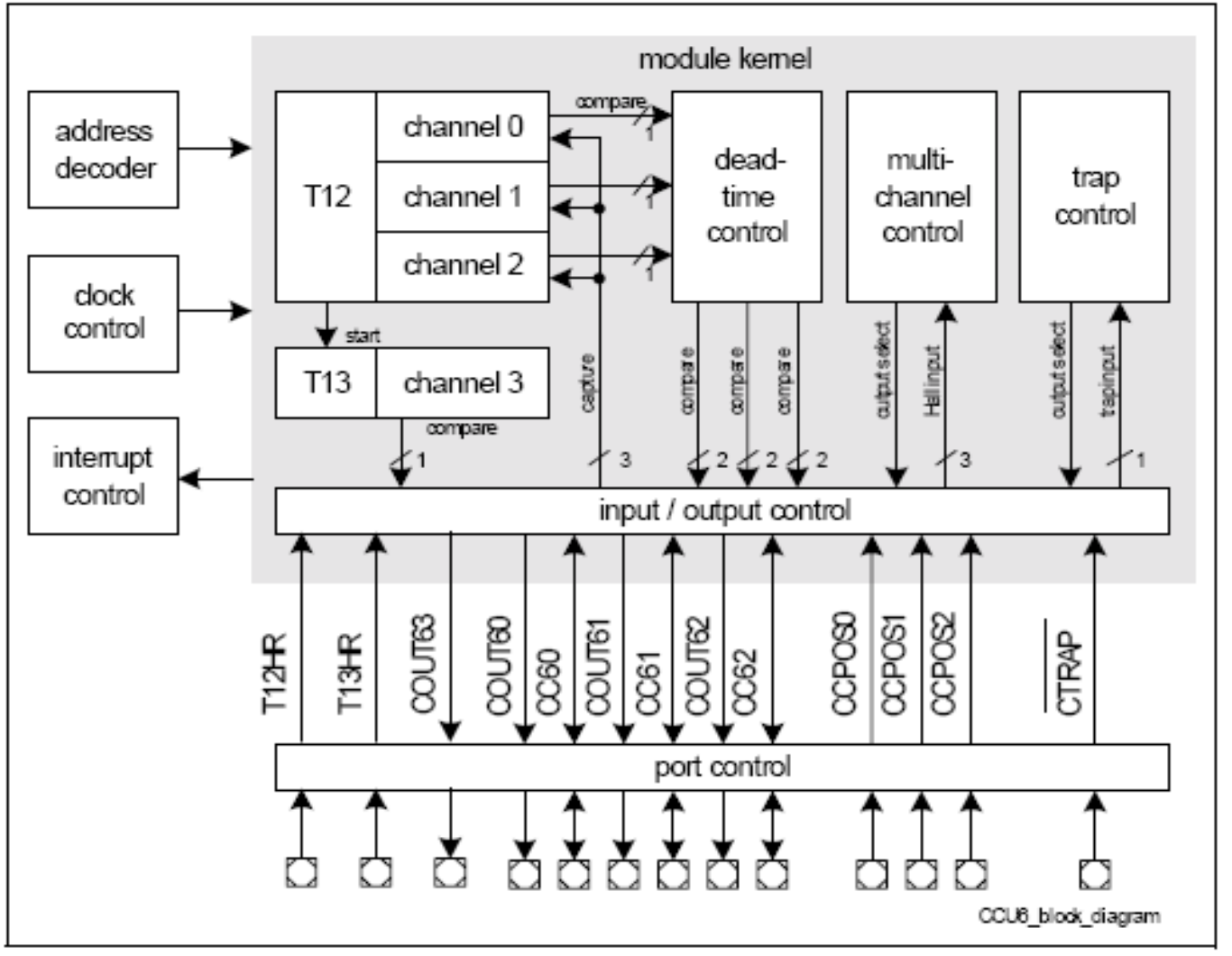
Sequential and Parallel Source



Full hardware support on priotization
Software is decoupled from hardware

CAPCOM6E

- CAPCOM6E – Block Diagram



CAPCOM6E

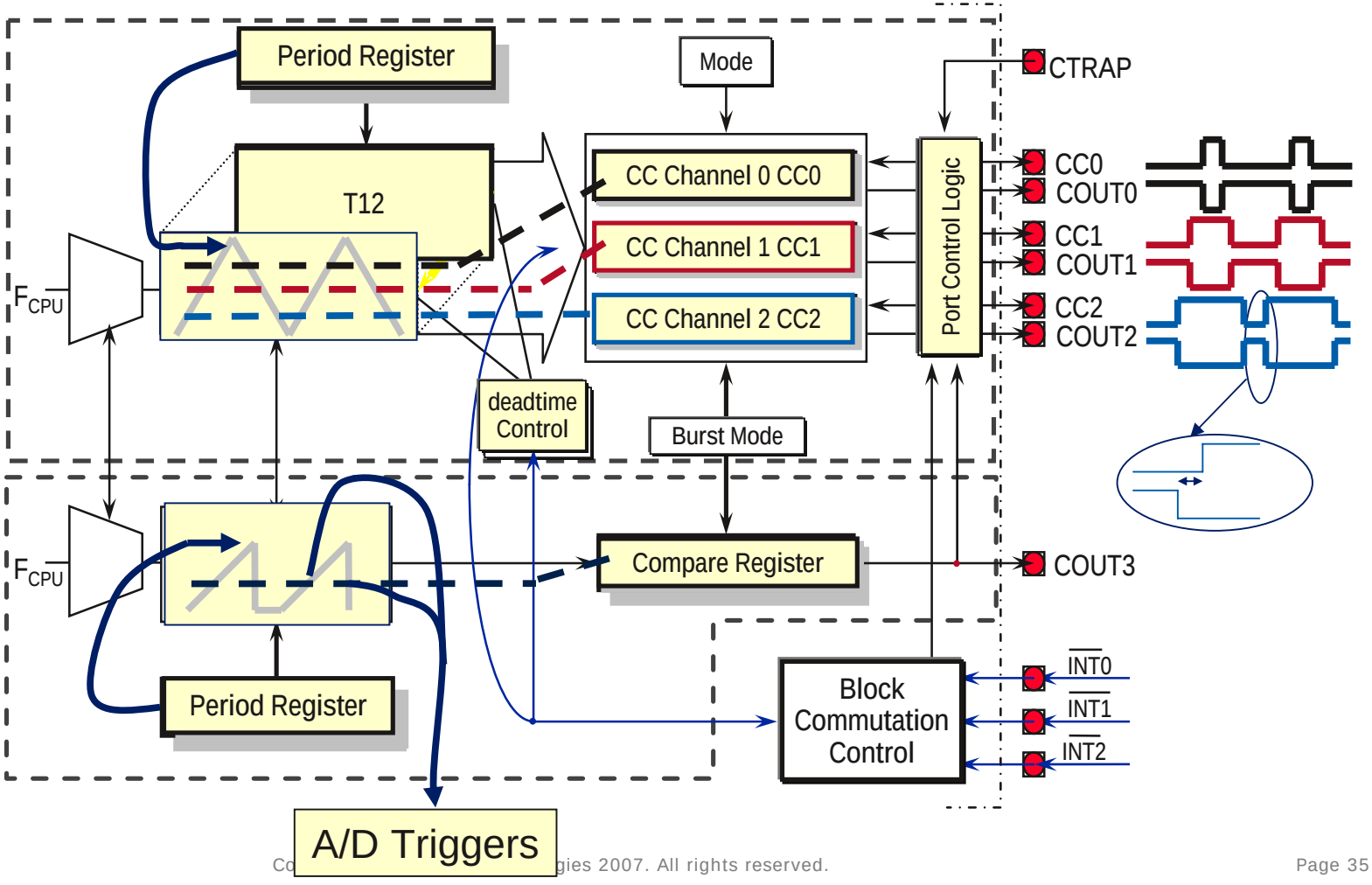
- Timer 12 features
  - Three capture/compare channels (each can be used as capture or as compare)
  - Supports generation of a three-phase PWM
  - 16-bit resolution
  - Dead-time control for each channel (avoid short-circuits in power stage)
  - Concurrent update of the required T12/T13 registers
  - Center aligned and edge aligned PWM
  - Single shot mode
  - Hysteresis-like control mode
  - Hall-mode for multiphase BLDC motors
- Timer 13 features
  - One independent compare channel with one output
  - 16-bit resolution
  - Can be sychonized to T12
  - Interrupt generation at period-match and compare-match
  - Single-shot mode supported

CAPCOM6E

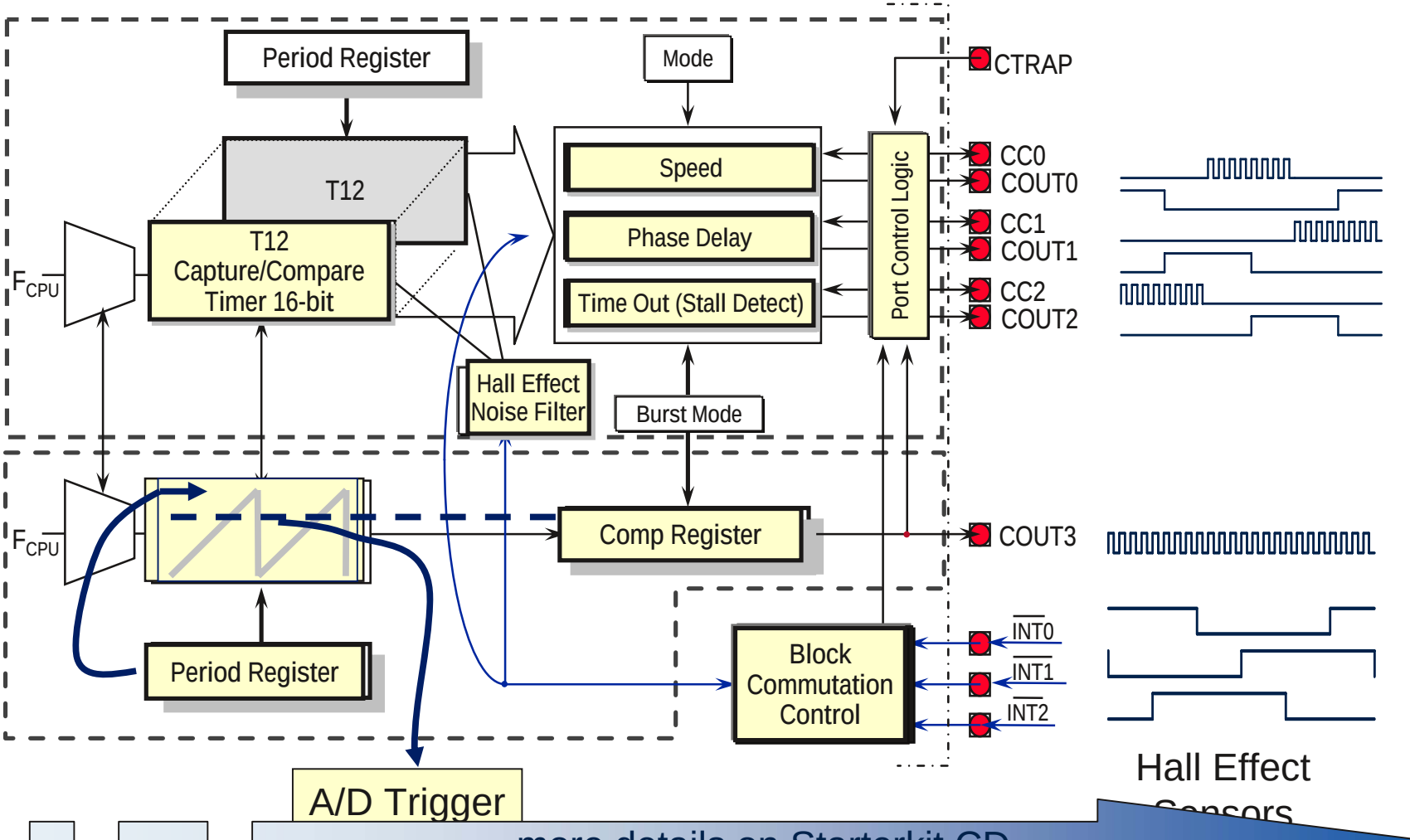
- Additional Features
  - Block commutation for Brushless DC-drives implemented
  - Position detection via Hall-sensor pattern
  - Automatic rotational speed measurement for block commutation
  - Integrated error handling
  - Fast emergency stop with CPU load via external signal (CTRAP)
  - Control modes for multi-channel AC-drives
  - Output levels can be selected and adapted to the power stage
- Module Interface
  - T12 and T13 can be started from external pin (T12HR, T13HR)
  - ADC can be synchronized on
    - T12PM
    - T12CM0,1,2
    - T13PM
    - T13CM
    - STR
    - CHE

CAPCOM6E – FOC of BLDC Motors

- T12 Generates Symmetric PWM with Dead-Time
- T13 in single shot mode and synchronized to T12 generates 2 A/D Triggers for current measurement



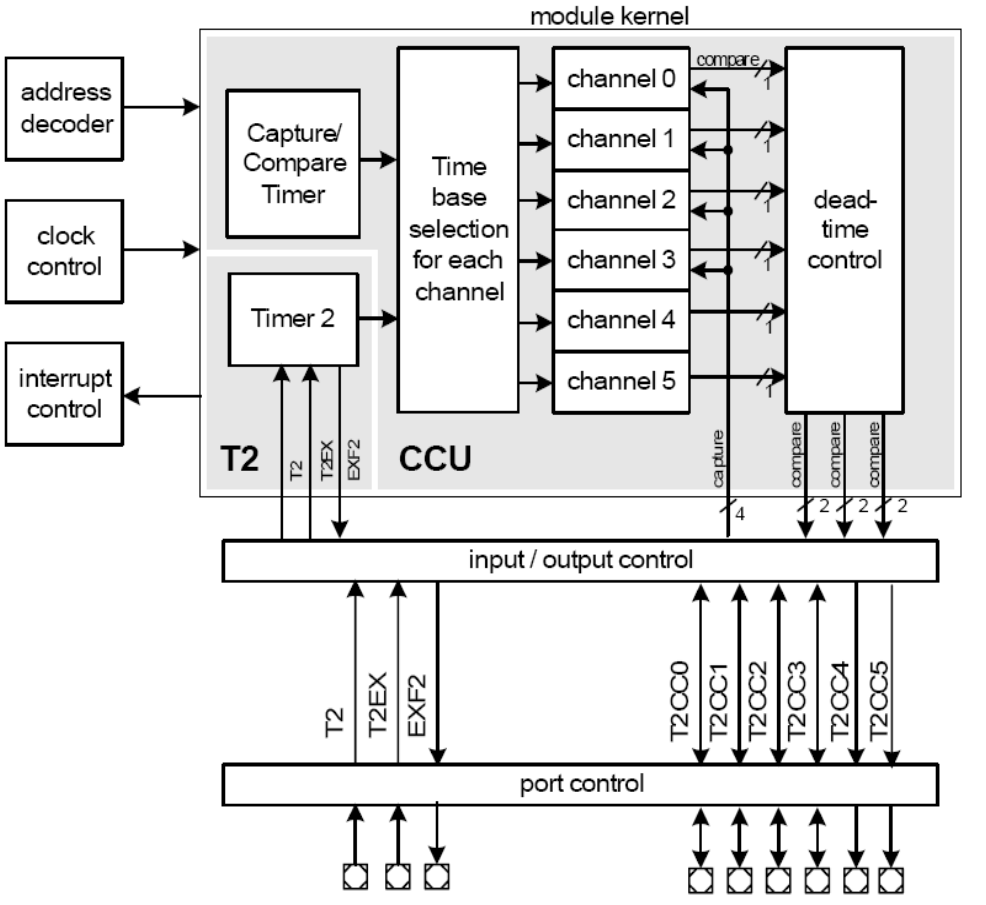
CAPCOM6E – BLDC Motors with Hall Sensors



more details on Starterkit CD

T2CCU – Overview

- T2CCU is a simplified Capture/Compare Unit
  - one 16bit autoreload timer which counts up
  - programmable reload value
  - interrupt on overflow
  - 6 independent capcom channels interrupt
  - two selectable time base units: CCT or T2
  - clock prescaler options up to ft2ccu = 2x fcpu (48MHz)
  - synchronize features for CCT & T2
  - ADC trigger features

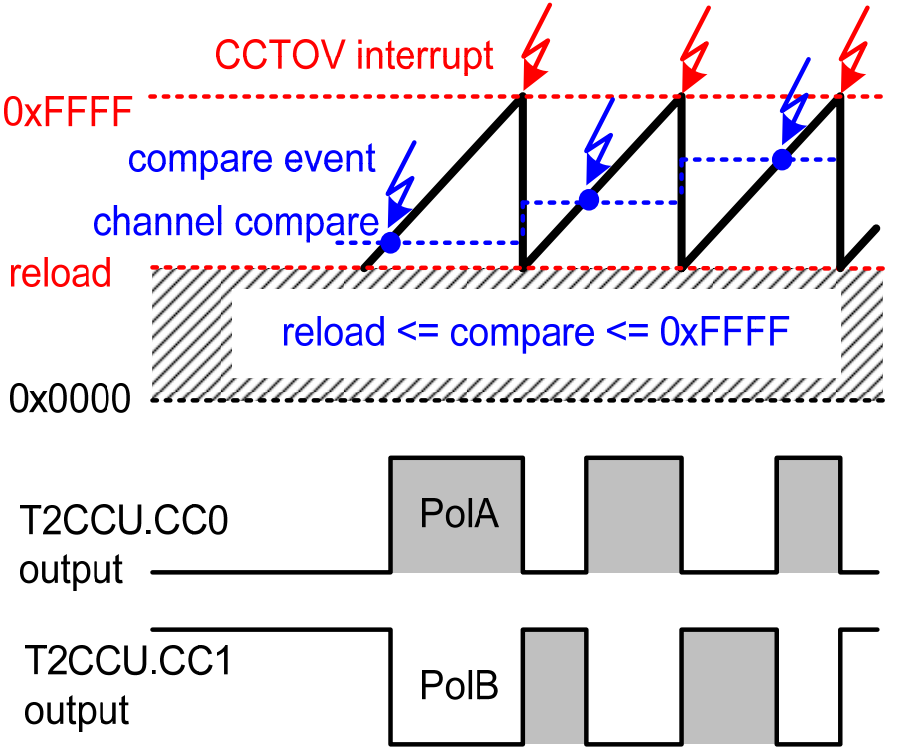


T2CCU – Applications

- T2CCU can be used for
  - stepper motor control (full-/half-/microstep)
  - 6 channel PWM generation (e.g. LED control)
  - 3 phase PWM with deadtime (motor control, PFC, lampballast)
  - multiple trigger pulses (e.g. for valve control)
  - capturing external events

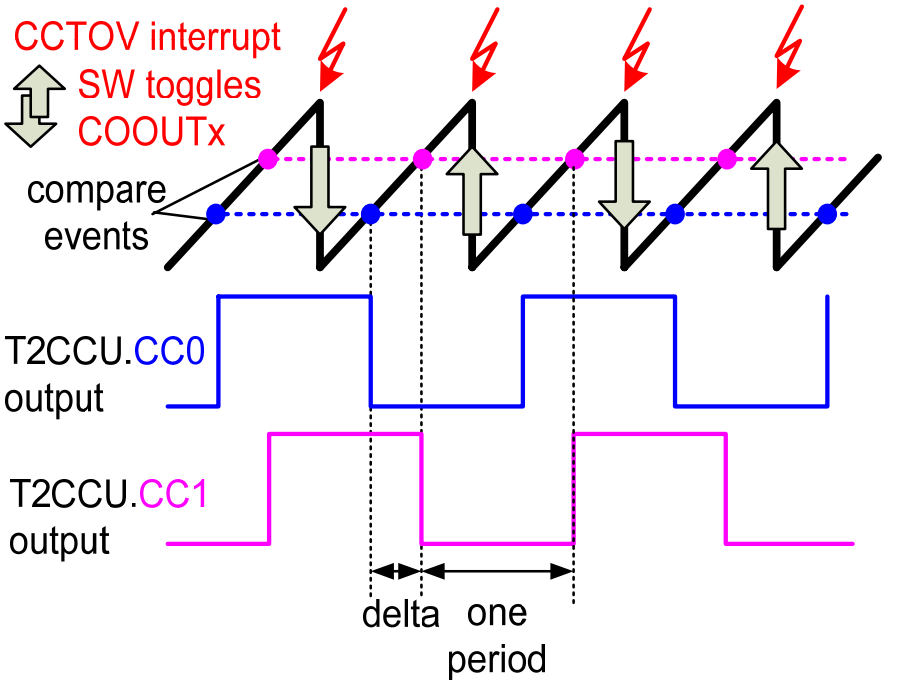
T2CCU – PWM Generation

- Compare Mode 0:
  - output change (set / reset) on
    - compare and overflow
  - up to 6 channels
  - 2 can be combined with PolA/B and **deadtime** for 3 phase halfbridge control
- shadow transfer mechanism for compare value update
  - update compare channels
  - set TXOF
  - clear TXOF
  - compare value is active with next timer overflow
- note: compare value must not be smaller than reload value



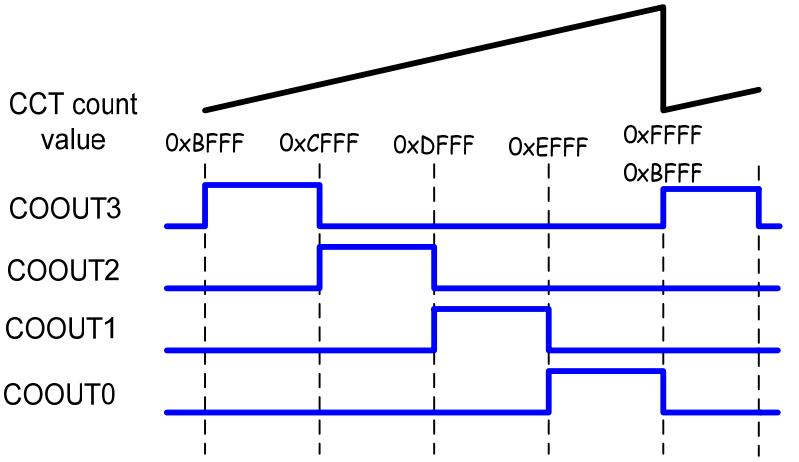
T2CCU – Pulse Pattern Generation

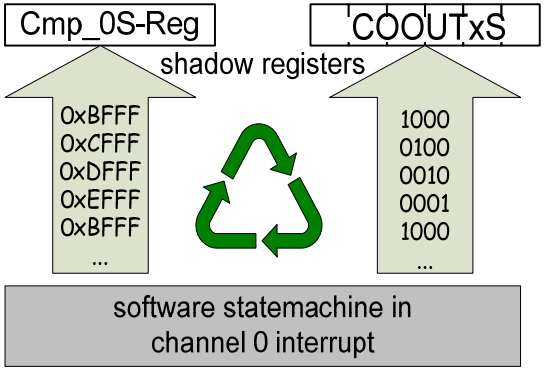
- Compare Mode 1:
  - use this mode for flexible pulse pattern generation
  - use TXOF for timer synchronous update for shadow transfer of all compare values



T2CCU – Stepper Motor Control

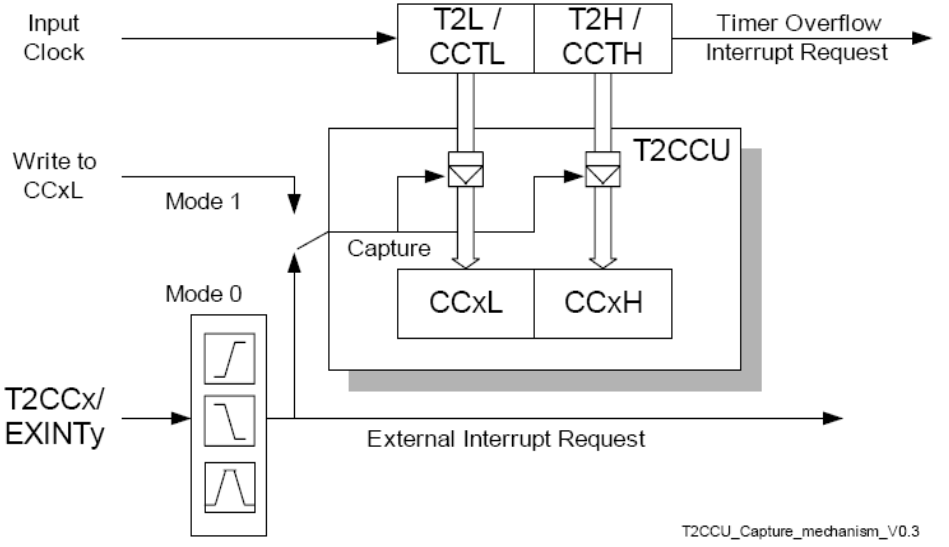
- Concurrent Compare Mode:
  - similar to Compare Mode 1
  - but only Compare 0 register has to be written
- Stepper Motor Control
  - fullstep / halfstep mode
  - timer period refers to speed
  - equidistant compare values
- use ENSHDW to update next compare value
- pattern & time schedule table can be used
- note: realtime update is mandatory





T2CCU – Capturing External Events

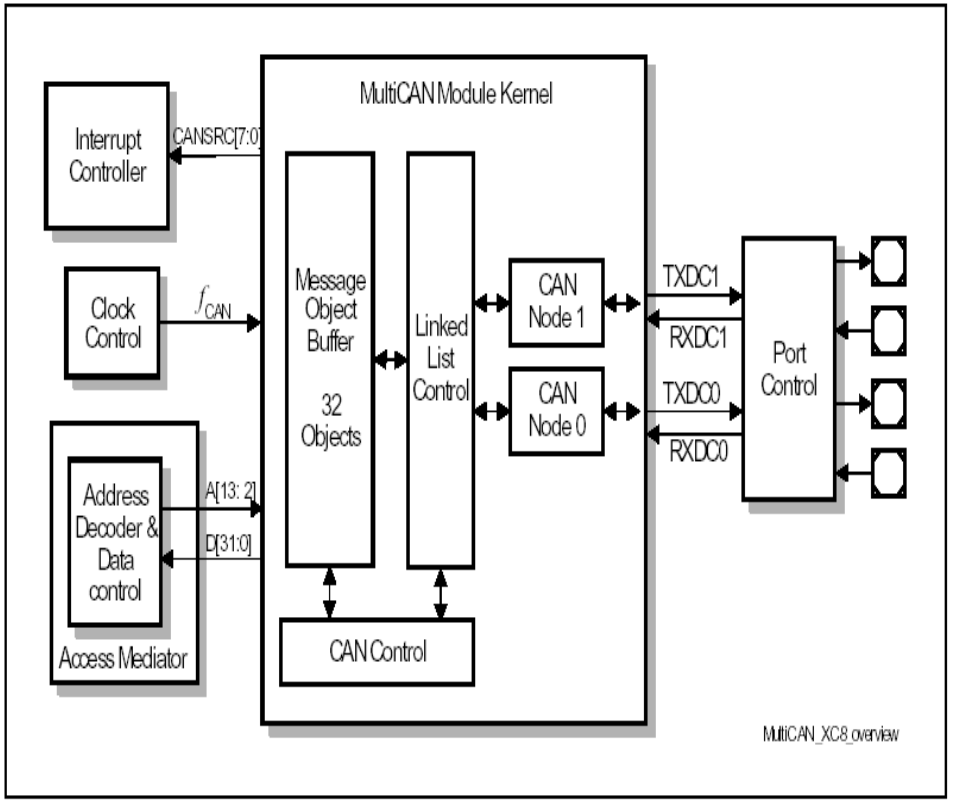
- Capture Modes :
  - capture external events on
    - rising / falling / both edges
  - soft-capture – read actual timervalue
  - individual interrupt flags for every capture event
- note: take care on timer overflow while capturing



more details on Starterkit CD

MultiCAN

- ISO 11898 compliant CAN module (V2.0B active)
- 2 independent CAN nodes, with dedicated control registers for each CAN node
- 32 independent message objects with acceptance mask filtering for each MO
- Data transfer rate up to 1MBaud
- Flexible and powerful message transfer control (double chained list) and error handling capabilities to offload CPU
- Automatic gateway mode support
- CAN Analyzer Mode for bus monitoring



MultiCAN Module Conformance Test

- CAN **Conformance test** for XC88xC passed
- CAN **Gateway test** passed

Fachhochschule
- University of Applied Sciences -
C&S communication & systems group
Prof. Dr.-Ing. W. Lawrenz
- Director C&S -

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D-38302 Wolfenbüttel

Infineon
CAN-Components

Authentication on CAN Conformance

C&S group is a subdivision of the Fachhochschule Wolfenbüttel. As such C&S is worldwide recognized as a neutral expert in testing of communication systems such as CAN Transceivers, CAN, CAN Software Drivers, (CAN) Network Management and LIN.

Herewith C&S group is proud to confirm that the following tests on the subsequently specified device implementations have been performed by C&S resulting in the findings given below:

C&S Conformance Test Results

CAN Component/Part Number	Infineon SAK XC886 CM-8FFA 5V AB-ES ZA602044 GE617
Hardware Manual Version	XC886/888 CLM V0.1, Jan 2006 XC886C_8FF_AB_Errata_Sheet_v1_1D1
Date of Tests	October 2006
Version of Test Specification	• ISO 16845:2004 Road vehicles – Controller area network (CAN) - Conformance test plan C&S enhancement / corrections: Reference: CAN Conformance Testing Test Specification C&S V1.4 • C&S Register Functionality/ Processor Interface Test Specification V2.0 • C&S Robustness Test Specification V1.3 • C&S Gateway Test Specification for XC886CLM V1.0
Corresponding Test Report	2006_159_022_Final_Report_01
Types of Tests:	
◦ ISO 16845 (+ C&S enhancements)	Pass
◦ Register Functionality (C&S defined tests)	Pass
◦ Robustness (C&S defined tests)	Pass
◦ Gateway (C&S defined tests)	Pass

Wolfenbüttel, 2006-Oct-11 Fischer, Senior Engineer Meitrodt, Project Manager

Quote No. 2006-159 R00

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Coprocessors – MDU

- MDU can be used for e.g.
  - long divisions
  - shifting data for scaling operations
  - together with Cordic in interleaved mode
  - example code available

Table 6-1 MDU Operation Characteristics

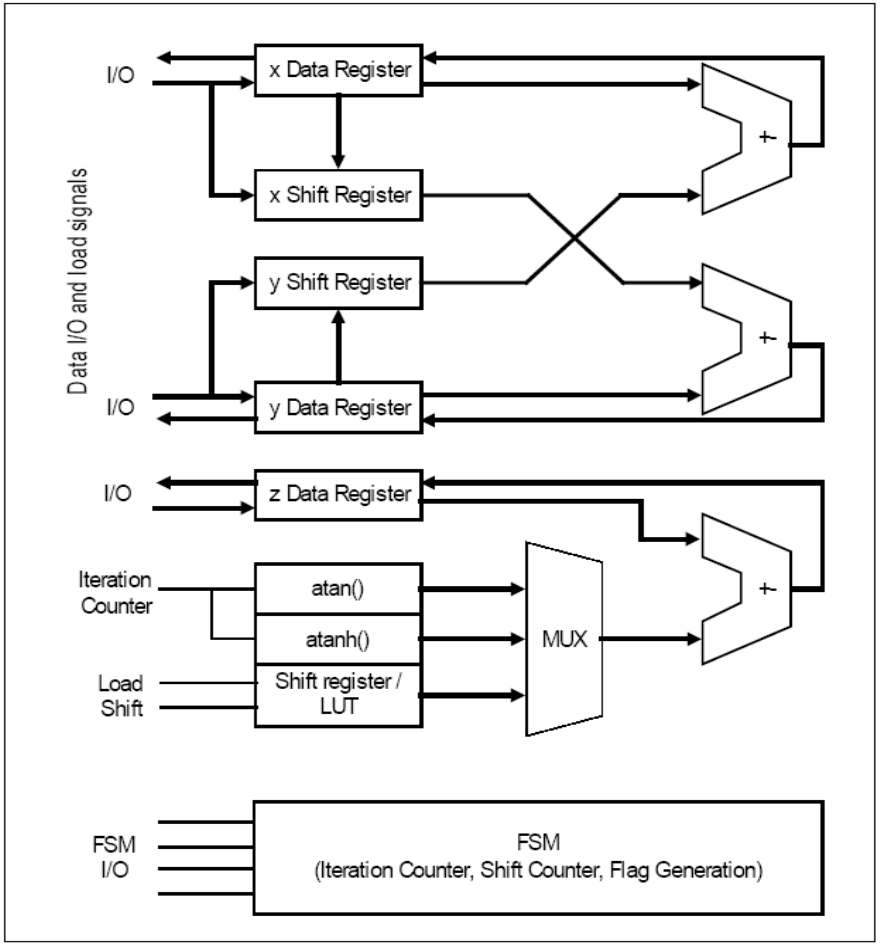
Operation	Result	Remainder	No. of Clock Cycles used for calculation
Signed 32-bit/16-bit	32-bit	16-bit	33
Signed 16-bit/16bit	16-bit	16-bit	17
Signed 16-bit x 16-bit	32-bit	–	16
Unsigned 32-bit/16-bit	32-bit	16-bit	32
Unsigned 16-bit/16-bit	16-bit	16-bit	16
Unsigned 16-bit x 16-bit	32-bit	–	16
32-bit normalize	–	–	No. of shifts + 1 (Max. 32)
32-bit shift L/R	–	–	No. of shifts + 1 (Max. 32)

- MDU runs at 2xfcpu at XC878
- CPU has to MOVE the operands and result
  - e.g. signed multiplication 16bit x 16bit: number of clocks 32 (load operands) + 16/2 (multiplication) + 32 (fetch result) = 72clk = 3.0µs @ 24MHz
- For continues MDU operation, next operands can be loaded in parallel to current calculation
  - e.g. continuous (interleaved) signed multiplication 16bit x 16bit: 16/2(multiplication) || 32 (load operands for next multiplication) + 32 (fetch result) = 56clk = 2.3µs @ 24MHz

Coprocessors – Cordic

- Cordic (**CO**ordinate **R**otation **DI**gital **C**omputer)
  - Mathematical co-processor for 16bit trigonometric, hyperbolic and linear functions (e.g. to solve SIN, COS, LOG, EXP, SQRT...)
  - Hardcoded - Look Up Table based on iterative approximation algorithm (16 iterations, max 41 cycles = 1.7us @24MHz)
  - Cordic runs at 2xfcpu at XC878

- Cordic can be used for e.g.
  - PI Controller
  - PT1 Filter
  - Clark / Park Transformation
  - Space Vector Modulator
  - ... example code available



Cordic – Math Functions

CORDIC		Rotation	Vectoring
Linear **MUL/DIV/MAC** **K = 1**	IN	x_n, z_n, y_n	x_n, y_n, z_n
	OUT	$y_{n+1} = x_n * z_n + y_n$	$z_{n+1} = y_n / x_n + z_n$
Circular **SINE/COSINE** **angle/** **magnitude** **K = 1.64676**	IN	z_n=angle, x_n=1/K, y_n=0	x_n, y_n, z_n=0
	OUT	$x_{n+1} = \cos(\text{angle})$ $y_{n+1} = \sin(\text{angle})$	$z_{n+1} = \arctan(y_n/x_n)$ $x_{n+1} = K*(x_n^2 + y_n^2)^{1/2}$
Hyperbolic **K = 0.828**	IN	z_1=angle, x_1=1/K, y_1=0	$y_1 < x_1$, z_1=0
	OUT	$x_{n+1} = \cosh(\text{angle})$ $y_{n+1} = \sinh(\text{angle})$	$z_{n+1} = \text{arctanh}(y_1/x_1)$ $x_{n+1} = K*(x_1^2 - y_1^2)^{1/2}$

more details on Starterkit CD

Agenda

- XC878 Product Presentation (Technical Overview)
  - Family Overview
  - System & Core
  - Embedded Memories
  - Standard Peripherals
    - GPIO
    - Timers & WDT
    - UART & LIN
    - SSC
  - Special Peripherals
    - ADC
    - CAPCOM6E
    - T2CCU
    - MultiCAN
    - MDU & Cordic
  - Debug Support & Toolchain

On-Chip Debug Support

- On-Chip Debug Support (OCDS)
  - Two interfaces can be used to access the OCDS system:
    - The JTAG interface is the primary channel
    - The UART is an alternative channel
  - Two dedicated pins are used for external configuration
    - TMS – JTAG activate (active high, integrated pulldown)
    - MBC – Bootstraploader activate (active low, external pullup required)
  - Breakpoints:
    - Up to 4 HW breakpoints on CODE and DATA
    - Unlimited SW breakpoints using the TRAP instruction within the code
      - The TRAP_EN bit must be set to 1 within the Extended Operation (EO) register.

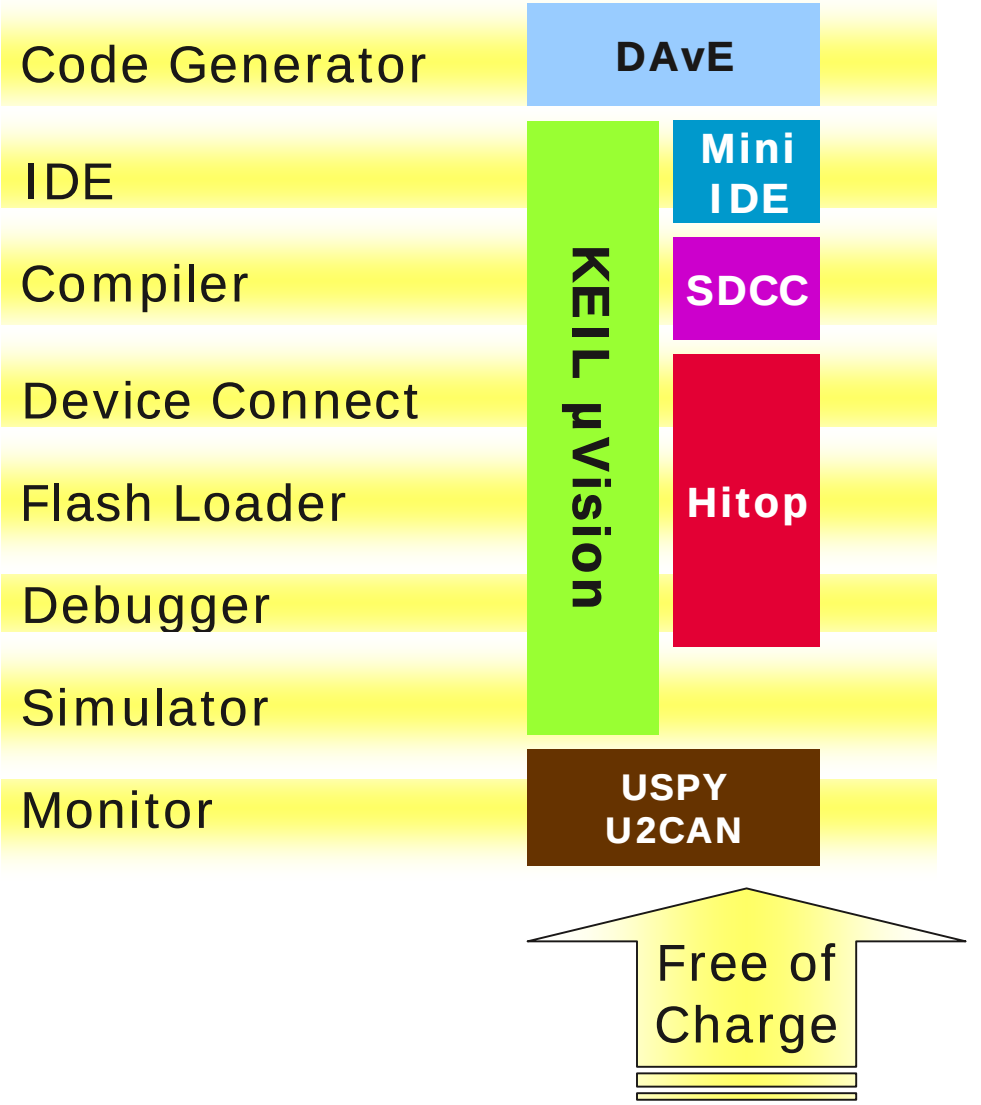
Getting Started Tools

- Starterkits, EasyKits, Evaluation Boards
  - for the XC800 family we offer hardware kits which can be ordered easily on
    - www.ehitex.de → Starter Kits for XC800

- All kits come with a complete toolchain with getting started presentation and tested example code - they are ready for use.

- The goal is that the getting started example can be repeated within 30min after unpacking.

Toolchain



Never stop thinking