UniversityDay 2020

Poster Sessions

Agenda

Time	What to Expect
09:00 – 09:10	Welcome and Introduction
09:10 – 09:50	1st Keynote Speech **“Quantum Computing”** Clemens Rössler, Process Integration Engineer (IFAT FE TV MMD)
09:50 – 10:20	Virtual Poster Session (FEOL & BEOL)
10:20 – 11:00	2nd Keynote Speech **“Master or Servant of Mankind? The Rise of Artificial Intelligence”** Martin Gebser, Endowed Professor for Adaptive and Connected Production Systems (AAU)
11:00 – 11:30	Virtual Poster Session (Device Characterization & Chip Design)
11:30 – 13:30	Lunch Break
13:30 – 14:10	3rd Keynote Speech **“Technology of Tomorrow”** Herbert Pairitsch, Head of R&D Funding PSS (IFAT PSS RDF)
14:10 – 14:40	Virtual Poster Session (Application)
14:40 – 15:30	PhD Quiz (PhD Students Only)

FEOL

Electrochemistry of SiC Semiconductors

Katharina Mairhofer

Mechanisms of photo-assisted anodic etching of SiC using different electrolytes are investigated. Electrochemical methods are complemented by surface sensitive qualitative and quantitative analysis using XPS.

Link to WebEx Meeting (9:40 am – 10:20 am):
https://infineon.webex.com/infineon/j.php?MTID=m0d961934e6309e8d61abcec75698c334

Predicting Materials Properties Using Artificial Intelligence And First Principles Calculations

Sebastian Bichelmaier

By combining machine learning techniques with highly accurate quantum mechanical simulations, a Proof of Concept virtual laboratory can be created. We use this framework to explore the properties of the highly complex Hafnia phase space.

Link to WebEx Meeting (9:40 am – 10:20 am):
https://infineon.webex.com/infineon/j.php?MTID=mb11e3505c789dd981c90c5fc2bd7f59f

Electron Mobility Increase by Strain Engineering in Modern Power MOSFETs

Stefan Karner

Electron mobility in Si trench power nMOSFETs is modified by functional stress layers. Strain-modified devices are investigated electrically as well as physically and are compared to state-of-the-art power devices.

Link to WebEx Meeting (9:40 am – 10:20 am):
https://infineon.webex.com/infineon/j.php?MTID=mf89834dac25587e62050331df830fc9e

Cylindrical Gas-Gap Capacitor Structure

Peter Oles

The aim is to obtain a physical understanding of gas gaps within micro- and nanometer silicon structures at high electric fields. In the semiconductor industry gas gaps are on the rise as the ultimate low-k dielectric and also occur in MEMS devices. The fundamental approach of this study enables a profound assessment of the evolution of such systems in terms of performance and reliability.

Link to WebEx Meeting (9:40 am – 10:20 am):
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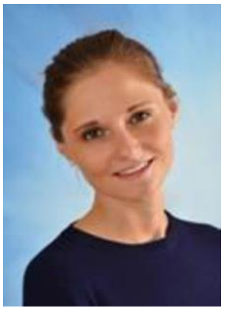

Challenges of Interface Characterization: Technical Requirements for SiC

Sabrina Frager

Explanation of common used methods to characterize interfaces.

Link to WebEx Meeting (9:40 am – 10:20 am):
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Analysis Of Voiding in Thin Cu Metallizations

Manuel Kleinbichler

In order to improve reliability, it's important to understand the early stages of thermo-mechanical fatigue. This work deals with the experimental observation and thermo-dynamical simulation of voids, who are known to be the earliest stage of fatigue.

Link to WebEx Meeting (9:40 am – 10:20 am):
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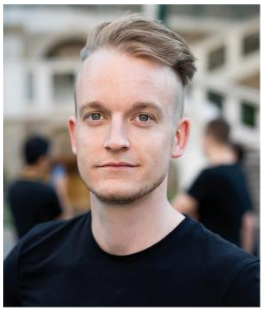
Tuning High-Performance Polyimides for Microelectronics

Elias K. Bumbaris



Polyimides are high-performance polymers of the utmost thermal, chemical and mechanical stability. As they additionally exhibit very high breakdown voltage and low dielectric constant, they are the polymer of choice in the microelectronics industry. Nonetheless, certain corrosion phenomena taking place on vital parts of microelectronic components throughout their operating time are assumed to be due to the ability of commercially available polyimide compositions to let ions and humidity migrate through the protective layer they form. Our goal is to minimize the effect of ion and water migration by tuning polyimides in terms of synthesis, choice and combination numerous suitable monomers, in order to enhance the reliability of affected electronic components.

Link to WebEx Meeting (9:40 am – 10:20 am):
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New Photo Resist Concepts For Wet Etch Metal Layers

Julia Modl

In recent times problems with unwanted etching of metal lines arose due to the poor adhesion of photo resists to metal substrates. The cooperation with the resist supplier Merck KGaA targets the development of a photo resist that meets several requirements.

Link to WebEx Meeting (9:40 am – 10:20 am):
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BEOL

Development Of a Process Flow To Enable Packaging On Wafer Level

Barbara Glanzer

Currently used serial processing steps are aimed to be transferred into parallelized process steps to enhance packaging throughput. Based on this motivation, the development of a process flow enabling packaging on wafer level is comprised in this work.

Link to WebEx Meeting (9:40 am – 10:20 am):
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Electropolishing as a Preparation Technique for Bulk Degradation Analysis of Cu

Sebastian Moser

Power semiconductor devices may be subjected to rapid heat cycles caused by electrical overload events resulting in fatigue of their metallization.
Electropolishing is a new sample preparation technique that allows studying early stages of bulk fatigue (void and crack formation) and, therefore, compare different materials in terms of their robustness in order to be able to increase the lifetime of future products.

Link to WebEx Meeting (9:40 am – 10:20 am):
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Atomistic Simulations of Elasticity and Interface Properties in Layered Metal Systems

Rishi Bodlos

In this poster we characterise the thermomechanical properties of WTI ar properties of Cu-Wti.

Link to WebEx Meeting (9:40 am – 10:20 am):
https://infineon.webex.com/infineon/j.php?MTID=m24337ef538aa72c09a5558bd1574de68

Impact of Morphology on Residual Stresses in TiW Thin Films

Rahulkumar Sinojiya

Residual stresses in thin films depend strongly on composition, morphology, thickness, thermal loading etc. To design efficient thin films, study of residual stresses in depth is necessary.

Link to WebEx Meeting (9:40 am – 10:20 am):
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Locally Resolved Deformation and Fracture Processes Near Interfaces

Markus Alfreider

The ongoing miniaturization of microelectronic devices creates a rather challenging environment for materials from a structural as well as thermo-mechanical point of view. Especially, the various interfaces (grain-/phase- boundaries; substrate-thin film interface) appearing in these devices undergo a unneglectable strain and are therefore important to understand. Using the WTi/Cu interface as a demonstrator, the aim of this work is to:

- Develop advanced techniques to investigate interface fracture.
- Understand the influence of these interfaces on local mechanical properties.

Link to WebEx Meeting (10:50 am. – 11:30 am.):
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Buffer and Surface Trapping in GaN Based HEMTs

Valeria Padovan

Hot carrier degradation is a process in which electrons injected from the source can be accelerated by the high electric field and be trapped in the buffer or in the AlGaN surface. For GaN HEMT is important to understand this degradation because is probably the cause of the device's failure during Hard Switching.

Link to WebEx Meeting (10:50 am. – 11:30 am.):
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Carrier Mobilities in 4H-SiC Trench MOSFETs

Judith Berens

The electron channel mobility of SiC power MOSFETs is still significantly smaller than theoretically reachable mobilities because of electrically active traps at the interface to the oxide. This thesis deals with the understanding of the reduced channel mobility and reliability challenges caused by interface and oxide defects.

Link to WebEx Meeting (10:50 am. – 11:30 am.):
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Simulation of Fatigue Damage in Power Semiconductors

Paul Hoffmann

Development and calibration of a physical lifetime model to predict fatigue damage in power semiconductor devices. In the poster, the developed bulk fatigue approach is applied to generic copper-on-silicon geometries which are exposed to various transient thermo-mechanical loading.

Link to WebEx Meeting (10:50 am. – 11:30 am.):
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Electrochemical Investigation of Ion Diffusion Through Polymer Membranes in Combination with FEM Modelling

Lars Varain

Ion diffusion coefficients are determined by an combination of electrochemical measurements and FEM simulation.

Link to Webex Meeting (10:50 am. – 11:30 am.):
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Electrical Characterization of Point Defects in Si High Voltage Diodes

Lena Bergmann

Characterization of relevant point defects in Si and their impact on devices (power diodes). Further development of the DLTS measurement method for higher voltages to measure defects throughout whole thickness of sample.

Link to WebEx Meeting (10:50 am. – 11:30 am.):
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Understanding the Role and Impact of Holes in Epi-Based Degradation Mechanism In GaN Devices

Dominik Wieland

The work aims to continue the investigation on the fundamental electrical behavior of holes in the buffer as well as in the lateral device behavior and furthermore study the physical origin of dynamic fails of GaN Hybrid-Drain Gate-Injection Transistors (HDGIT).

Link to WebEx Meeting (10:50 am. – 11:30 am.):
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Matrix Independent Quantification of Trace Elements in Polymers Using Laser Induced Breakdown Spectroscopy (LIBS)

Lukas Brunnbauer

Contaminations of various metals in polymers may lead to severe corrosion problems. Laser Induced Breakdown Spectroscopy (LIBS) is a powerful analytical tool for trace metal detection which is evaluated for quantitative trace metal determination in this work.

Link to WebEx Meeting (10:50 am. – 11:30 am.):
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Degradation of Silicon Trench MOSFETs in Repetitive Avalanche Breakdown

Bernhard Ruch

The degradation of the Si-SiO2 interface of trench MOSFETs is investigated after hot carrier stress and the interface defects are characterized with charge pumping and capacitive methods. Those results will be supported by TCAD simulations.

Link to WebEx Meeting (10:50 am. – 11:30 am.):
https://infineon.webex.com/infineon/j.php?MTID=m7a36d934da6cb125637adacfbd8be978

Development of a Mixed Flowing Gas System for Accelerated Aging of Protective Polymer Coatings to Stimulate Atmospheric Corrosion With In-Situ Electrochemical Measurement and Subsequent Laterally Resolved Chemical Analysis

Jakob Willner

The development of a mixed flowing gas system for accelerated weathering of semiconductor devices for the study of atmospheric corrosion effects is the primary goal at first. After the evaluation of a reproducibly working MFG system, the focus switches to testing different protective polymer coatings in different weathering conditions, coupled with in-situ electrochemical measurement methods (metallization structure between silicon substrate and protective polymer) and subsequent chemical analysis of weathered samples (protective polymer, metallization and interface) using LIBS and LA-ICP-MS.

Link to WebEx Meeting (10:50 am. – 11:30 am.):
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EMI Robustness of Three-Electrode Electrochemical Sensor Front-Ends

Markus Haberler

Electrochemical sensor front-ends are susceptible to EMI due to a demodulation of the disturbance signal in corresponding front-end amplifiers. The demodulation process leads to a dc offset in the electrode controlling amplifiers, which influences the electrochemical analysis.

Link to WebEx Meeting (10:50 am. – 11:30 am.):
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Sub-Microwatt CMOS Rectifier for a Passive Wake-Up Receiver

Darshan Shetty

A fully-passive wireless wake-up receiver reduces the power consumption of a Internet of Things Node. The focus of the research is the design of an ultra-low power CMOS rectifier which is the front-end block of the wake-up receiver, responsible for converting the incoming wireless energy to DC energy.

Link to WebEx Meeting (10:50 am. – 11:30 am.):
https://infineon.webex.com/infineon/j.php?MTID=m25e4e29b981527c6781f8577ec04d1a3

Microstructure Segmentation in SEM & FIB Images

Dženana Alagić

The microstructure characteristics define physical and mechanical properties of a material, an important information in different areas of research. In this PhD, an image processing algorithm to automatically extract quantitative microstructure information out of SEM & FIB images is developed.

Link to WebEx Meeting (2:00 pm. – 2:40 pm.):
https://infineon.webex.com/infineon/j.php?MTID=m1e0d6b9a0549e9a84e26fd059f15b457

Modular Vehicle Authentication Architecture with Hardware Security Support

Dominic Pirker

Authentication is important for any application where permissions need to be checked, or access rights are required to be verified. Authentication information has to be protected, this is where hardware security needs to be in place.

Link to WebEx Meeting (2:00 pm. – 2:40 pm.):
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Monitoring Concepts for FMCW Radar Receiver

Matthias Wagner

Monitoring functions can be used to cope with the strict safety requirements of modern radar sensors. One of the most significant nonlinearities is caused by the analog to digital converter and has high impact to the sensitivity of the radar receiver.

Link to WebEx Meeting (2:00 pm. – 2:40 pm.):
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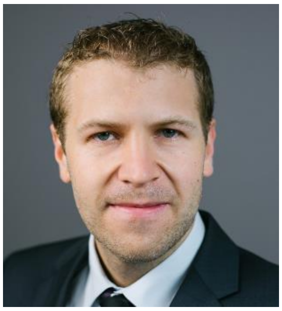
Application

Prediction of FIT Rates with Confidence

Patrick Plum



The FIT Rate is a crucial reliability metric for ATV power ICs, which is currently determined from lookup tables of industry standards. Because Base Failure Rates from these standards often overestimate the observed failure rates in the field by orders of magnitude, we are investigating, how to predict these by utilization of data from technology reliability testing while accounting for uncertainty.

Link to WebEx Meeting (2:00 pm. – 2:40 pm.):
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Robustness Validation of SiC MOSFETs

Markus Sievers

This project investigates how to construct a robust application stress test for high power SiC MOSFETs. It also researches various ways to characterize the devices under test within the application stress test without having to remove the DUT from the test hardware.

Link to WebEx Meeting (2:00 pm. – 2:40 pm.):
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Flexible Real-Time Communication with Elastic Slot Boundaries

Sascha Einspieler

The presented poster describes a flexible time-triggered communication approach allowing real-time behavior under normal conditions while it provides a fallback when temporal boundaries are violated. To investigate its performance it has been compared to a purely time-triggered communication system running different communication scenarios.

Link to WebEx Meeting (2:00 pm. – 2:40 pm.):
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Application

InterCEPT: Interference Mitigation Concepts and Efficient Processing Techniques

Mate Toth

Mutual automotive radar interference may seriously degrade the detection sensitivity and accuracy of objects on the road, which is of utmost importance for safety. To deal with the issue, novel concepts and algorithms for interference mitigation are investigated in this project.

Link to WebEx Meeting (2:00 pm. – 2:40 pm.):
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High-Resolution Tomographic Radar

Andreas Och

A novel high-resolution radar tomography system for the non-destructive characterization of low permittivity materials provides detailed real-time information in industrial processes. Infineon's 77 GHz radar modules are employed to realize a low cost and low complexity solution that helps to reduce carbon emissions, e.g., in steel manufacturing.

Link to WebEx Meeting (2:00 pm. – 2:40 pm.):
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Single Trapped Ions For Quantum Computing

Silke Auchter

Single ions that are trapped with electromagnetic fields can be used as a basis for quantum operations. The highly precise industrial microfabrication of such an ion trap chip brings us one step closer to realizing a scalable, universal trapped-ion quantum computer.

Link to WebEx Meeting (2:00 pm. – 2:40 pm.):
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FMEA Assistant
Houssam Razouk

Data driven hypotheses generation system for root cause analysis and risk assessment knowledge completion system.

Link to WebEx Meeting (2:00 pm. – 2:40 pm.):
https://infineon.webex.com/infineon/j.php?MTID=m21c01cf0f15d084127b5e295b61430d2

Sensor Data Fusion System for Optimization of Human/Robotic Collaboration
Feryel Zoghlami

The proposed solution consists in developing a compact intelligent system that combines data from different kinds of 3D sensors in order to achieve a fast, adaptive and robust perception of the surrounding environment (with a focus on the human behavior tracking and predicting).

Link to WebEx Meeting (2:00 pm. – 2:40 pm.):
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Dynamic Pulse Test Methods for Discrete High Power Semiconductors
Konstantinos Patmanidis

Construction of a multichannel system for stressing discrete high voltage power devices under dynamic pulse stressors.

Link to WebEx Meeting (2:00 pm. – 2:40 pm.):
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GaN Switching Locus Curve Determination for Application Related Reliability Test System
Sybille Ofner

The thesis aims to develop stress test concepts and systems for GaN HEMT devices under application-related conditions with switching frequencies from 1 MHz to 10 MHz to study the interaction between the device and the application. It includes investigation of suitable circuit topologies, sensing techniques, protection concepts, electromagnetic compatibility, and control.

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Temporal Fault Analysis of a Distributed Hard Real-Time System for Application-Oriented Stress Tests
Arpitha Prabhakara

The objective of the thesis are to investigate the temporal faults of the hard real-time system and to develop fault recovery mechanism for the industrial safety-critical system.

Link to WebEx Meeting (2:00 pm. – 2:40 pm.):
https://infineon.webex.com/infineon/j.php?MTID=ma582ac8156574aa2c54ab3a9cd12c0d1

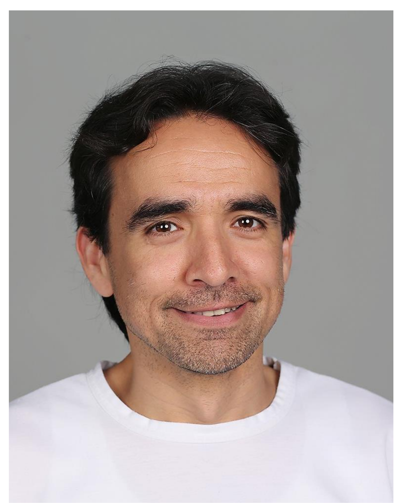
Posters

FEOL

Katharina Mairhofer

Silvia Larisegger

Francisco Santos



Electrochemistry of SiC Semiconductors

Introduction

Anode (Oxidation): (as postulated in literature)

$SiC + 3\,H_2O + 6\,h^+ \rightarrow SiO_2 + CO + 6H^+$

$SiO_2 + 6\,HF \rightarrow SiF_6^{2-} + 2\,H_2O + 2\,H^+$

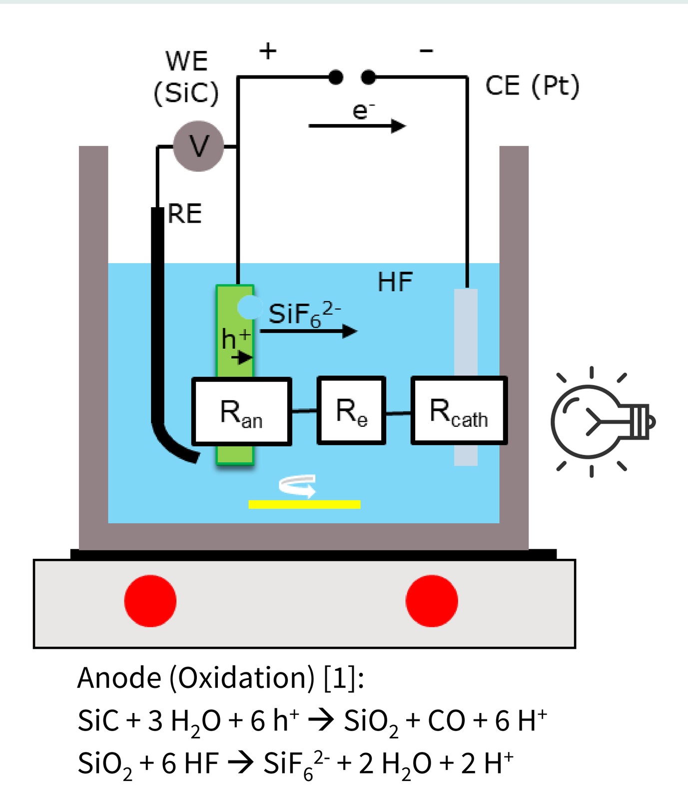


Figure 1: Schematic set-up with three electrodes for photo-assisted electrochemical etching of SiC.

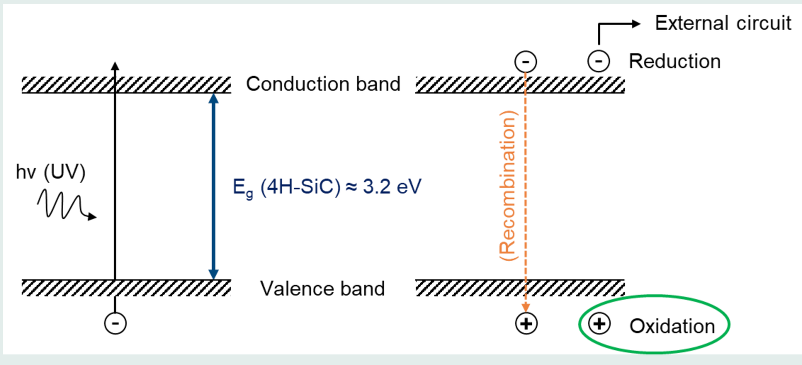


Figure 2: Etching mechanism of photo-assisted etching [2].

The distinctive chemical and physical properties of silicon carbide open up a wide field of possible applications. This in turn opens up completely new surface treatment approaches. (Photo-assisted) anodic etching as a specific form of wet etching represents a possible approach, for which the particular mechanisms and surface reactions are not elucidated yet.

[1] van Dorp, D. H., Sattler, J. J. H. B., den Otter, J. H., & Kelly, J. J. (2009). Electrochemistry of anodic etching of 4H and 6H-SiC in fluoride solution of pH 3. *Electrochimica Acta*, *54*(26), 6269–6275.

[2] Zhuang and Edgar, "Wet etching of GaN, AlN, and SiC: A review," *Materials Science and Engineering: Reports,* vol. 48, no. 1, pp. 1-46, 2005.

Experimental Set-Up

Modification of n-type SiC is done using a combination of anodic polarization and irradiation with UV light in a liquid electrolyte. In this work, the Si face of SiC wafers is investigated.

Different electrolytes relevant for etching, e.g. hydrofluoric acid (HF), potassium hydroxide (KOH) and tetramethylammonium hydroxide (TMAH), are used. Etching in n-SiC occurs according to three fundamental steps: (1) Generation of electron-hole pairs through UV illumination (2) oxidation of Si and C (3) dissolution of SiO_x in the electrolyte [2].

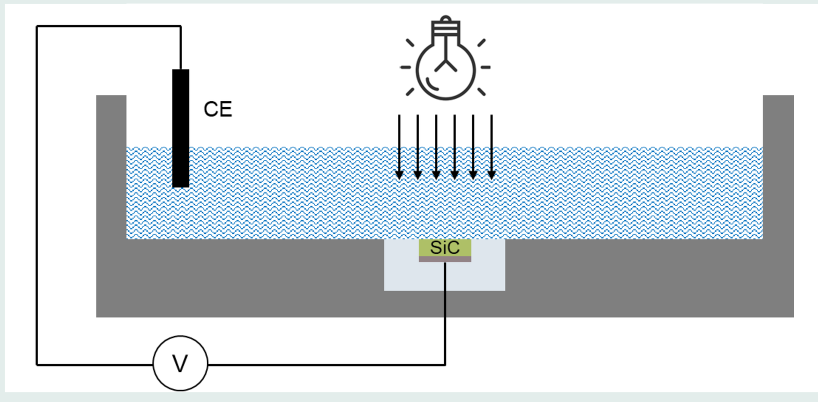


Figure 3: Simplified sketch of the PEC set-up.

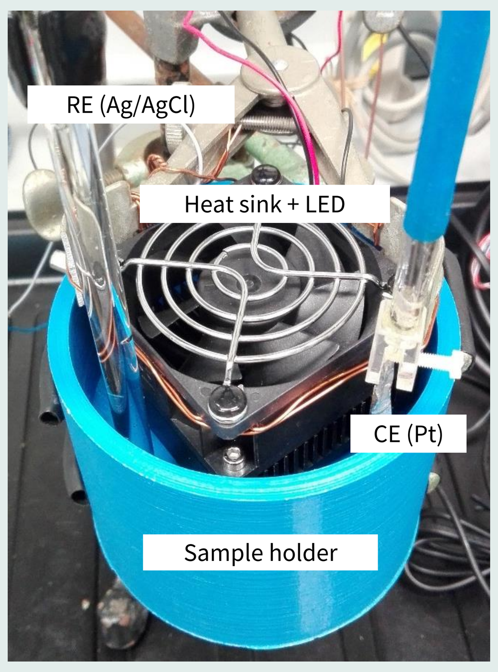


Figure 4: Photograph of the PEC set-up.

Concept of a Rotating Disk Electrode (RDE)

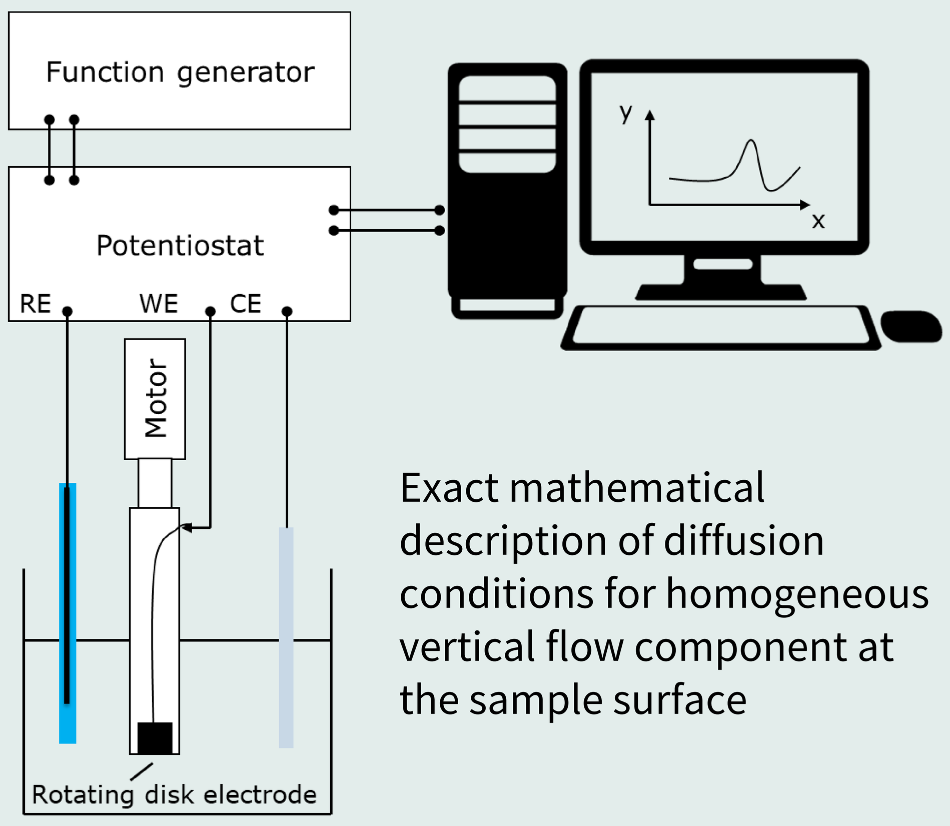


Figure 5: Schematic of an RDE set-up.

Investigation of different electrochemical reactions regimes through defined diffusion conditions

Exact mathematical description of diffusion conditions for homogeneous vertical flow component at the sample surface

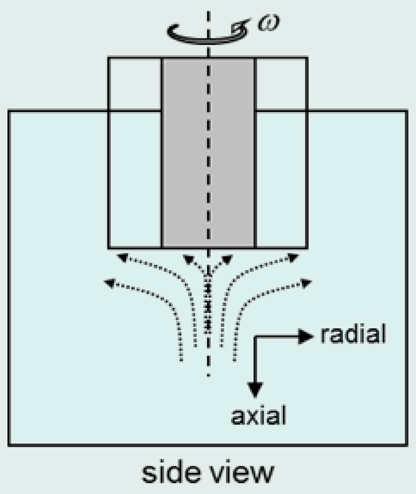


Figure 6: Flow profile in an RDE in side view.

Challenges Using Conventional RDEs

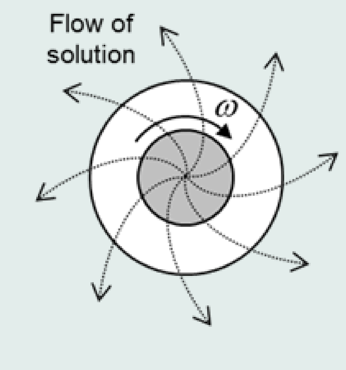


Figure 7: Flow profile in an RDE in bottom view.

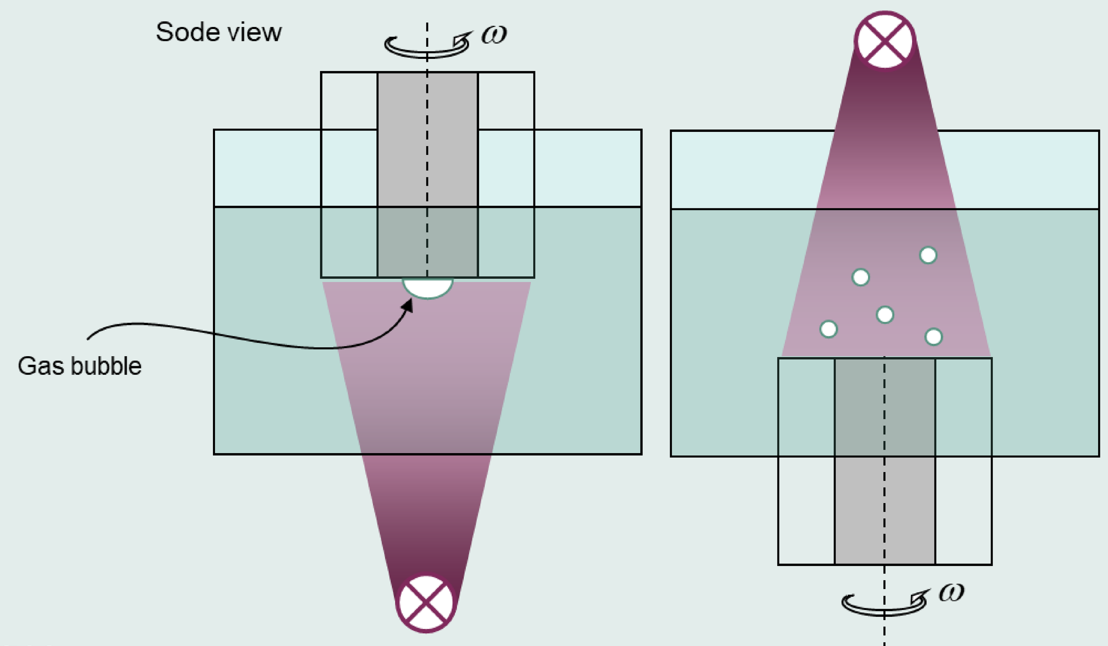


Figure 8: Conventional (left) and reversed (right) RDE set-up.

Additional challenges:

- Leak tightness
- Homogeneous illumination of the sample surface
- Evolution of gaseous reaction products

Construction of Adapted RDE Cell

CAD cell construction complemented by CFD simulations

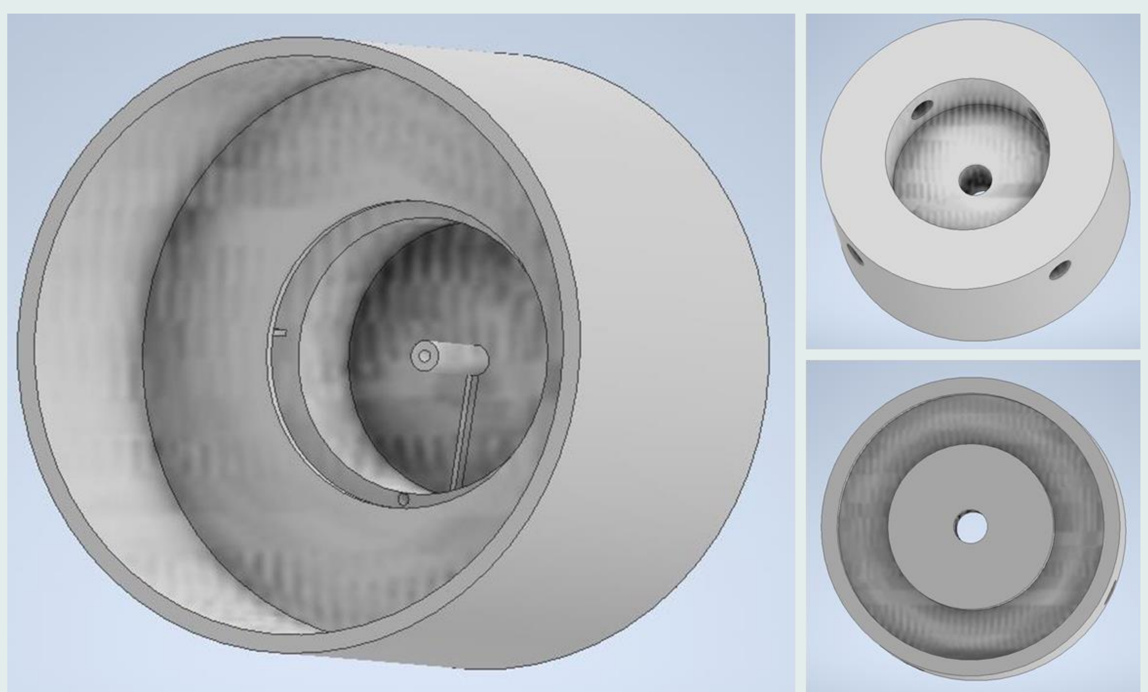


Figure 9: 3D model for stator (left) and rotor (right).

CFD Simulation

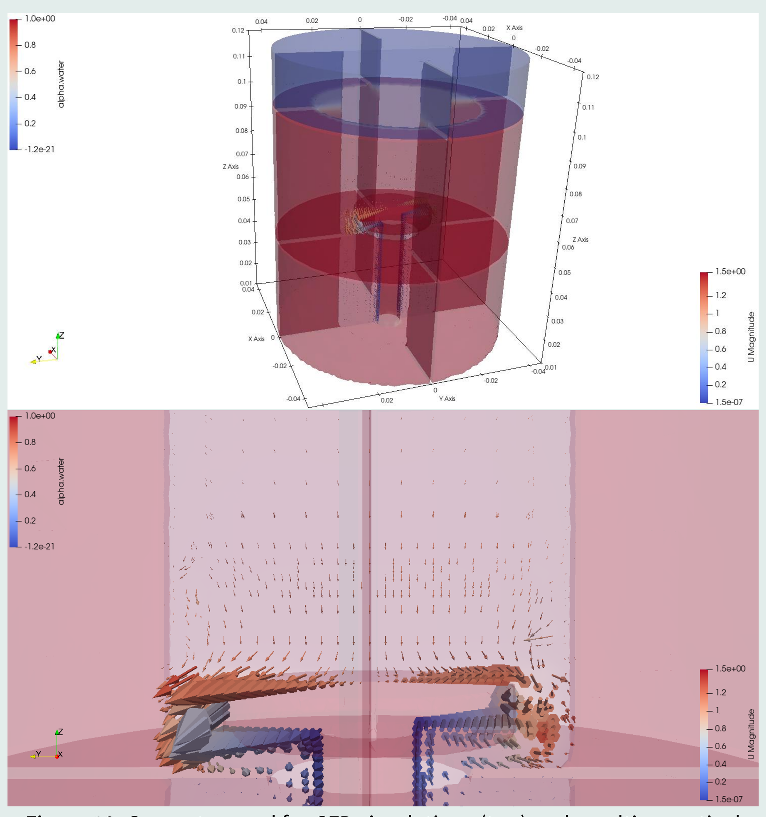


Figure 10: Geometry used for CFD simulations (top) and resulting vertical flow profile (bottom) [Philipp Mayr, TU Graz].

Surface Characterization by XPS

Gathering information about surface elements and their quantities, binding states and depth distribution using XPS permits to draw a connection between electrochemical pro-cesses and measureable surface conditions.

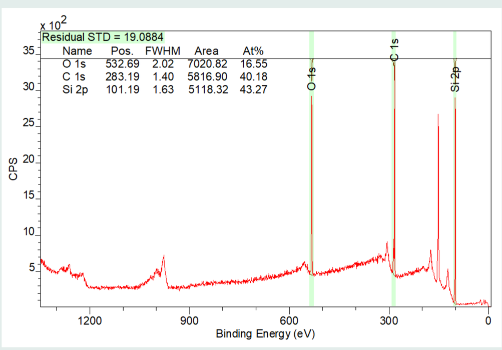


Figure 11: XPS spectrum of blank SiC wafer.

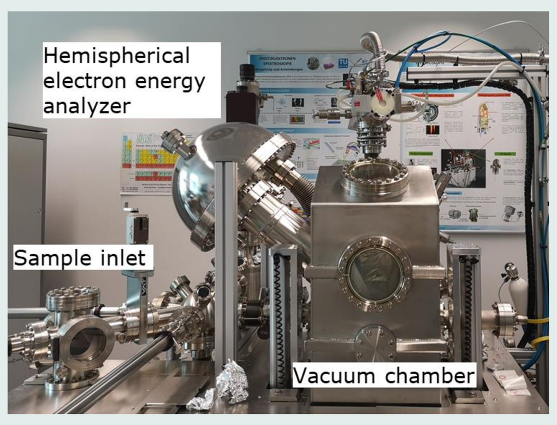


Figure 12: XPS system with monochromatic Al Kα X-ray source.

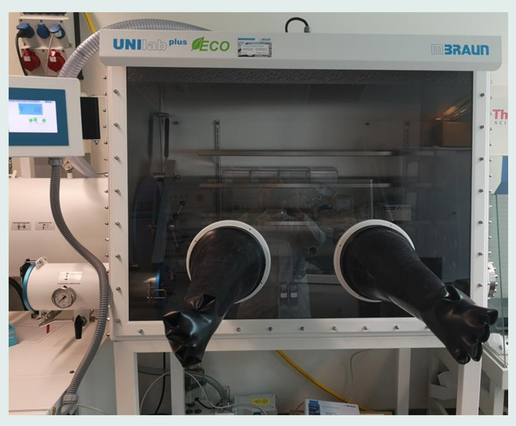


Figure 13: Glove box for quasi in-situ sample preparation.

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PREDICTING MATERIALS PROPERTIES USING ARTIFICIAL INTELLIGENCE AND FIRST PRINCIPLES CALCULATIONS

Introduction

The recent developments in the field of Artificial Intelligence have touched on many aspects of life and business. Materials research is no exception, and currently combining ab initio simulations with machine learning is becoming a hot topic.

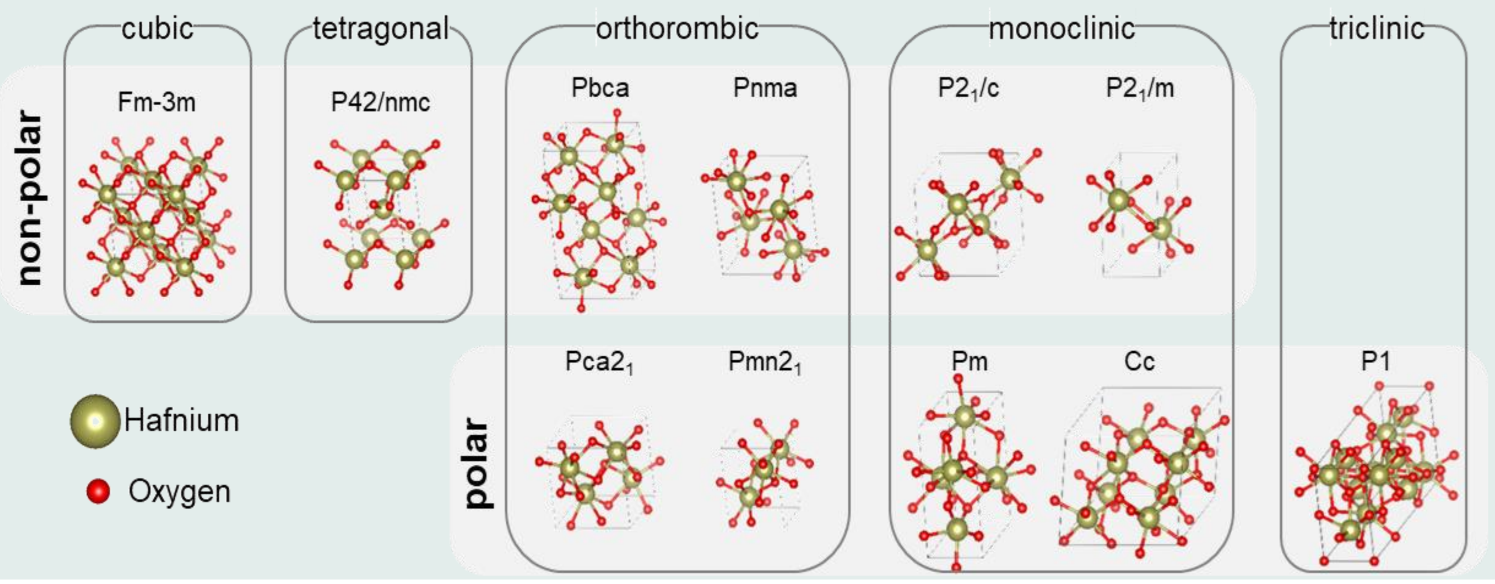
These developments can be exploited to drastically increase flexibility and speed of atomistic simulations, thereby establishing a „Virtual Laboratory“ for materials assessment.

As a demonstrator material, HfO_2 was chosen: with the quite recent discovery of ferroelectric properties, and vast processing experience within semiconductor industry as a high-k dielectric, HfO_2 is a material of high scientific impact and interest.

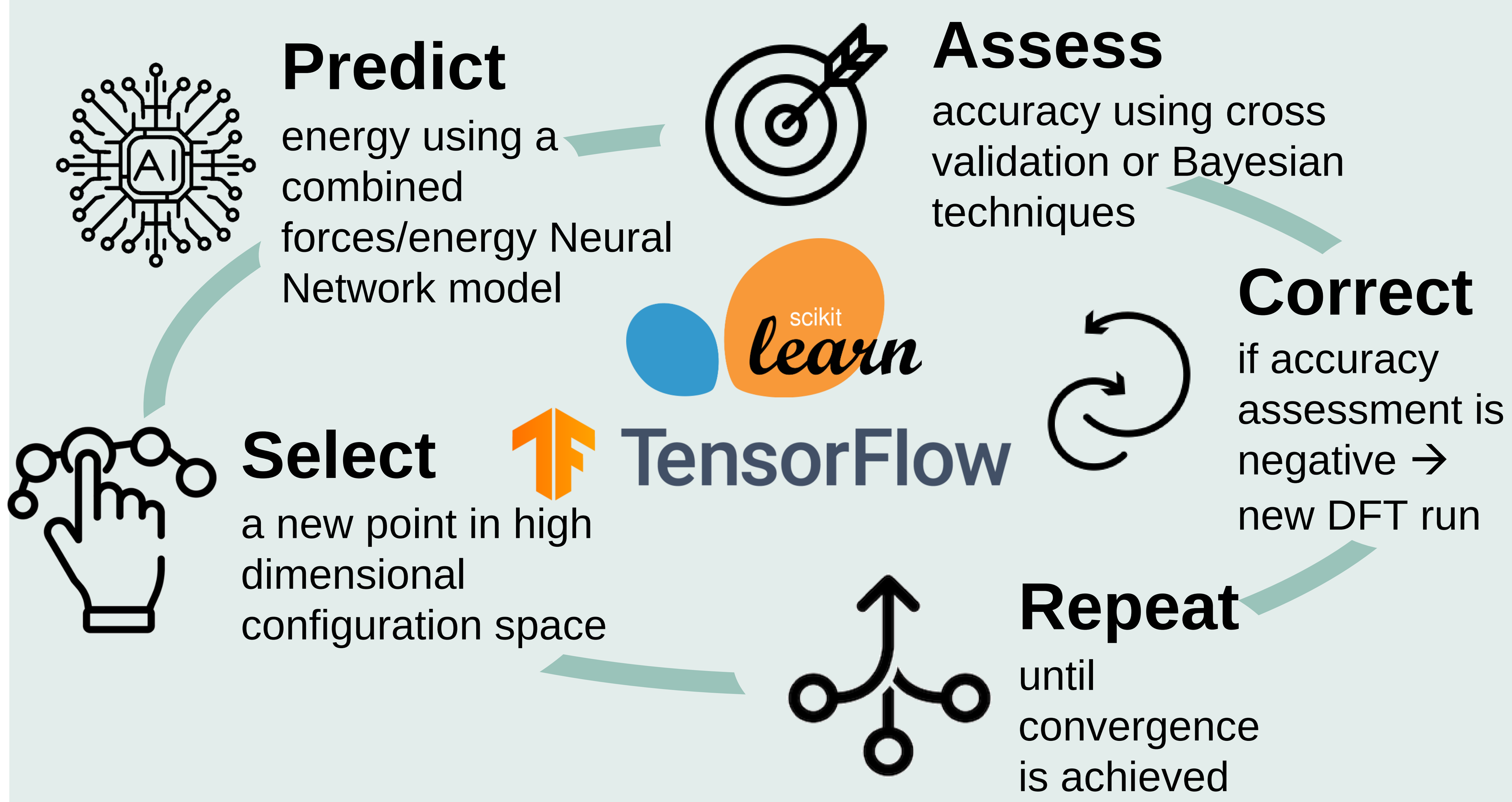
- Evaluate and demonstrate the possibilities of a “Virtual Laboratory” based on AI-enhanced atomistic materials simulation
- Assess phase stability of HfO_2 in various situations

The Material - HfO_2

Hafnia has highly complex phase and energy landscape, the impact of temperature, strain and dopants on those phases is the subject of the thesis.

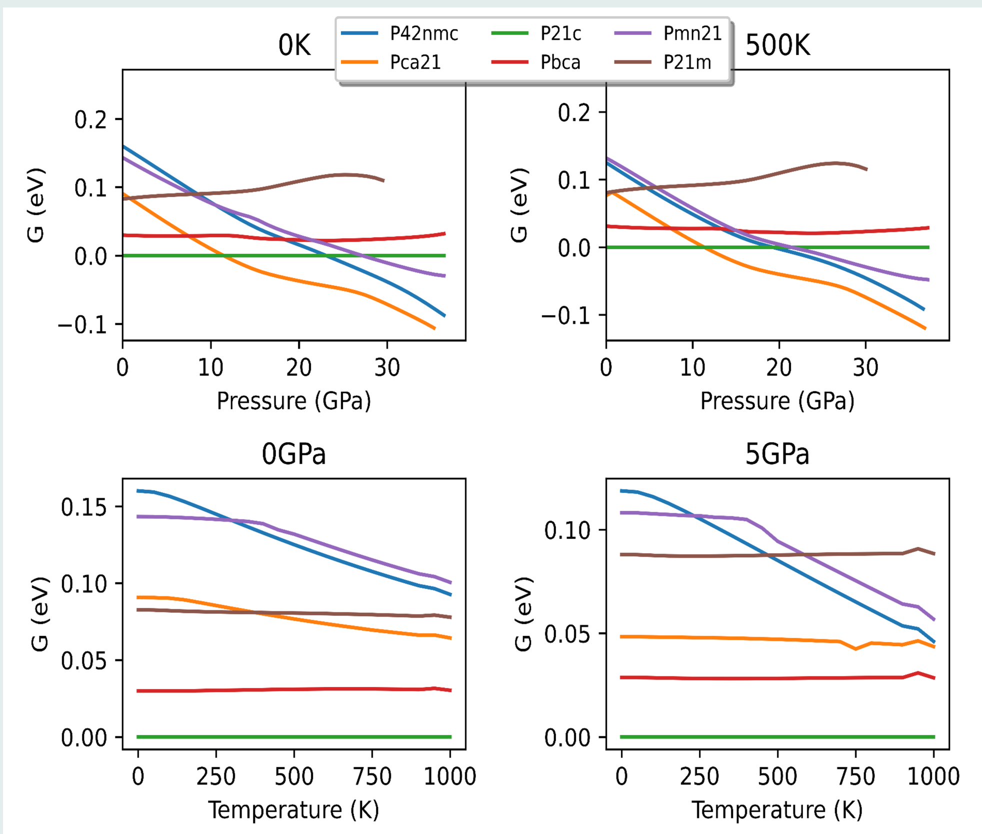


Methodology



Results and Next Steps

- T and p clearly impact phase behavior
- This alone not sufficient to drive polar phase in acceptable region (→ study directional strains & dopants)



AI enhanced DFT

- As of now ML methods used to extend DFT calculations
- Local exploration of phase space w.r.t. temperature and strain in finalization stage
- Publication in preparation

Novel AI Framework

- Next step → after publication
- NN potential generation and global phase space exploration through Nested Sampling

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Electron Mobility Increase by Strain Engineering in Modern Power MOSFETs

Introduction

Performance of Si trench power MOSFETs is limited by intrinsic material properties since device scaling is approaching a physical and economic limit. However, further performance increase for next generation power MOSFETs is enabled by **strained Si** due to enhanced mobility of charge carriers.

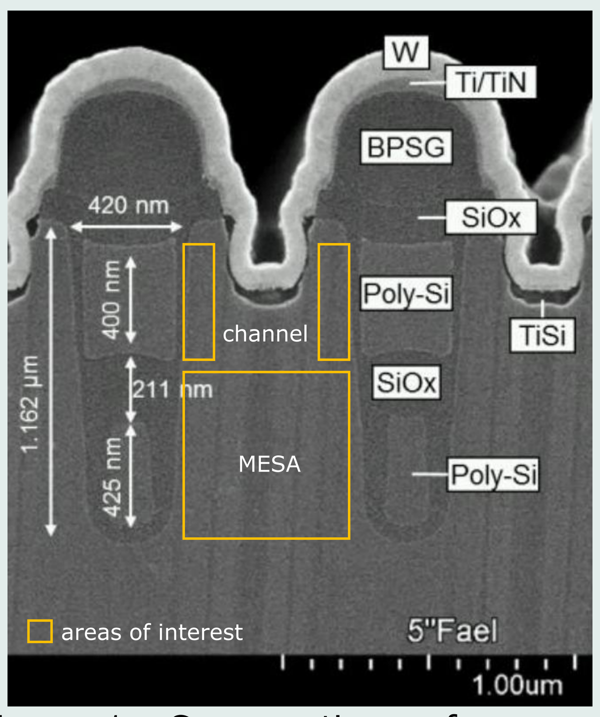

Figure 1: Cross-sections of a power MOSFET transistor, consisting of single-crystalline substrate, polycrystalline as well as amorphous glass regions.

Electron mobility in Si trench power nMOSFETs is modified by **functional stress layers**. Strain-modified devices are investigated electrically as well as physically and are compared to state-of-the-art power devices.

A procedure to accurately measure and predict local strain fields in a complex MOSFET device, consisting of insulator, semiconductor and conductor multilayers with amorphous, single and polycrystalline structures is evaluated within this thesis.

Theories

Strain alters the **electrical, mechanical and chemical properties** of a semiconductor material [1].

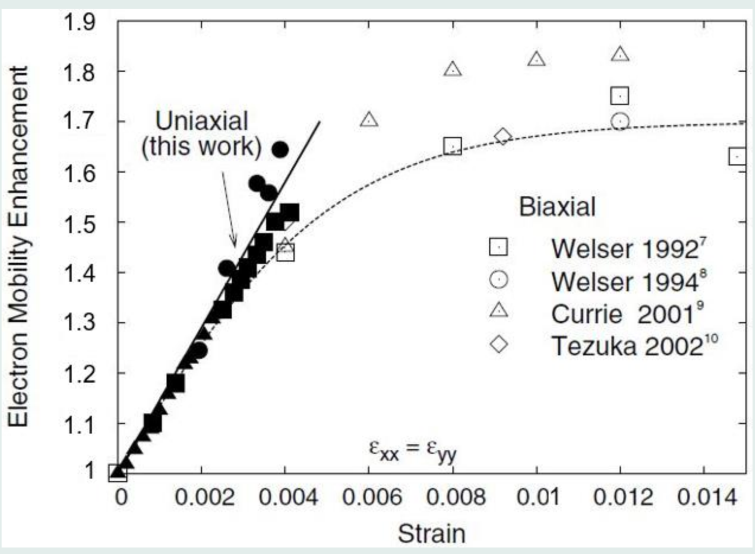

Figure 2: Electron mobility enhancement as a function of applied strain [3]

Electron mobility increases with tensile strain up to a maximum enhancement factor of 1.8 due to strain-induced changes in conductivity effective mass and scattering rate of charge carriers [2, 3].

Methodology

Local strain mapping across state-of-the-art and strain-modified MOSFET cross-sections is conducted by TEM and high resolution synchrotron XRD methods.

Technique	Sample Preparation	Spatial Resolution
TEM (NBD)	destructive	> 1 nm
Synchrotron-XRD	non-destructive	> 20 nm

Figure 3: Overview of strain metrology methods

Verification:
- **Electrical measurements** on wafer level
- **Finite element simulation** of strain and device parameters (e.g. R_{DSON})

Results

TEM NanoBeam Diffraction (NBD) strain mapping [4] is successfully conducted for state-of-the-art power MOSFETs.

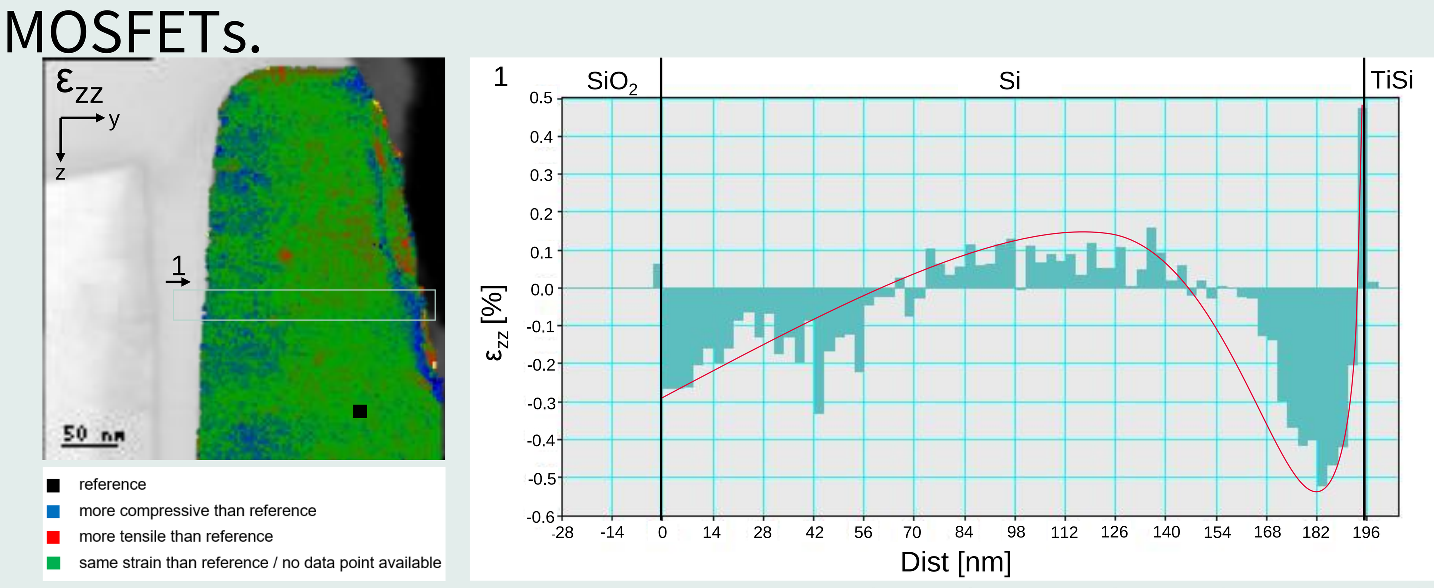

Figure 4: TEM NBD strain mapping in a MOSFET channel region (carried out @ Erich Schmid Institute of Materials Science in Leoben)

Thermomechanical strain simulation shows comparable results to TEM strain mapping within channel/MESA.

<u>Next steps:</u>
- **Methodology development** for precise stress determination
- Evaluation and verification of **"Strain Engineering" concepts**
- **Simulation (TCAD)** of strain-enhanced mobility and R_{DSON}

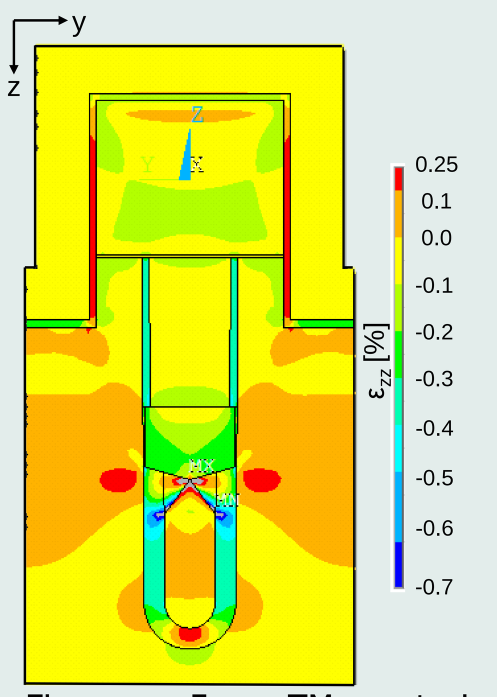

Figure 5: TM strain simulation of state-of-the-art power nMOSFET in vertical direction (top to bottom)

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[1] C. K. Maiti and T. K. Maiti. Strain-Engineered MOSFETs. *CRC Press*, Boca Raton, 2018.
[2] M. L. Lee et al. Strained Si, SiGe, and Ge Channels for High-Mobility Metal-Oxide-Semiconductor Field-Effect Transistors. *Journal of Applied Physics*, 97(1) (2005) 1.
[3] S. E. Thompson et al. Future of Strained Si/Semiconductors in Nanoscale MOSFETs. *In 2006 International Electron Devices Meeting*, San Francisco, CA, (2006) 1-4.
[4] T. C. Pekin, C. Gammer, J. Ciston, A. M. Minor, and C. Ophus.Optimizing Disk Registration Algorithms for Nanobeam Electron Diffraction Strain Mapping, *Ultra-microscopy*, 176 (2017) 170-176.

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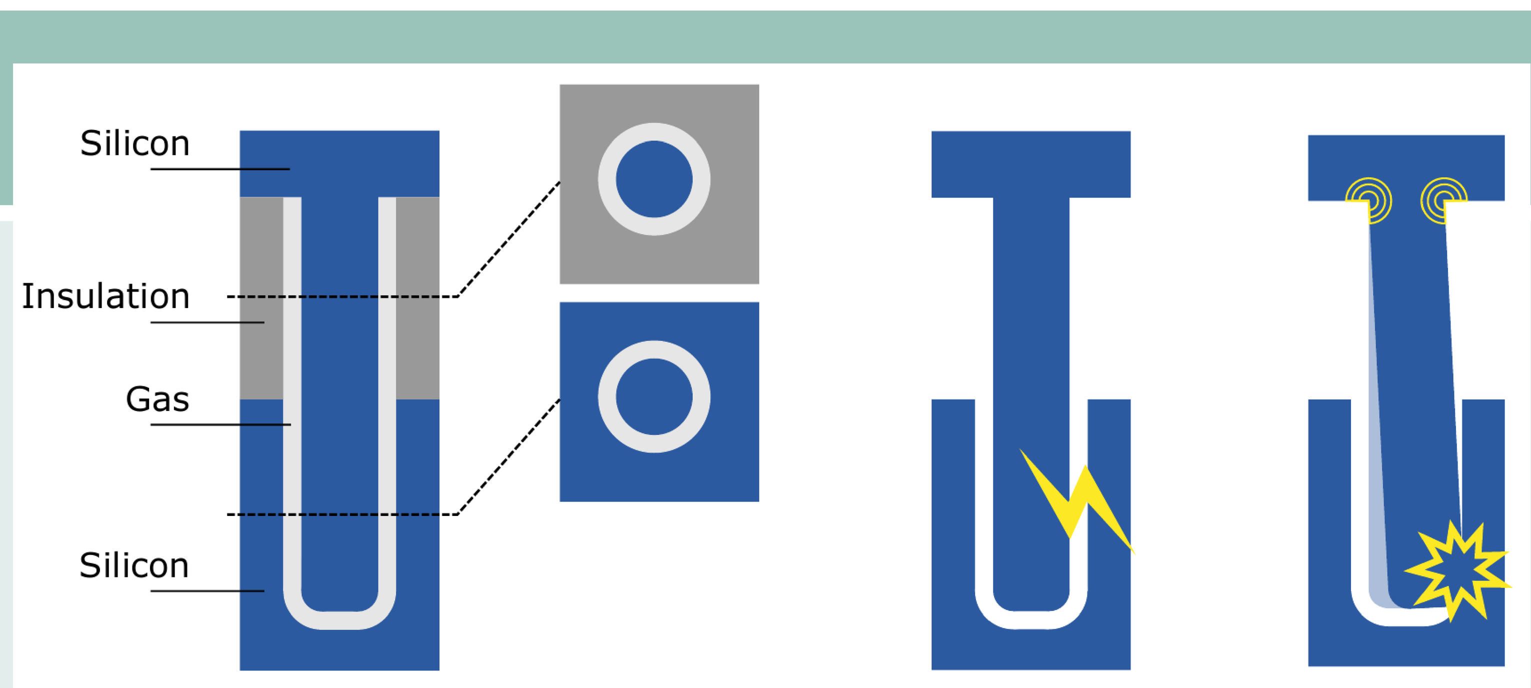
Cylindrical gas-gap capacitor structure

Introduction

The aim is to obtain a fundamental physical understanding of **gas gaps** within micro- and nanometer silicon structures at **high electric fields**. In the semiconductor industry gas gaps are on the rise as the ultimate **low-k dielectric** and also occur in **MEMS** devices.

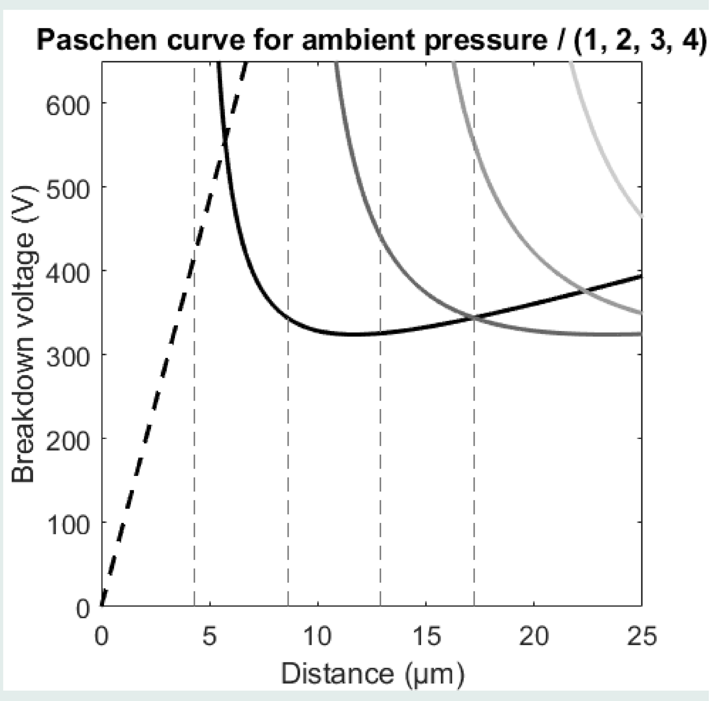
The fundamental approach of this study enables a profound assessment of the **evolution** of such systems in terms of **performance and reliability**.



A **cylindrical capacitor structure** serves to explore the physics of a gas gap at high electric fields. We consider both **electrical** and **mechanical** effects with **simulations** and **measurements**.

Theories

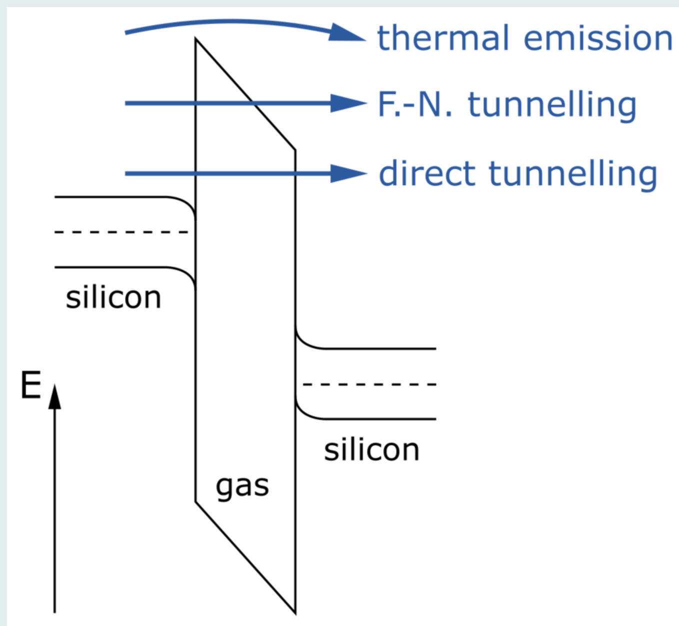
Typically, **Paschen's law** is used to predict the electrical breakdown of gases. In this model the breakdown voltage increases rapidly for **small gap distances** and **low pressure**. In this regime, additional mechanisms need to be considered to correctly predict the behavior of the gas.



Methodology

If the influence of the gas can be neglected for the **electrical model**, the major contribution to the leakage current is expected to be **tunneling**.

$$J_{tunnel} = \int_{E_1}^{E_2} e\, D(E) N(E)\, dE$$

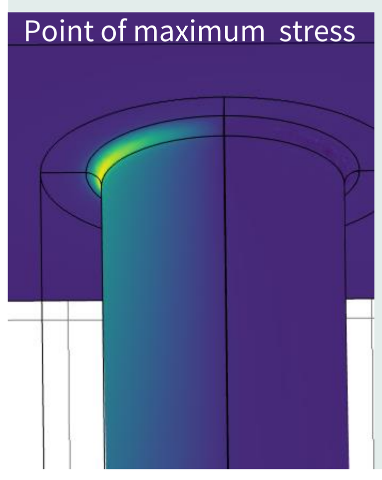


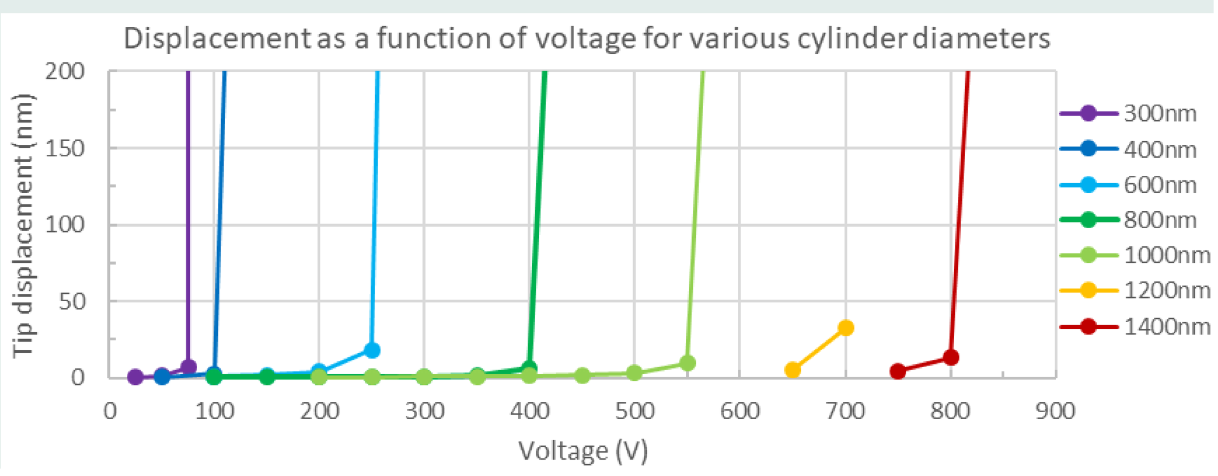
We aim to investigate this statement by measuring the **leakage current to voltage** characteristics.

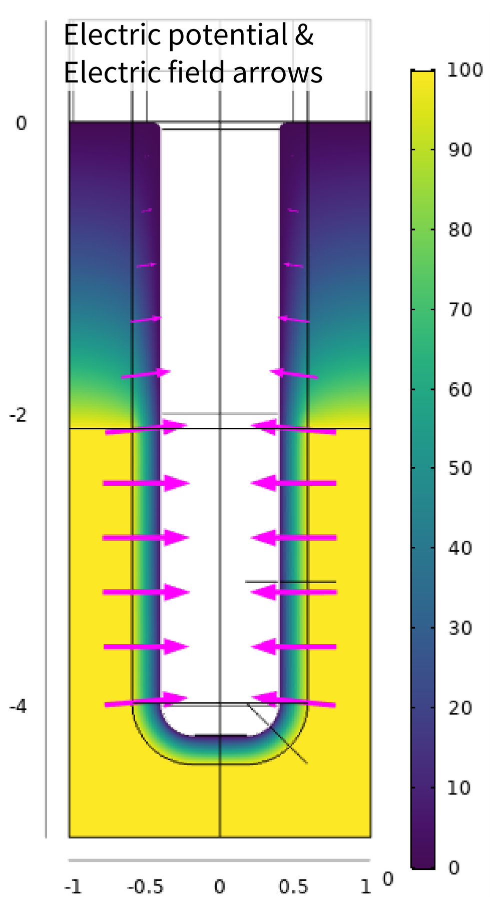
Results

Electro-mechanical simulations have been performed to study the interplay of **electric field**, electro-static **displacement**, **stress** and **mechanical breakdown**.

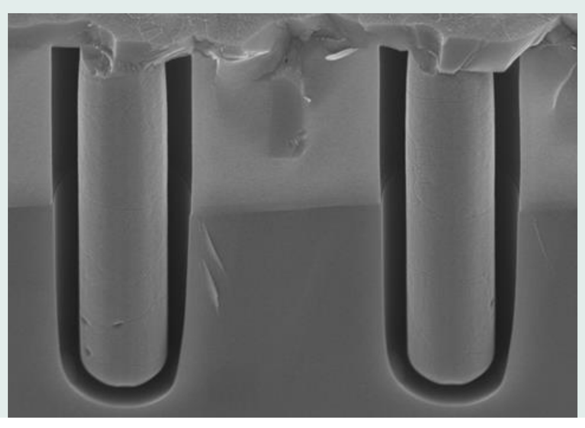
$$breakdown\ voltage \sim gap\ size \cdot diameter \cdot length^{-2}$$







The first **test structures** are almost finished and electrical measurements are planned for **autumn**.



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Challenges of Interface Characterization

Technical Requirements for SiC

Introduction

The primary emphasis was to identify suitable methods for interface analysis especially on transparent semiconductor materials. Applied interface characterization methods such as HR-TEM and ARXPS requires special sample preparations and do not provide timely information of alteration up to analysis, nevertheless these are the interface characterization methods of choice up to now. AES and TOF-SIMS are destructive with less spatial resolution, thereof they are less suitable for interface analyses. Optical techniques such as IR, MIR, ATR and ellipsometry are strongly affected by basic material properties, such as transparency to the probing wave length, surface roughness, well defined interface limits, sample thickness or by added dopant concentrations. Kinds of interface defects are schematic illustrated in Fig. 1.

Methodology for SiO_x/SiC Interface Characterization

X-**R**ay **R**eflectometry**,** information about…
- Layer thickness and density,
- Interface & surface roughness,

…independent of material's degree of crystallinity.

Angle **R**esolved **X**-Ray **P**hotoelectron **S**pectroscopy**,** information about…
- elemental & chemical composition of interface.

High **R**esolution **T**ransmission **E**lectron **M**icroscopy**,** information about…
- Interface thickness,
- Element distribution **(ELNES)**,
- Crystallographic order.

µ-Raman, information about…
- induced stress and crystallinity of layer,

Capacitance **V**oltage measurements**,** information about…
- Electrical verification of defect quantities on the basis of electron velocity, any kind of types and sizes of interface traps are being measured – very sensitive.

Additionally, **spot size** vs. **info content** should be under consideration (Fig. 3).

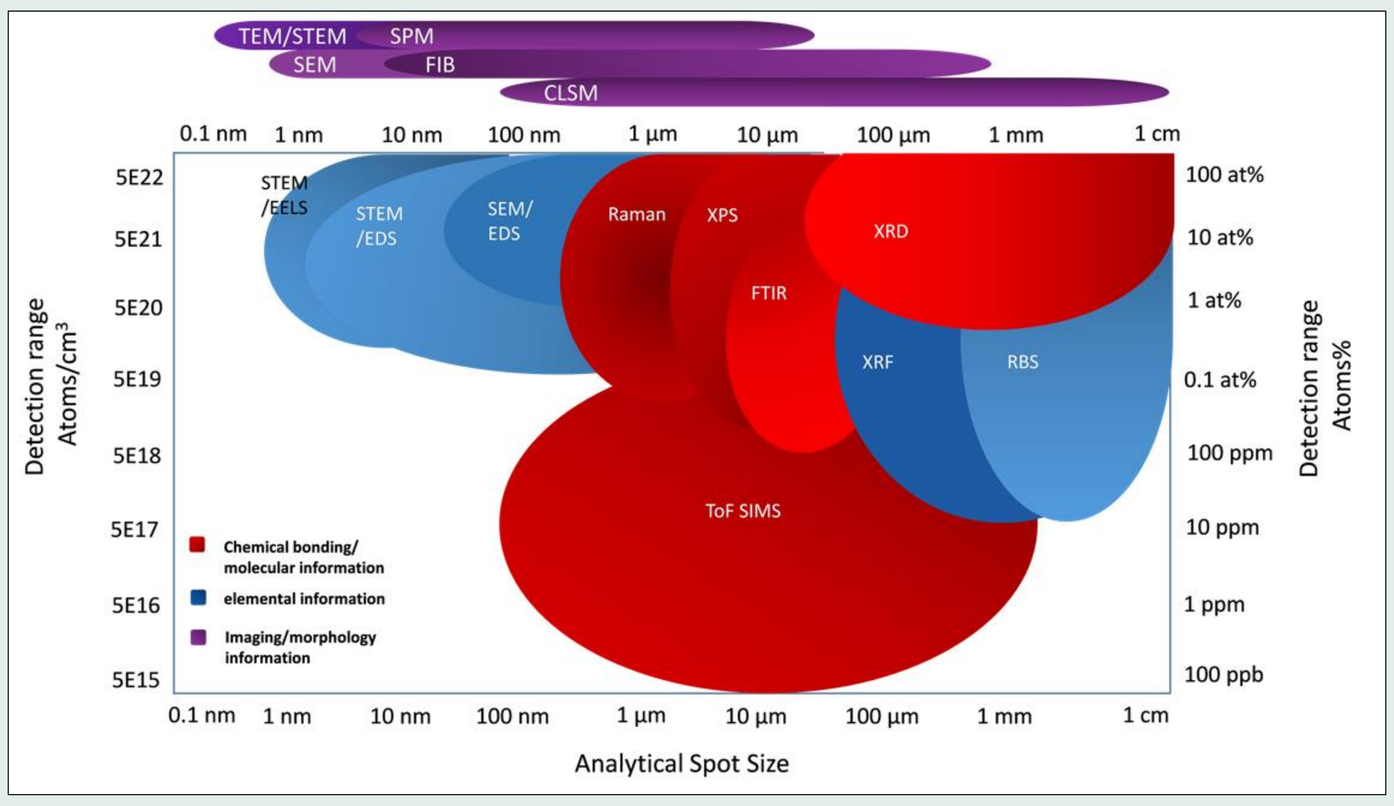

Fig. 3. Analysis spot size vs. detection range of difference techniques. Source: https://www.aif.ncsu.edu/analytical-spot-size/

Scientific issue

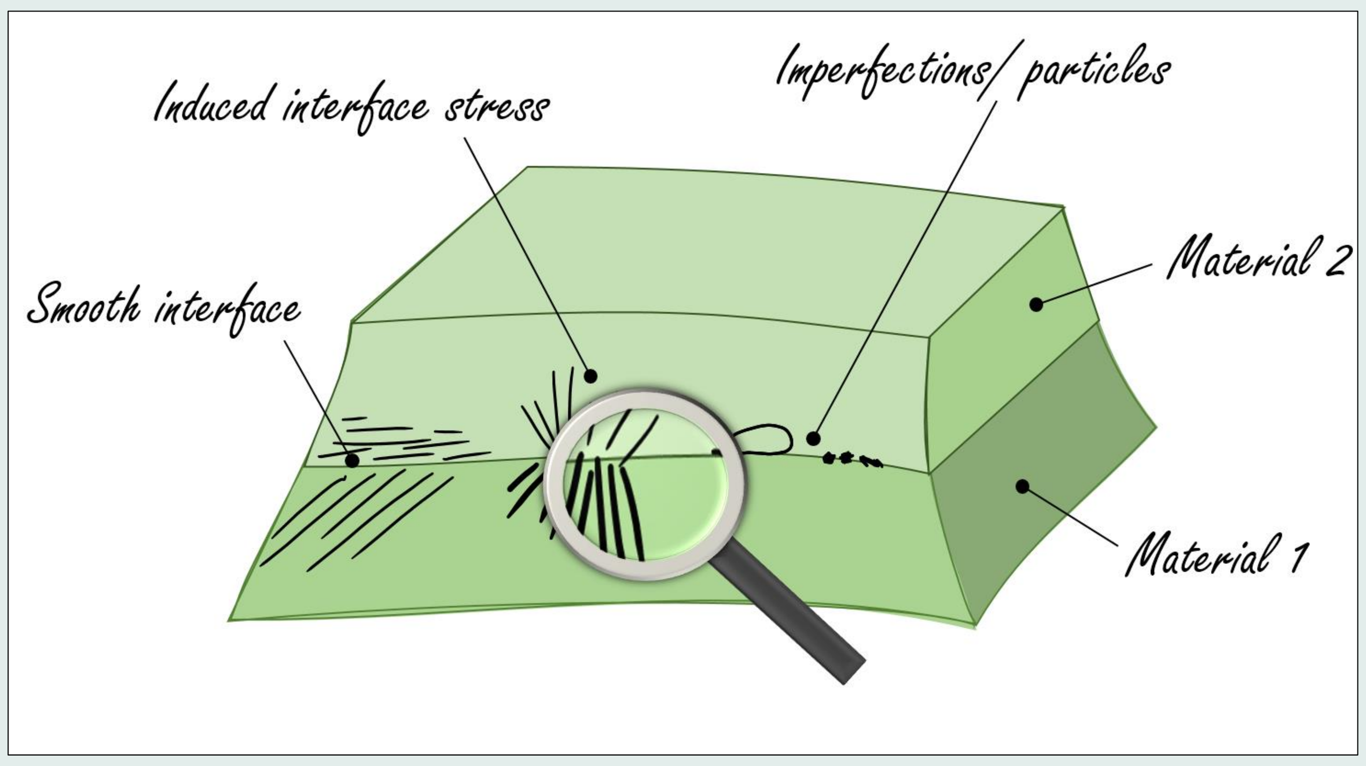

Fig. 1. Schematic illustration of possible interface defects, which has to be characterized.

Compared to Silicon MOS devices, SiC MOSFETs show inferior gate oxide (GOX) reliability, which leads to lower dielectric breakdown field strengths and threshold voltage instabilities [1]. Therefore, it is important to further investigate and improve the SiC surface in different crystallographic orientations, and the respective SiO_2/SiC interface in order to generate adequate gate oxide layers. Despite their recent success, the processing of SiC MOSFET devices still did not reach the maturity level of Si technology. Especially the low channel mobility and the rather high on-resistance (R_{on}) are known vulnerabilities due to the high interface trap density at the SiO_x/SiC interface [2] see Fig. 2.

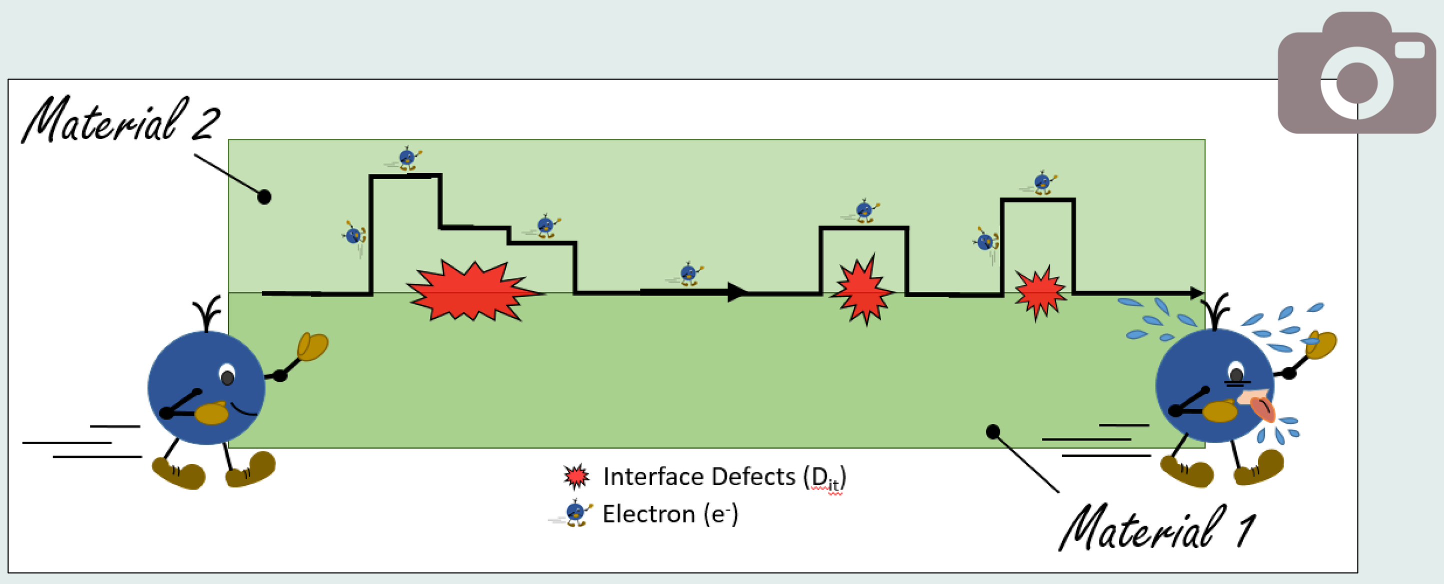

Fig. 2. Schematic illustration of low channel mobility of SiC MOSFETs due to interface traps. Electrons indirectly detours or get trapped along the channel interface, which negatively influence the electron mobility at interface.

Conclusion & Outlook

The aim of this work is to investigate and characterize the SiO_x/SiC interface in order to generate optimal gate oxide layers to improve the channel mobility and reliability of high-power SiC MOSFETs. The main tasks in this work can be divided into four parts:

- Investigation of SiO_x/SiC interface by selected characterization methods
- Research on thermal/native oxide SiO_x/SiC interface
- Elaboration of chemical conditioning to improve the gate oxide interface
- Electrical verification and evaluation of the SiO_x/SiC interface

[1] Y. Hijikata, S. Yagi, H. Yaguchi and S. Yoshida, pages 181-206. Intech, (2013).
[2] T. Kimoto and J.A. Cooper. *Fundamentals of Silicon Carbide Technology*. Wiley (2014).

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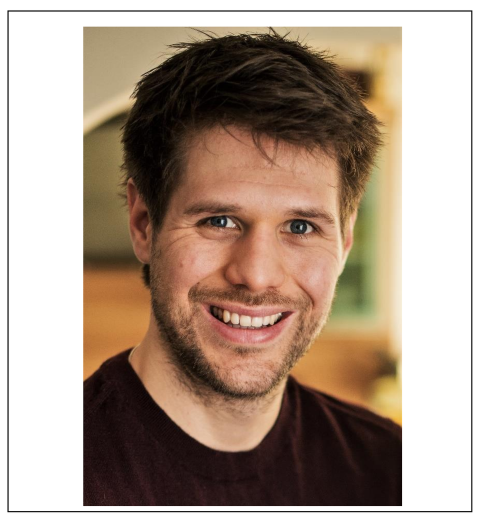


Analysis of Voiding in Thin Cu Metallizations

Introduction

- In order to improve the thermo-mechanical fatigue behavior of modern power semiconductor metallizations it is important to understand the underlying mechanisms.
- One of the observed damage modes in Cu metallizations is intercrystalline voiding (Bigl et al. [1]), where the driving mechanism should be elucidated.
- A thermodynamics-based model can provide this understanding and enables the possibility to predict voiding based on a few state parameters.

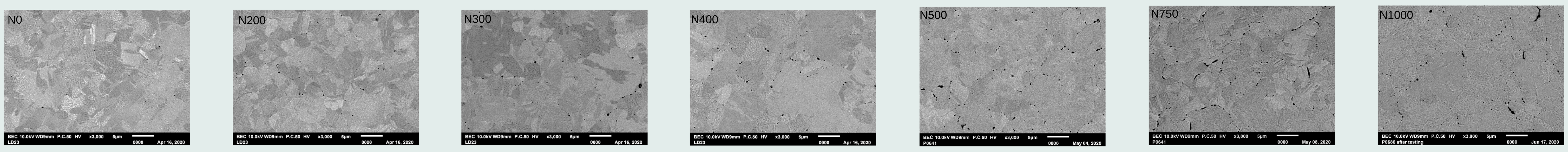


Figure 1: Evolution of early degradation (voiding) of polyheater Cu metallizations as function of cycle number (e-polished)

Damage Quantification

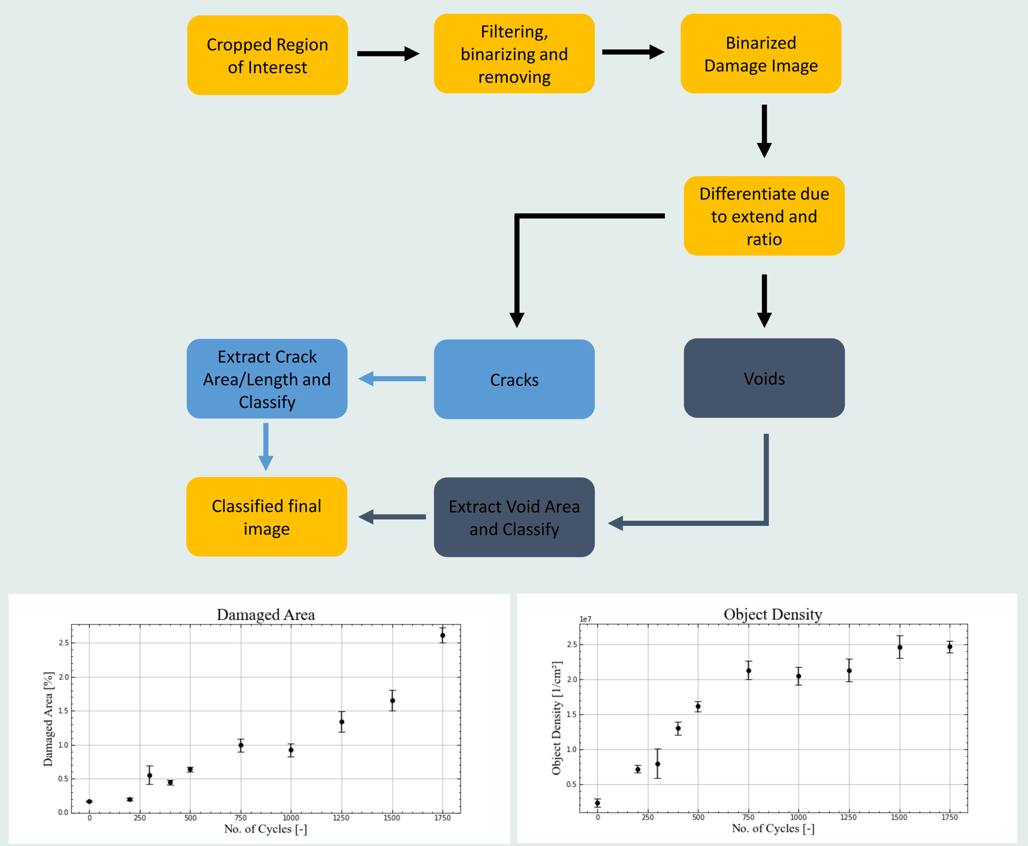


Figure 2: Damaged area and object density as a function of cycle number: polyheaters stressed from 100 °C to 400 °C with 200 µs heating time and 1 s waiting between pulses

EBSD

› Anisotropy of Cu leads to microstructure- and orientation-dependent voiding

› Crystal plasticity simulations (CP-FEM) show a mis-orientation dependent stress state

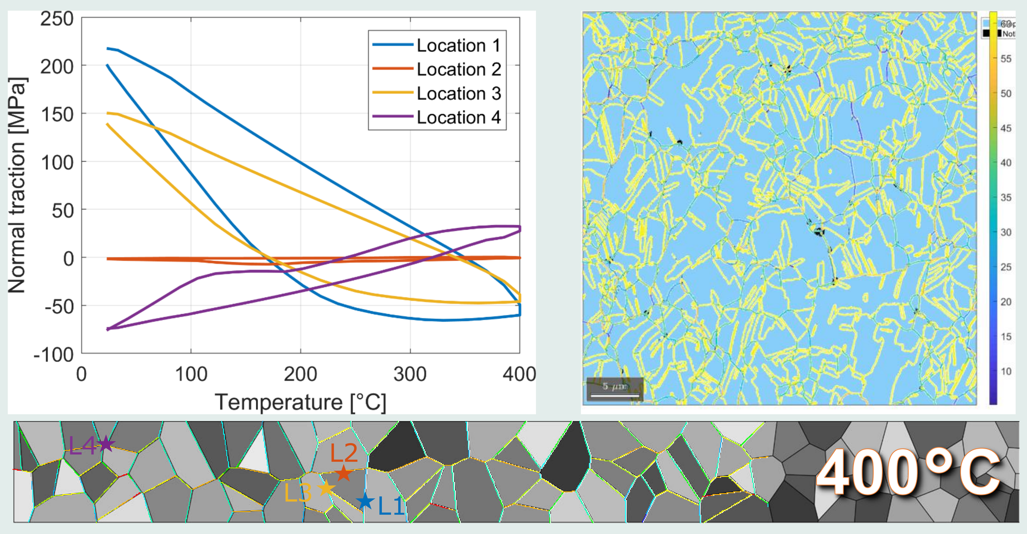


Figure 3: right: EBSD analysis of a sample after 10³ heating-cycles preferential misorientations for voids left/bottom: CP-FEM (D. Tscharnuter, KAI), diffrenent stress state due to local misorientations

FIB Tomography

› Cracks are results of the connection of single voids

› Void chains preferentially in z-direction

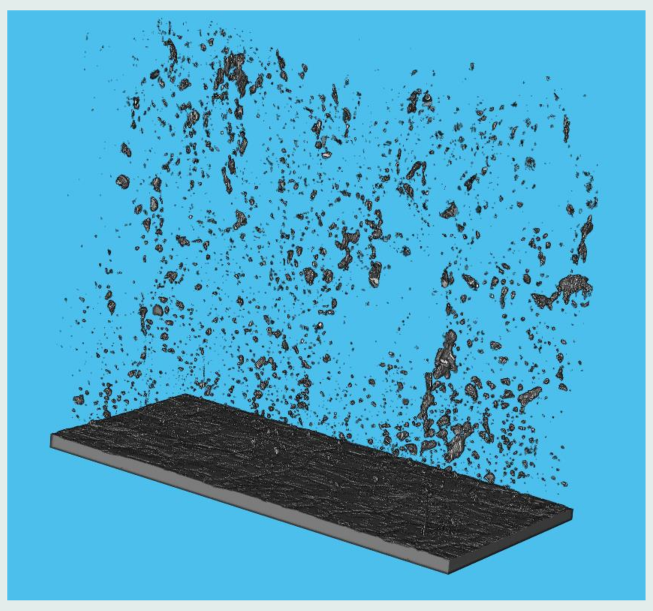
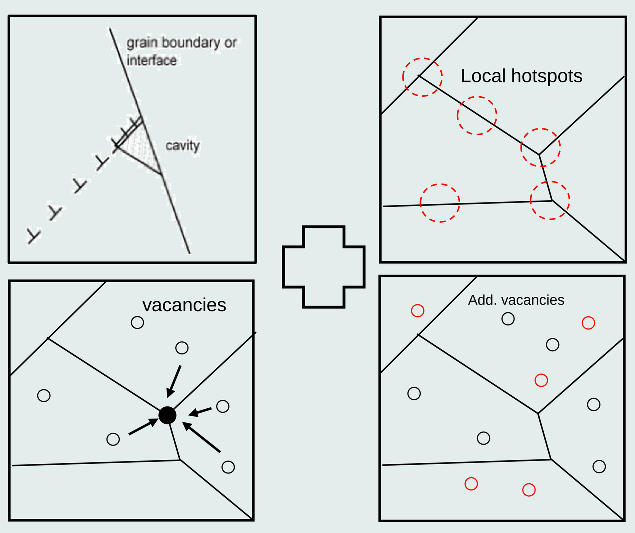


Figure 4: FIB tomography (M. Stabentheiner, FA VIH) of a sample after 10³ heating-cycles (analyzed volume: 15x15x8 µm³) Pixel and slice size: 30 nm, ~250 slices reconstructed in 3D

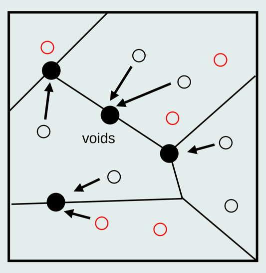
Thermo-dynamical modelling – Modified voiding theory and key findings

Mechanisms — **Driving Forces** — **Void Nucleation**



ABC dislocation model
SFAK vacancy model

Stress-state simulations using FEM



› Models reported in literature require unrealistically high stresses

› Modifications including vacancy supersaturation need to be performed

› Cl has an additional impact on surface energy

$$I = \nu \exp\left(-\frac{U_d}{kT}\right) * A^* n_v \delta_s * \frac{1}{\Omega n}\left(\frac{G^*}{3\pi kT}\right)^{\frac{1}{2}} \exp\left(-\frac{G^*}{kT}\right)$$

Key Findings

› DFT simulations (R. Bodlos) showed a decrease in surface energy (one magnitude) due to Cl influence

› Modifications including vacancies and Cl showed huge effects:
- no Cl & no vac: 0 Voids/sm^3
- no Cl & vac: 10^{-50} Voids/sm^3
- Cl & vac: 10^4 Voids/sm^3

Figure 5: Results of a void nucleation analysis for 10 pulses from 100 – 400 °C with vacancies and Cl effect included
orange: number of total nucleation events per m³ and s. Nucleation rate is high at holding the temperature (tensile stress) and low at heating (compressive)
blue: Gibbs free energy is mirrored to the nucleation events, low during waiting high at heating

Summary and Outlook

› EBSD analysis showed that voiding is misorientation-related

› FIB tomography revealed that void chains leading to cracks form along z-direction

› The dominant mechanism seems to be vacancy condensation, strongly assisted by impurities

› Outlook: - Further improvement of simulation by considering further mechanisms
- FIB tomography study for different cycle numbers (evolution in 3D)
- Calibration of the model with respect to experimental data

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[1] S. Bigl, S. Wurster, M. J. Cordill, D. Kiener. "Accelerated thermo-mechanical fatigue of copper metallizations studied by pulsed laser heating." Micr. Eng. 167 (2017), 110-118

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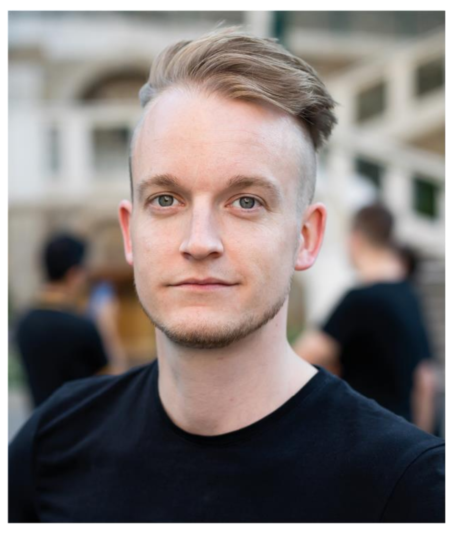


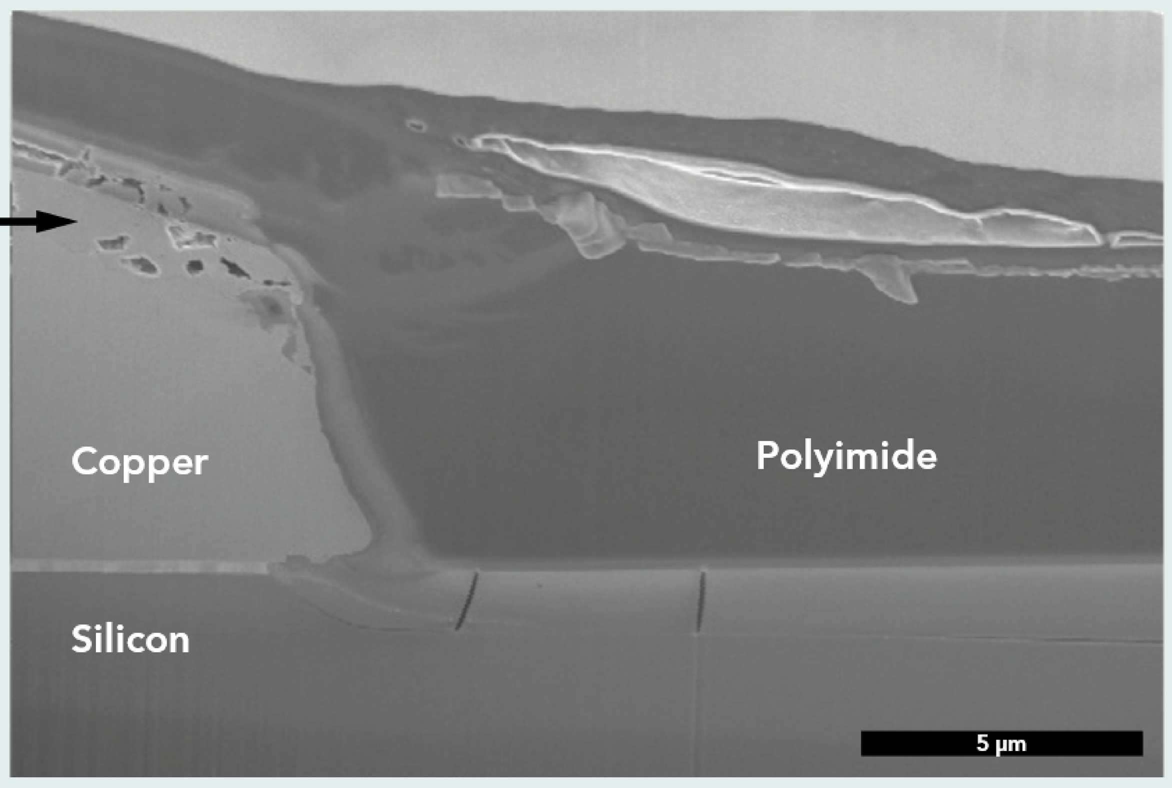
Silvia Larisegger (KAI)

Tuning High-Performance Polyimides for Microelectronics

What is the Problem?

Corrosion

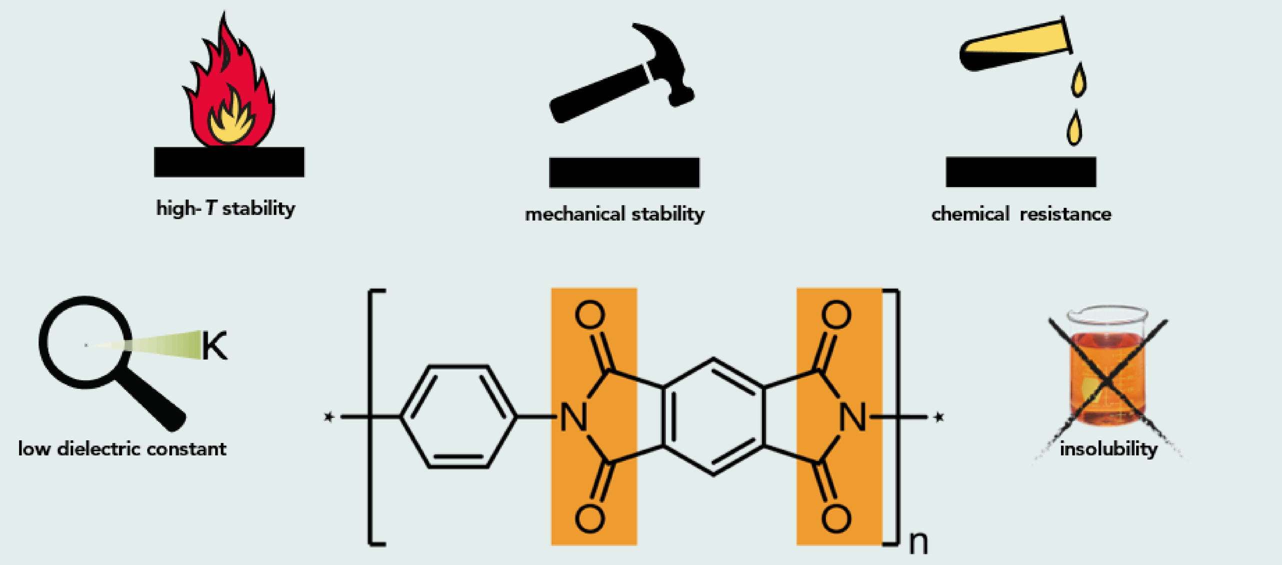
With progressing operation time of microelectronic components, corrosion phenomena take place on the surface of (semi-)conducting parts, which ultimately lead to component failure. It is assumed that corrosion is facilitated by migration of water and ions throughout the protective polyimide layer.



SEM [PhD thesis Elke Ludwig]

What is a Polyimide?

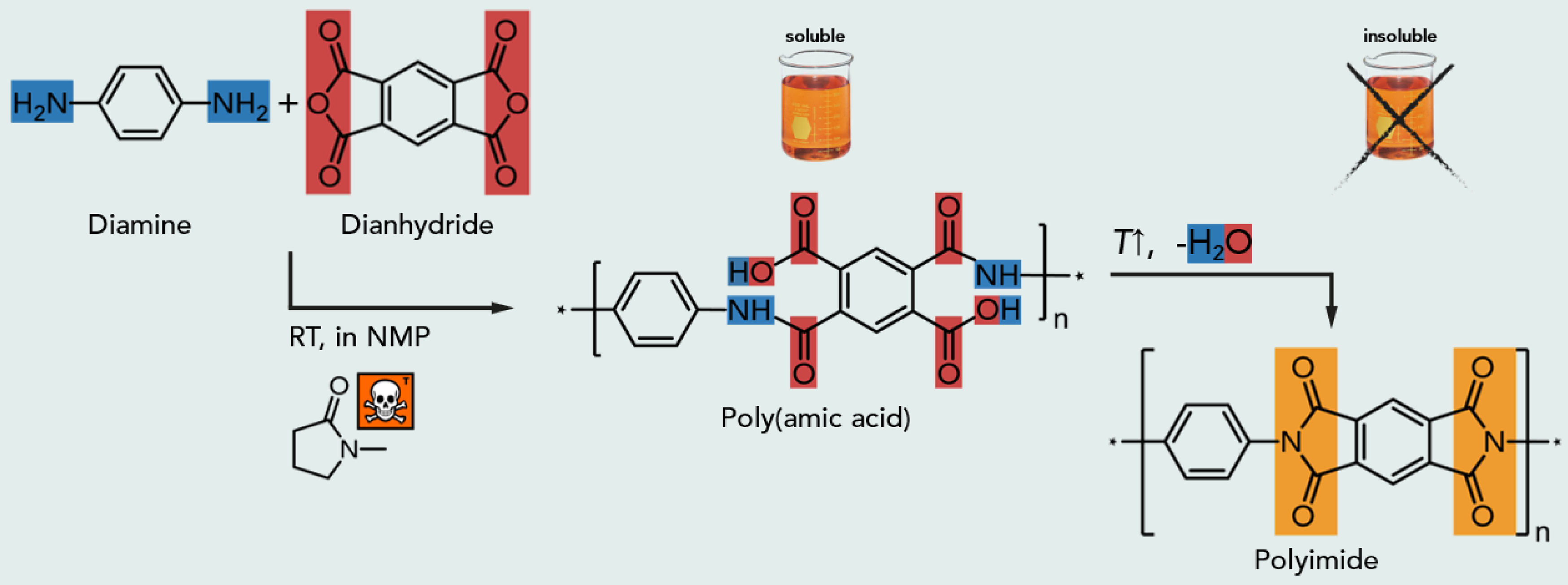
Polyimides are high-performance polymers which exhibit outstanding properties such as high thermal and chemical resistance, high mechanical strength and low dielectric constants. They are composed of the monomer classes diamines and dianhydrides linked to each other by an imide bond.



Example of a polyimide: *PPPI*
Poly(*p*-phenylene pyromellitimide)

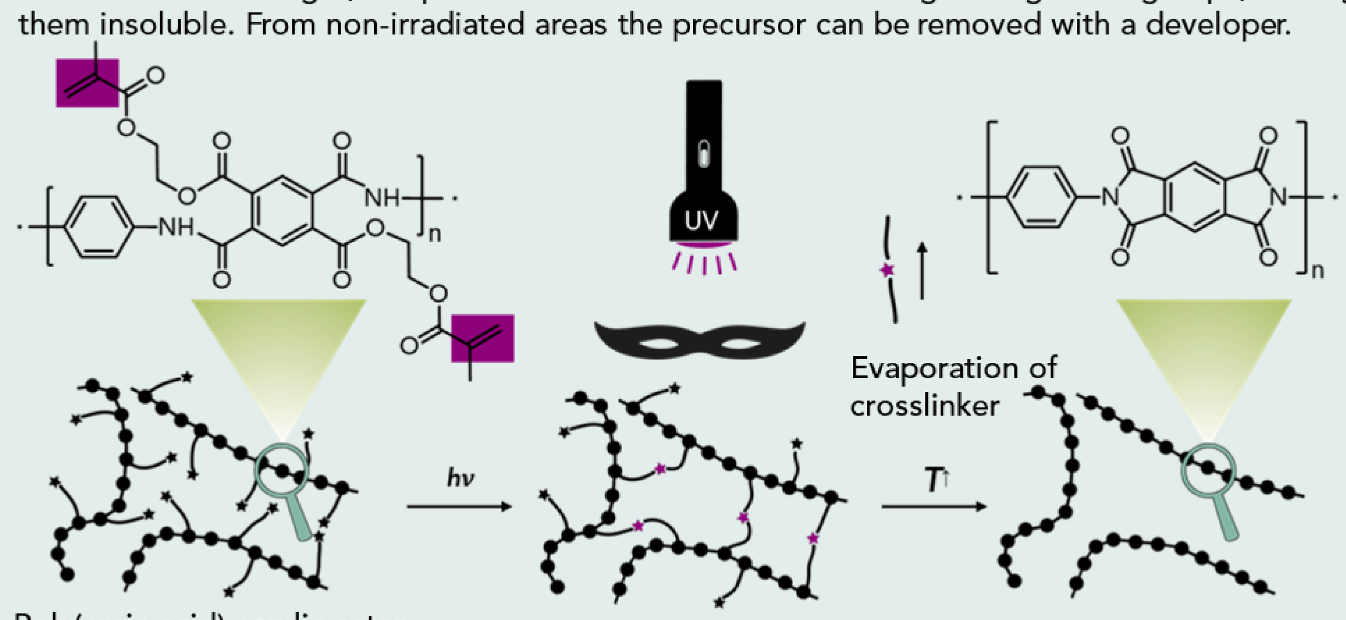
Classical Synthesis of Polyimides

As most polyimides are insoluble, their classical synthesis includes a processable precursor polymer, a so-called poly(amic acid). It can be obtained by combining the monomers in a polar aprotic solvent such as NMP at room temperature. This precursor polymer can be cured into a polyimide by exposing it to high temperatures up to 400 °C.



Photosensitivity in the Process

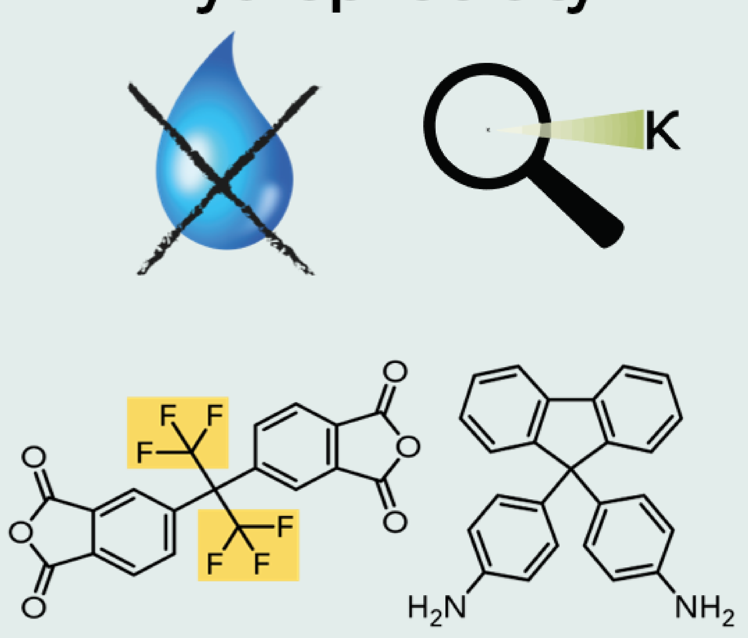
In order to be able to structure the polyimide layer on the component surface, free acid groups of the poly(amic acid) are esterified with alcohols that contain photopolymerizable groups. When irradiated with UV light, the photosensitizier initiates crosslinking among these groups, making them insoluble. From non-irradiated areas the precursor can be removed with a developer.



What are the Challenges and How to Overcome Them?

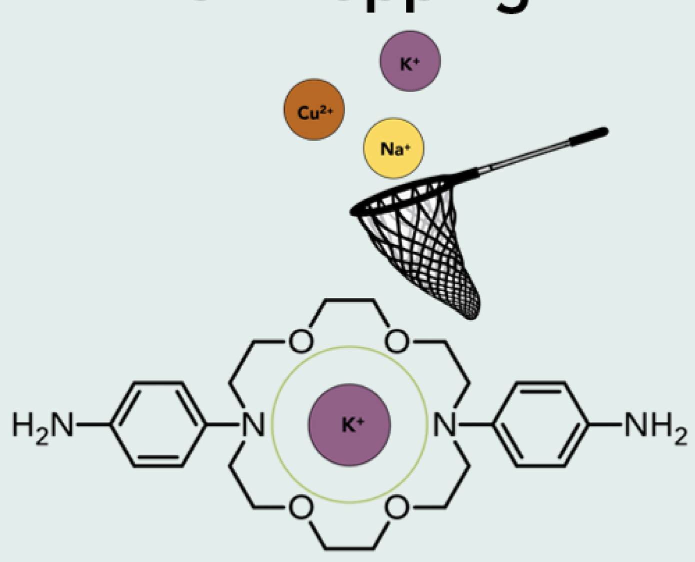
For avoiding corrosion, the polyimide systems have to be tuned in order to suppress the migration of water and ions. But at the same time they have to be able to sufficiently adhere to the substrate surface while still being structurable by UV irradiation. The first steps are to copolymerize different monomers per class for adjusting the properties of the resulting polyimide. Copolymerization turns out to be quite challenging itself.

Hydrophobicity



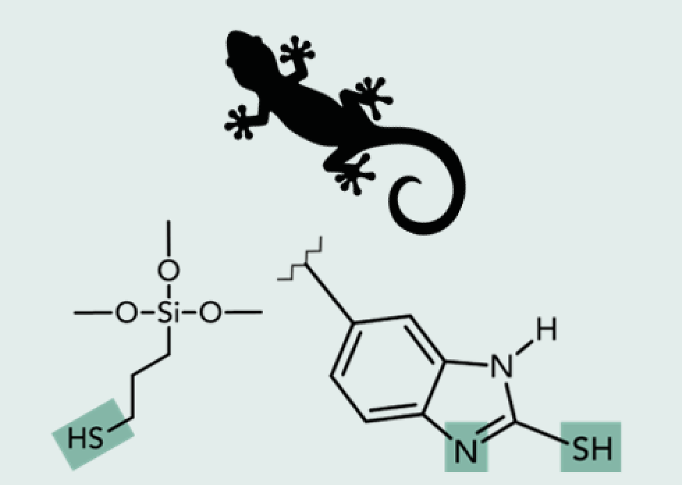
Employing monomers which are bulky and/or fluorinated is known to lead to more hydrophobic polyimides. This would exacerbate the migration of water and ions. As a positive side effect the polyimides' dielectric constants are being lowered simulta-

Ion Trapping



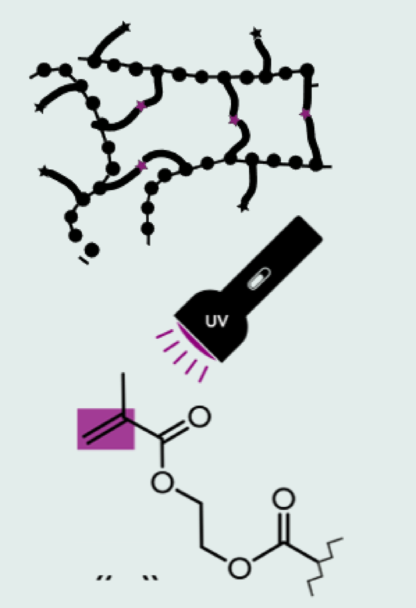
There is also the possibility of incorporating ion-trapping monomers into the polymer chain. They are able to coordinate ions, hence keeping them in place, i.e. suppressing their migration. The molecule shown here is a crown ether derivative which can be used as monomer for polyimides [patented by Stefan Schwab and Herbert Hutter for INFINEON].

Adhesion



In order to ensure adhesion to the surface of the substrates, usually silane-based adhesion promotors are added to the precursor solution. Another option could be the incorporation of certain molecular functionalities into the polymer chain. As an example, the 2-mercaptobenzimidazole derivative shown above has a high affinity to copper surfaces.

Photosensitivity



Esterification of pendant acid groups of the precursor polymer with acrylate-containing alcohols is assumed to be feasible as long as the current route *via* a poly(amic acid) is maintained.

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New photo resist concepts for wet etch metal layers

Introduction

In recent times problems with unwanted etching of metal lines arose due to the poor adhesion of photo resists to metal substrates. Especially when multilayer stacks are used and the wet etch process includes rinse steps during the exchange of chemicals.

The cooperation with the resist supplier Merck KGaA targets the development of a photo resist that meets several requirements as adequate adhesion to substrate, low defect density, high photo speed and removal without leaving residues.

- Which methods are capable to measure the adhesion at the metal polymer interface?
- What mechanisms are responsible for good adhesion of photo resists on metal substrates during a wet etch process?
- What is the impact of photo resist polymer design on adhesion to metal substrates?

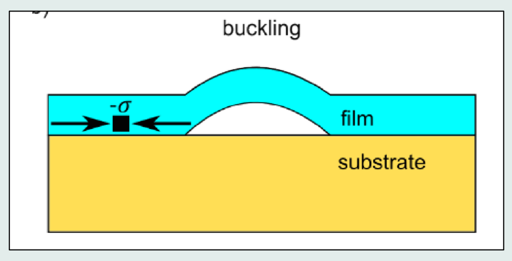
Theories

Surface conditions have a high impact on the adhesion behavior. Hydrophobic surfaces are expected to be mandatory for good resist adhesion during wet etch processes.

Different preconditioning, for instance plasma treatments, will change the surface properties of the substrate. A similar effect can be achieved by application of certain adhesion promoters.

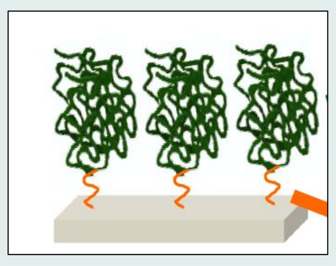
Methodology

Evaluating appropriate methods to characterize adhesion, like indentation or shear testing and relate results to performance during wet etch process



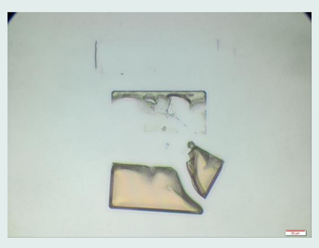
Buckles induced via indentation

Systematic checking of concepts for adhesion promotion like plasma treatments, adhesion promoter for instance brush approach


Brushes with head group and non-polar polymer backbone

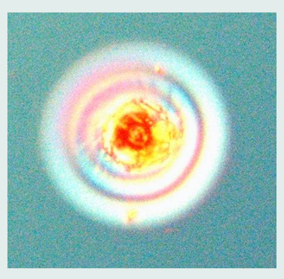
Results

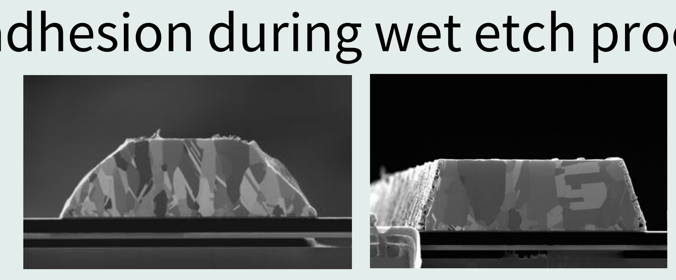
Shear testing responds to resist properties instead of adhesion to substrate


Sheared resist pad

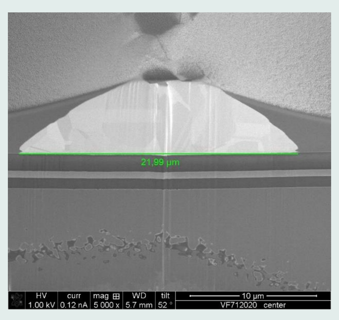
Delamination inducible by indentation
→ suitable model to determine adhesion values needed

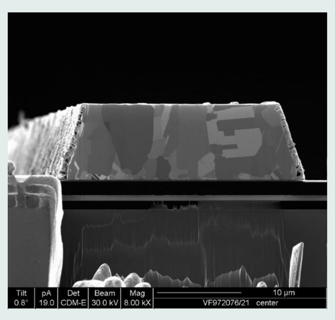
Evaluation of wet etch profiles displays adhesion during wet etch process

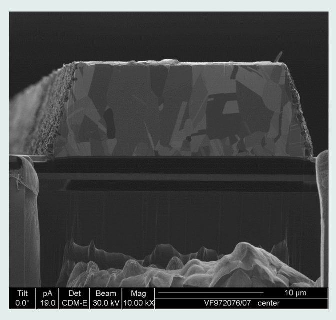

Delamination induced by indentation

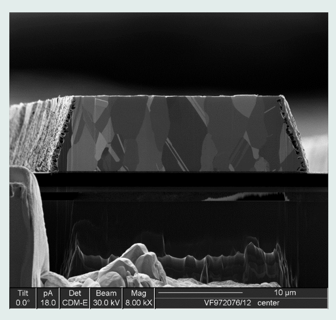

Poor adhesion vs. excellent adhesion
Cross section of metal line profile after wet etch

Certain adhesion promoter on Cu substrate significantly improves adhesion


Wet etch profile of Cu line without adhesion promoter and IX335


Wet etch profile of Cu line with adhesion promoter and IX335


Wet etch profile of Cu line with adhesion promoter and TSMR9250


Wet etch profile of Cu line with adhesion promoter and AZ4620

Next step is to identify mechanism that works at interface and to imitate the performance with other adhesion promoters.

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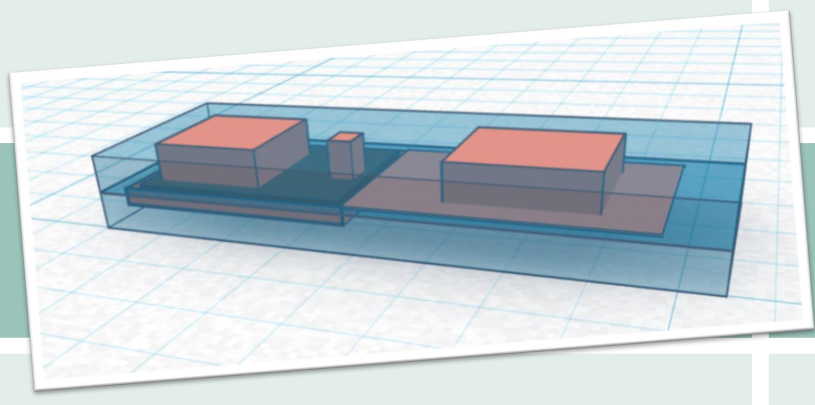
Development of a process flow to enable packaging on wafer level

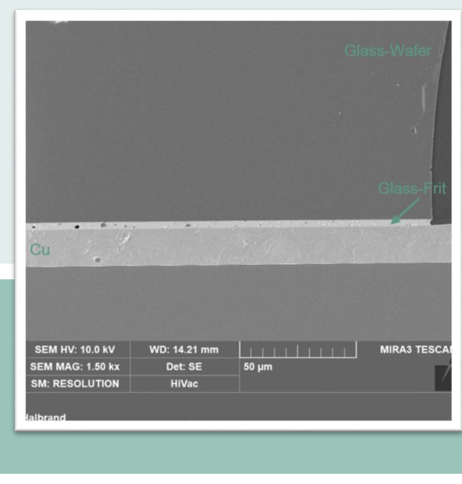
Introduction

State-of-the-art package types are based on semiconductor devices bonded on copper-leadframes before being casted into mold compound. Packaging throughput of these serial processing steps can be enhanced by transferring this flow into parallelized process steps. This can be achieved by using FrontEnd-processing on wafer level. Therefore, the plastic packages as well as the leadframes has to be replaced by insulating packaging material, e.g. glass, already including conducting lines.

The aim of this project is to demonstrate the feasibility of implementation into volume production of such a new package. Apart from this, the characterization of device specific electrical parameters as well as diverse metal/metal and metal/glass – interfaces are the focus of this work.



Wafer bonding (glass-frit-bonding) with thick copper-interlayer



Theories

Using FrontEnd-applicable, insulating, wafer material, e.g. glass, as a packaging material can have a beneficial effect on the throughput while main package-requirements (e.g. electrical isolation, heat dissipation,..) remain fulfilled.
Additionally, as glass-frit-bonding is used as bonding technique, the encapsulated chip is sealed hermetically by the glass-frit. Hence, compared to state-of-the-art package types, chips being packaged by glass-frit concepts show high robustness when exposed to humidity.

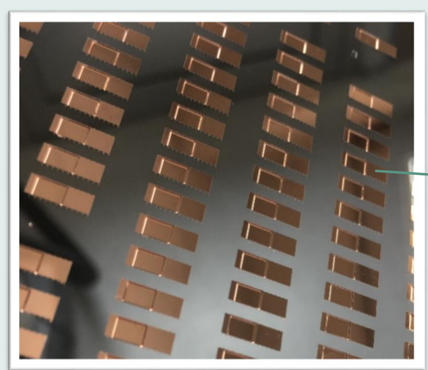
Methodology

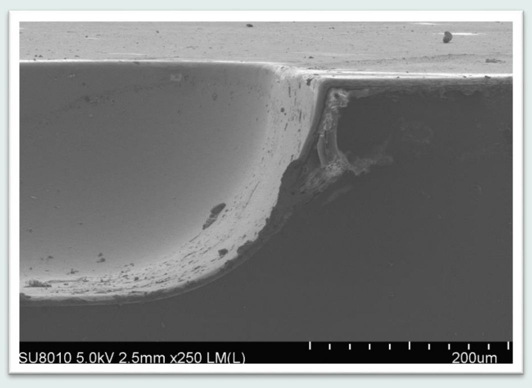
The introduction of glass-substrate as a packaging material requires the adaption and integration of various established unit-processes in combination with the implementation of novel process steps.
Therefore, the focus is set on the following process steps:

- substrate structuring → glass etching (isotropic/anisotropic)
- metallization
- bonding (device, substrate-wafers)

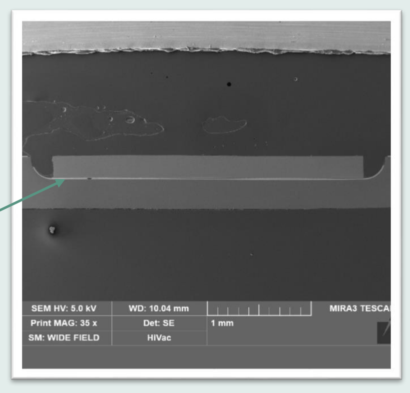
Results

Structured Cu-layer by using inkjet-printing for applying photoresist on substrate-wafer including deep cavities:





Proof-of-concept: Chip-Bonding



Proofing feasibility of full-package concept requires following next steps:

- Adapting feasible chip-bonding techniques for different backside metallization stacks
- Optimization of Cu-structuring for bonding & sawing requirements
- Filling glass-vias by usage of electrically/thermally conductive pasty material
- Reconsideration of design parameters depending on electrical performance

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Electropolishing as a preparation technique for bulk degradation analysis of Cu

Introduction

Power semiconductor devices may be subjected to rapid heat cycles caused by electrical overload events. In the long term, these events cause the devices to fail due to fatigue of their metallization.

New techniques to study early stages of bulk fatigue (void and crack formation) allow the comparison of different materials in terms of their robustness and, therefore, increase the lifetime of future products.

Device for Cu fatigue testing: "polyheater"

- Test chip mimicking a power semiconductor
  - Active heating
  - Temperature sensor
- Application of heat pulses
- Study thermo-mechanical fatigue of copper
  - Voids, cracks, etc.

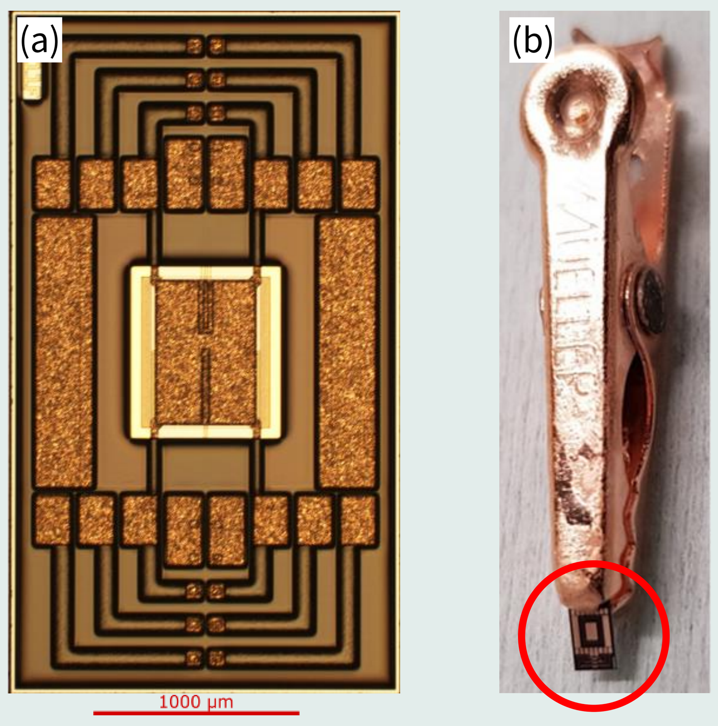

Fig. 1: Polyheater. (a) Optical micrograph. (b) Crocodile clip contacting the chip.

Working principle of electropolishing

- Electrochemical process
  - Remove material from a metallic work piece
  - Smoothen surface by levelling micro-peaks and valleys
- Driving force: DC voltage
  - Anode = sample to be electropolished
  - Electrolyte = medium, in which the Cu-ions travel
  - Cathode = cylindrical net, where Cu is deposited onto

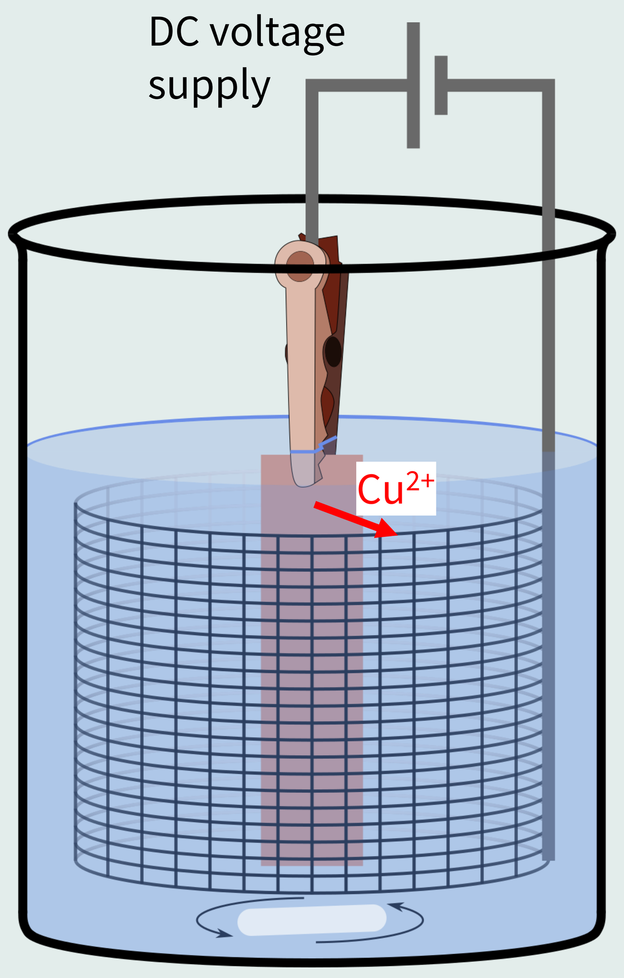

Fig. 2: Schematic of an experimental setup for electropolishing.

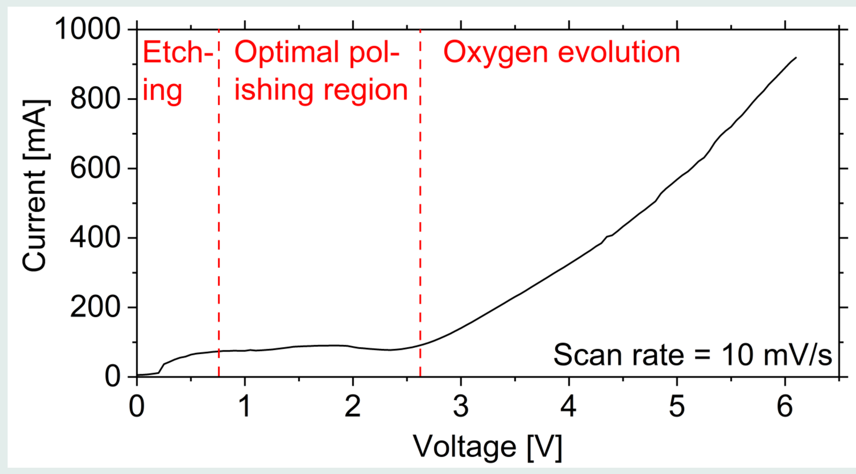

Fig. 3: Current-voltage characteristics.

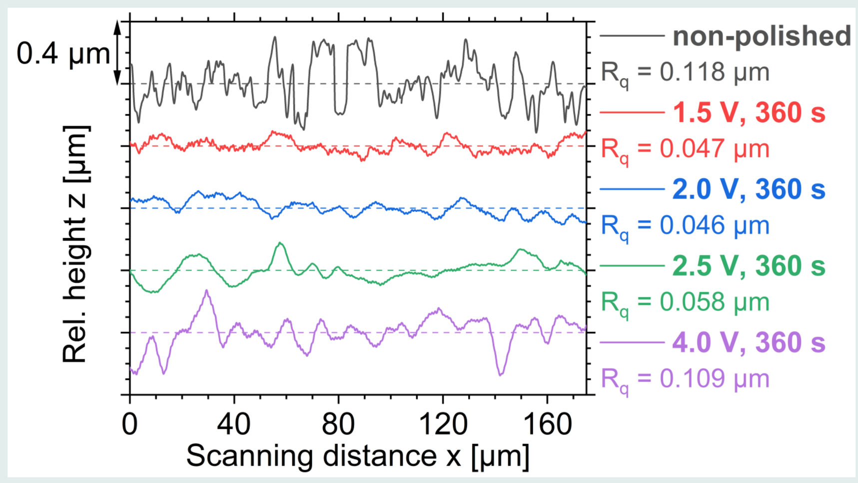

Fig. 4: Height profiles (confocal microscopy) of differentely electropolished samples.

Compilation of results

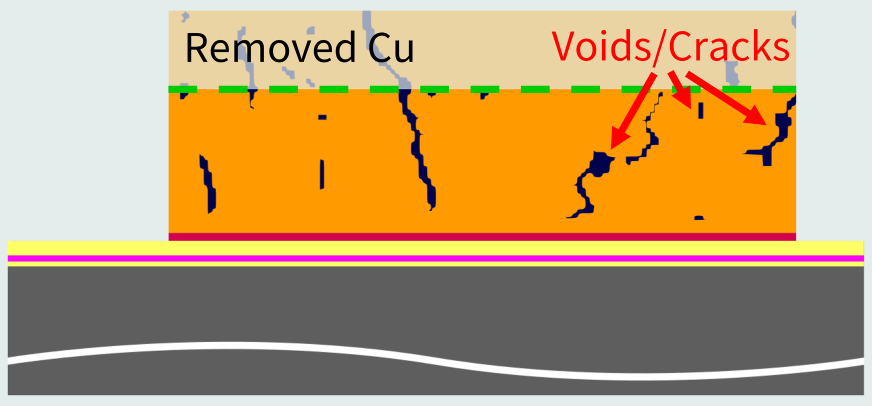

Fig. 5: Schematics illustrating the material removal by means of electropolishing in order to access bulk degradation features from the top.

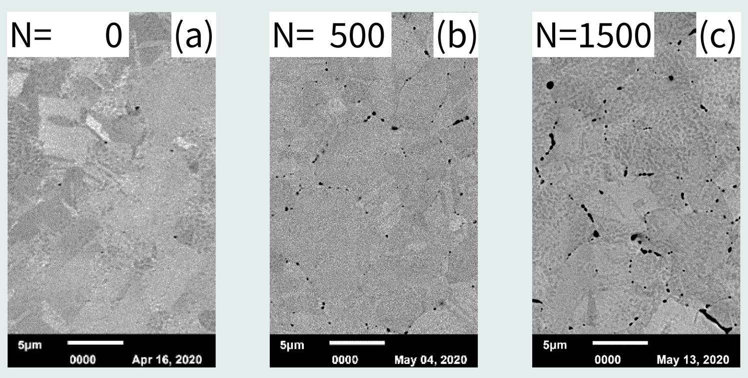

Fig. 7: Top-view SEM images of polyheaters (*N* cycles: 100°C → 450°C in 200 µs). Samples electropolished prior to analysis.

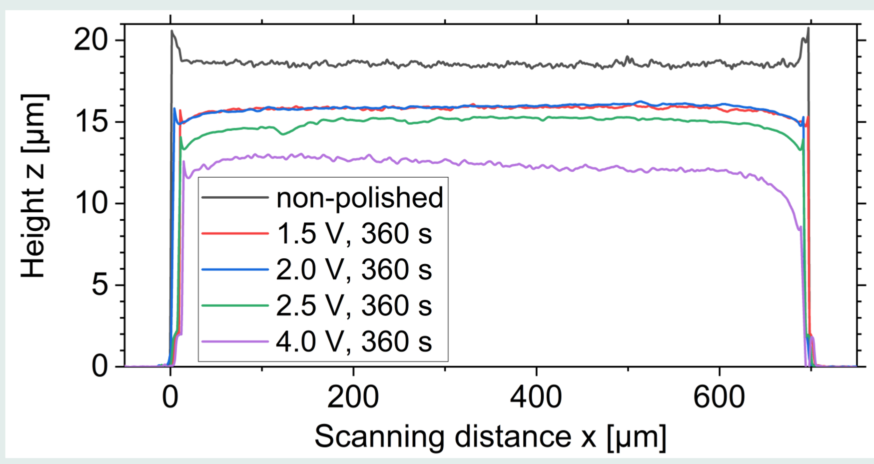

Fig. 6: Calibration of the material removal for different polishing voltages.

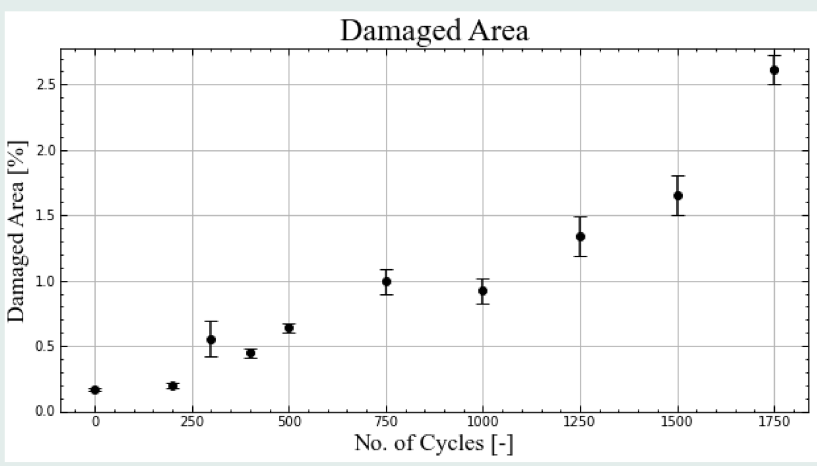

Fig. 8: Evolution of voiding as being extracted from the SEM images.

Possible applications

- Material removal
  - Bulk degradation analysis
  - Selective removal of pads
- Surface smoothing
  - Sample preparation method for EBSD

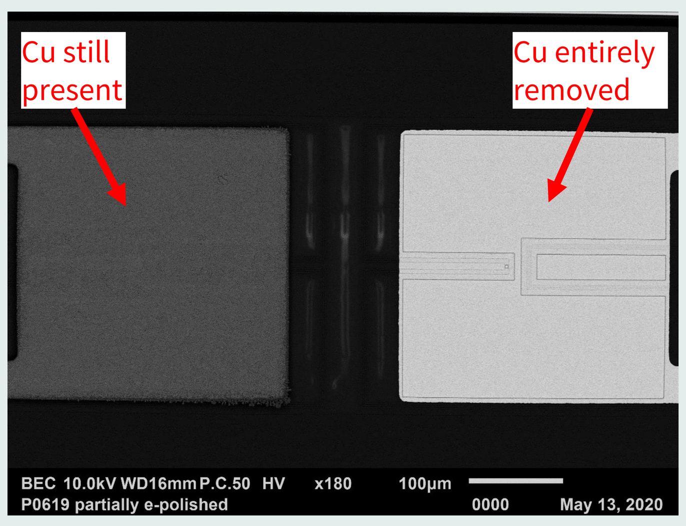

Fig. 9: Polyheater, from which the Cu has been partially removed by means of electropolishing.

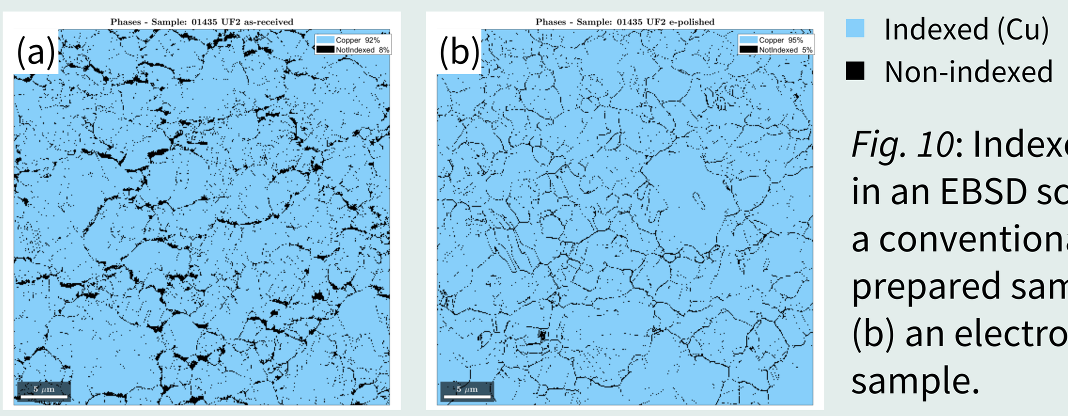

Fig. 10: Indexed pixels in an EBSD scan of (a) a conventionally prepared sample and (b) an electropolished sample.

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Atomistic simulations of elasticity and interface properties in layered metal systems

Introduction

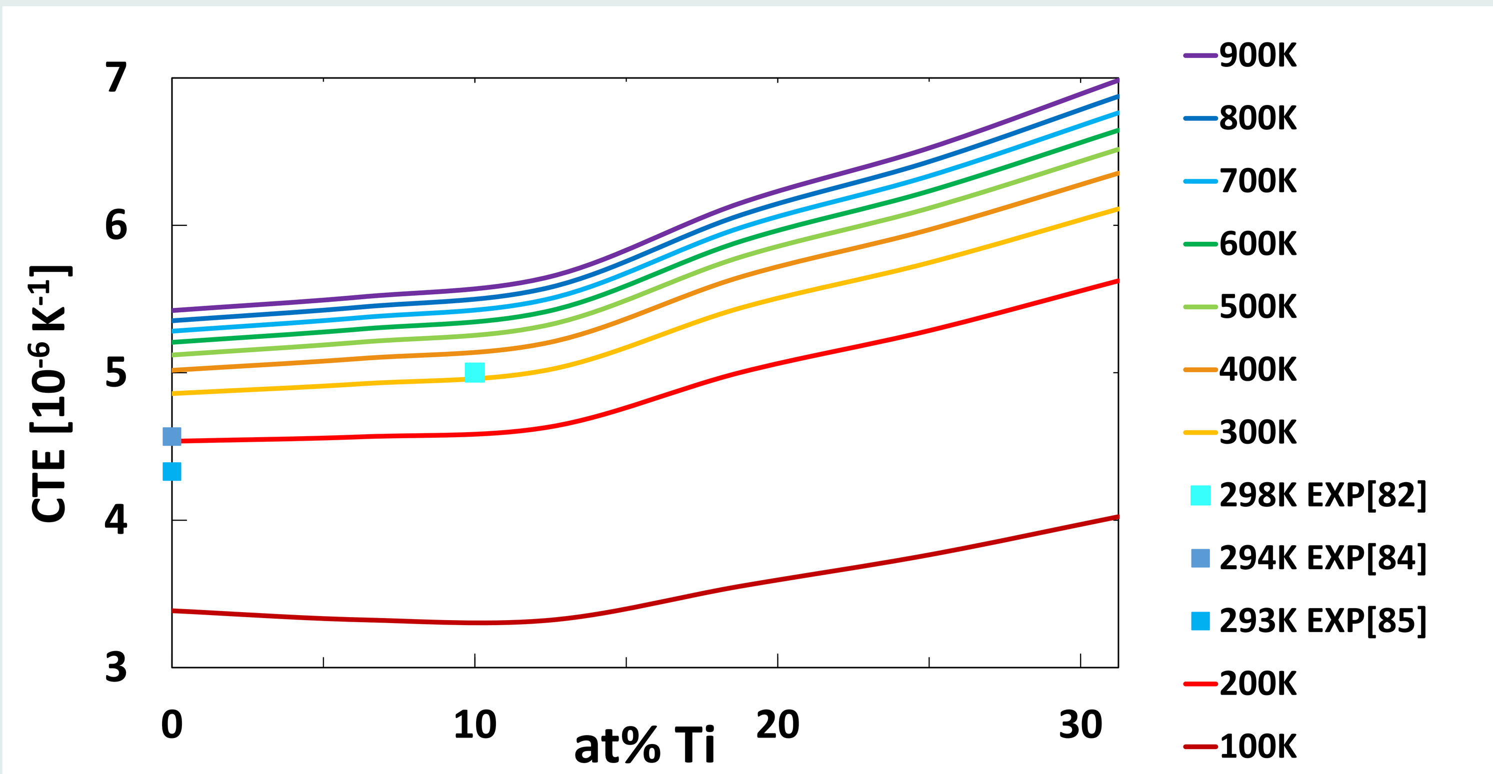
Cu is the main metallization material in integrated circuits. To separate semiconductor and metallization, WTi is a commonly used as an interlayer. The thermomechanical properties of WTi and the adhesive properties of the interface between metallization and interlayer are not fully understood. In this PhD, the thermal expansion elastic constants, as well as the chemistry and structure of the interface are investigated to provide insights how damage in metallizations can be reduced.

Theory and Methodology

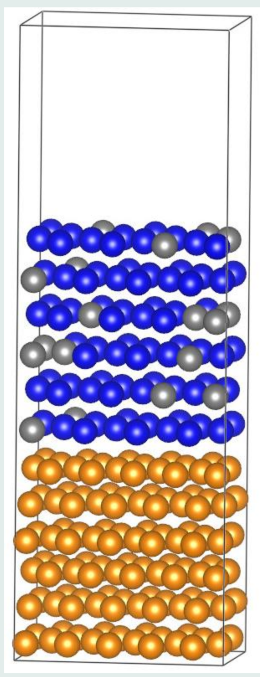
The elastic constants and thermal expansion of WTi have been calculated using density functional theory (DFT) and thermodynamic models implemented in phonopy.
Solute segregations and their impact on cohesive strength of Cu grain boundaries and Cu-W and Cu-WTi interfaces are evaluated with representative atomistic models of Cu grain boundaries and calculation of appropriate energetic differences.

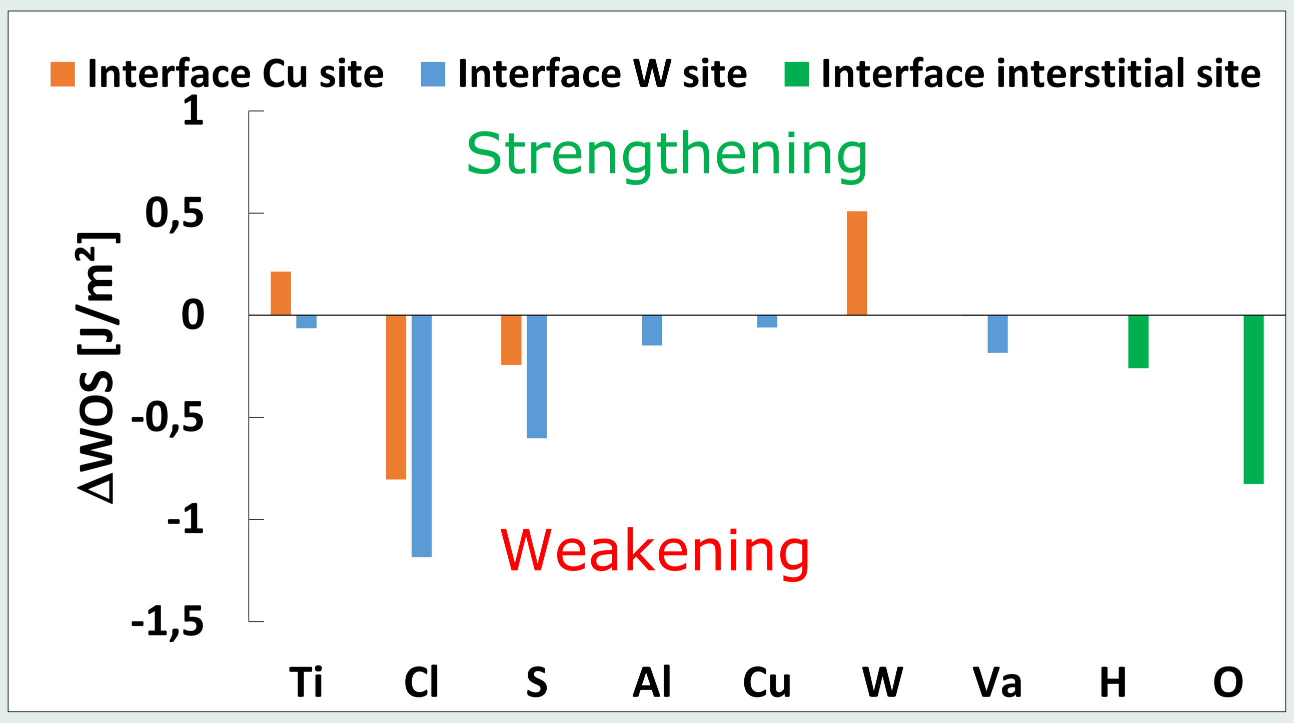
Results

The CTE of WTi have been calculated for different temperatures.

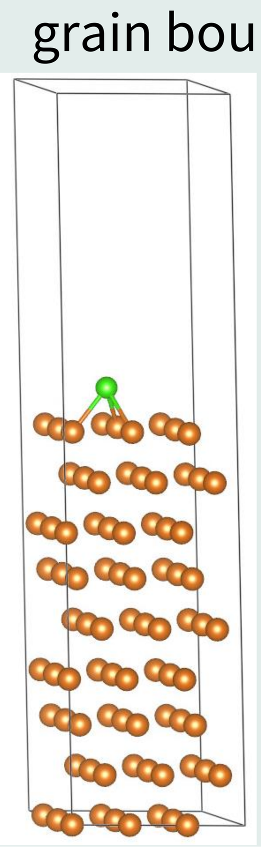


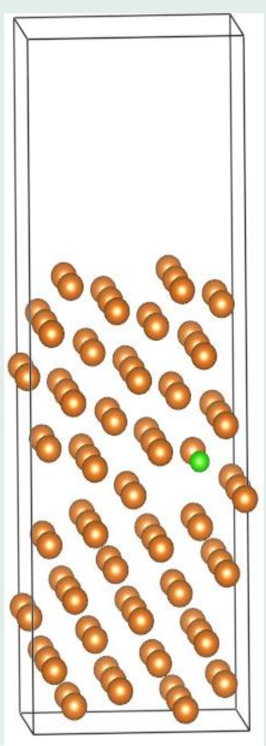
The effect of impurities on the cohesion of the Cu-WTi interface has been calculated.

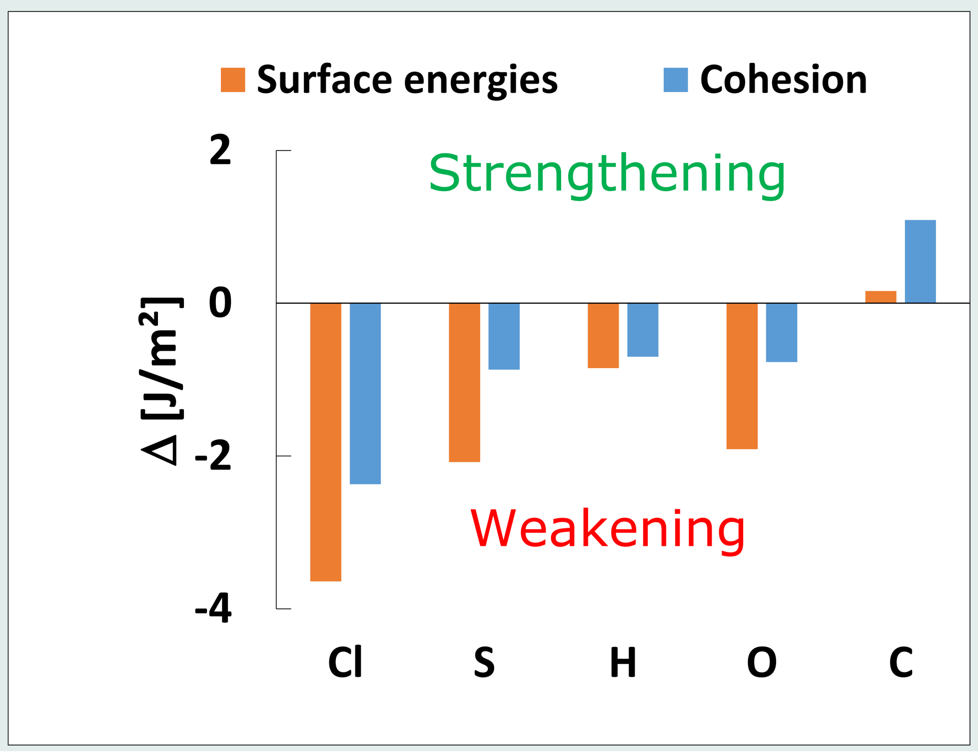




The effect of impurities on the surface energy and strength of the grain boundary have been investigated.







Conclusions

The CTE of WTi at low concentrations and temperature is negative in respect to concentration.
The calculated CTE and elastic constants will be used for residual stress simulation via FEM.
Most of the common impurities of Cu and CuWTi lower the cohesive energy of the system and therefore the fracture toughness of the interface.
These results will be correlated with micromechanical fracture tests and thermokinetic simulations of pore growth kinetics.

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84. Nix, F. C. & MacNair, D. The Thermal Expansion of Pure Metals. II: Molybdenum, Palladium, Silver, Tantalum, Tungsten, Platinum, and Lead. *Phys. Rev.* **61**, 74–78 (1942).
85. Deshpande, V. T. & Pawar, R. X-RAY DETERMINATION OF THE THERMAL EXPANSION OF TUNGSTEN. *Curr. Sci.* **31**, 497–499 (1962).

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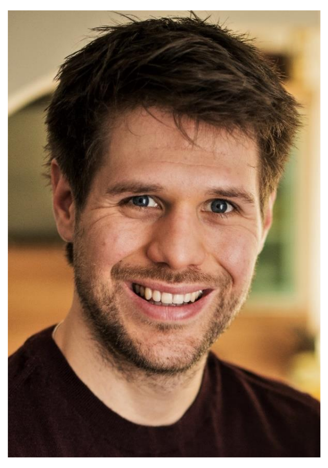


Impact of morphology on residual stresses in TiW thin films

Introduction

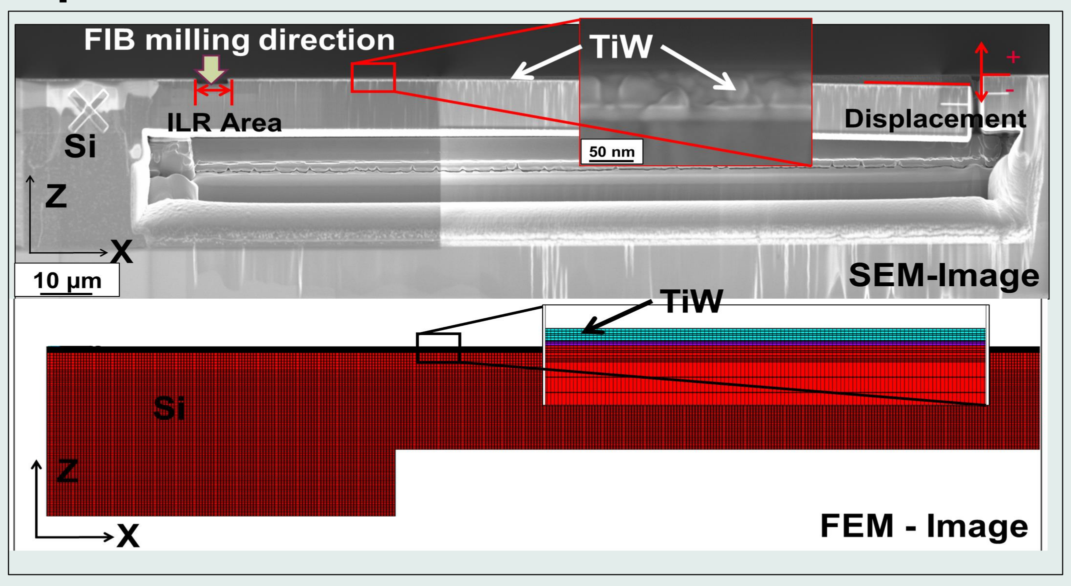
- Residual stresses in TiW thin films depend strongly on composition, morphology and thickness.
- A cross-sectional study to evaluate these correlations is done using:
    - Depth-resolved, high resolution residual stress measurements
    - Morphological and microstructural characterization

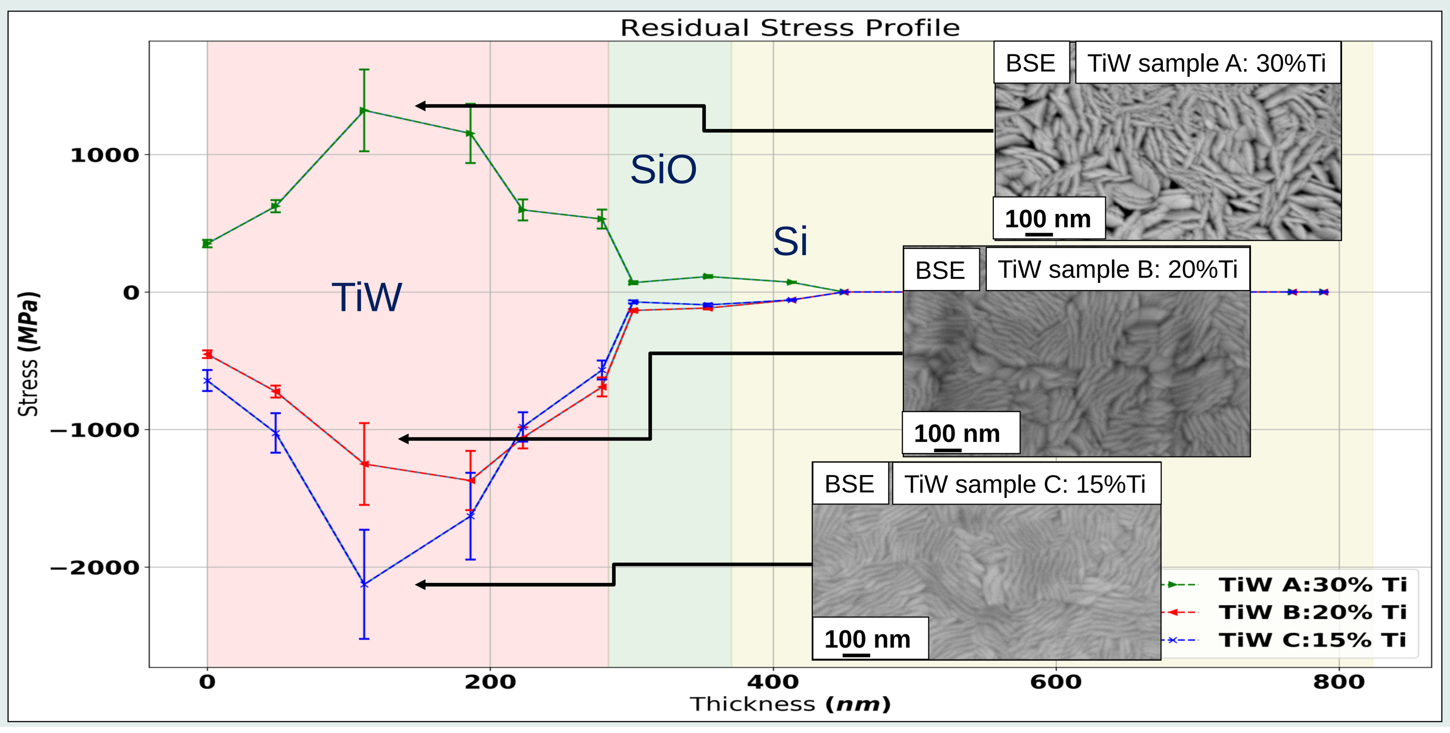
Material Parameter Characterization: ILR-Method

Ion Layer Removal method (ILR):

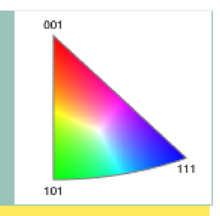
- ✓ Local depth resolved stress measurement method using a **micro-cantilever**.
- ✓ Layers are removed by focused ion beam in **ILR area** (**10 nm resolution**).
- ✓ **Change of cantilever deflection** due to gradual film removal

  → **Stress profile as function of thickness** is evaluated by FEM from **experimental deflection**.



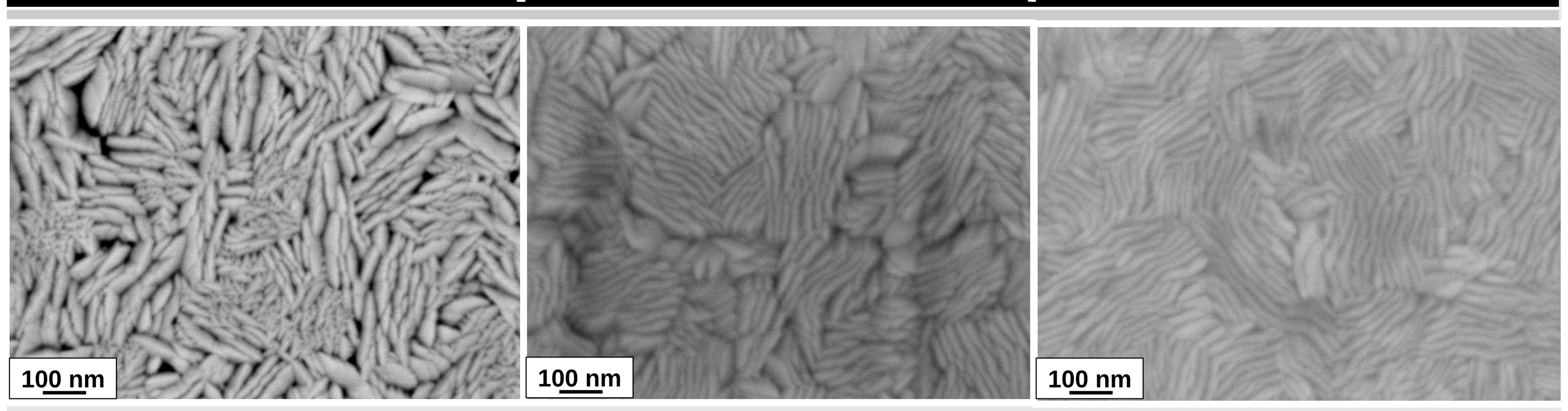


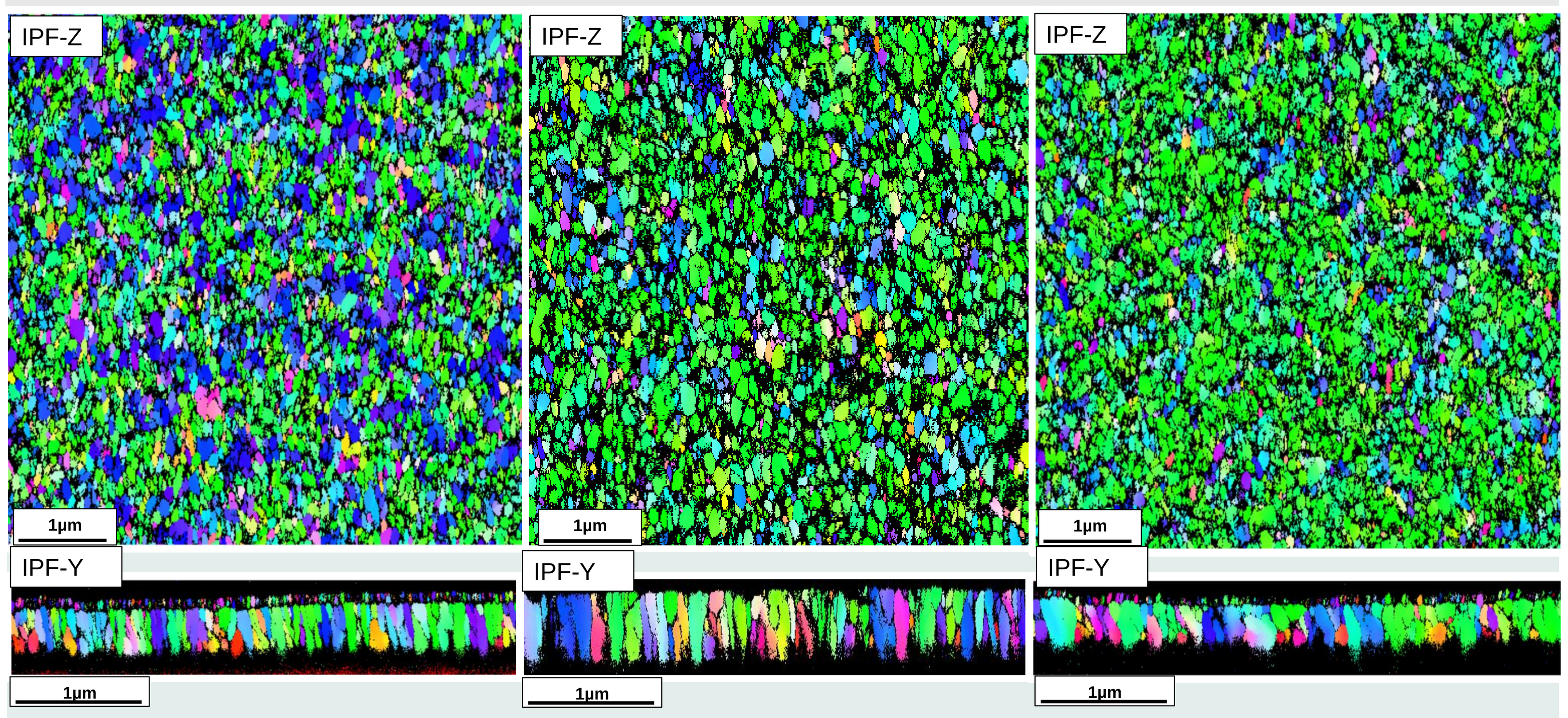
Microstructural analysis



Surface analysis of TiW sample A,B and C → FESEM

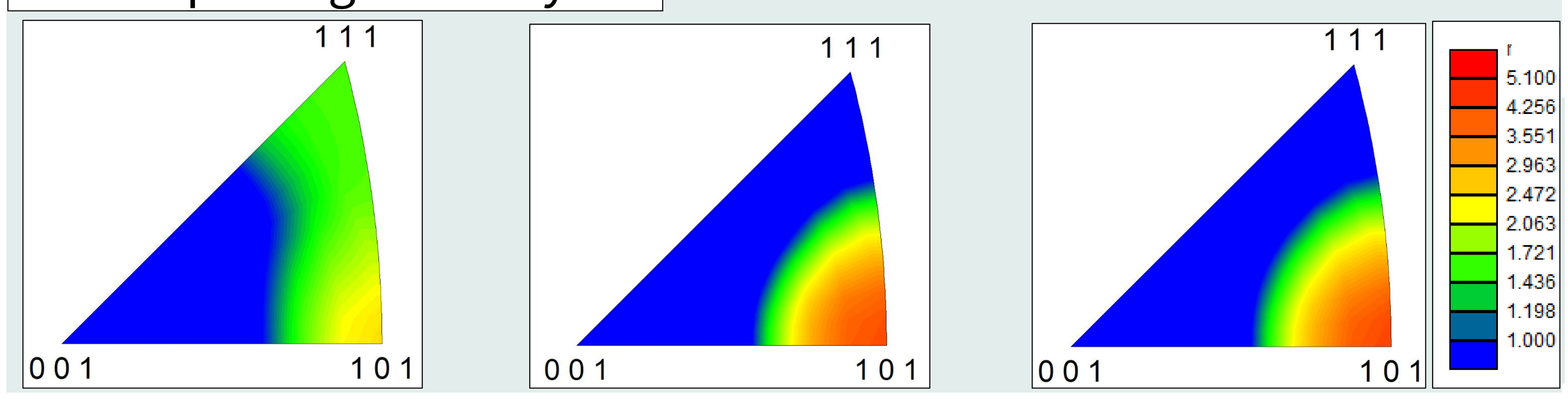
TiW sample A: 30%Ti	TiW sample B: 20%Ti	TiW sample C: 15%Ti





Grain size diameter: Mean = 70 ± 30 nm	Grain size diameter: Mean = 60 ± 30 nm	Grain size diameter: Mean = 80 ± 40 nm

Inverse pole figure analysis:



Results: Residual Stress Profile & Gradient

- **Sample A** with coarse morphology has preferred 110 orientation with tendency of 111 orientation leading to a lower surface energy.
- **Sample B and C** with dense morphology has preferred 110 orientation leading to comparatively high surface energy.
- **Morphology** effects residual stresses

- **Evaluated Stress Profile & Gradient:**
    - ➢ 30%Ti sample A: **Tensile stress**
    - ➢ 20%Ti sample B: **Compressive stress**
    - ➢ 15%Ti sample C: **Compressive stress**
- **Next step:** Image analysis will be carried out to quantify the effects of morphology on residual stress profile

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Device Characterization

Locally resolved deformation and fracture processes near interfaces

Markus *Alfreider*

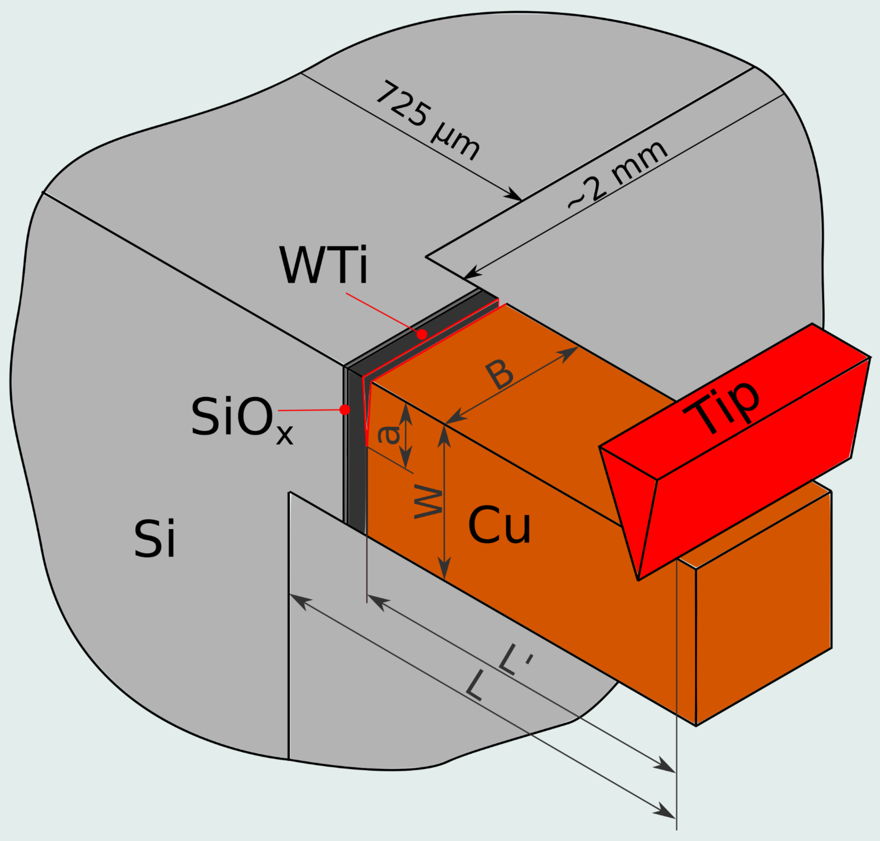
Daniel *Kiener*

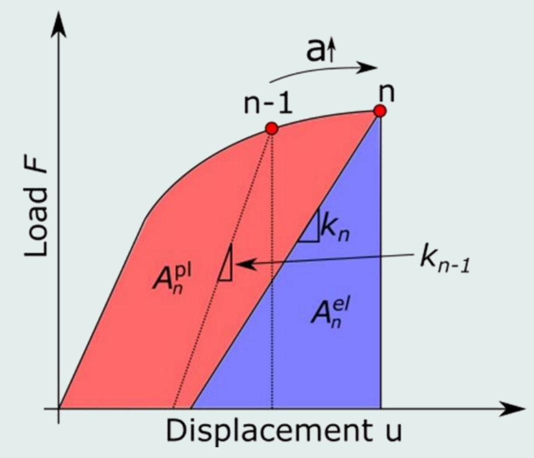
Introduction

The ongoing miniaturization of microelectronic devices creates a rather challenging environment for materials from a structural as well as thermo-mechanical point of view. Especially, the various interfaces (grain-/phase-boundaries; substrate-thin film interface) appearing in these devices undergo a unneglectable strain and are therefore important to understand.
Using the WTi/Cu interface as a demonstrator, the aim of this work is to:

- Develop advanced techniques to investigate interface fracture.
- Understand the influence of these interfaces on local mechanical properties.

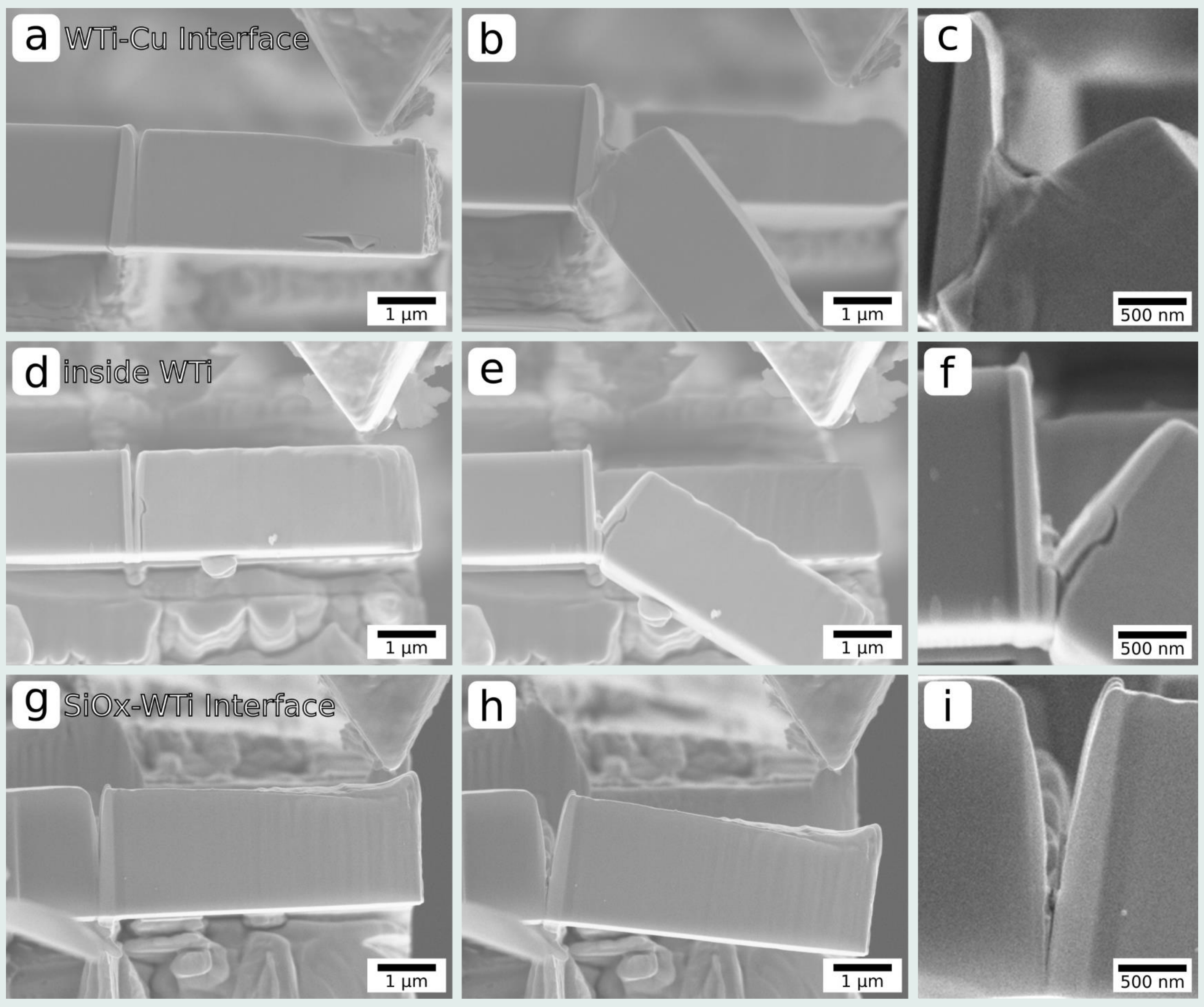
Methodology and Theory

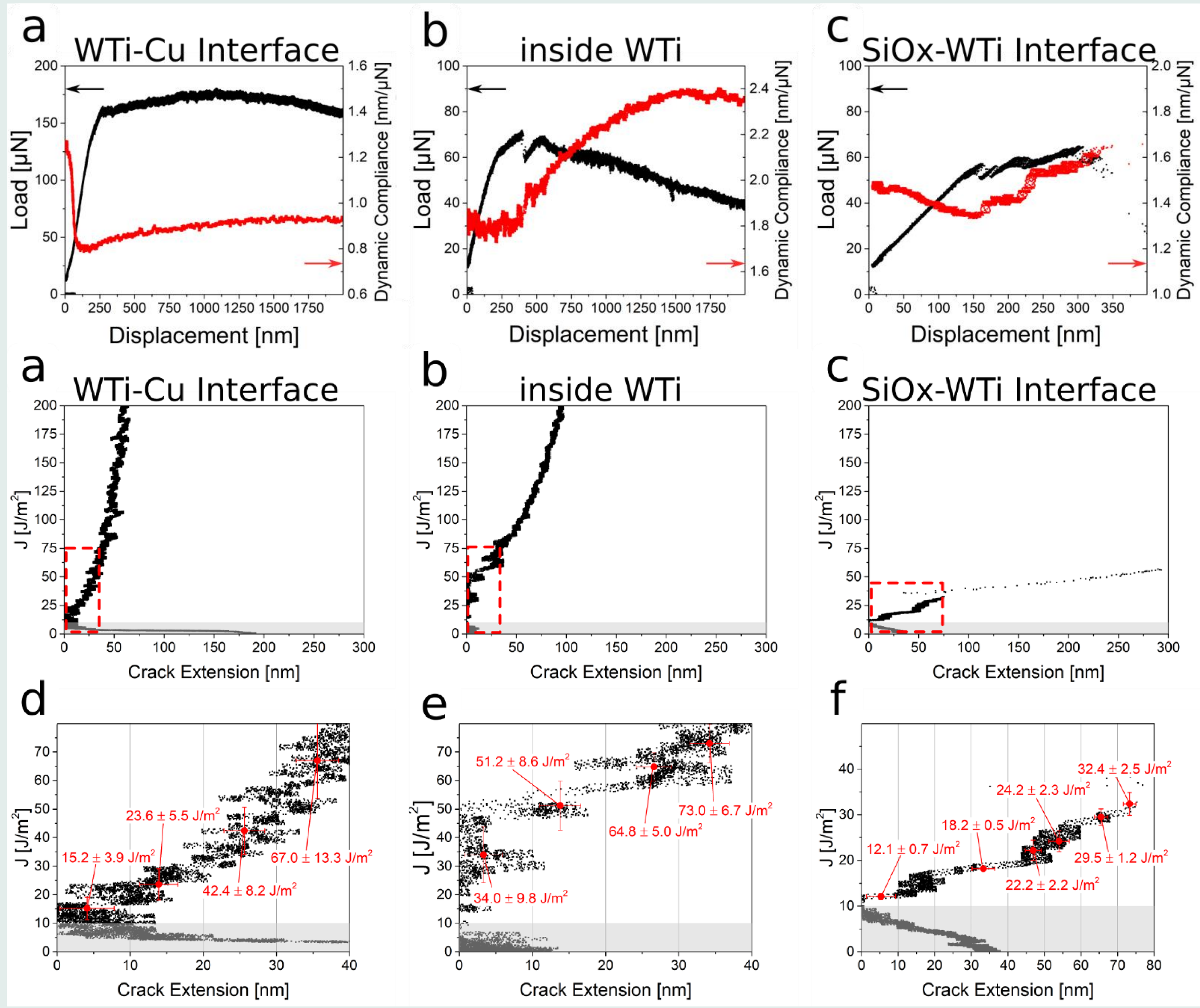


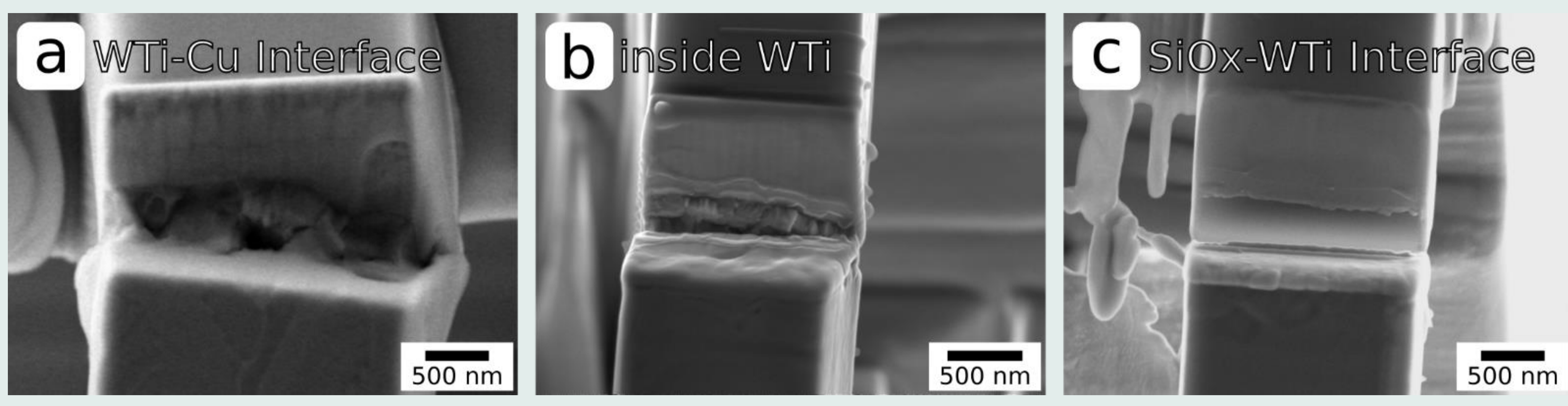


Evaluation J-Δa curves for individual interfaces in the multilayer material stack

Results







Depending on the position of the notch distinctive differences with respect to plastic deformation vs. Interface decohesion and crack propagation are evident.

Summary and Outlook

Possibility to measure tougher features close to weaker features.
Future research will focus on resolving interfaces with fluctuations in local chemical composition.

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Device Characterization

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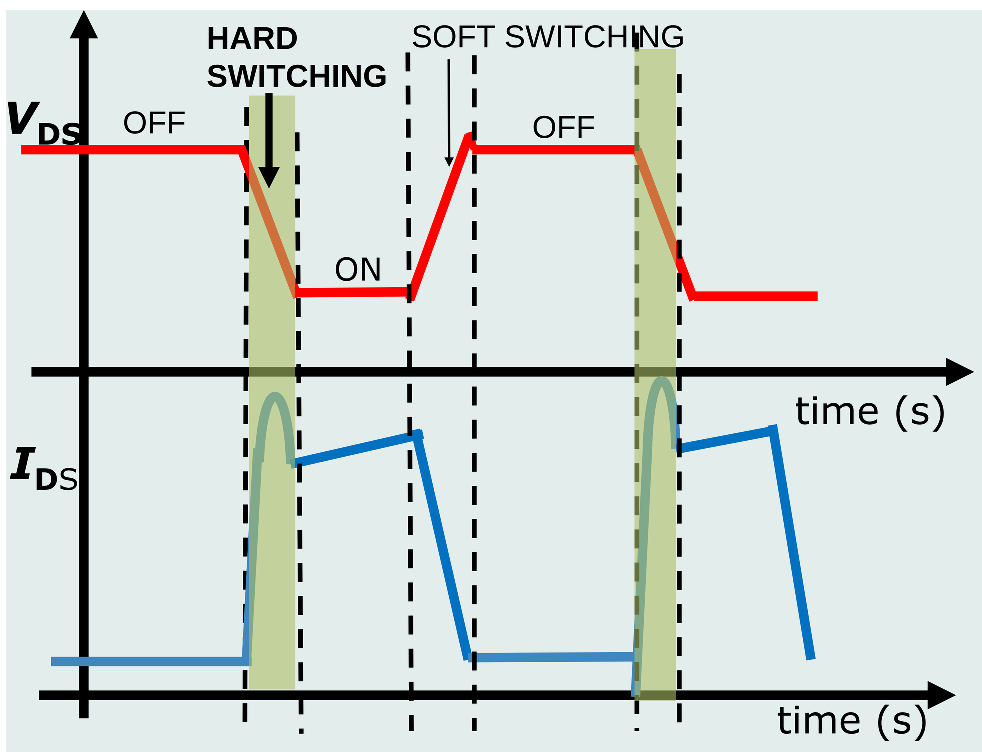
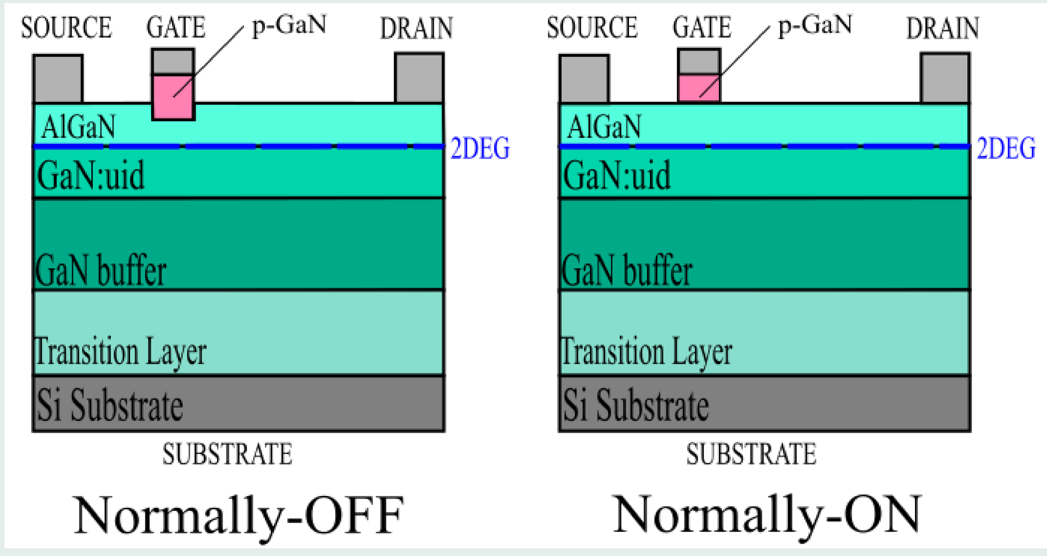
Buffer and surface trapping in GaN based HEMTs

Introduction

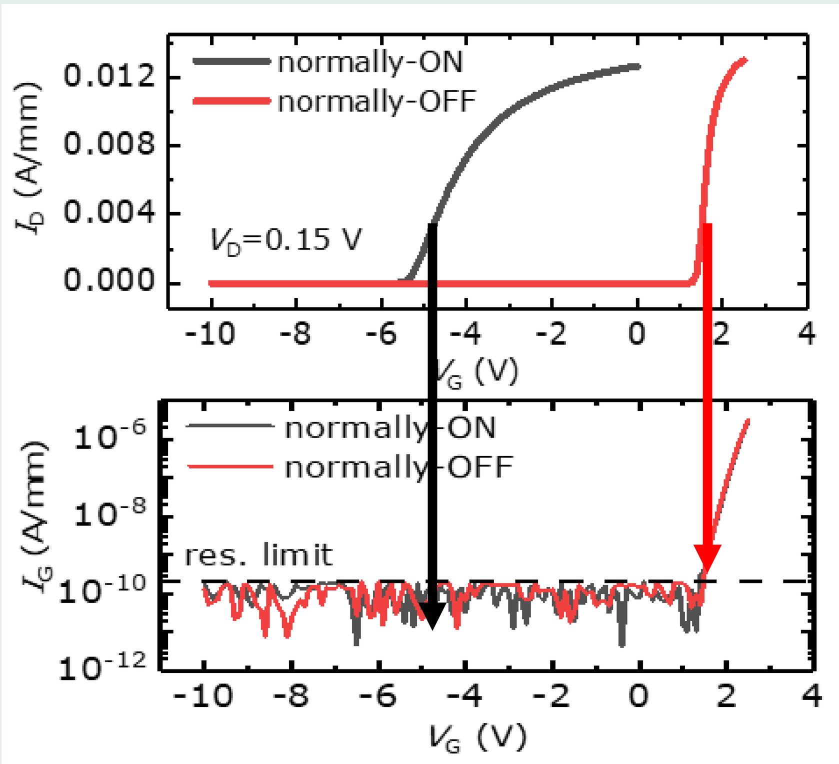


Hard switching → high current and high voltage → hot carrier trapping that is not present during OFF-state

- **Is the trapping in the buffer or in the AlGaN surface?**
- Normally-ON devices are introduced



DC characterization

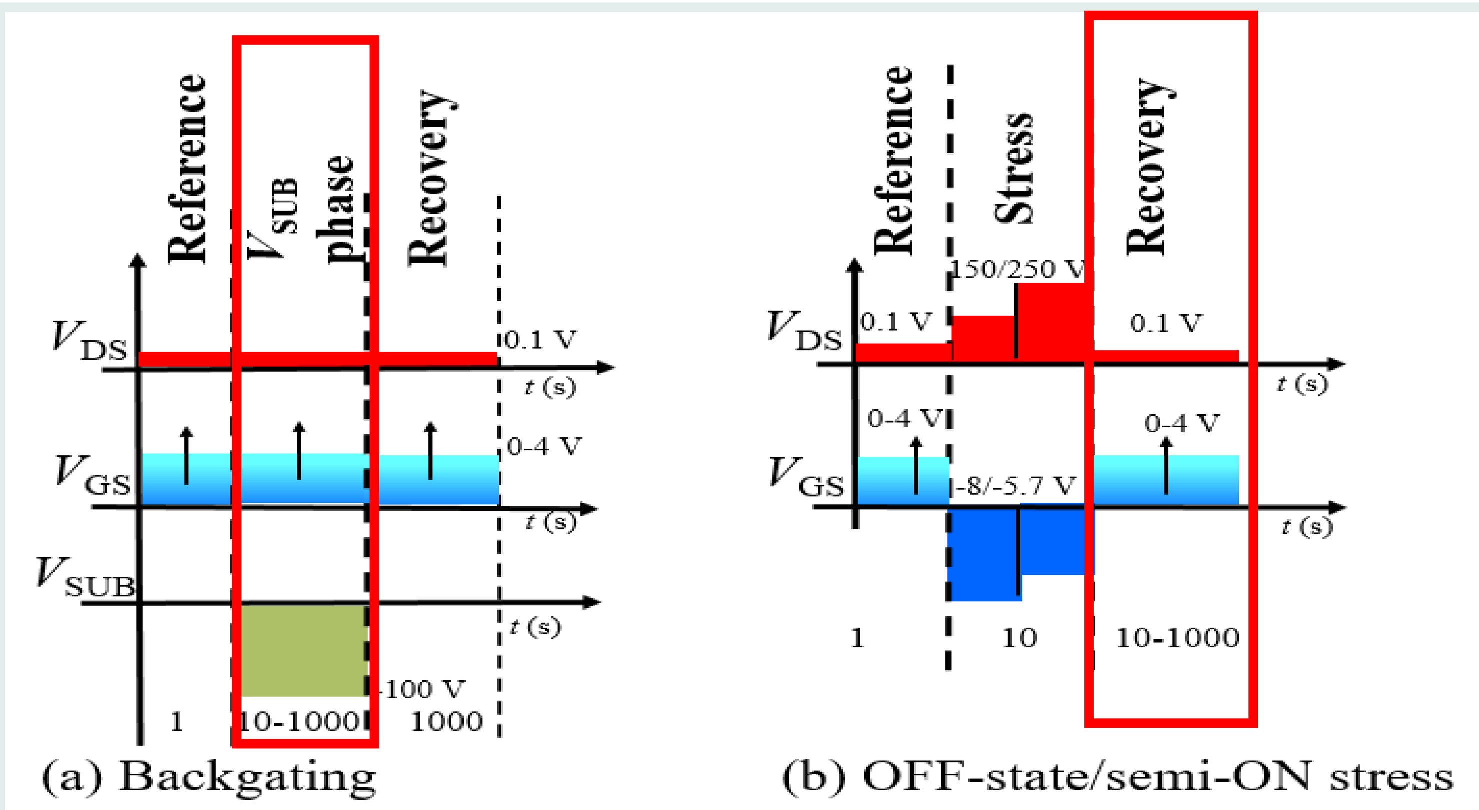


$V_{TH,NOF}$ =1.5 V
I_G=1e-9 A/mm

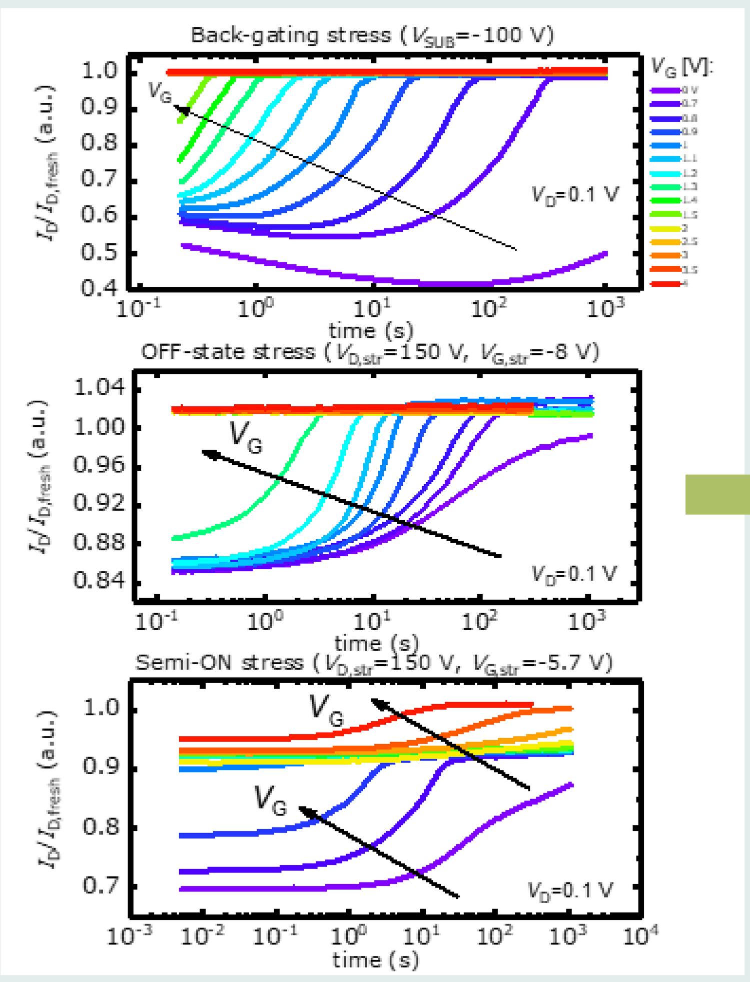
$V_{TH,NOF}$ =-5.5 V
I_G=0 A/mm

measurement of the I_D without any influence of I_G(=hole injection that changes the charge distribution in the device)

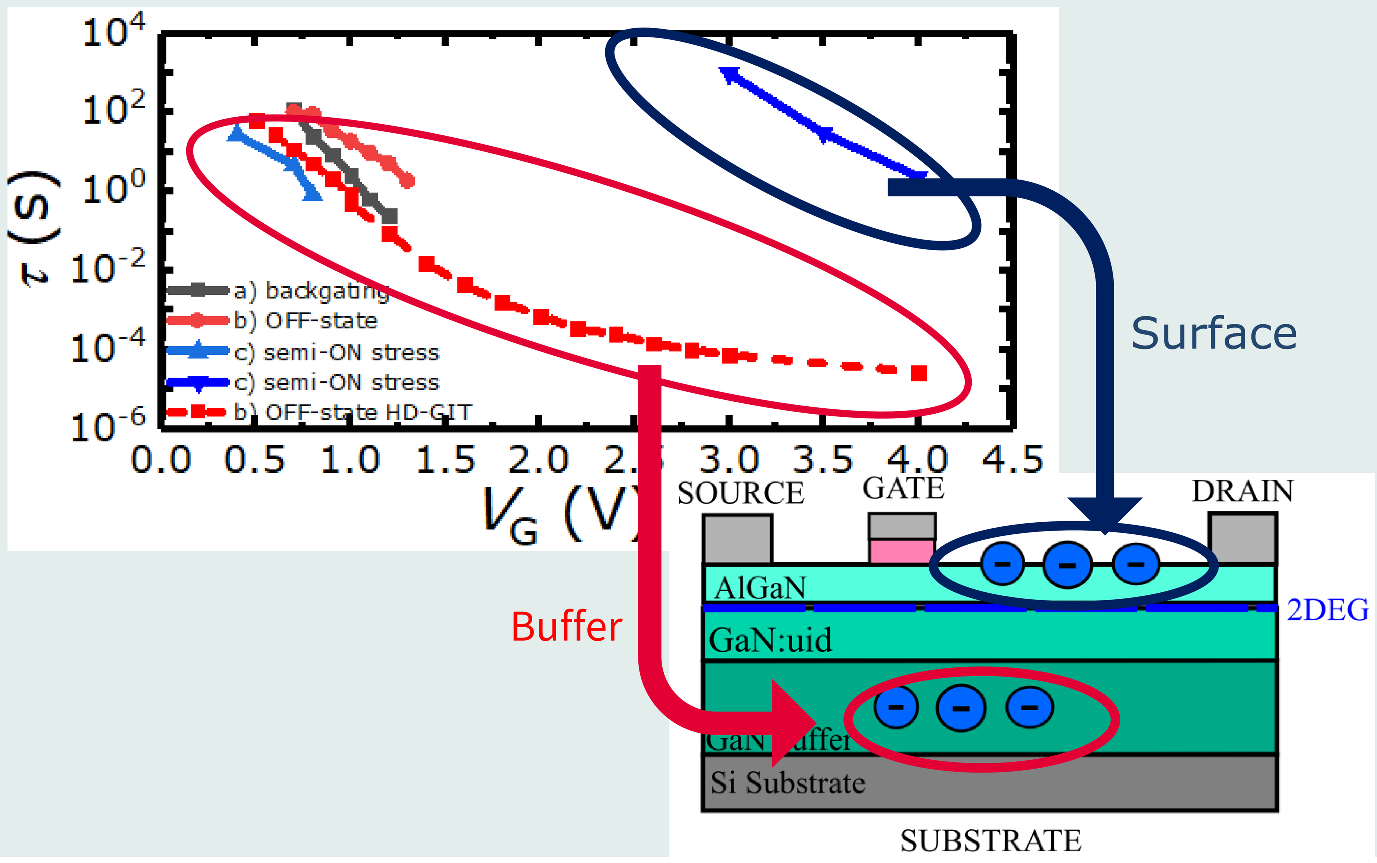
MSM Technique



Results



- Time constant are extracted from the transients
- OFF-state and back-gating show similar time constant→ traps in the buffer
- semi-ON stress → hot carrier degradation →traps in the buffer
+ AlGaN surface



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Carrier Mobilities in 4H-SiC Trench MOSFETs

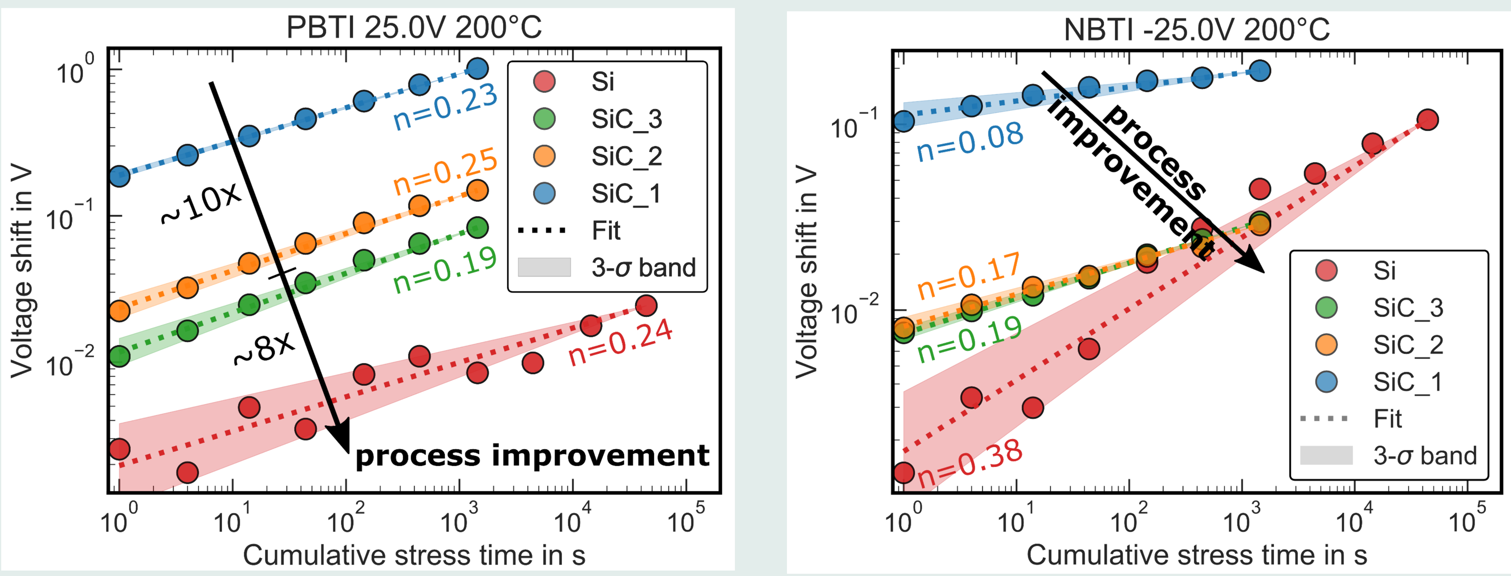
Motivation

- **Challenge:** Trapping at SiC/SiO_2 interface
  → reduced channel mobility µ
- **Current solution**: post oxidation annealing (POA) in nitric oxide (NO)
- **Research goal**:
  - Understanding of mechanism
  - Improvement of device performance and reliability

Methodology

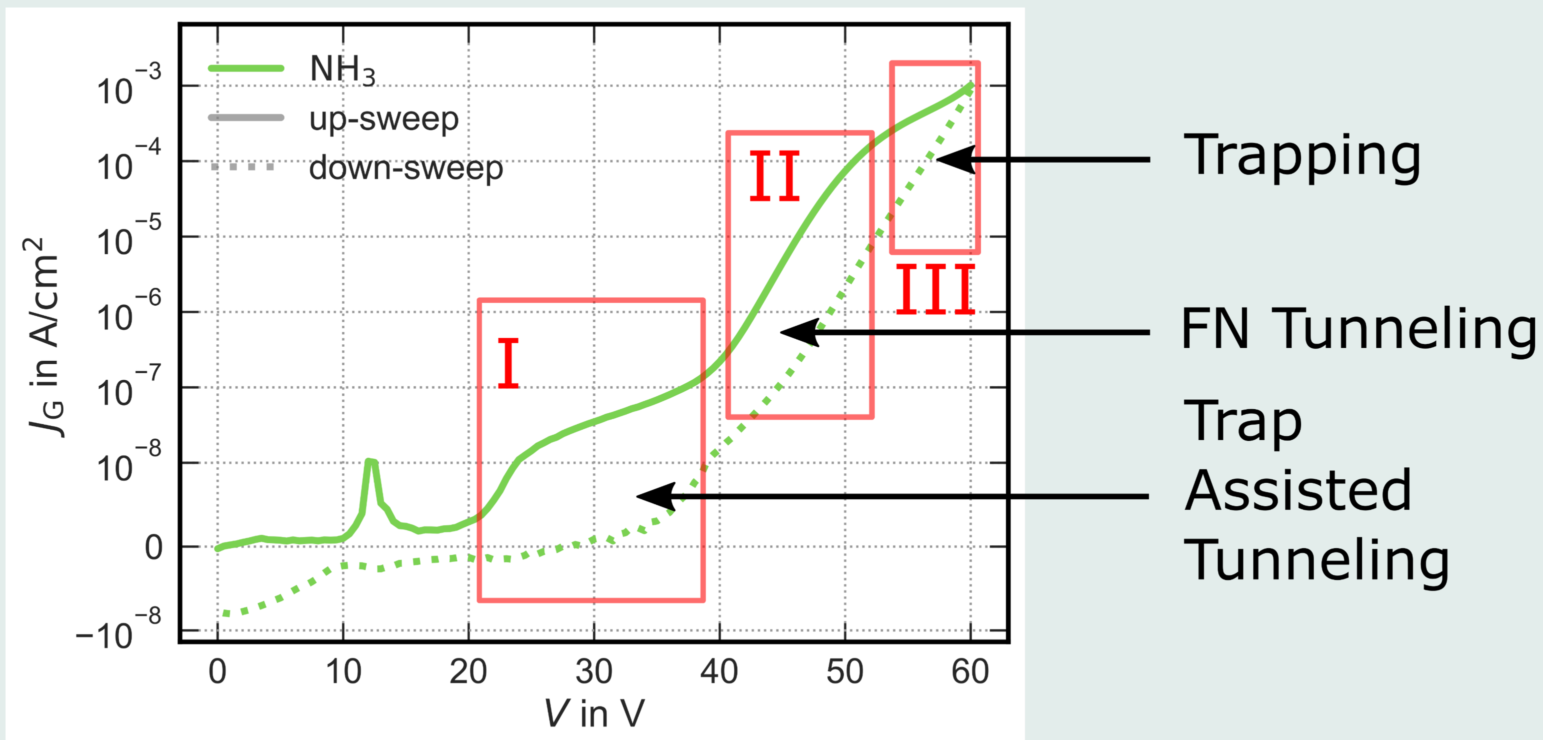
- **Mobility:** determination of apparent channel mobility directly out of I_D-V_G
- **Bias Temperature Instability (BTI):** repeated stress and readout to determine trapping related drift
- **Cryogenic measurements:** determination of trap densities and activation energies

BTI – SiC vs. Si [1]

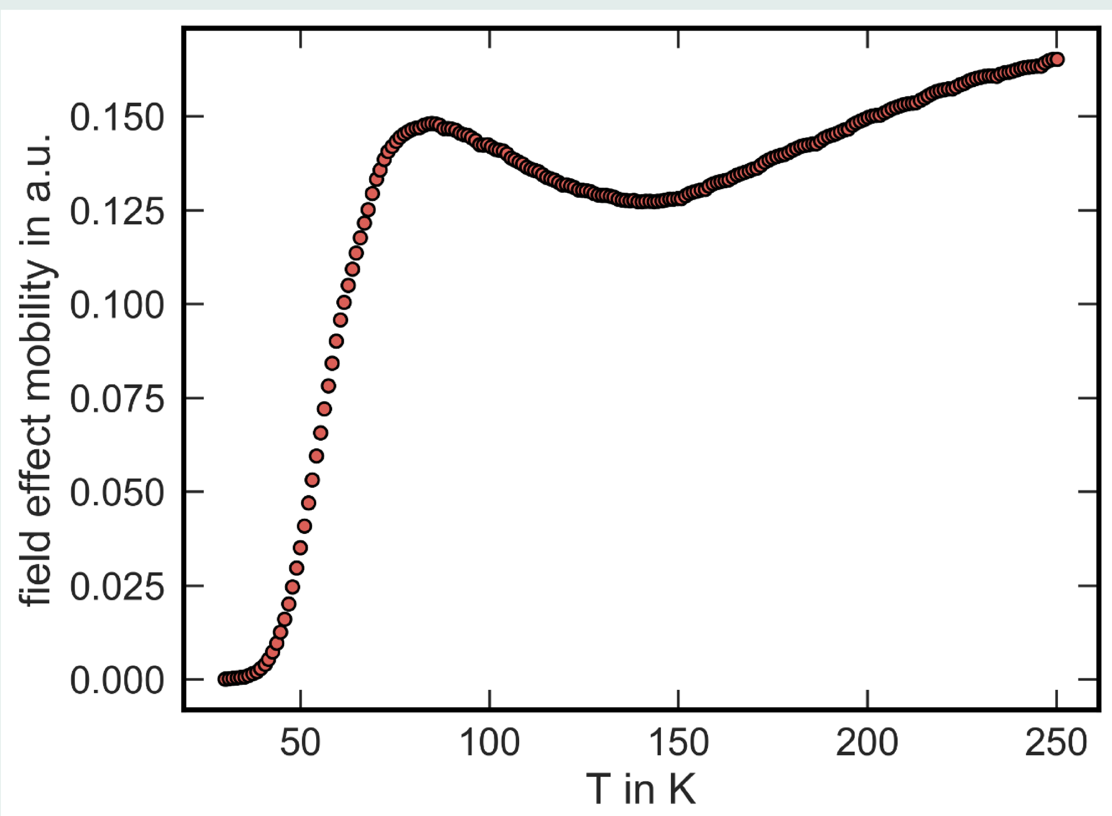


- Most likely same trap bands
- Drift optimization by device processing

Oxide Reliability NH_3 POA [2]



Cryogenic Mobility

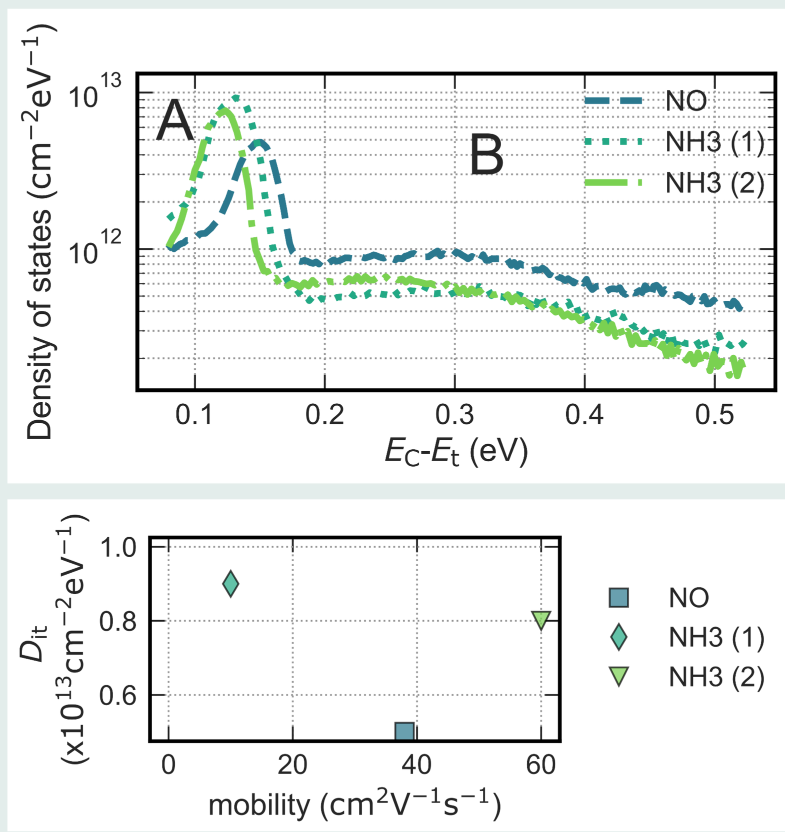


- Influence of single trap levels on µ(T)?
- Correlation between trap levels and µ(T) possible?

Cryogenic Mobility – TDRC [3]

A: interface traps (ITs)
B: near interface traps

- NO and NH_3 POAs reduce ITs
- ITs: not main origin of the low mobility



[1] J. Berens et al., IEEE International Reliability Physics Symposium, 2020
[2] J. Berens et al., Material Science Forum, 2020, Silicon Carbide and Related Materials 2019
[3] J. Berens et al., Material Science Forum, 2019, Silicon Carbide and Related Materials 2018

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Device Characterization

PhD
Paul Hoffmann

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Simulation of Fatigue Damage in Power Semiconductors

Introduction

Power semiconductors are often subjected to short electric overload pulses which induce very high temperature gradients in the metallization stack. Consequently, high mechanical stresses and strains occur. This active cyclic loading can lead to material failure and might result in overheating and destruction of the device.

Research Goal:
Development and calibration of a physical lifetime model to predict fatigue damage in power semiconductor devices.

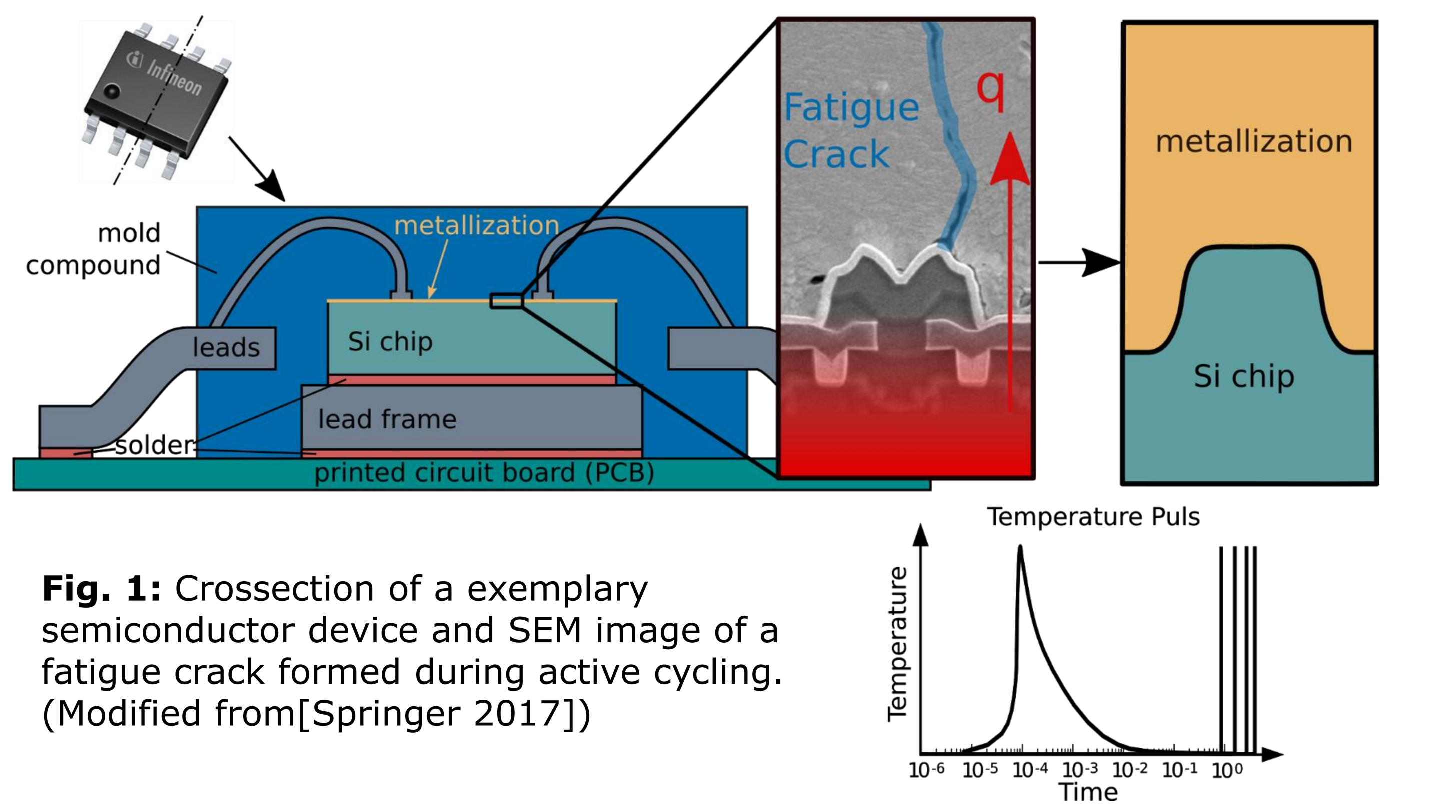

Fig. 1: Crossection of a exemplary semiconductor device and SEM image of a fatigue crack formed during active cycling. (Modified from[Springer 2017])

Methodology

- Numerical predictions of thermo-mechanical fatigue in power semiconductors are carried out.
- A previously developed approach [M. Springer, Dissertation TU Wien] to model bulk fatigue damage is extended towards the usage of more general transient thermo-mechanical loading conditions.
- For demonstration purposes, the developed bulk fatigue approach is applied to generic copper-on-silicon geometries which are exposed to various transient thermo-mechanical loading.

Results I

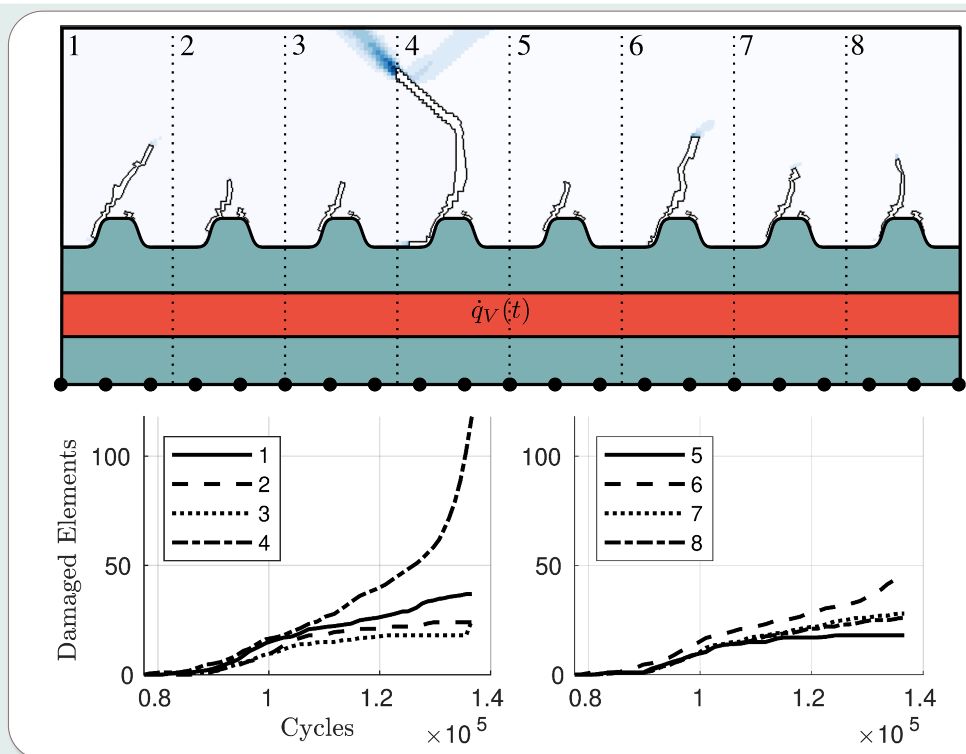

Fig. 2: Developing damage pattern and No. of damaged elements over cycle numbers within an arrangement of eight DMOS cell-like segments. In this model all 8 segments are heated. The shielding effect of the dominant crack can be seen in the plots. After an increase of damage in segment 4 all other segments experience a slow down in crack growth.

✓ Shielding effects of a dominant fatigue crack can be seen

Results II

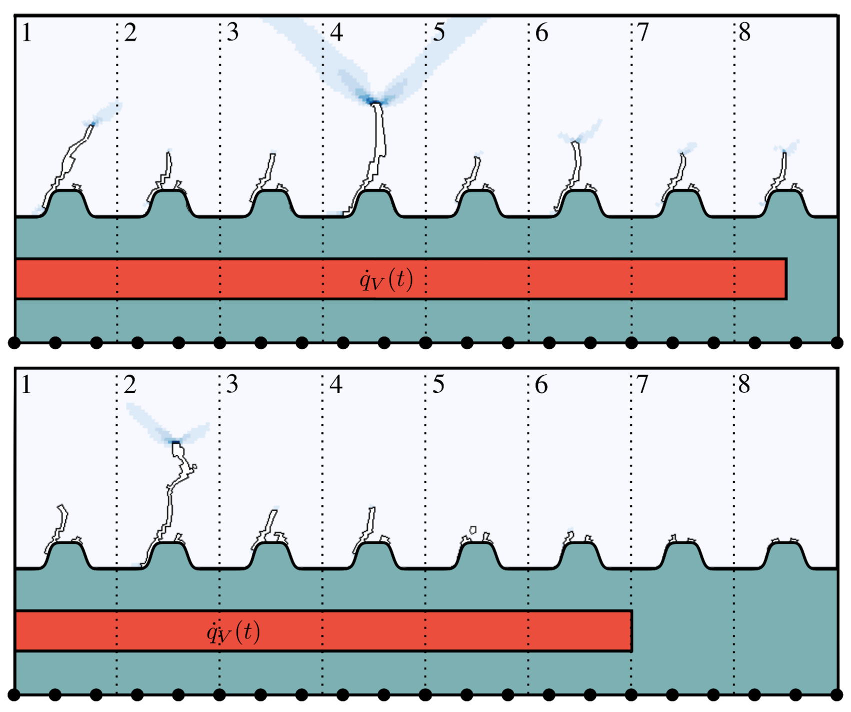

Fig. 3: Two further results highlighting the influence of lateral temperature gradients. In the top picture a very small thermal gradient is introduced by removing the heating beneath the rightmost half segment. The influence on the developing crack patterns is marginal. In the bottom picture a much larger thermal gradient is introduced by removing the heating beneath the two rightmost segments. A strong influence on the lateral distribution of fatigue cracks can be seen.

✓ The influence of lateral temperature differences is highlighted

Further Research

- The current framework cannot resolve individual fatigue cracks in the absence of stress concentrators.
- Currently an approach is developed to introduce information about the material microstructure into the fatigue framework.
- This approach will be employed to calibrate material date and subsequently predict critical cycle numbers for through film cracks.

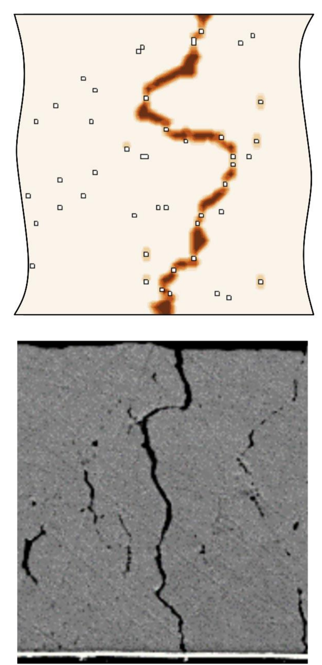

Fig. 4: Simulated and experimental cross-section crack

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Device Characterization

Electrochemical Investigation of Ion Diffusion through Polymer Membranes in Combination with FEM Modelling

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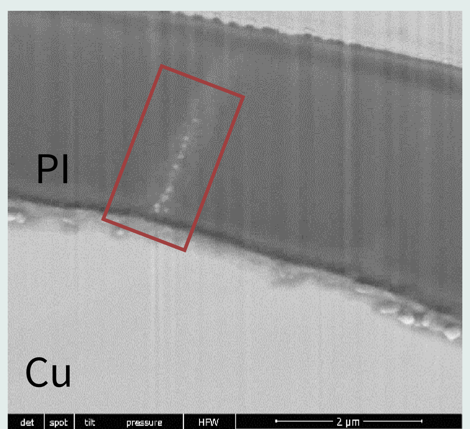
Motivation

What we have:
Cycled stress test showed
- Ion diffusion through polyimide
- Surface degradation



SEM image of a FIB cut of ion diffusion into PI on a Cu surface [1]

What we want:
Diffusion Coefficients for the transport of ions, contaminants and corrosion related species.

What we do:
Methods development for determining the ion diffusion:
- Electrochemical measurements
- Simulation
- Quantitative analysis

[1] E.Ludwig, "Corrosion of Copper in Combination with Polyimide", EUROCORR 2017, Corrosion reliability of Electronic Devices, 7 September 2017, Prague, Czech Republic. ID: 79211.

Diffusion cell made of PMMA with a PI membrane clamped inside

Simulation

Determination of transport parameters by fitting FEM simulation (made in COMSOL Multiphysics®) to the measurement.

- **"Transport of diluted species" (Nernst-Planck)**

$$f_i(x,t) = -\boldsymbol{D_i}\left[\frac{\partial c_i(x,t)}{\partial x} - z_i c_i(x,t)\left(\frac{F}{RT}\right)E(x,t)\right]$$

- **"Electrostatics" (Poisson)**

$$\frac{\partial E(x,t)}{\partial x} = \frac{\rho(x,t)}{\varepsilon}, \rho(x,t) = F\sum_i z_i c_i(x,t)$$

- **Convection and liquid flow are ignored**

- **Osmosis** effects make adjustment of the model necessary
- An additional amount of water is driven into the membrane by **osmosis**.

$$H_{osmo} = -\frac{1}{\ln\left(1 - \frac{p * V_{H_2O}^m}{RT}\right) * RH} \quad [2]$$

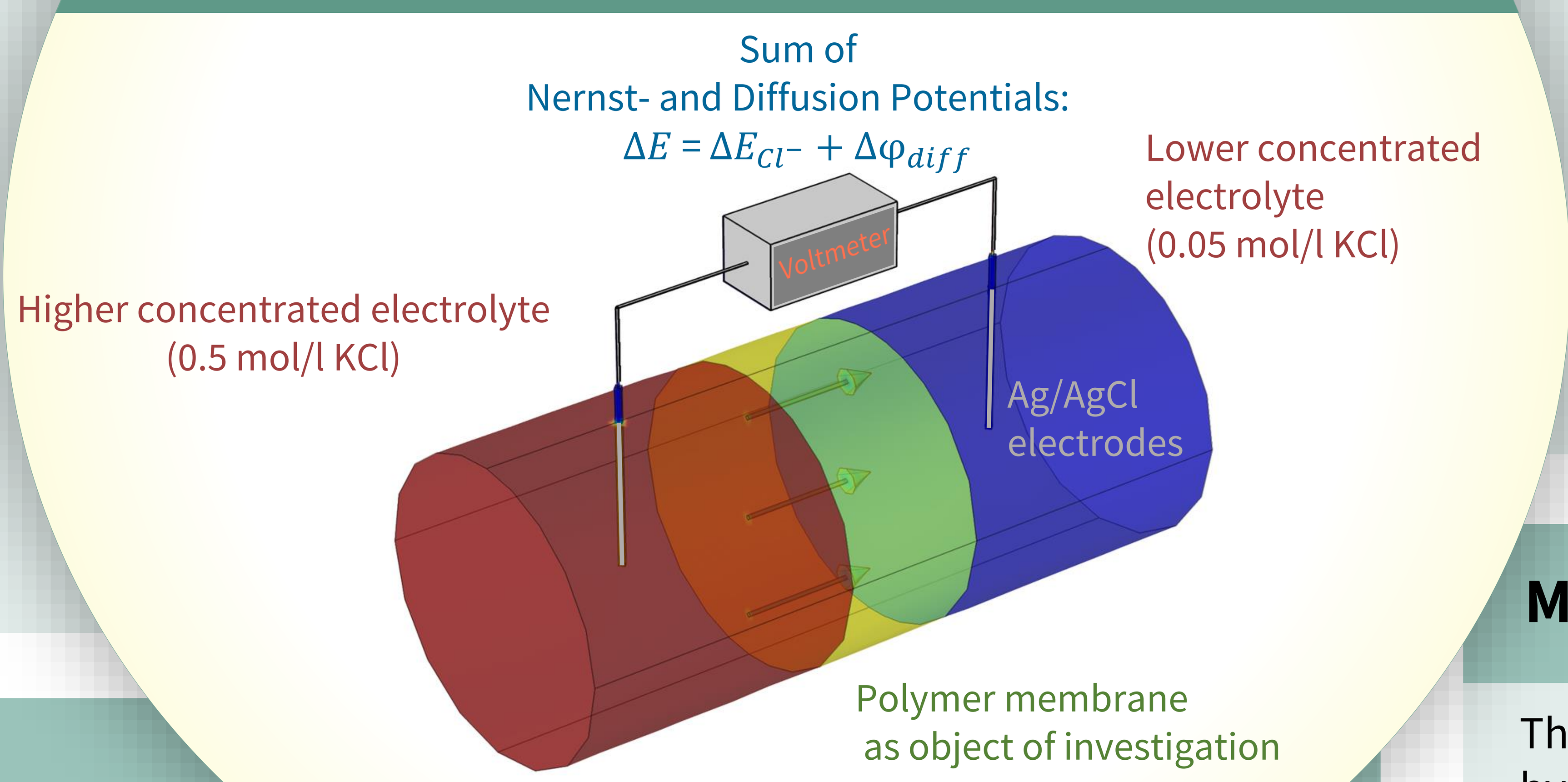
- The diffusion coefficient reacts exponentially to changes in the volume fraction of the diluent
- It is expressed by the water uptake *(H)* in the membrane

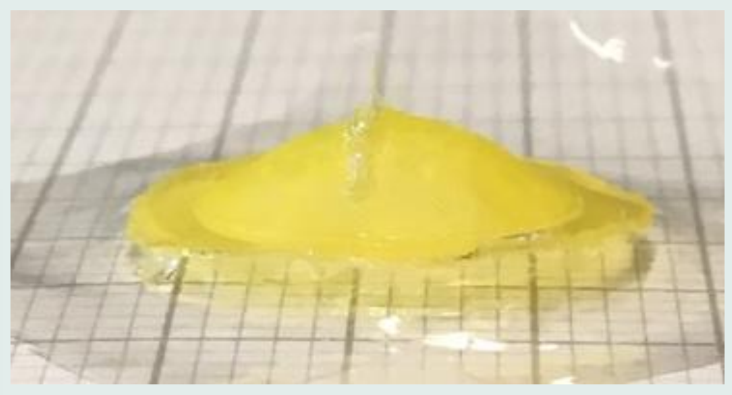
$$lnD_{eff} = lnD_0 - K(\frac{1}{H} - 1) \quad [2]$$

[2] K.-D. Kreuzer: „The role of internal pressure for the hydration and transport properties of ionomers and polyelectrolytes",Solid State Ionics, 2013, Vol. 252, pp.93-101.

Concept

Diffusion processes driven by concentration differences are measured with a "Diffusion Cell". Transport parameters are determined by fitting FEM simulation (made in COMSOL Multiphysics®) to the measurement.





Nafion membrane with stabilisation grid, destroyed by osmotic pressure

Measurement

The measured voltage is not just influenced by the different concentrations but also by the diffusion voltage over the membrane

1. Nernst Potentials of the Electrodes

$$\Delta E_{Cl^-} = -0.059V \cdot \lg\left(\frac{c_1}{c_2}\right)$$

immediate values!

2. Additional Diffusion-Potential

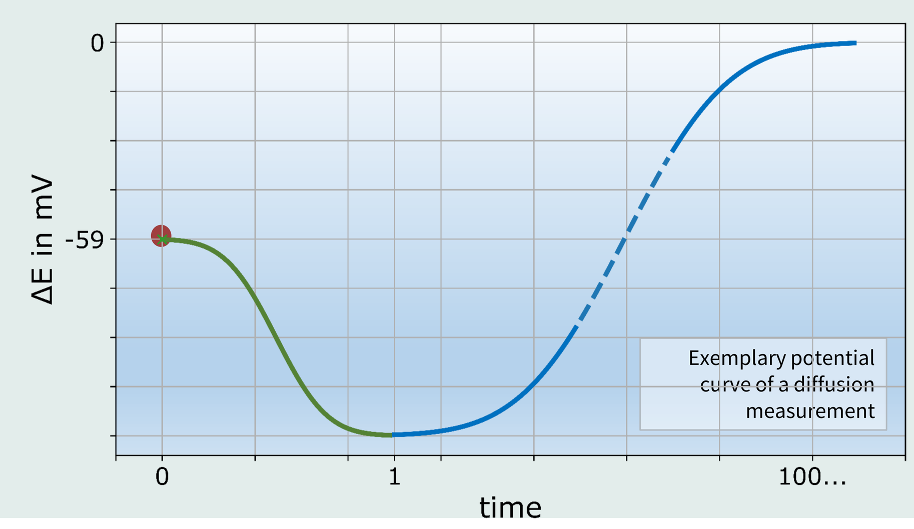
$$\Delta\varphi_{diff} = -\frac{RT}{zF}(t^+ - t^-) \cdot \ln\left(\frac{a_1}{a_2}\right)$$

(ultra-)fast process!
Diffusion of the faster ion across the polymer → development of the diffusion potential!

3. Change of Diffusion- and Nernst-Potential caused by change of concentration:

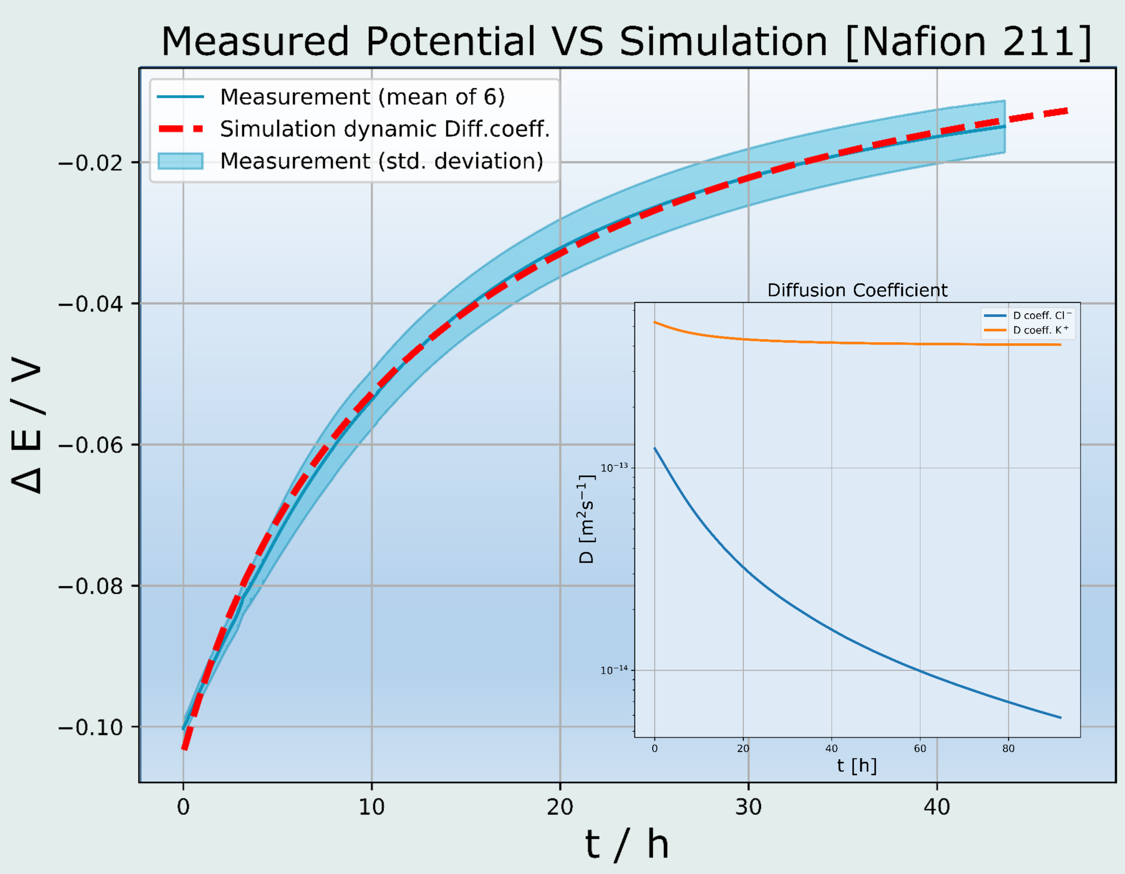
$$\Delta E = \Delta E_{Cl^-} + \Delta\varphi_{diff} \rightarrow 0$$

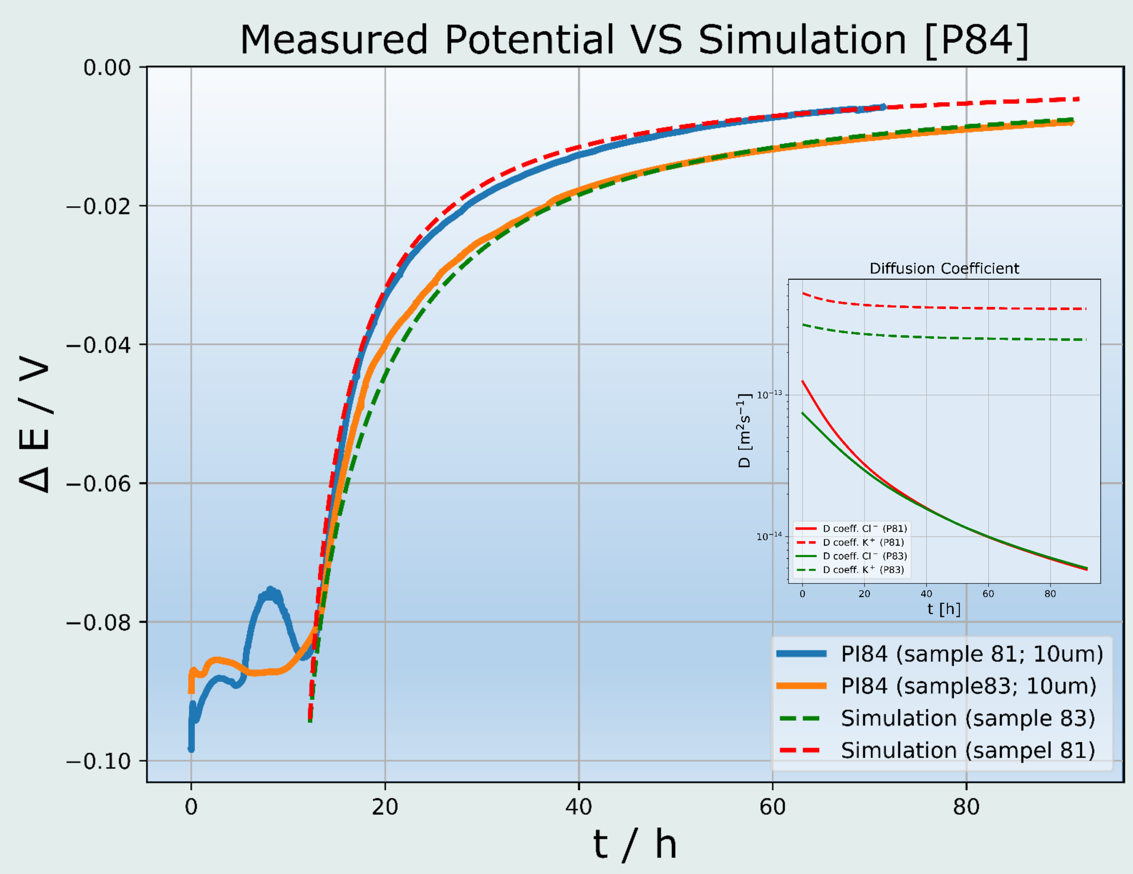
slow process!
Depends on the mobility of the slower ion!



Results

Diffusion coefficients for different model membranes (Nafion211 and self fabricated P84 polyimide).
The values have been extracted from the optimized simulation.





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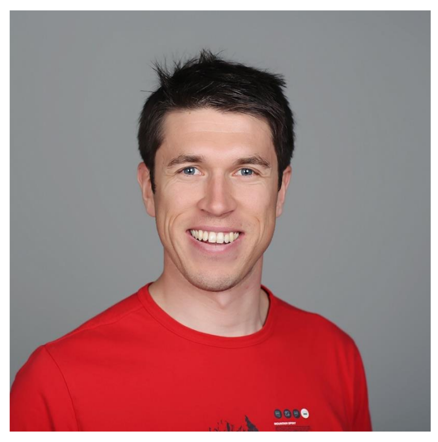
Device Characterization

Lena Bergmann

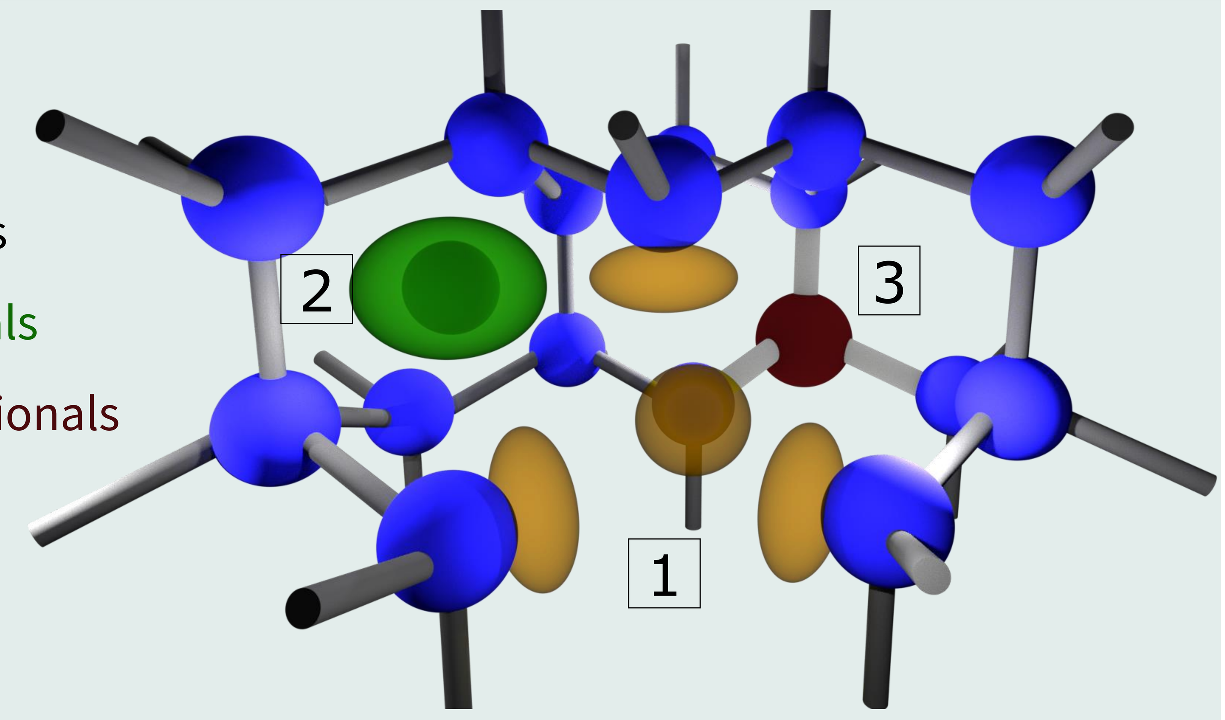
Gregor Pobegen



Electrical characterization of point defects in Si high voltage diodes

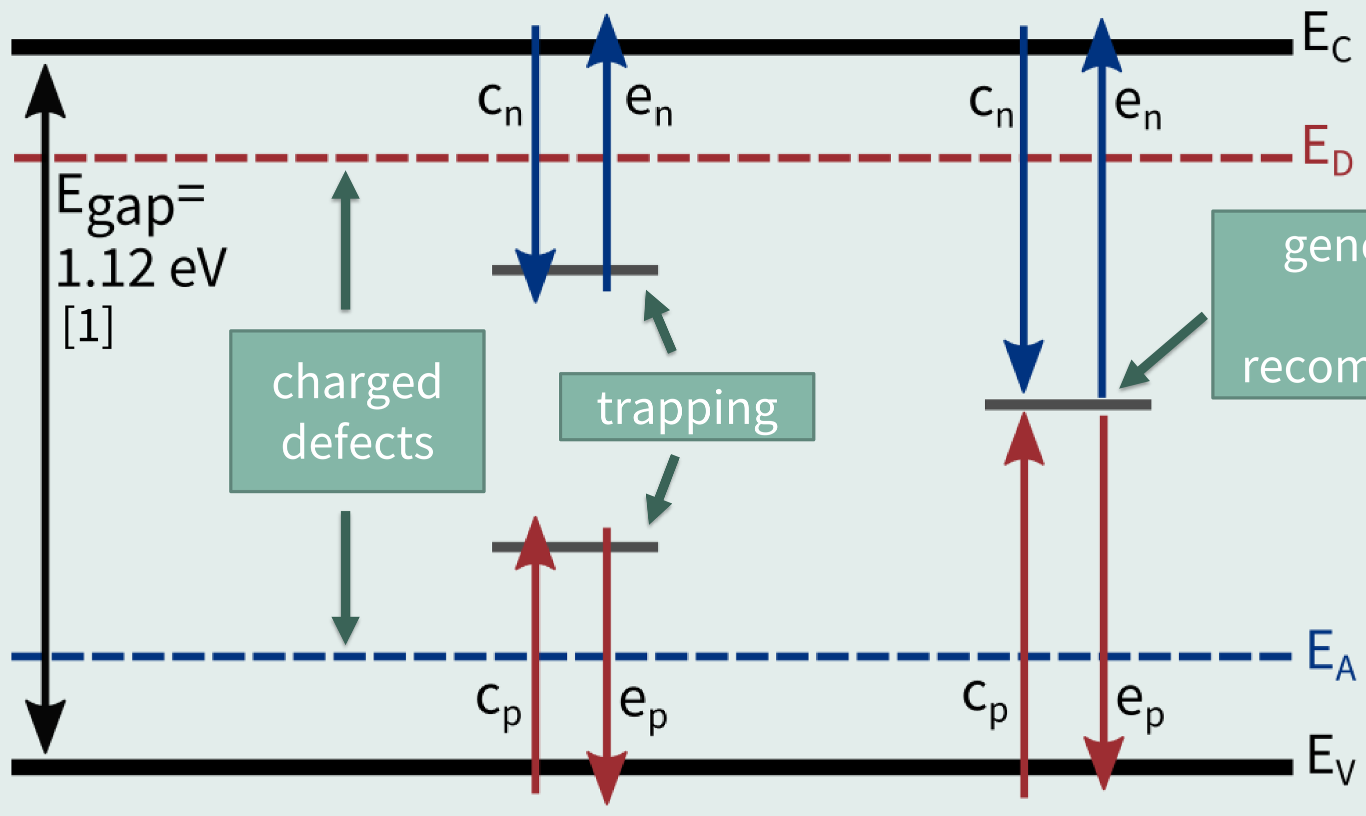
Defects in crystals

1. Vacancies
2. Interstitials
3. Substitutionals



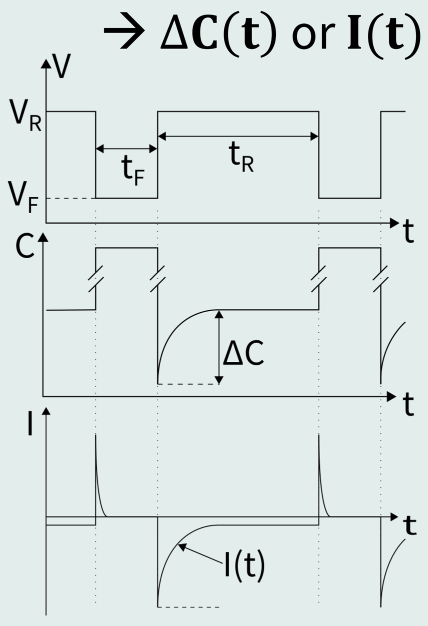
→ Influence device parameters, e.g. charge carrier concentration (n,p), carrier lifetime, …

Additional levels in Bandap

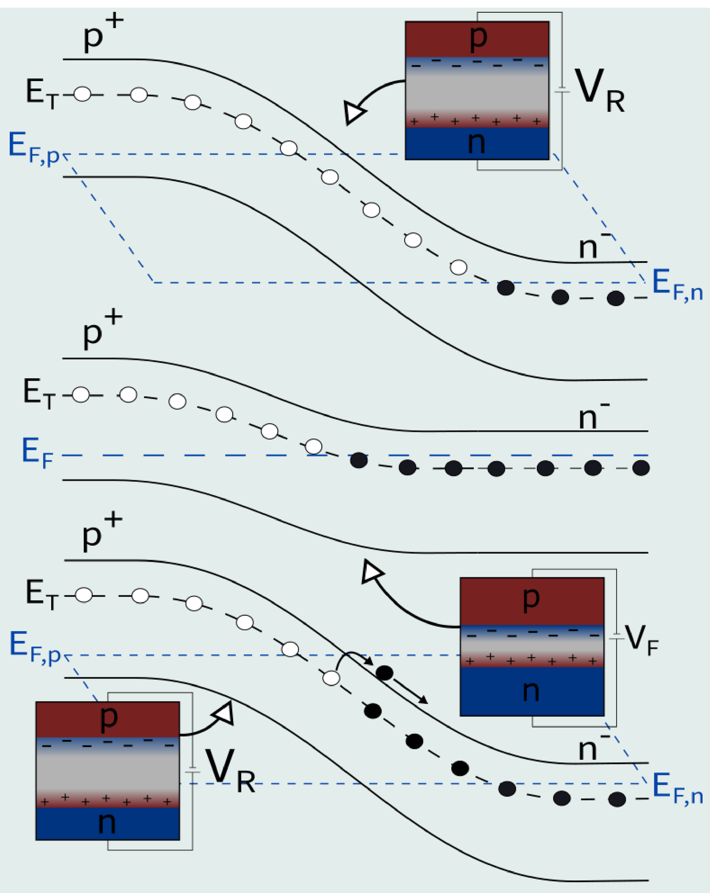


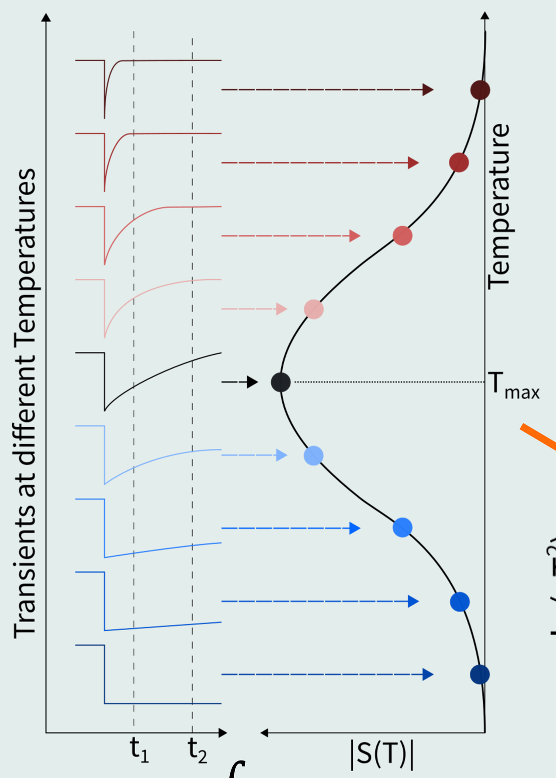
Deep level transient spectroscopy (DLTS)

1. $\mathbf{V = V_R}$: Sets width of depletion-layer (measured volume)
2. $\mathbf{V = V_F}$: Filling of deep traps
3. $\mathbf{V = V_R}$: Deep traps emit captured carriers → $\Delta\mathbf{C(t)}$ or $\mathbf{I(t)}$ is measured



$$\Delta C(t) \propto exp(-t/\tau_e) \quad [2]$$
$$I(t) \propto \frac{1}{\tau_e} \cdot exp(-t/\tau_e)$$
$$Q(t) \propto 1 - exp(-t/\tau_e)$$





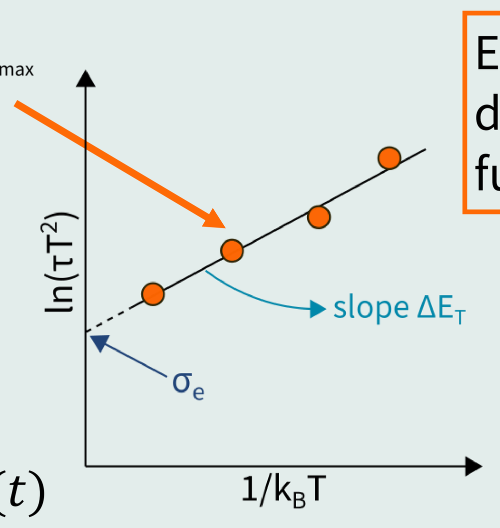
$$S(T) = \int dt\, C(t) \cdot w(t)$$

Trap characteristics (ΔE_T and σ)

Arrhenius plot:

$$ln(\tau T^2) = \frac{\Delta E_T}{k_B T} - ln(N_C v_{th} \sigma_e) \quad [3],[4]$$

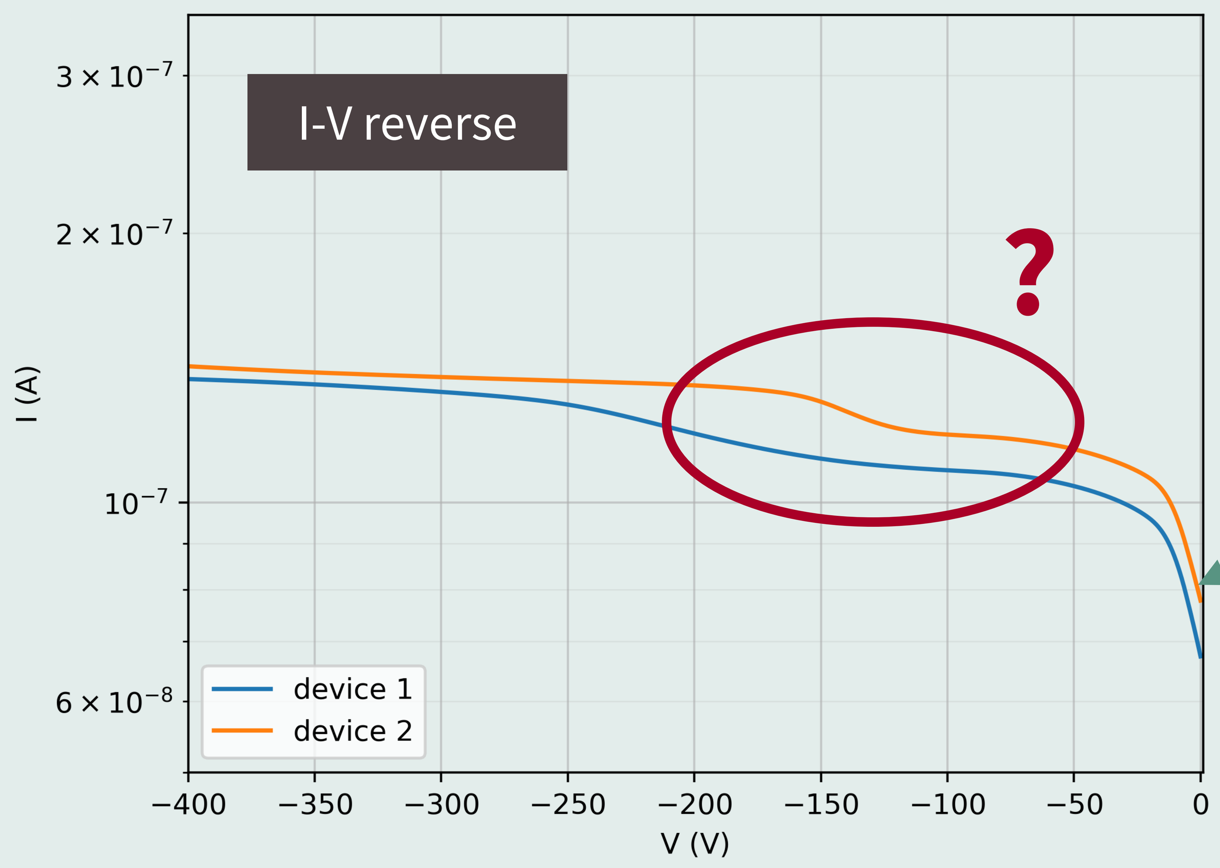
Evaluation with different weigth functions $w(t)$

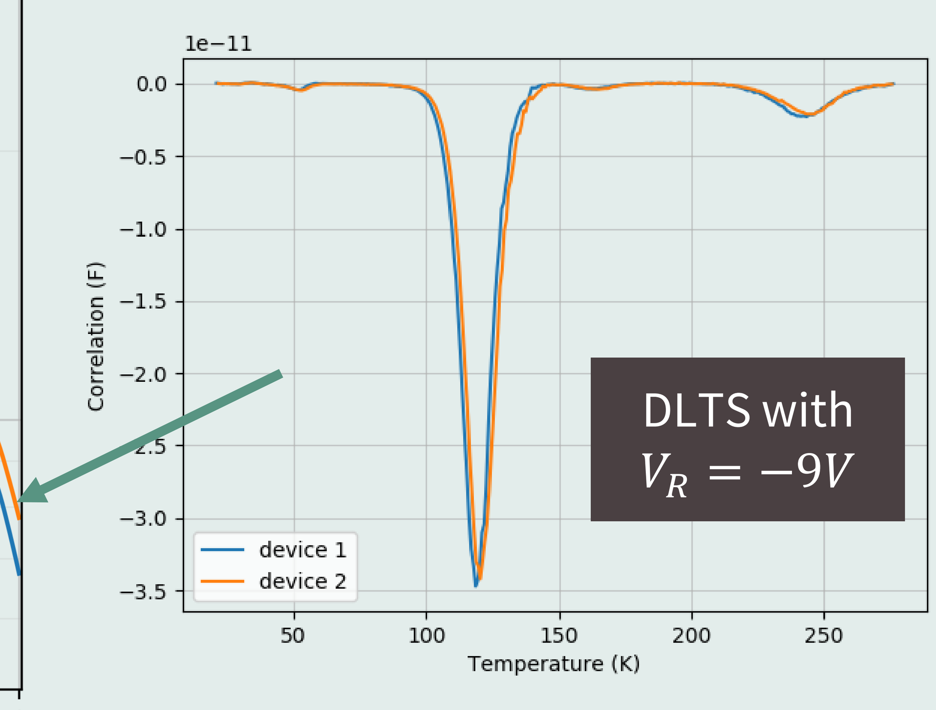


DLTS with high voltages

Motivation:
Characterize defects located deep inside the space charge region
Depdth profile

Challenges:
C becomes smaller for higher V, since $C \approx \frac{\varepsilon_{Si} A}{W}$ and $W \uparrow$ for $V \uparrow$
→ difficult to measure small C
→ **I-DLTS**





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[1] http://www.ioffe.ru/SVA/NSM/Semicond/Si/bandstr.html
[2] J. A. Borsuk et al., „Current Transient Spectroscopy: A High-Sensitivity DLTS System“, IEEE Transaction on electron devices, Vol. ED-27, No. 12, December 1980
[3] D .V. Lang, „Deep-level transient spectroscopy: A new method to characterize traps in semiconductors“, Journal of Applied Physics, Vol. 45, No. 7, July 1974
[4] W. Schockley et al., „Statistics of the Recombinations of Holes and Electrons“, Physical Review, Vol. 87. No. 5, September 1952

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Device Characterization

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Dominik

Ostermaier
Clemens

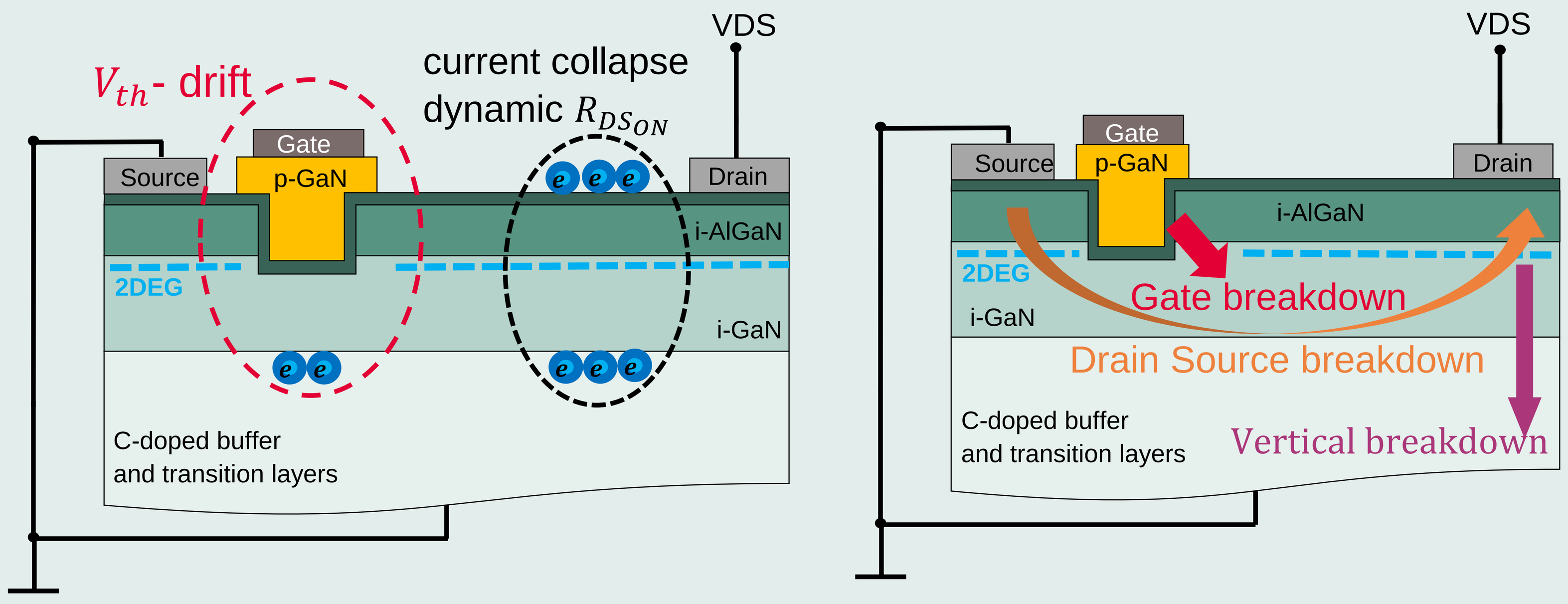
Understanding the role and impact of holes in epi-based degradation mechanism in GaN devices

Introduction

Widebandgap semiconductors benefit from their large bandgap and are therefore less sensitive to high electric fields.

However, in an electron majority carrier device as GaN HEMTs, recombination with holes presents an increased challenge due to the wide bandgap and the relatively large energy being released during such events.

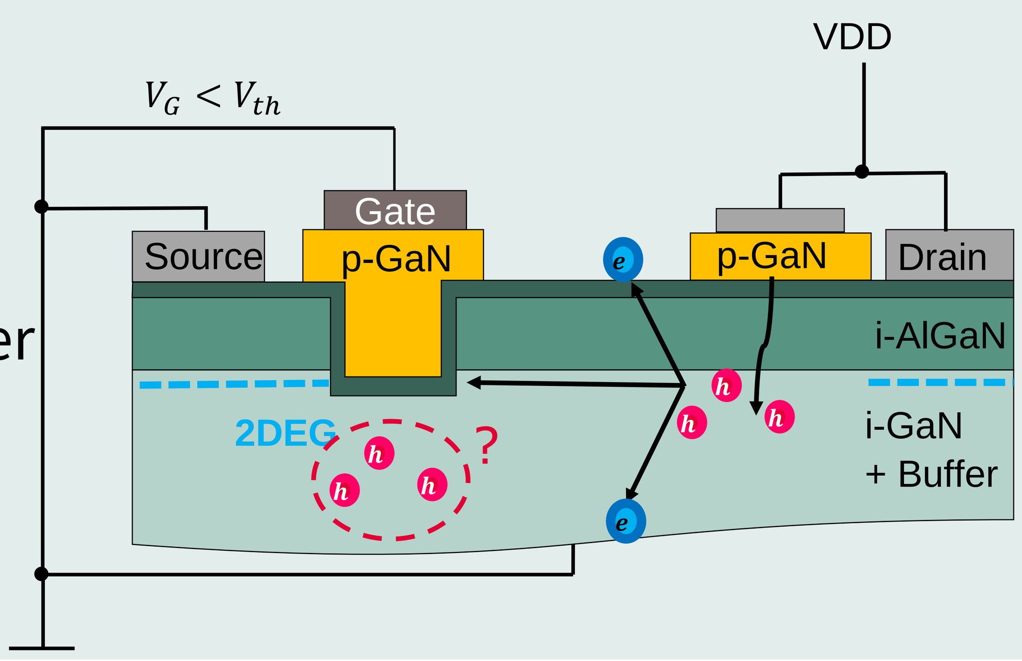
What is the mechanism behind vertical buffer and lateral device degradation and what is the role of holes in it?



Theories

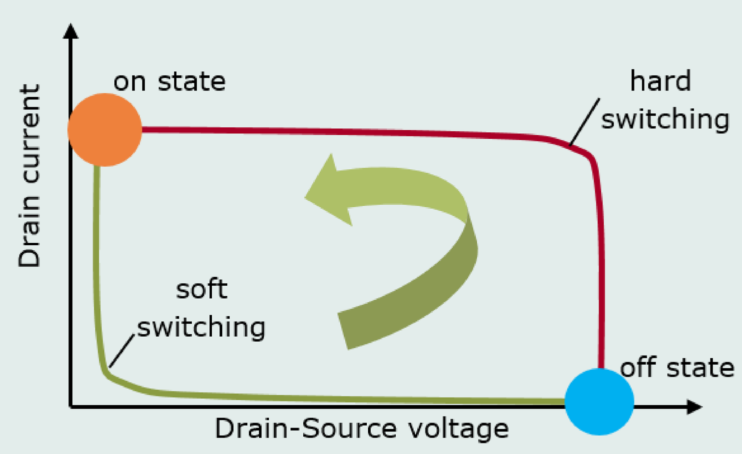
Holes are needed to create a stable device with low $R_{DS_{ON}}$ → Hybrid drain gate injection transistor (HDGIT)

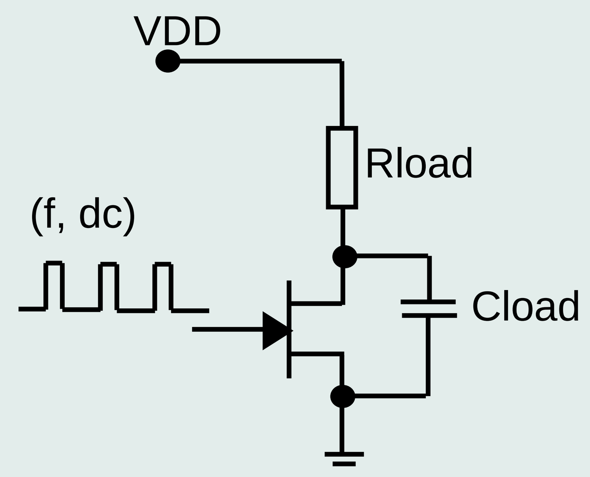
The conduction mechanisms in the various buffer layers are still under debate.



Methodology

DHTOL-Dynamic high temperature operating lifetime test = Repetitive accelerated life time test using hard switching and hot carrier-injection

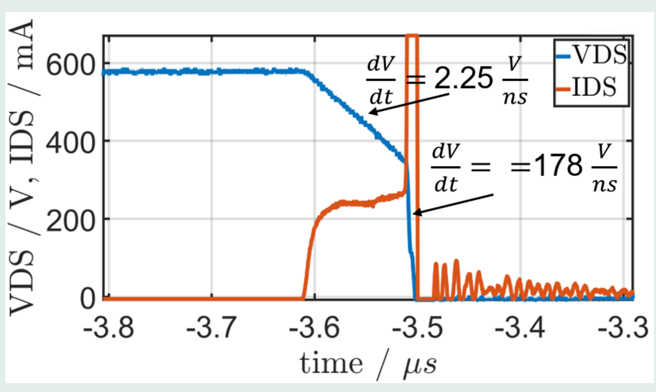


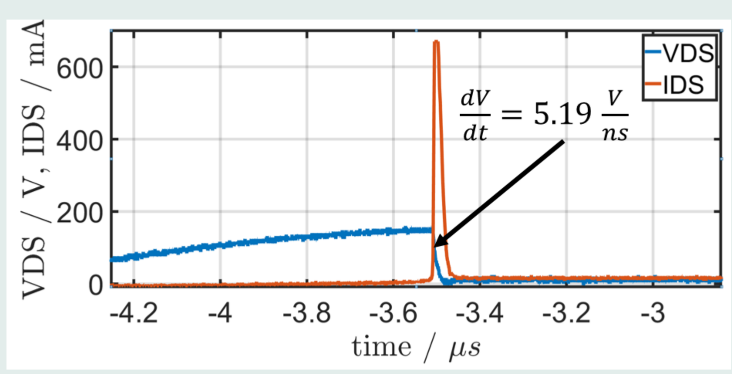


Results

We have clearly observed that pGaN HEMTs are capable of causing a hole induced none-thermal failure mode related to accumulation of minority carrier (=holes).

Two different failure modes with $I > I_{saturation}$





We have a good understanding in process and stress-related factors influencing the main degradation mechansim but the fundamental physical mechanism are still not fully developed and understood.

Next steps:

FBSOA measurements at Infineon and Transmission Line Pulse measurements at TU Wien to monitor device degradation and failure with ns resolution.

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Device Characterization

MATRIX INDEPENDENT QUANTIFICATION OF TRACE ELEMENTS IN POLYMERS USING LASER INDUCED BREAKDOWN SPECTROSCOPY (LIBS)

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Introduction

Conventional determination of the trace metal content of polymers includes complete digestion of the sample. As polymers are usually rather hard to dissolve, the procedure often requires a mixture of various strong acids and oxidants. Subsequently, the trace metal content of the solution is determined using e.g. liquid ICP-MS or ICP-OES measurement. As this approach reveals only the bulk trace metal content and is very laborious and error prone, direct solid-sampling methods are of great interest to determine the trace metal content in polymers.
In this work, we demonstrate the capabilities of laser induced breakdown spectroscopy (LIBS) combined with multivariate data evaluation strategies for matrix independent quantification of trace metals in polymers.

Experimental

Polymer Standards Preparation:

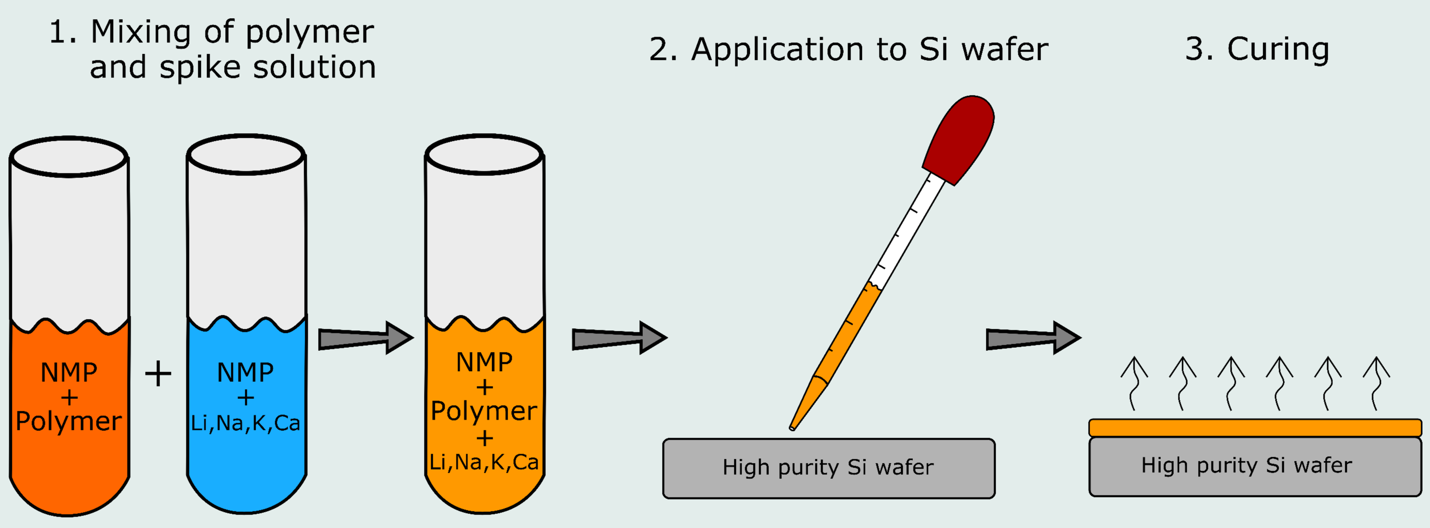

Figure 1: Schematic sample preparation procedure

LIBS Analysis:

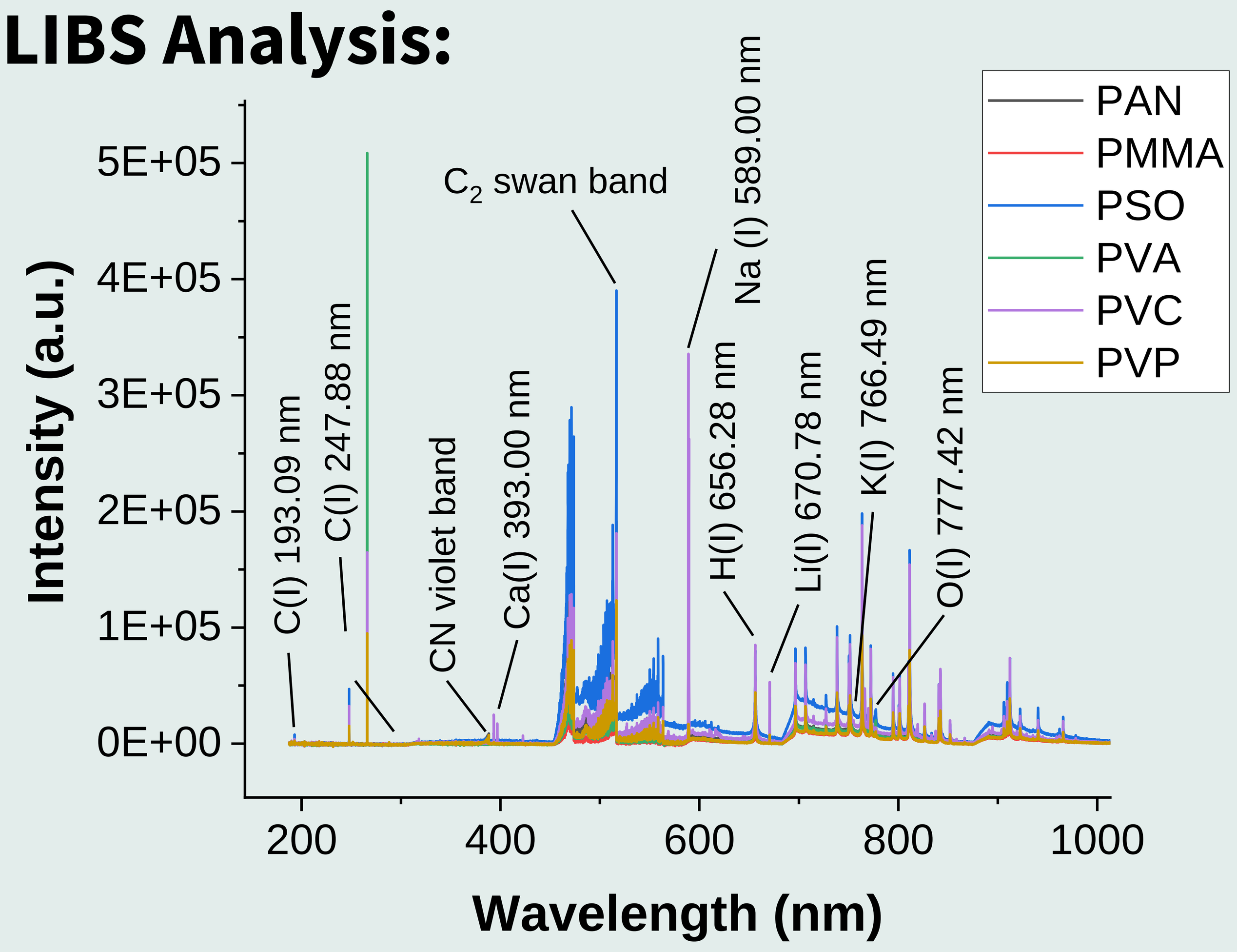

Figure 2: Representative LIBS spectra for the 6 investigated polymers with marked emission signals used for data evaluation

Results

Univariate Calibration Li:

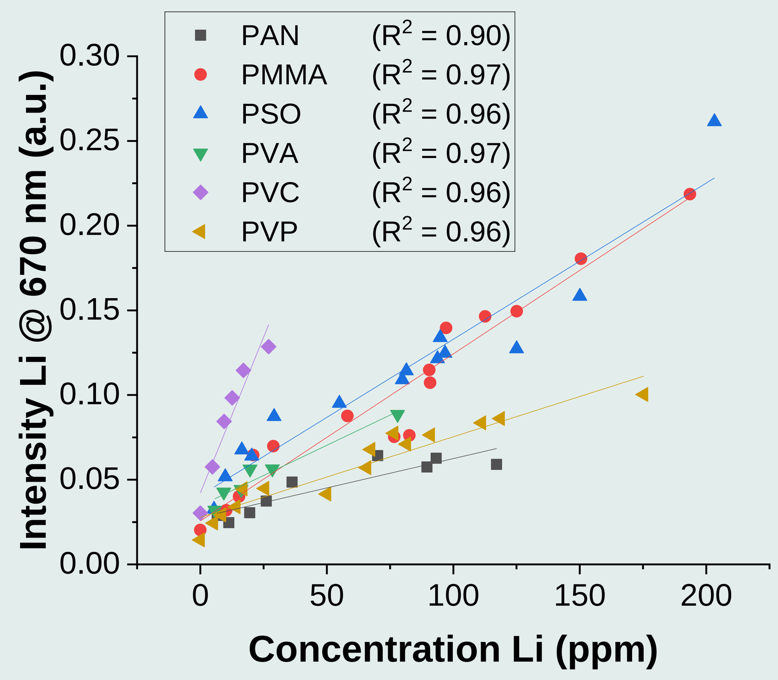

Figure 3: Univariate calibrations for Li of the 6 investigated polymers

Different slopes → matrix effects

Multivariate Calibration (PLS):

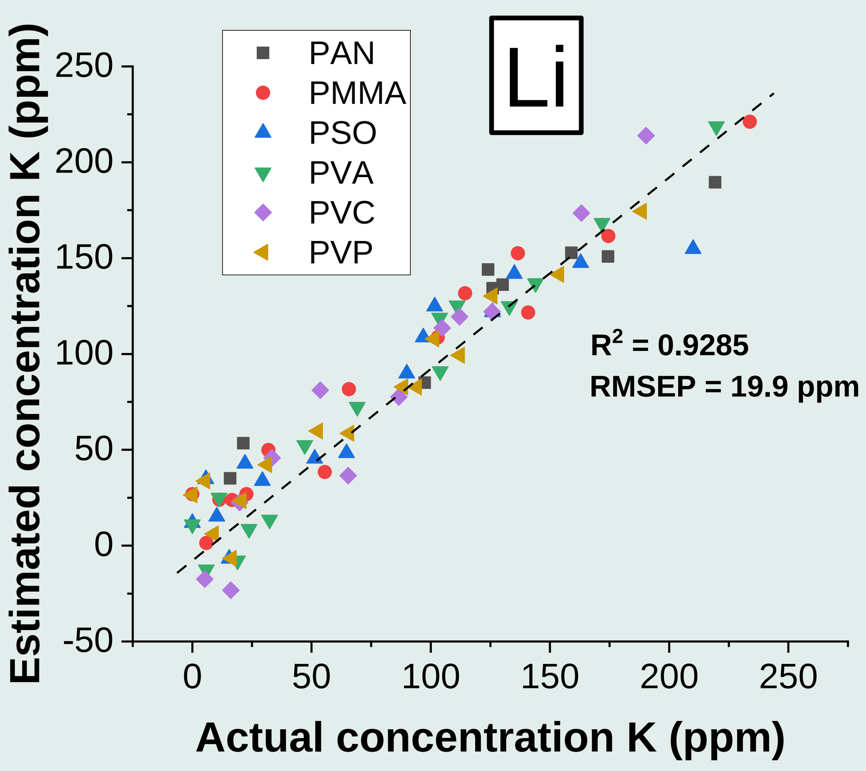

Figure 4: Actual concentration vs estimated concentration of the PLS model for K

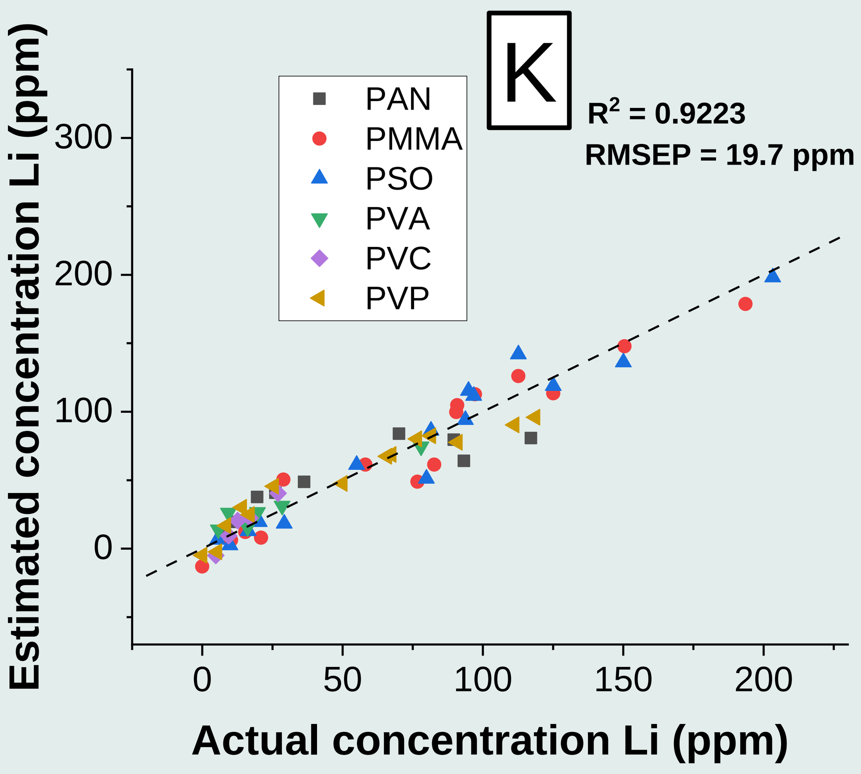

Figure 5: Actual concentration vs estimated concentration of the PLS model for Li

Multivariate model eliminates matrix effects and allows for quantification in unknown polymers

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TECHNISCHE UNIVERSITÄT WIEN

Device Characterization

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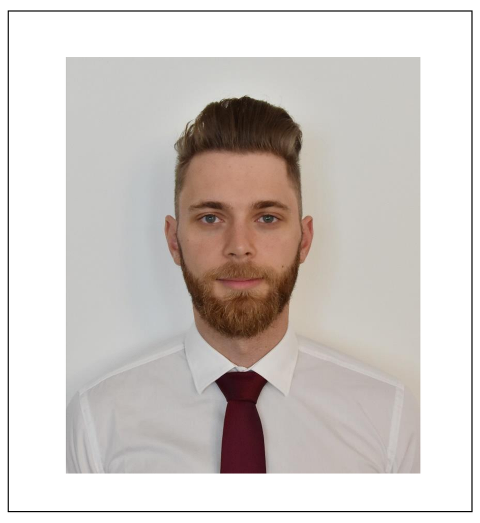
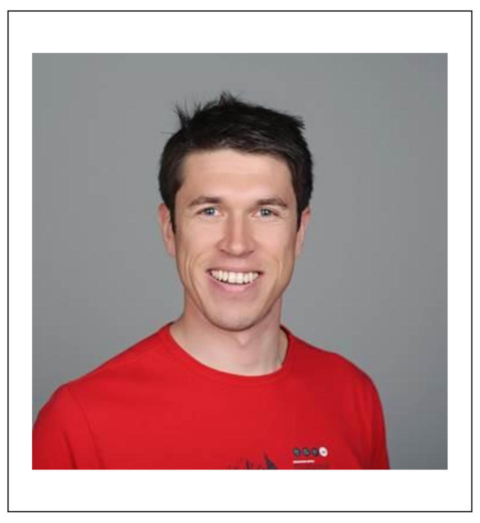
Gregor Pobegen



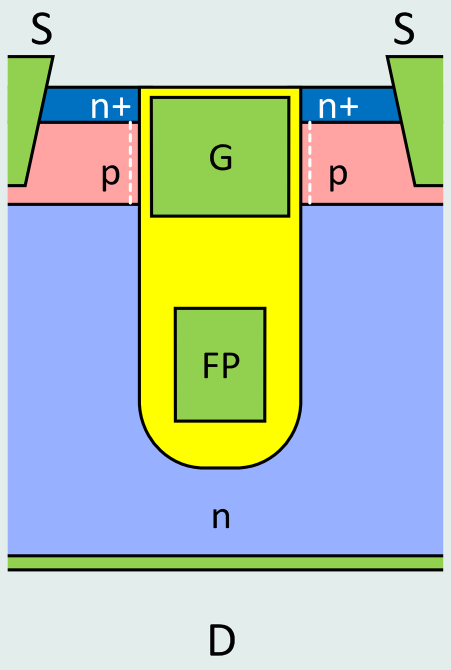


Degradation of silicon trench MOSFETs in repetitive avalanche breakdown

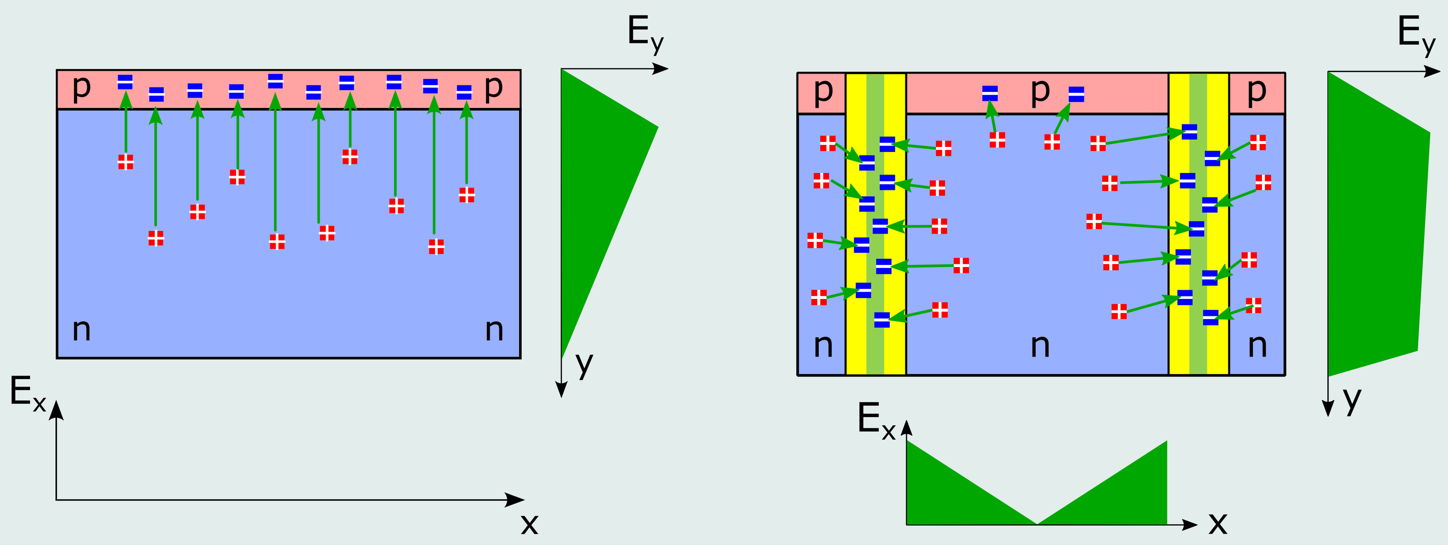
The device

Low voltage n-channel power MOSFETs
(V_{bd} between 25-40V)
Compensated trench design
Field Plate (FP) shorted with source

Application: DC-DC converters
Fast switching (~500kHz)

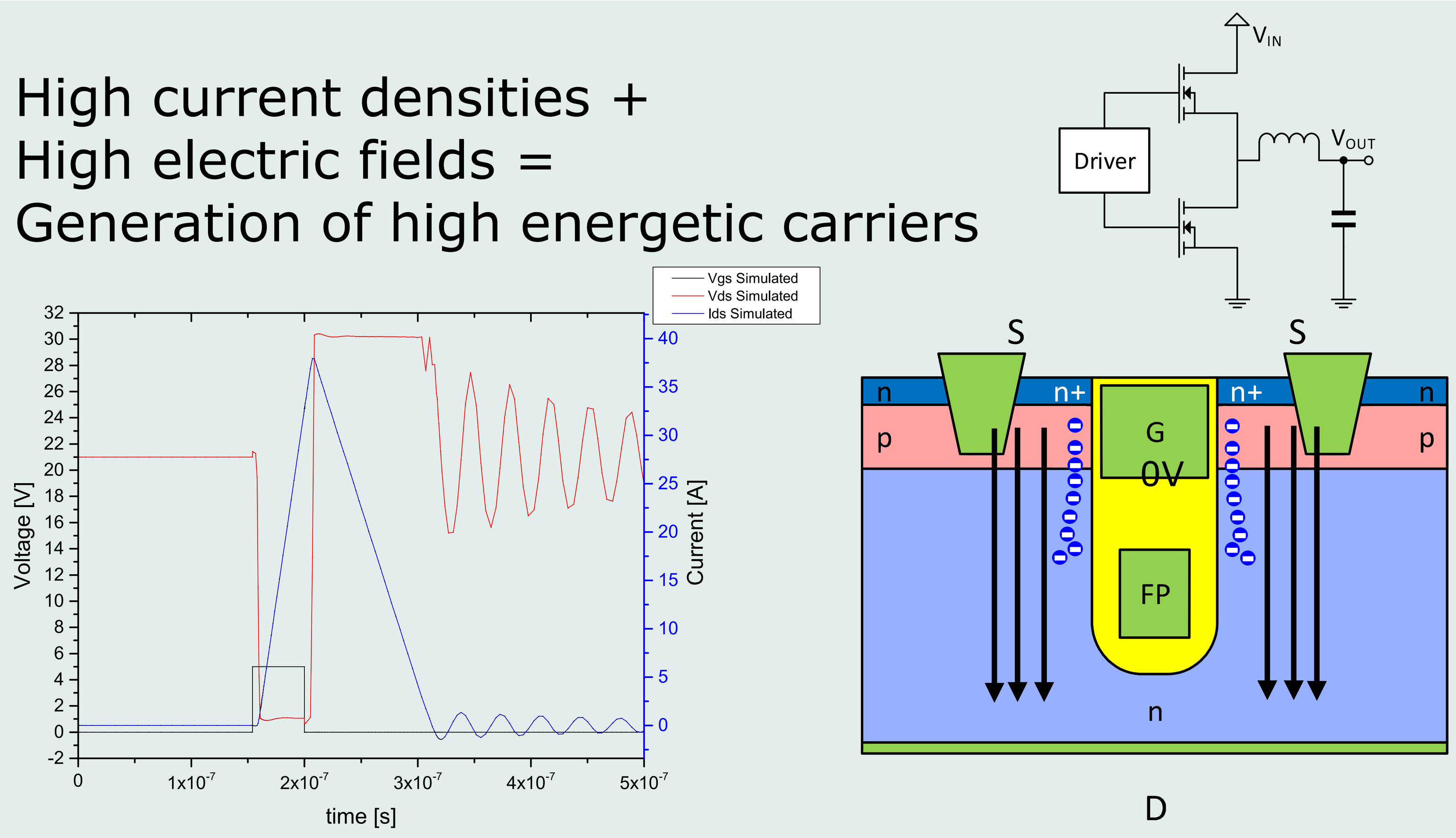


Compensation Principle (Field Plate)



Avalanche Breakdown Hard Switching

High current densities +
High electric fields =
Generation of high energetic carriers

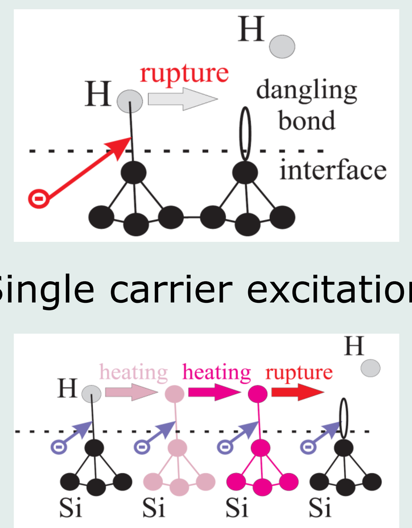


Degradation Mechanism: Hot-Carrier degradation

Si: crystalline, SiO2 : amorphous
↳ no crystalline match
interface with dangling bonds

Passivation with H

Impact of high energetic carriers:
↳ H-Bonds broken
Dangling bonds reestablished

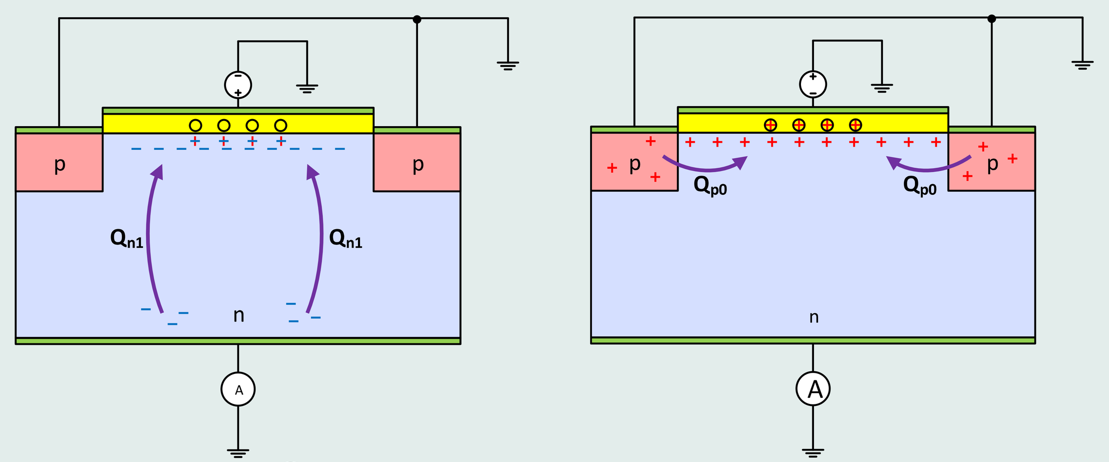


a) Single carrier excitation

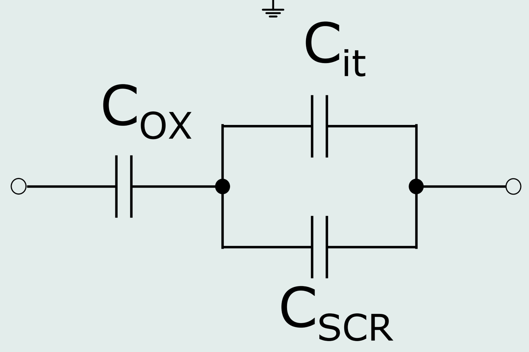
b) Multi carrier excitation

Broken passivated H-bond
(from [Tyaginov 2012])

Measurement methods



Charge Pumping



$$C_{it}(\Psi_s) = \frac{C_{OX} \cdot C(\Psi_s)}{C_{OX} - C(\Psi_s)} - C_{SCR}(\Psi_s)$$

Capacitive Method

MOS Model

Goal

Main parameters affected

- BV_{DSS} - V_{th} - C_{OSS} – I_{DSS}

Understanding complex degradation

- Improvement of reliability / lifetime estimation
- Improvement of efficiency

Technology-independent understanding of trench devices

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Device Characterization

Jakob Willner

Silvia Larisegger

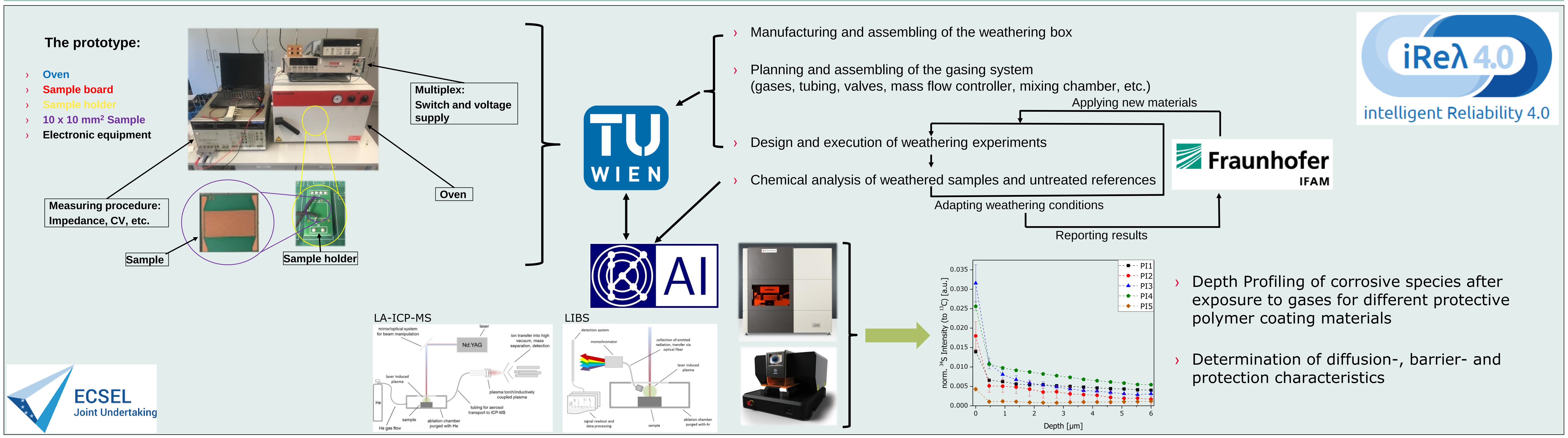
Development of a **M**ixed **F**lowing **G**as system for accelerated aging of protective polymer coatings to stimulate atmospheric corrosion with in-situ electrochemical measurement and subsequent laterally resolved chemical analysis

Introduction

- Product failure of chip-package-board/systems due to corrosion causes immense costs for manufactures and customers each year.
- Improvement of the reliability of products by gaining knowledge of failure mechanisms and hence possibilities to improve critical components and materials is a huge benefit regarding the value chain of the overall industry.
  - ➢ Therefore, accelerated aging procedures and detailed analysis methods are required.

This dissertation focuses on the development of a mixed flowing gas system (MFG) for accelerated simulation of atmospheric corrosion effects on electronic devices on a material base.
With varying critical parameters (Gas mixture and concentration, relative humidity, temperature,…) to exposed samples, the characteristics of different protective polymers and polymer-metal interfaces will be explored using in-situ electrochemical measurement methods (e.g. EIS, CV,…) as well as subsequent chemical analysis (LA-ICP-MS, LIBS, XPS,…)

Methodology



Status and next steps

- First prototype of the MFG system is soon ready to use for the weathering of test samples.
- Characteristics of the weathering chamber (homogeneity,…) will be determined using suitable dummy samples (bare metal surfaces).
  - ➢ Based on the results, if necessary, the setup will be further improved
- In the next project phase, samples received from Fraunhofer IFAM will be weathered and characterized
  - ➢ Reporting to Fraunhofer IFAM enables the specific change of target components, leading to an optimization of the protection properties of new materials

- Meanwhile the method development for chemical analysis (**L**aser **A**blation – **I**nductively **C**oupled **P**lasma – **M**ass **S**pectrometry and **L**aser **I**nduced **B**reakdown **S**pectroscopy) is in progress.
- First goal is the depth resolved, quantitative determination of the sulfur uptake in different protective polymer coating materials after exposure to H_2S and SO_2.
  - ➢ Enables the understanding of barrier- and diffusion characteristics for corrosive species in polymer coatings

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	Thomas Augustin	

TECHNISCHE UNIVERSITÄT WIEN

Chip Design

Markus Haberler

Christoph Steffan

EMI Robustness of Three-Electrode Electrochemical Sensor Front-Ends

Introduction

Sensors are the first element in a signal chain and in order to fulfill their function they often have to be placed in close proximity to the measured object and substance. Consequently, a certain amount of wiring is required that is vulnerable to electromagnetic interferences. This is particularly true, when sensors are used that exploit the electromagnetic field for powering and data-transfer. In this case, the robustness against electromagnetic interferences (EMI) is of fundamental importance since it limits the accuracy of the measurement.

The focus is on three-electrode potentiostats, which are used as a front-end for electrochemical sensors. A potentiostat consists of two operational amplifiers that are operated in a negative feedback configuration to maintain a desired voltage between the electrodes.

The main questions that have to be answered are:

- Are potentiostats susceptible to EMI?
- What are the effects of interferences in potentiostats and how can we minimize them?

Theories

Operational amplifiers in a feedback configuration demodulate EMI, which results in a dc offset [1]. The aim of our analysis is to investigate the properties of the topology shown in Fig. 1 regarding their robustness against RF interferences.

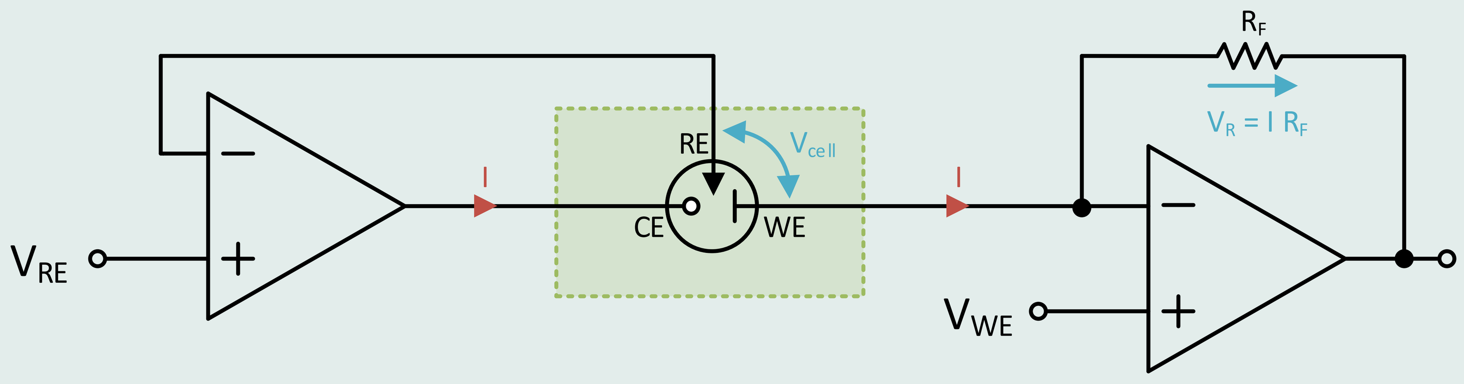
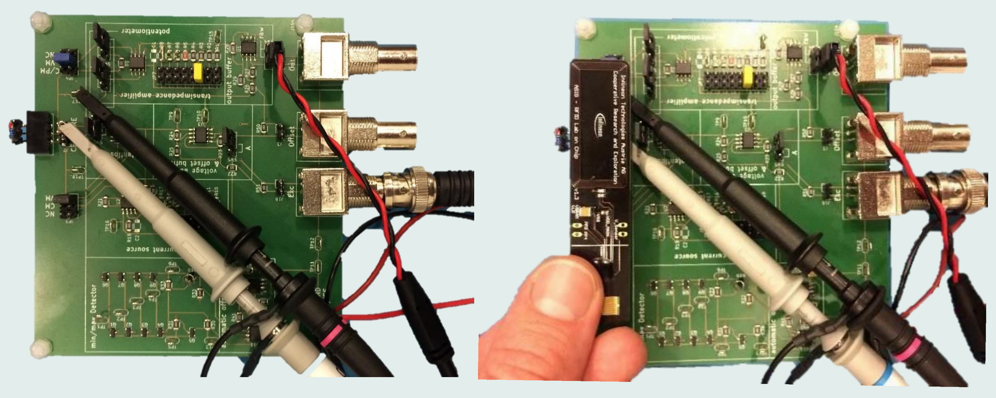


Fig. 1. Block diagram of the electrochemical measurement system.

Methodology

The robustness of the potentiostat against RF interferences was investigated on a non EMI optimized test board shown in Fig. 2. A dc voltage, V_{cell}, was applied to the sensor and the resulting voltage drop at the feedback resistor of the TIA, V_R, was captured.



(a) (b)

Fig. 2. Picture of the measurement setup (a) without / (b) with active NFC field (NFC reader device not shown).

Results

The investigations showed that there is a considerable influence on the resulting voltage drop, V_R, at the feedback resistor of the TIA caused by an active NFC signal. The captured waveforms of the signal at the TIA, V_R, and the applied voltage, V_{cell}, are shown in Fig. 3. The dc offset in the measured signal arose due to the disturbance signal, which drove the amplifiers of the potentiostat in non-linear region. This out-of-band signal led to a dc offset at the input of the amplifiers. Thus, the sensor was excited by an altered voltage V_{cell}, which resulted in a influenced voltage drop V_R.

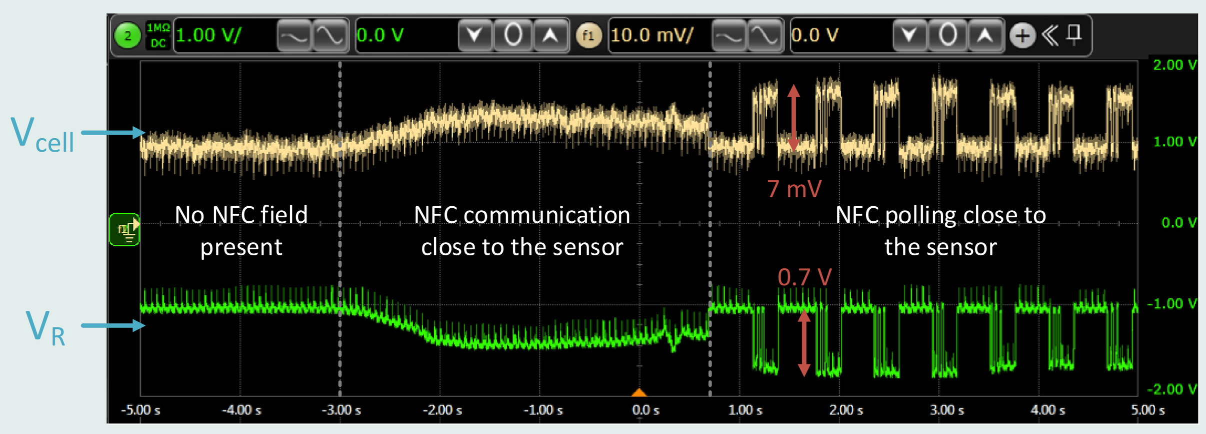


Fig. 3. Measured waveforms of V_{cell} and V_R.

In a future work, suitable countermeasures in terms of circuit techniques and layout optimizations have the be found to improve the inherent robustness of the sensor front-end against EMI.

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References

[1] F. Fiori, Design of an operational amplifier input stage immune to EMI, IEEE Trans. Electromagn. Compat., vol. 49, no. 4, pp. 834–839, Nov. 2007.

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Sub-Microwatt CMOS Rectifier for a Passive Wake-Up Receiver

Introduction

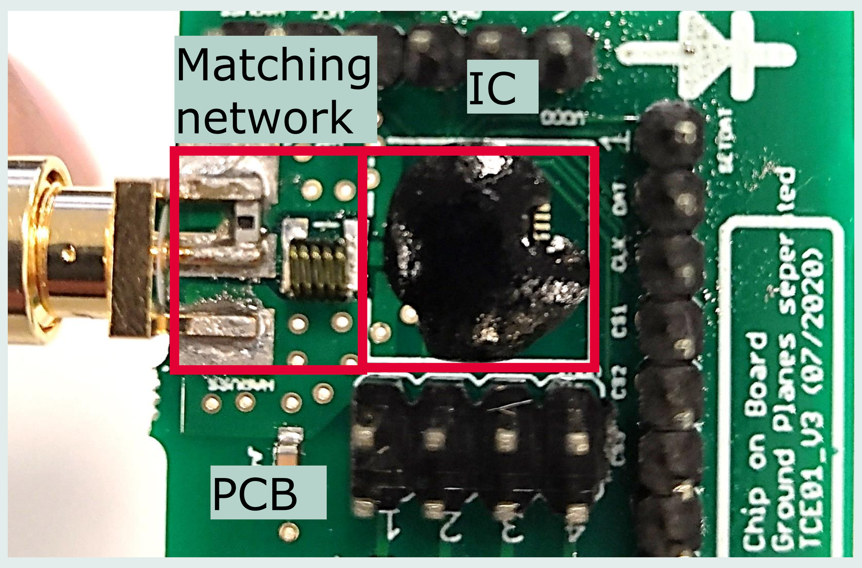
Energy efficient solutions are required in order to sustain the growth of a 1-trillion-node Internet of Things (IoT) by the next decade. Power consumption of the battery operated devices can be reduced to a great extent by using a event-driven wake-up mechanism of a passive wake-up receiver (WuRx). The CMOS rectifier which sits at the analog front-end of the WuRx converts the incoming radio frequency (RF) energy to a direct current (DC) energy.

The communication range of the WuRx depends predominantly on the power conversion efficiency (PCE) and the sensitivity of the CMOS rectifier.

The research focusses on the design of a sub-microwatt CMOS rectifier which can enable a robust passive wake-up receiver with a high communication range.

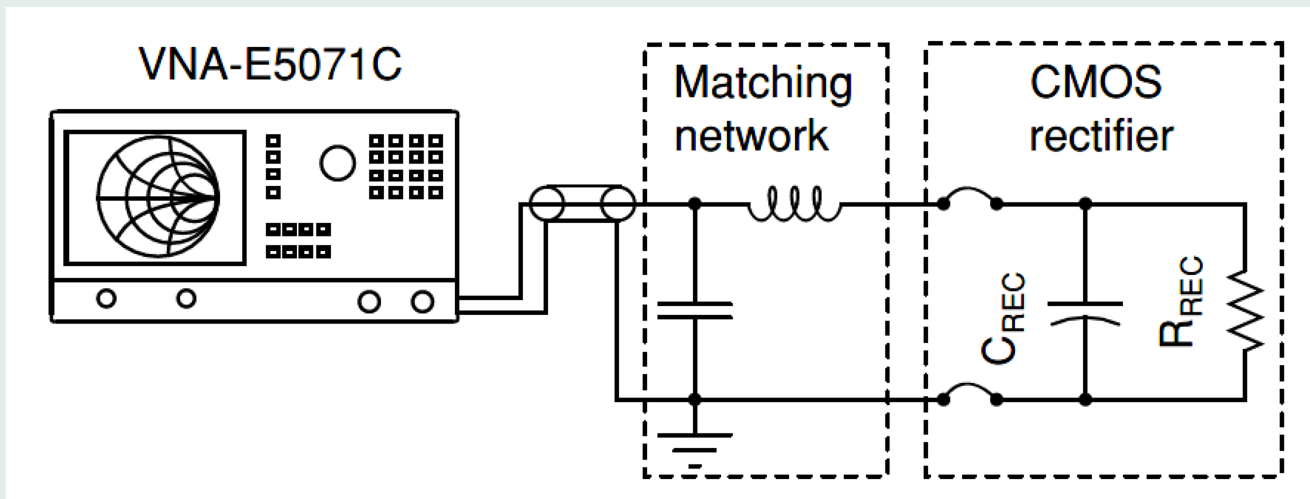
Design

Design in 130 nm CMOS technology. Internal diode precharging methodology boosts the performance at low input power levels.

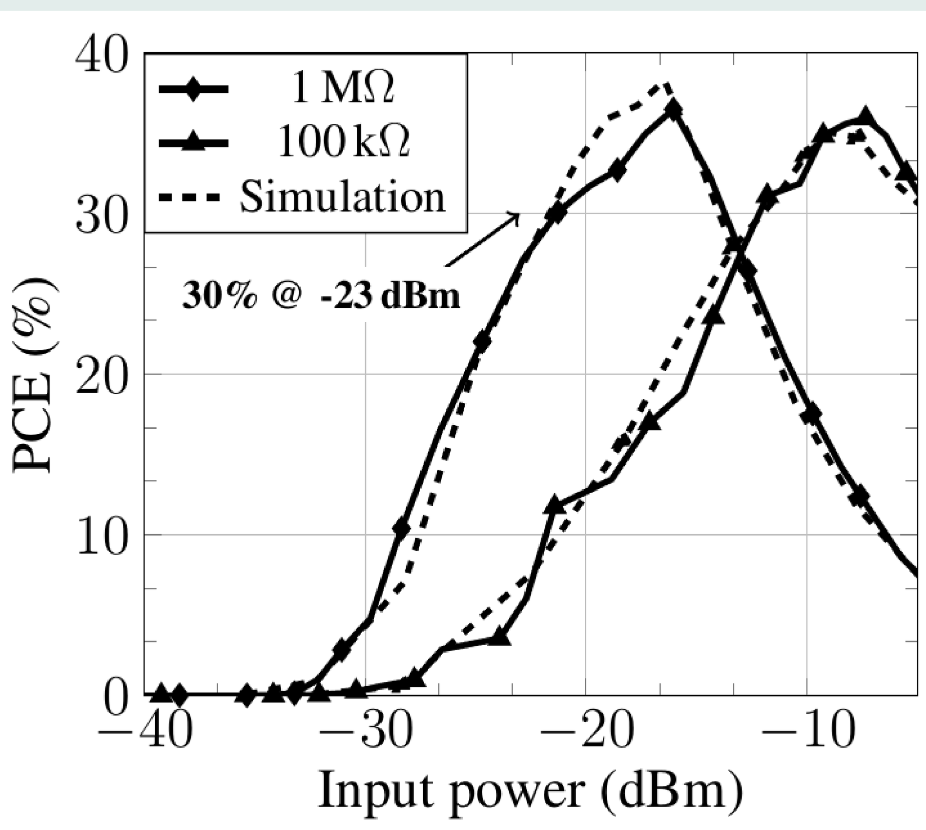


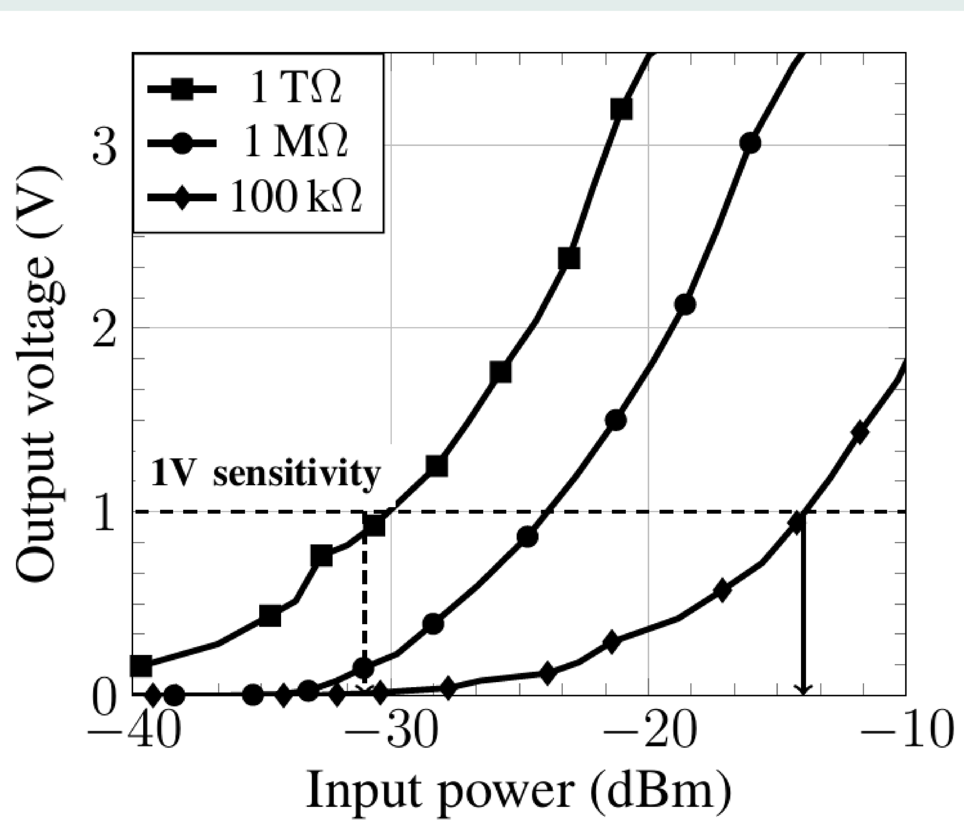
Test Methodology

The CMOS diodes need minimum input voltage level to start up. Matching network boosts the output signal of the vector network analyzer (VNA) to the input of the CMOS rectifier.



Results and Outlook





The CMOS rectifier delivers a good PCE of 30% at input power levels of -23 dBm for a resistive load of 1 MΩ.
Output sensitivity of 1 V is achieved at -31 dBm input power for a purely capacitive load.

The planned passive wake-up receiver will integrate the designed CMOS rectifier. A co-design approach of matching network and CMOS rectifier would further help to optimize the overall power transfer.

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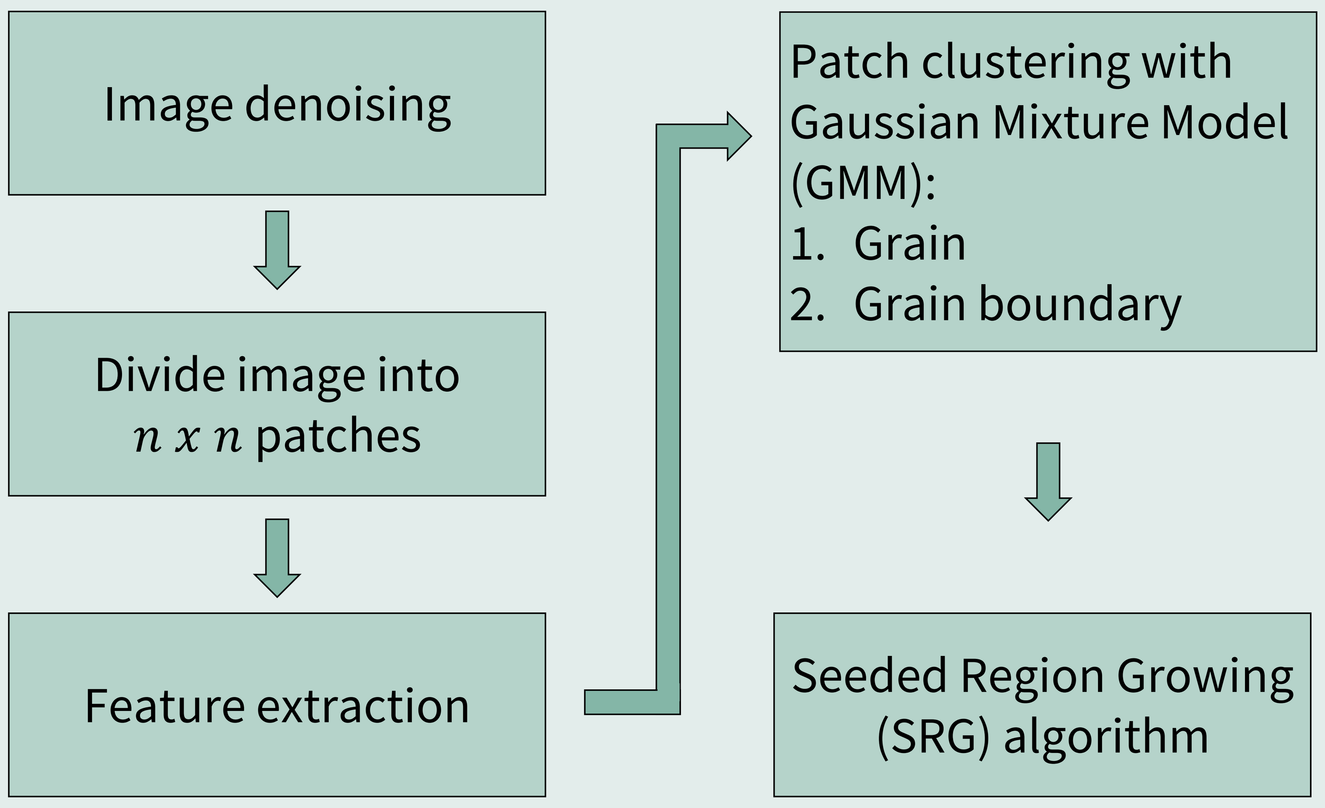
Microstructure Segmentation in SEM & FIB Images

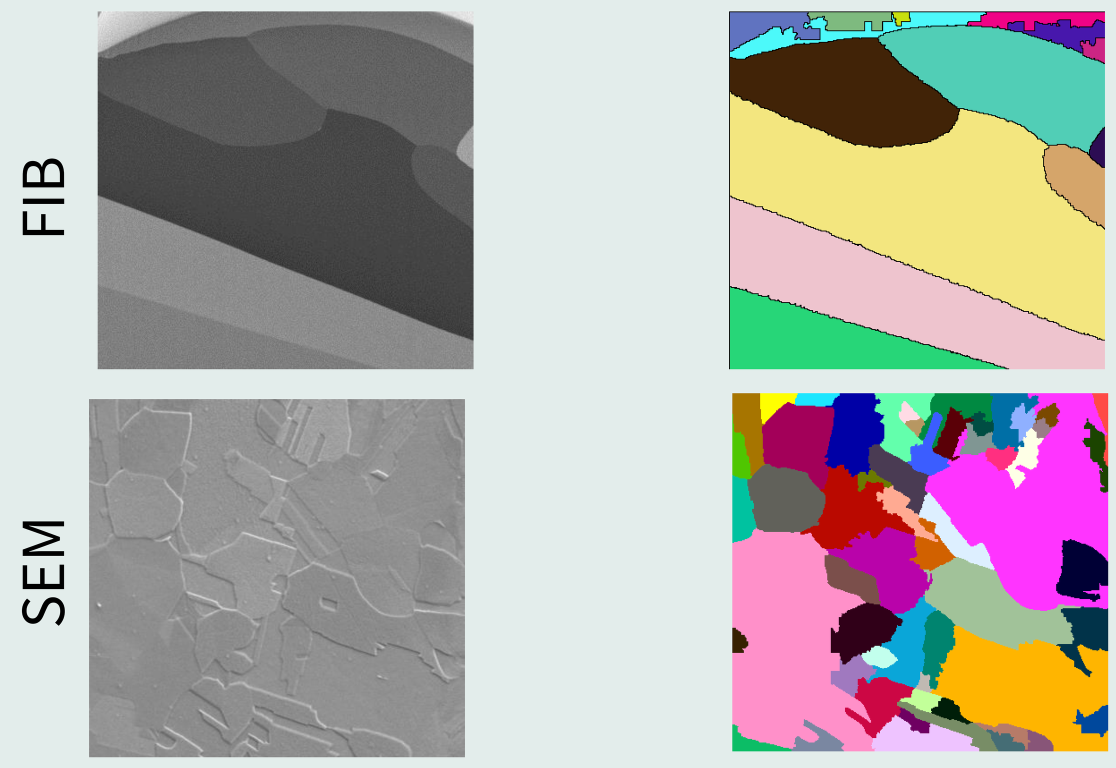
Introduction

- The microstructure defines physical and mechanical properties of a material
- With SEM and FIB the microstructure of a material and the possible changes caused by thermo-mechanical fatigue can be visualized
- An efficient and reproducible segmentation algorithm via advanced image processing and statistical methods is developed to quantify the microstructure of a material via SEM and FIB images

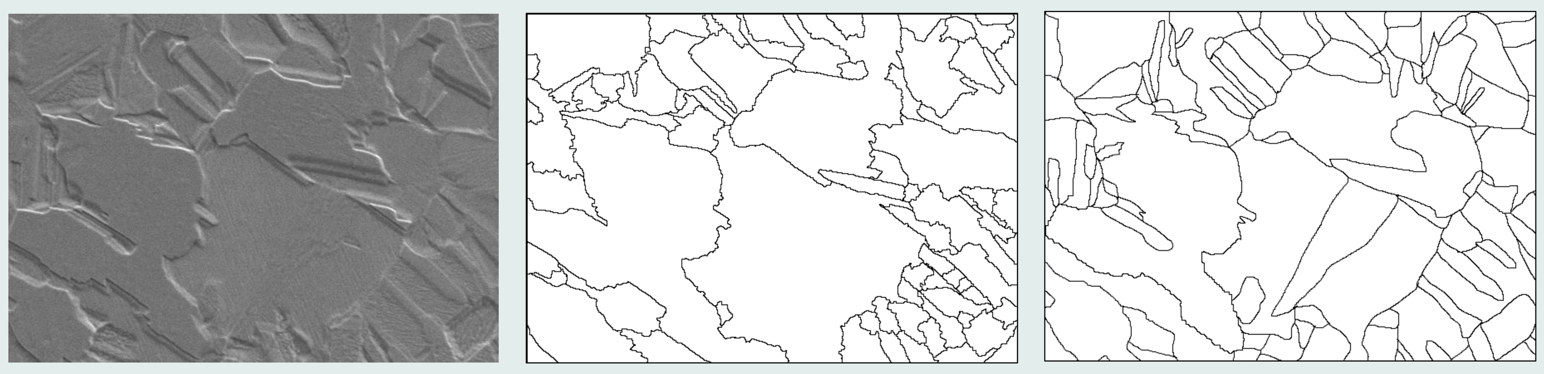
Methodology



Algorithm Output – First Results



Algorithm Evaluation



alg-all-labels-overlap-measurements

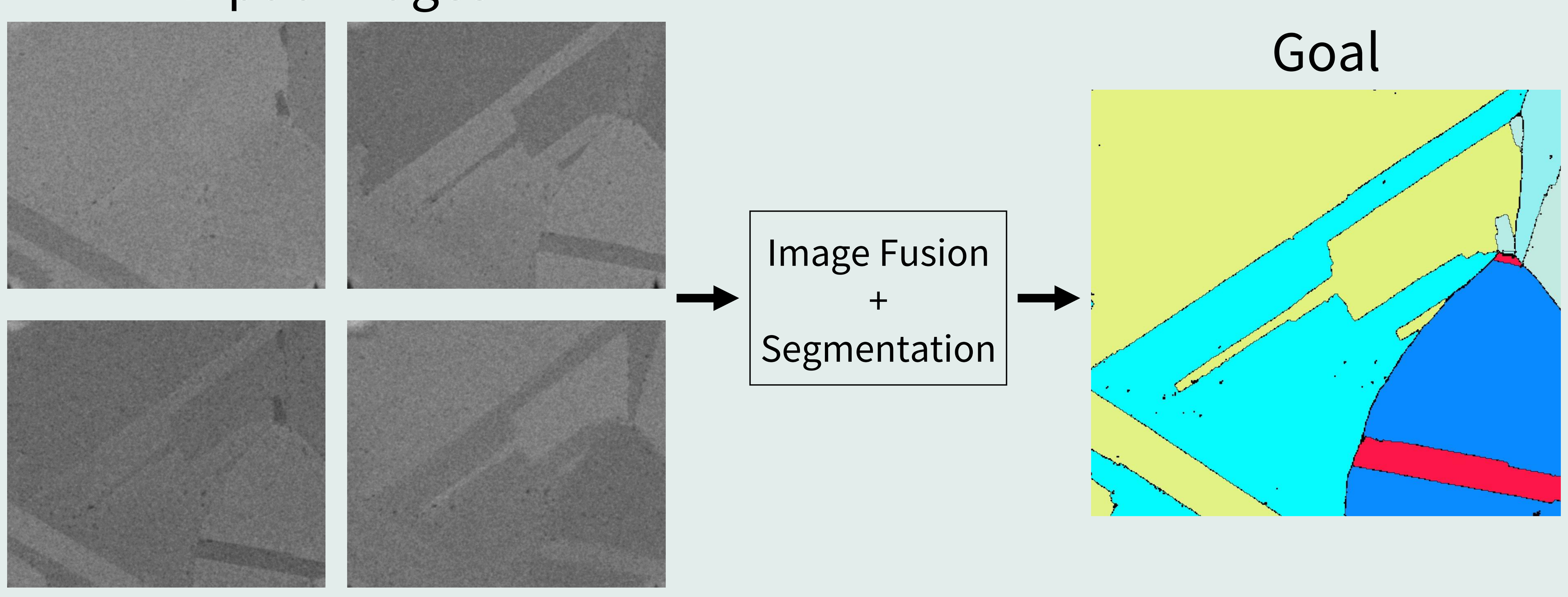
File Edit Font

TotalOverlap	JaccardIndex	DiceCoefficient	VolumeSimilarity	FalseNegativeError	FalsePositiveError
0.647734	0.476601	0.645538	0.006781	0.352266	0.356644

- Problem: Missing grain boundaries in SEM images due to physical reasons

Image Fusion – Theory and Future Work

- Image Fusion - the process of combining information from multiple images into one single image that contains all relevant information
- Application for SEM images
  - The sample is tilted at different angles
  - Each angle visualizes different grains
  - Combine the images' information
- **Goal:** Increase segmentation accuracy



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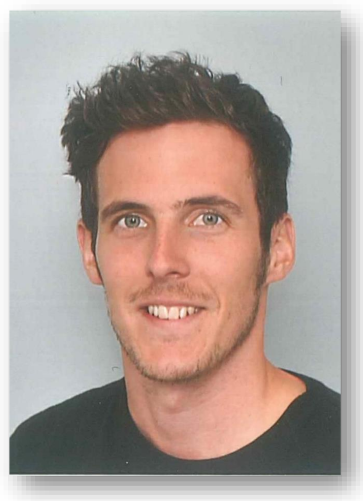


Modular Vehicle Authentication Architecture with Hardware Security Support

Introduction

Identification, or more specifically, authentication is important for any application where permissions need to be checked, or access rights are required to be verified. One example are shared mobility services, which are gaining momentum in recent years. There is an uncontrolled growth of available applications to choose from, resulting in the necessity for registering for each and every new service again.

Research questions:

- What are the requirements for a modular and global available vehicle authentication system?
- How needs the architecture to be designed, in order to cover as many services as reasonable?
- How, and based on which parameters, can such a system be evaluated in regards of security and threads?

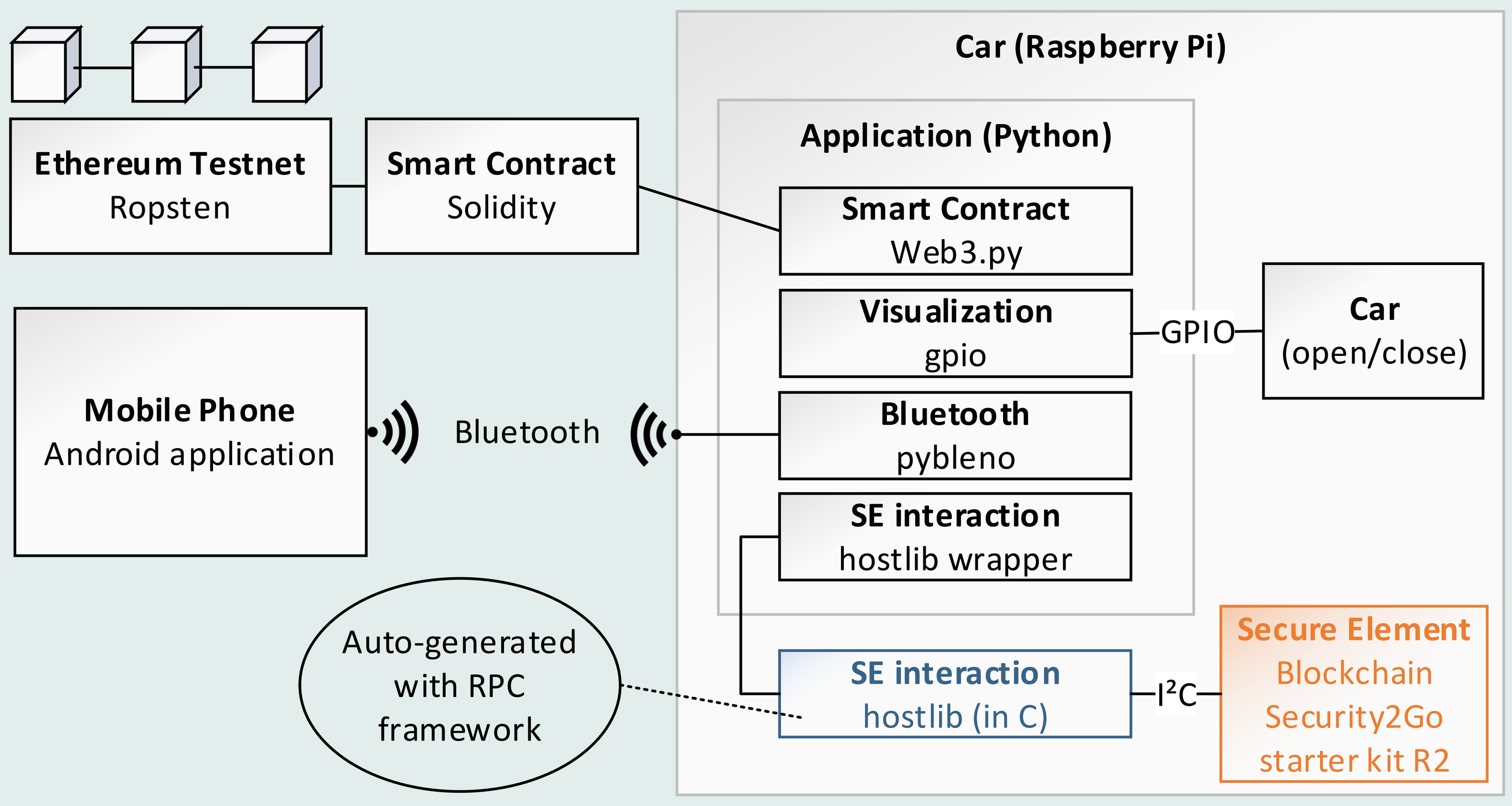
Theories

To tackle the given problem statement, two contrasting concepts can be chosen for designing the architecture:

- Centralized/hierarchical approach
- Decentralized approach

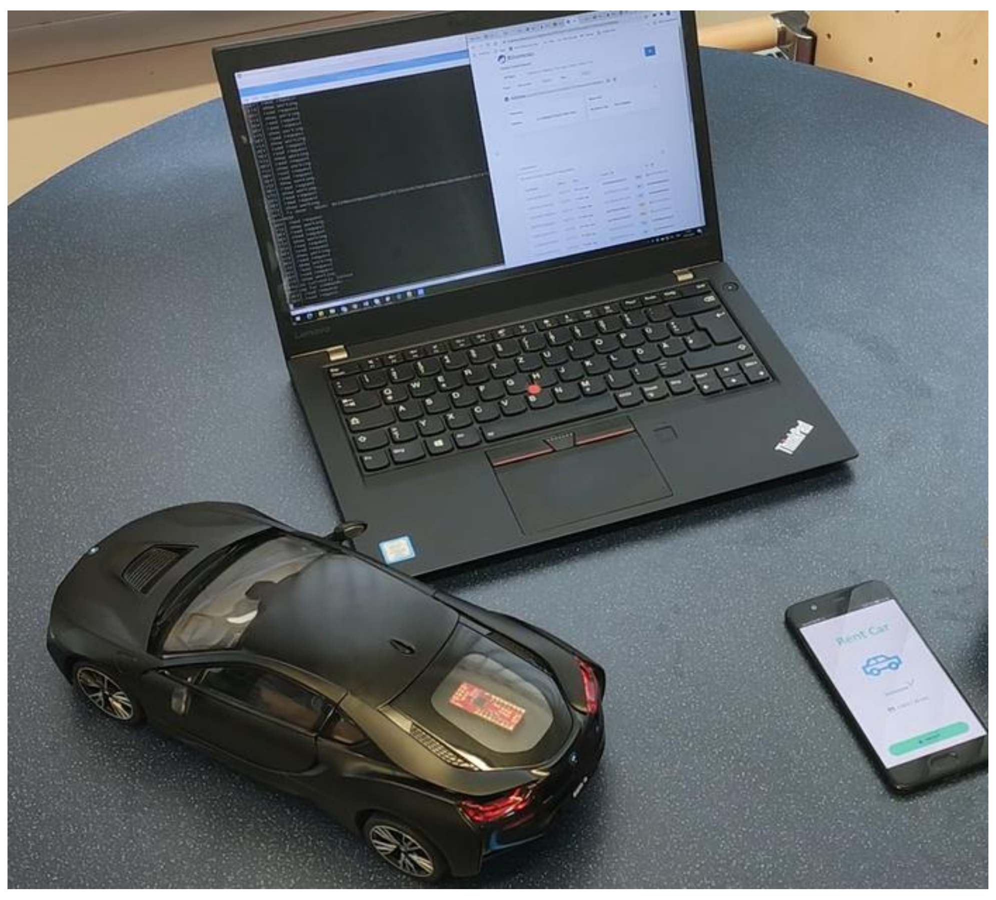
One of the goals is to verify which concept suits best, and how is it possible to combine the strengths of both concepts in the architecture design.

Demonstrator Architecture



Results

A demonstrator for the shared mobility use case was built to proof the concept of a blockchain-based shared mobility platform.
Core of the demo is the *Blockchain Security2Go starter kit R2*, used to securely store key material and sign transactions.



Next steps:

- Adopt to different vehicle types (e.g. drones)
- Follow up on Ethereum 2.0 development (e.g. proof-of-stake)
- 2-factor authentication
- Eliminate weaknesses by combining strengths of central system design (hybrid)

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Application

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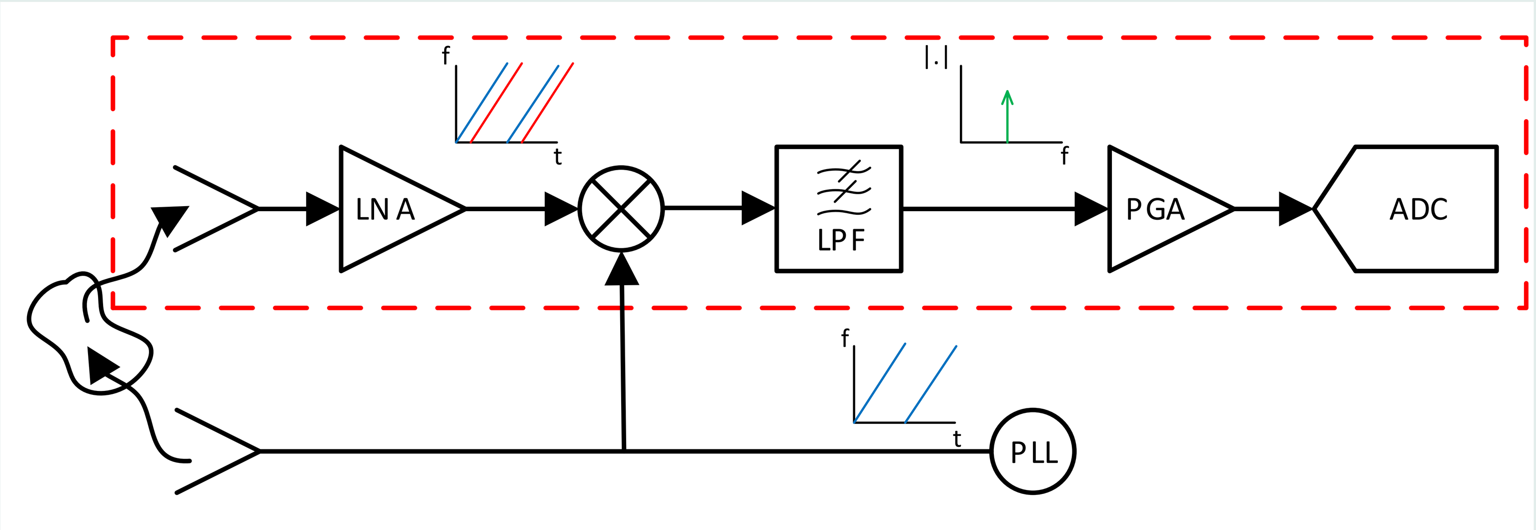
Thomas Bauernfeind

Prof. Mario Huemer



Monitoring Concepts for FMCW Radar Receiver

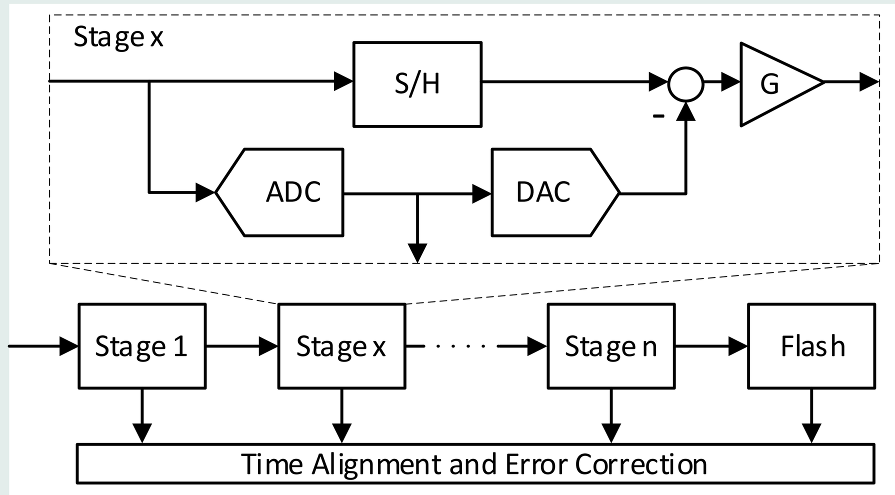
Introduction

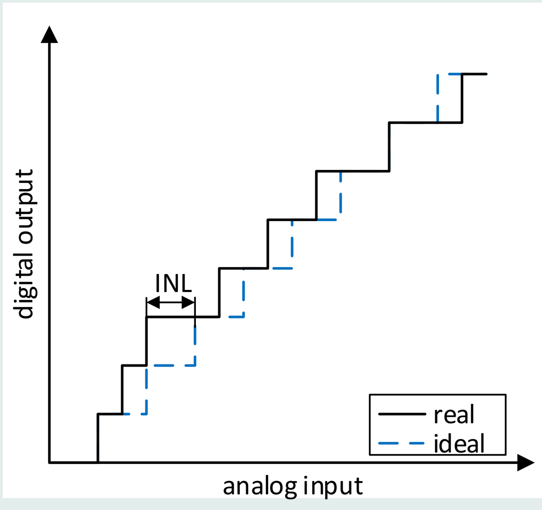


- The non-ideal components in the receive (Rx) path of an FMCW radar sensor may limit the detection performance of the sensor.

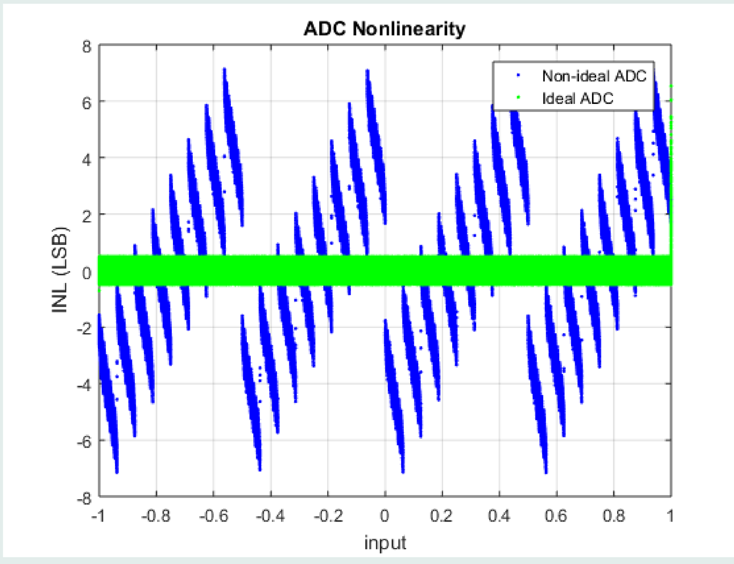
- Monitoring functions are essential to meet the strict safety requirements of modern radar sensors.
- Already available monitoring functions:
  - Rx-gain
  - SNR
  - Rx-corner frequencies
- Currently, these concepts do not include the monitoring of the inherent nonlinearities of specific components, i.e. PGA, ADC.

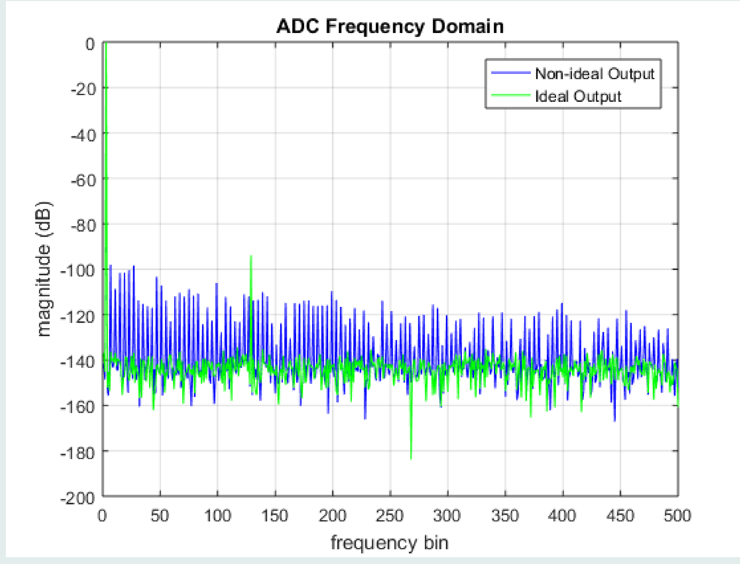
ADC Nonlinearities





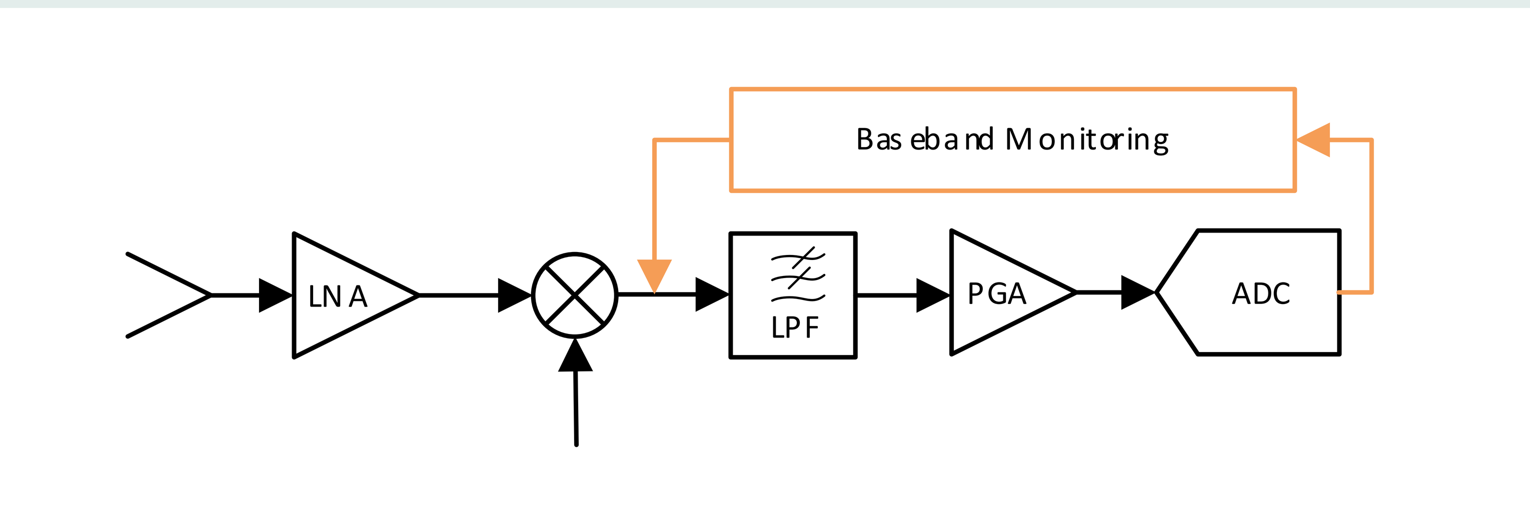
- The integral nonlinearity (INL) is the most prominent ADC nonlinearity.
- Caused by the architecture of the pipeline ADC, the INL is mainly effected by gain as well as capacitor mismatches.





- ADC nonlinearities directly effect the spurious free dynamic range (SFDR).

Objectives



- INL and SFDR monitoring via test signal injection.
- Monitoring function during the radar operation.

Challenges / Future Work

- Challenges of online monitoring:
  - Interference caused by the radar measurement
  - Test signal extraction
- To be monitored in the future:
  - Amplifier nonlinearities in the Rx-path
  - Filter transfer function
- Investigate monitoring concepts on MMIC as well as on system level.

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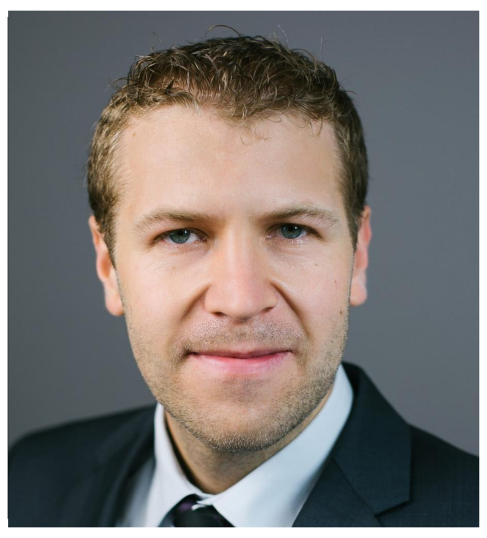
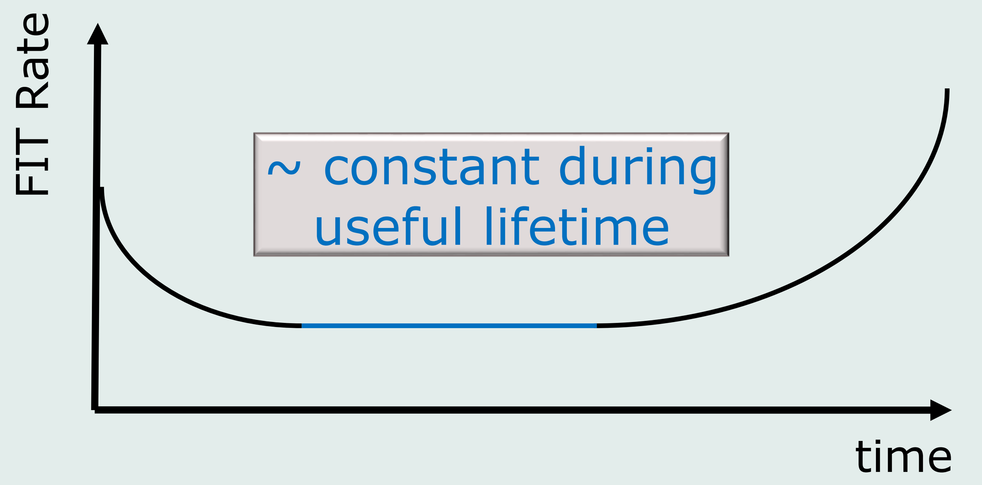


Prediction of FIT Rates with confidence

FIT Rate and Bathtub Curves

A gazillion of ICs, but few failures

The **FIT** (**F**ailure **I**n **T**ime) **Rate** is the
(expected) number of failures
during useful lifetime
within 10^9 total operating hours

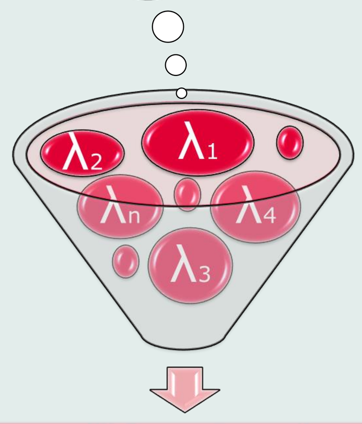


Problem

???

There is no method in use, which
- gives **upper confidence limits**
- applies a **bottom-up estimation**

for FIT Rate determination



$\lambda_{total} = f(\lambda_1, \lambda_2, \lambda_3, \ldots)$

Background

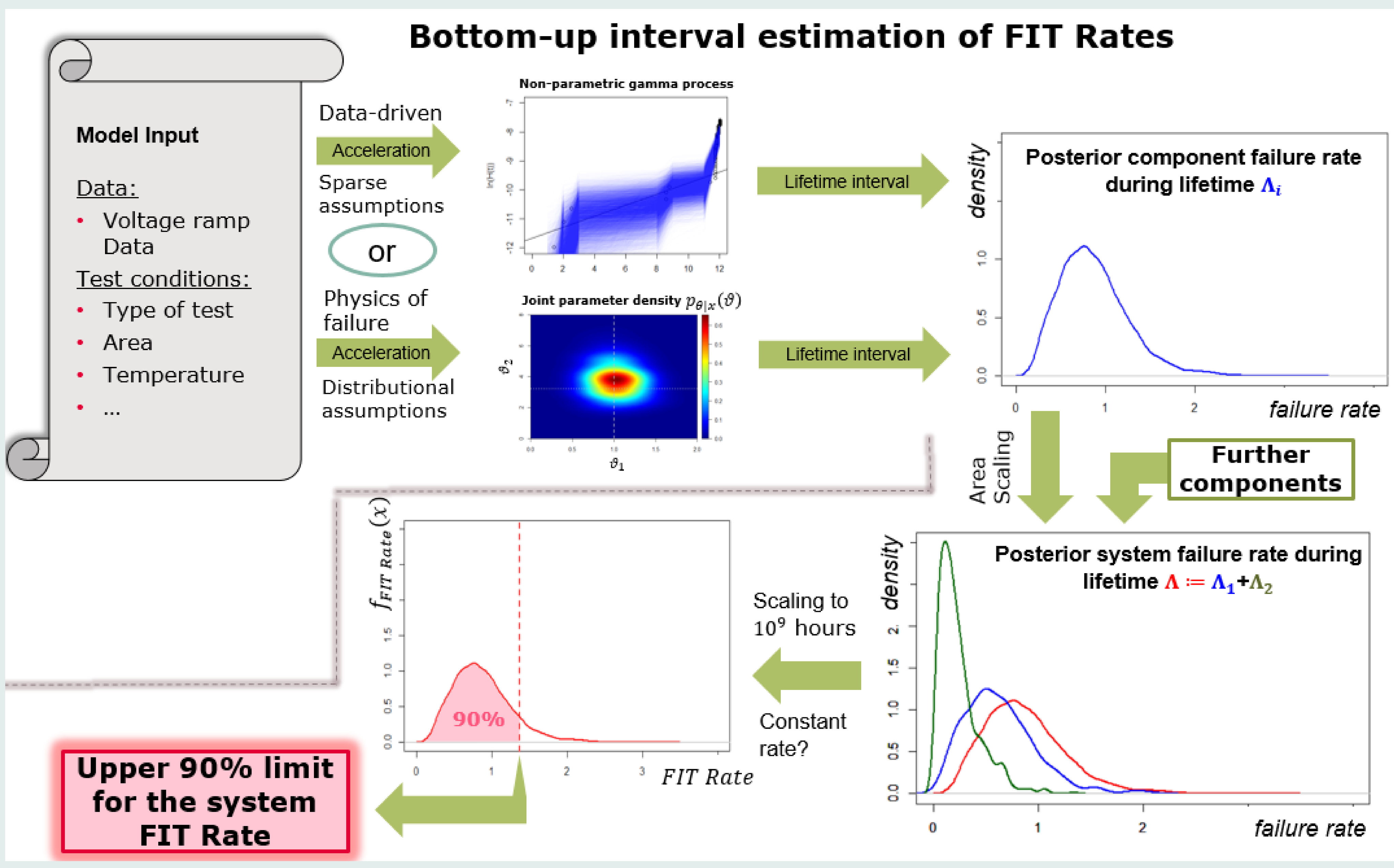
FIT Rate = Hazard rate $\lambda(t) = \frac{f(t)}{1-F(t)}$

Serial Reliability System:
$$\lambda_{System}(t) = \sum \lambda_{component}(t)$$
Use lifetime data of destructive test structures against failure mechanisms

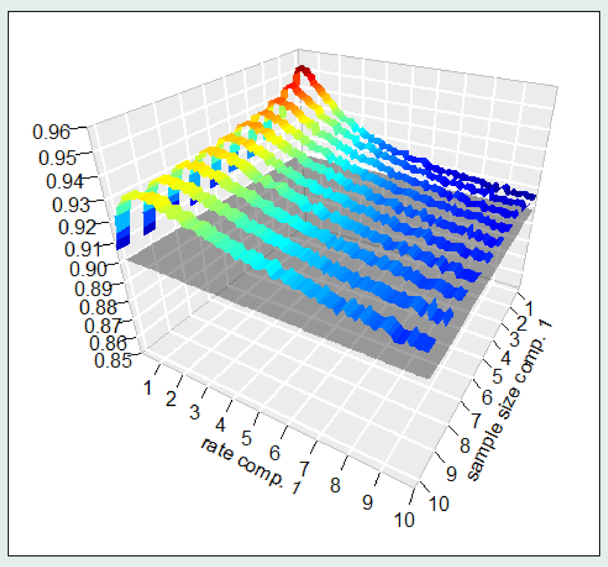
Bayesian Statistics: Prior
$$p_{\theta|x}(\vartheta) = \frac{l(\vartheta, x) p_\theta(\vartheta)}{\int l(\vartheta, x) p_\theta(\vartheta) d\vartheta}$$

Randomized hazard rates $\Lambda_{(j)}(t)$ according to the data observed

Proposed Strategy



Results



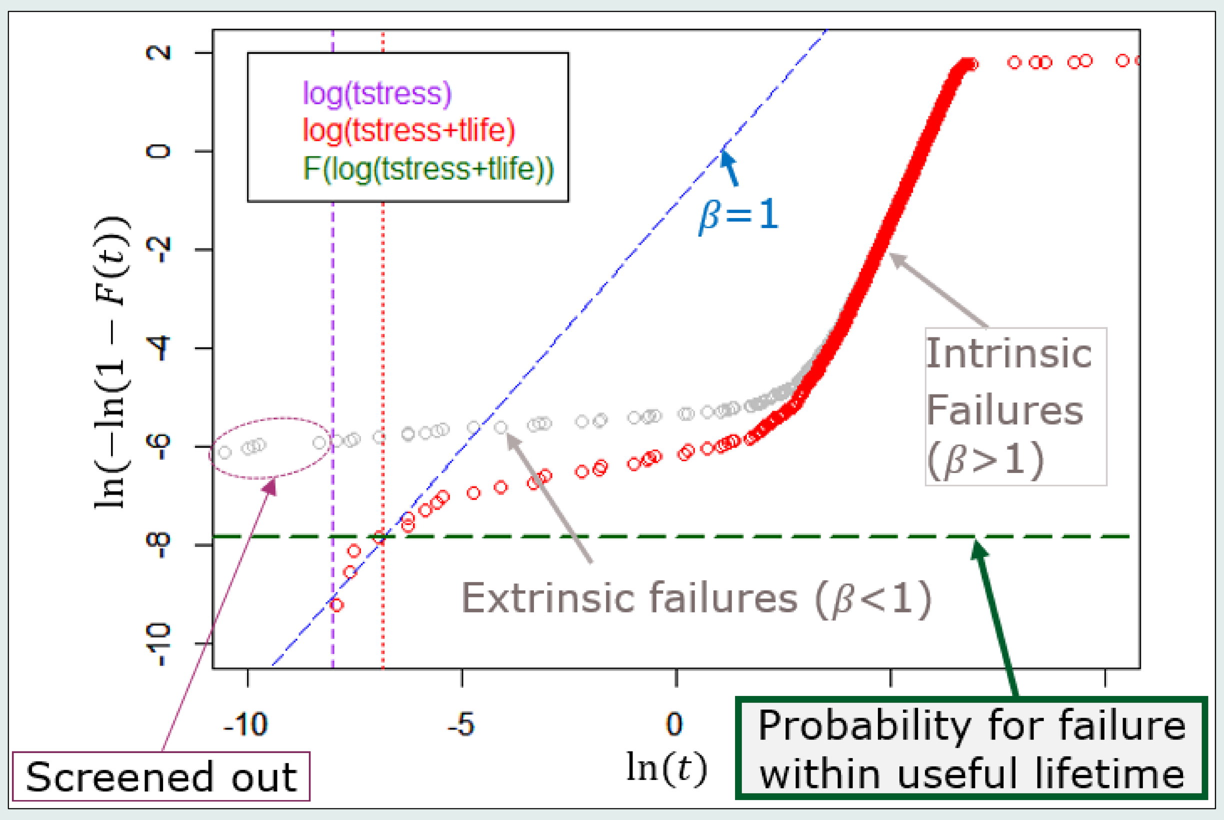
Coverage Probabilities for exponential failure time components are conservative!

Outlook

Dielectric Breakdown as a major failure mechanism

Non-parametric Bayesian estimation as robust method
Alternative: Mixture Weibull lifetime distribution if physics-of-failure known

Could be used to extend the CAPRI*-Tool with confidence



*by courtesy of Michael Röhner and Rainer Duschl

This work was funded by the Austrian Research Promotion Agency (FFG, Project No. 874907).

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Application

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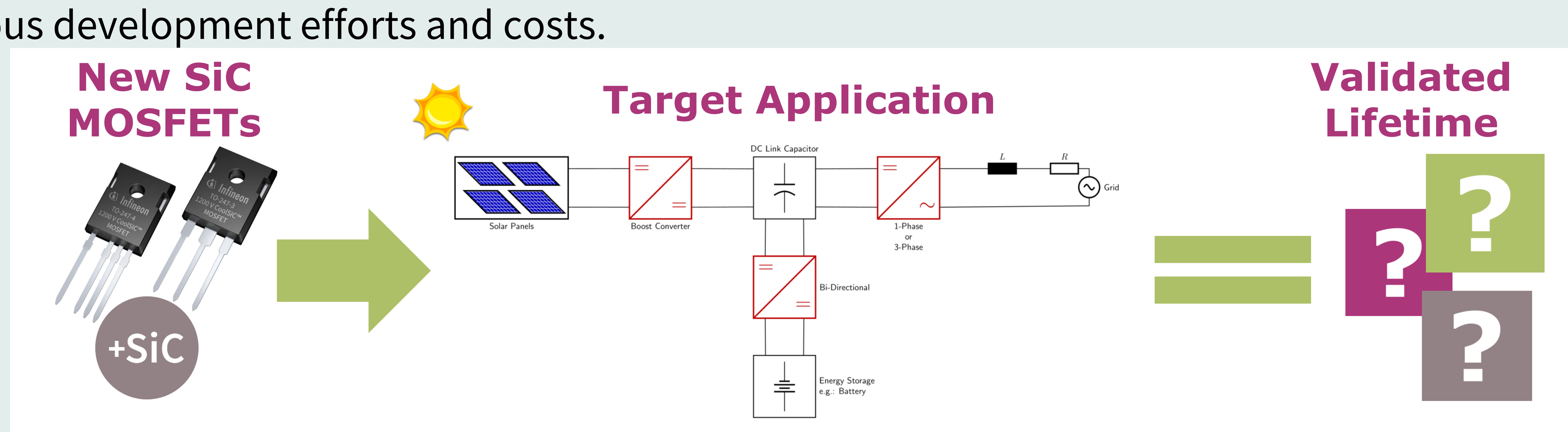
Robustness Validation of SiC MOSFETs

Introduction

Before a new power semiconductor technology is released into the market, IFX strives to ensure the robustness of its products in their target application. To account for the unpredictable interactions of stress conditions occurring within the target applications, appropriate stress-testing is necessary. However, statistically relevant data requires a large number of tested devices, making application relevant stress testing very costly. In addition, different products have different target applications requiring different test topologies, which may result in tremendous development efforts and costs.

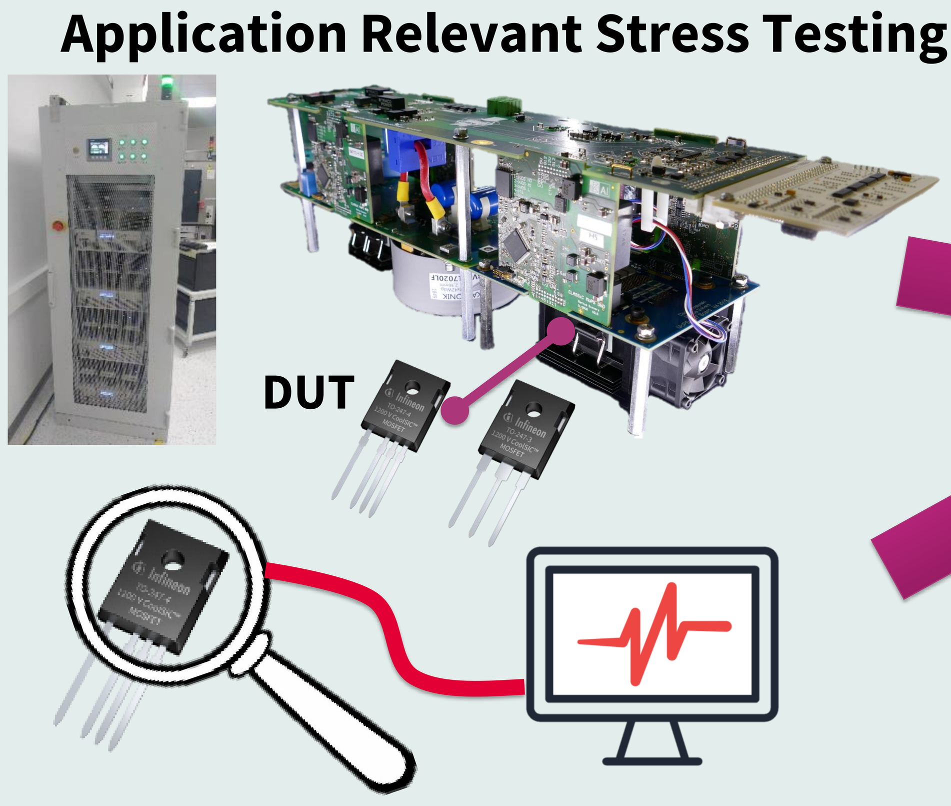
Research Questions:

- How to characterize WBG device parameters in an application test environment
- How to make a stress test robust for reliable testing

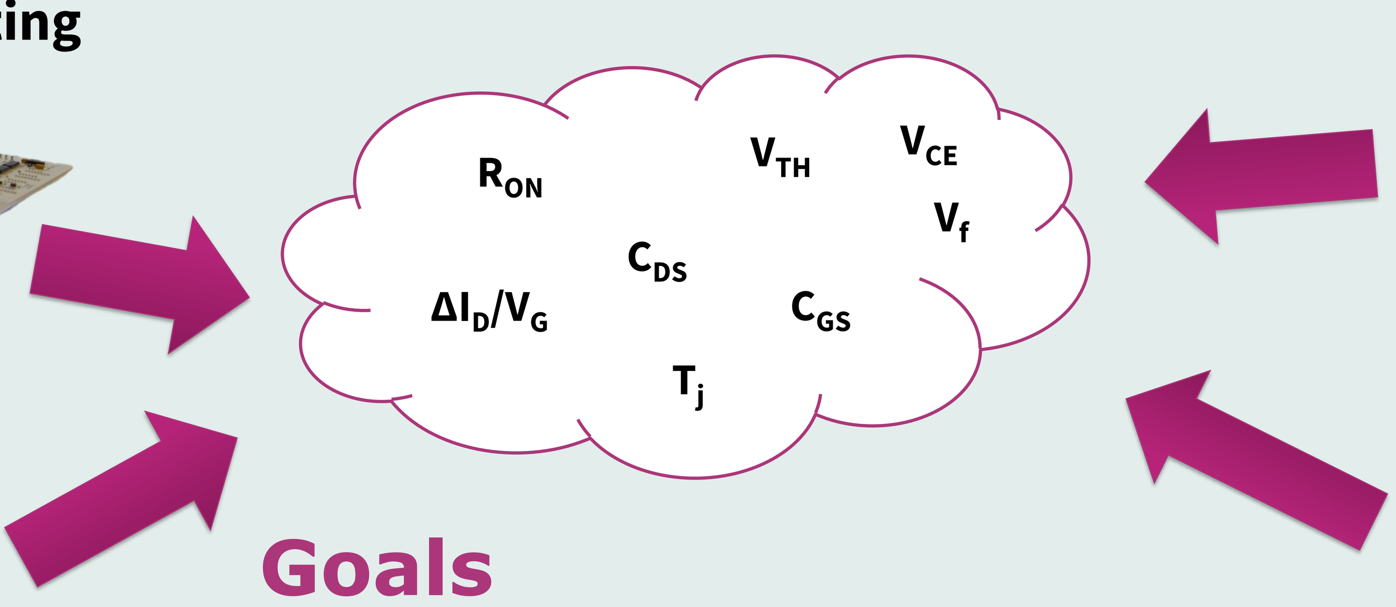


Methodology

Application Relevant Stress Testing

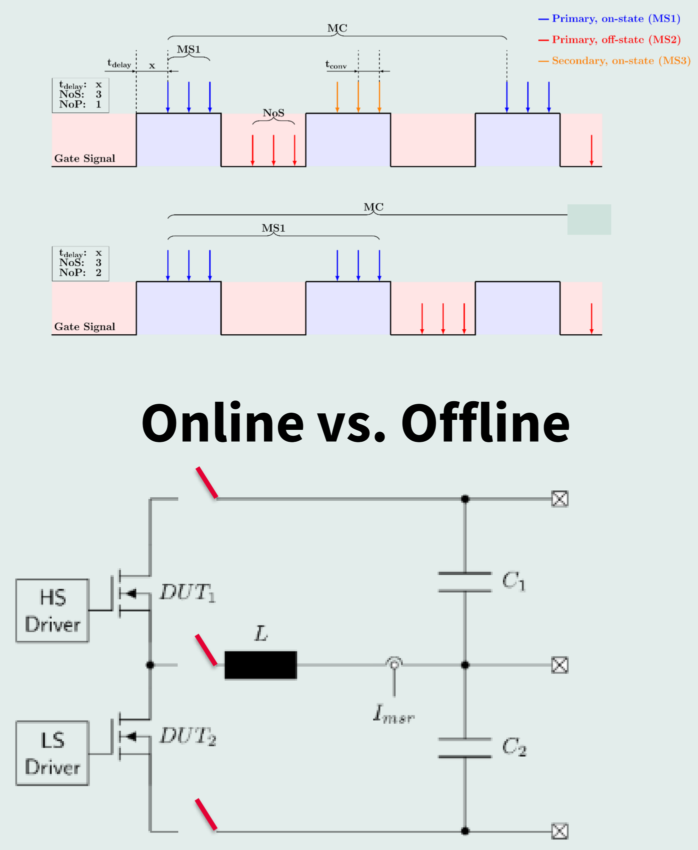


In-Situ Condition Monitoring



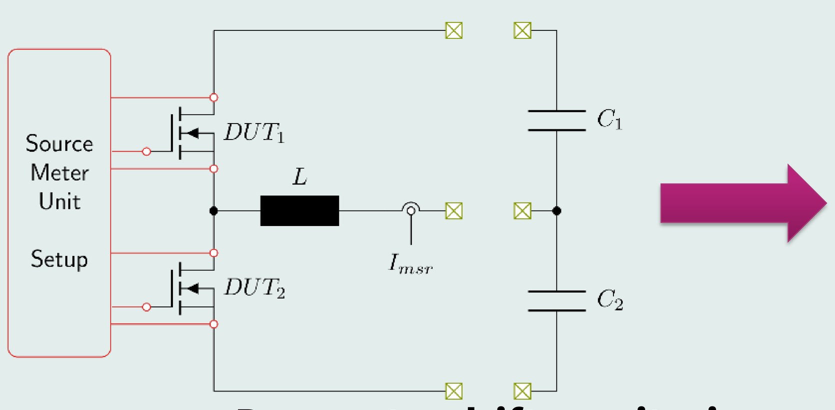
Goals

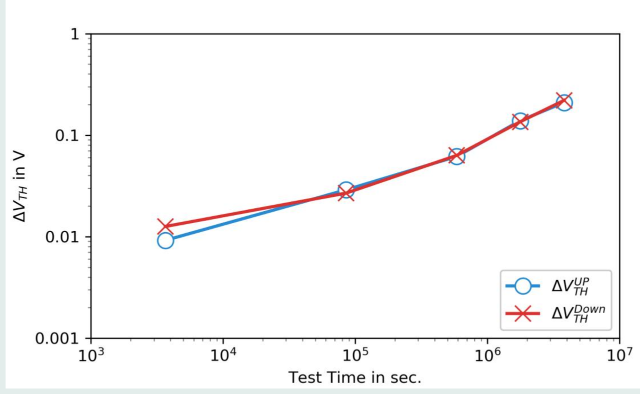
- Automated device characterization
- Static vs. dynamic data acquisition
- EMI robust operation & measurements



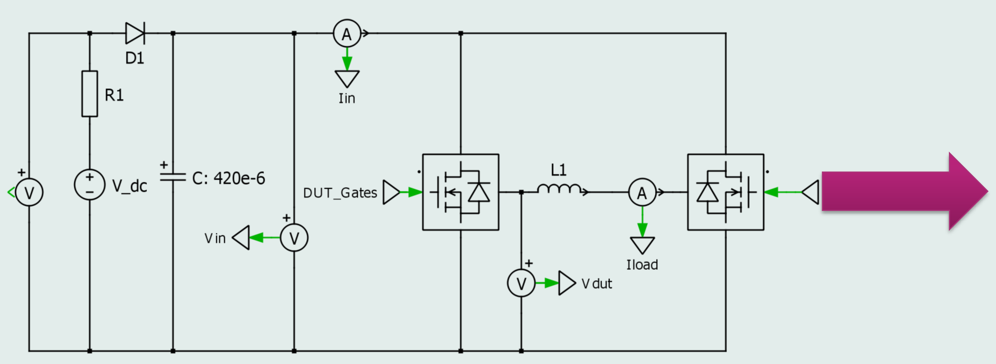
Device Characterization

Results





Parameter drift monitoring results for 1000 hrs. test



- New concept for modular application relevant stress testing
- Prototype is being designed
- Increased DUT count compared to existing system
- Simplified safety features

Outlook

- Develop robust temperature measurement for accurate and robust device monitoring
- Build advanced prototypes of the new system
- Improve EMI behavior of converter, controller and measurement solutions
- Evaluate dynamic vs. static in-situ device characterization
- Improve source meter unit characterization capabilities & performance

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Application

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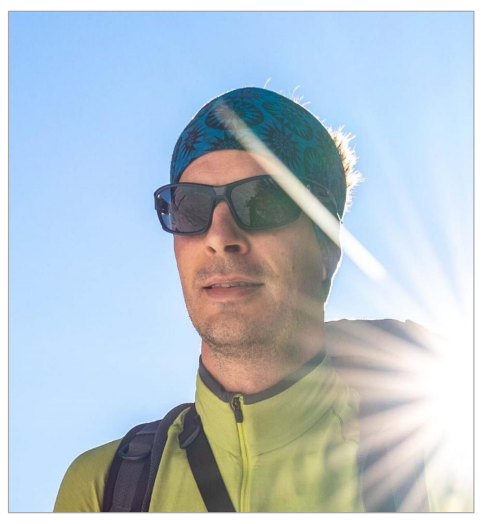


Flexible Real-Time Communication with Elastic Slot Boundaries

Introduction

In distributed real-time communication systems, there is a high demand on dependable and timely exchange of messages. As a result, bus-based time-triggered communication protocols have evolved over the last decades addressing this topic. However, these protocols are mainly applied in static systems. Having a highly flexible system, the protocols are unable to handle sporadic violations due to limited system knowledge. This work focuses on a mixed-triggered communication approach which provides real-time behavior under normal conditions while it flexibly transitions to a fallback mode when temporal boundaries are not met.

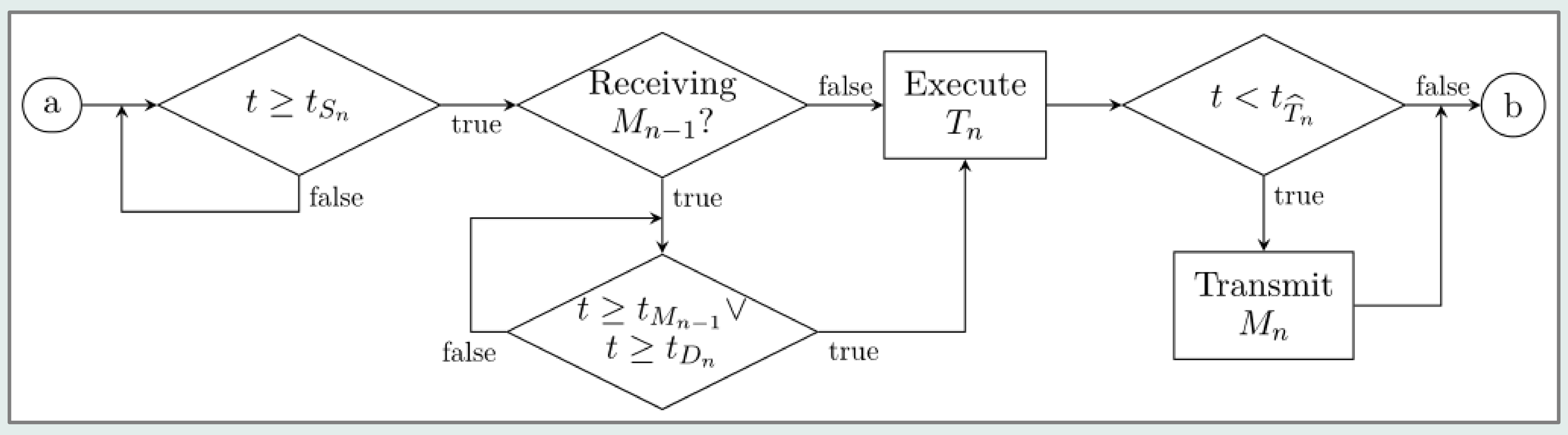
Research Questions

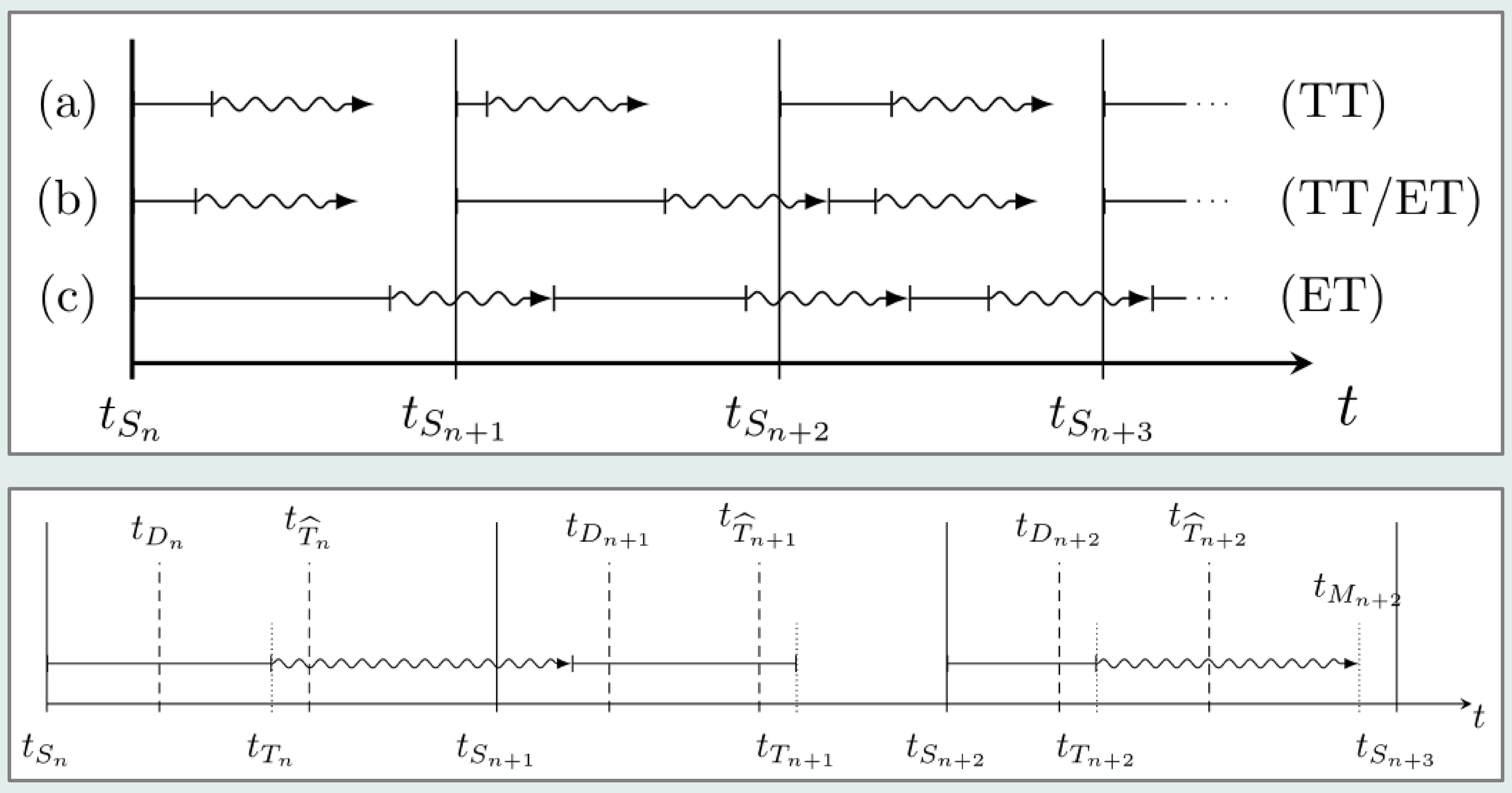
- Is it possible to tolerate sporadic slot violations without endangering the system's functionality?
- How to deal with special communication scenarios which may impair the system's proper functionality?
- What is the performance of the fault-tolerant extension on the overall communication compared to a purely time-triggered approach?

Theories

Elastic Slot Boundary Mechanism

- Basic mechanism including fault-tolerant features
- Activates fallback in case of a slot violation
- Preserves operation even in case of extended tasks





Results

Monte-Carlo Simulation

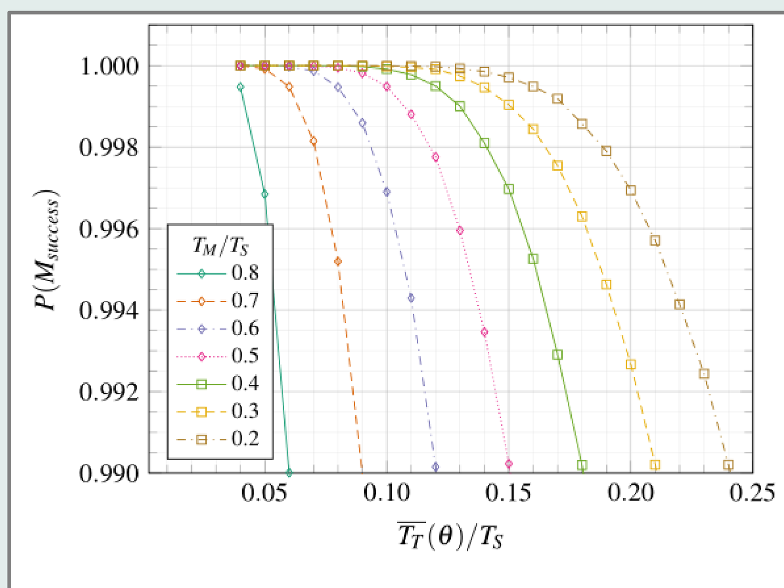


Figure 10. Message transmission probabilities for different message-to-slot ratios using the *standard time-triggered* mechanism.

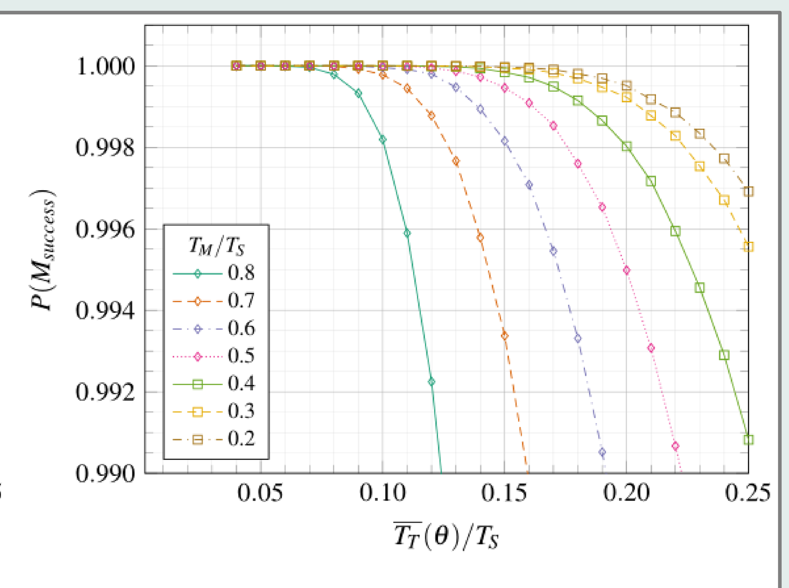
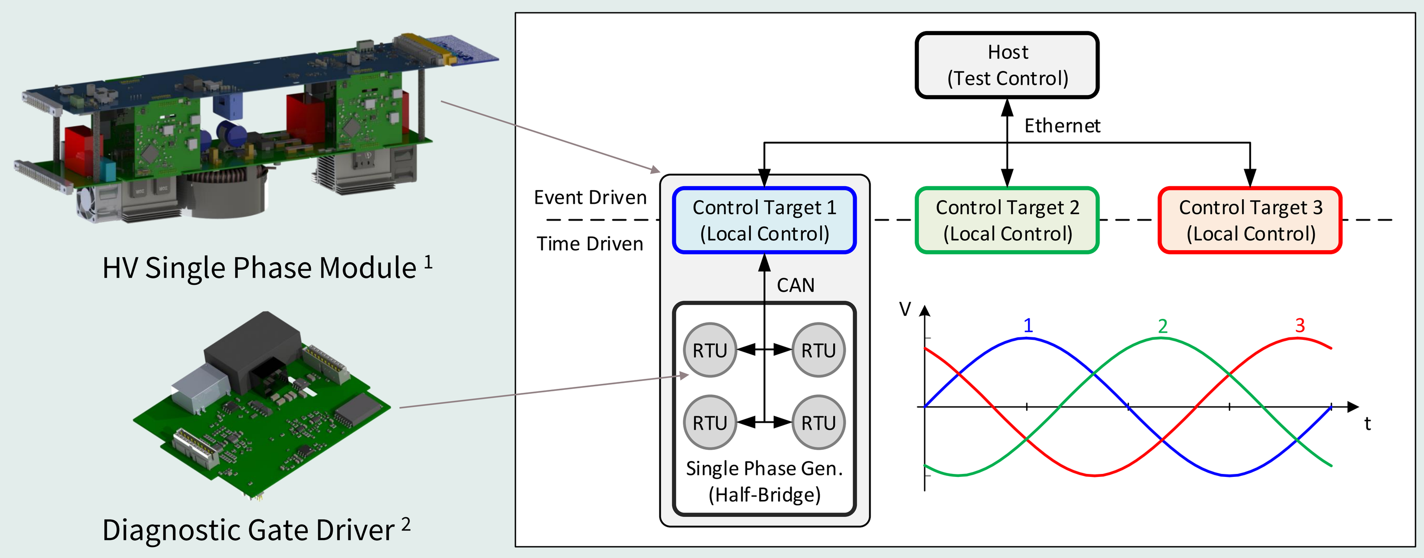


Figure 11. Message transmission probabilities for different message-to-slot ratios using the RESB mechanism.

Next Steps: Verifying the proposed approach using a distributed bus network of a modularized application stress test system



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Application

PhD
Mate Toth

Supervisor
Paul Meissner

InterCEPT:

Interference Mitigation Concepts and Efficient Processing Techniques

Introduction – Motivation

- Number of deployed radar sensors on the road increasing → mutual interference
- Reduction of object detection sensitivity severe in a safety-critical ADAS application

Figure: Simple traffic scenario example.

Introduction – Research Goals

- Analysis of probability and impact of interference
- Novel mitigation methods within a consistent quantitative performance evaluation framework
- Validation of model and algorithms

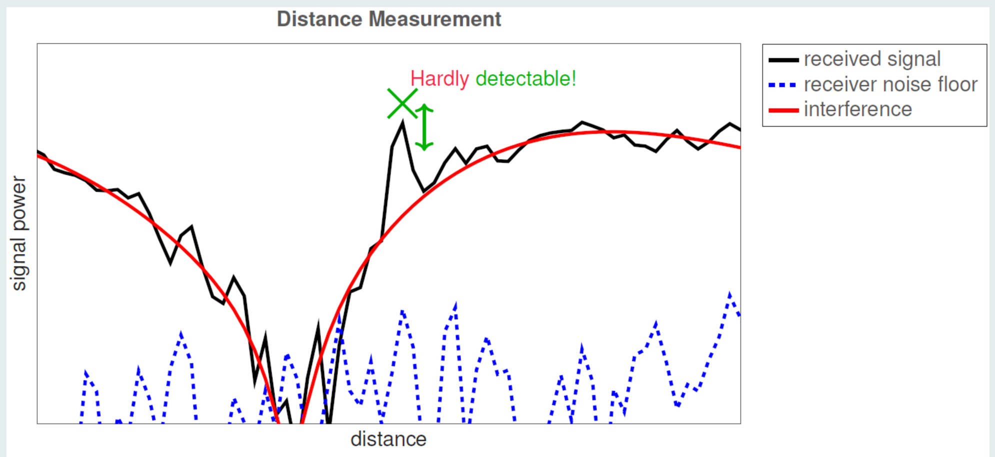


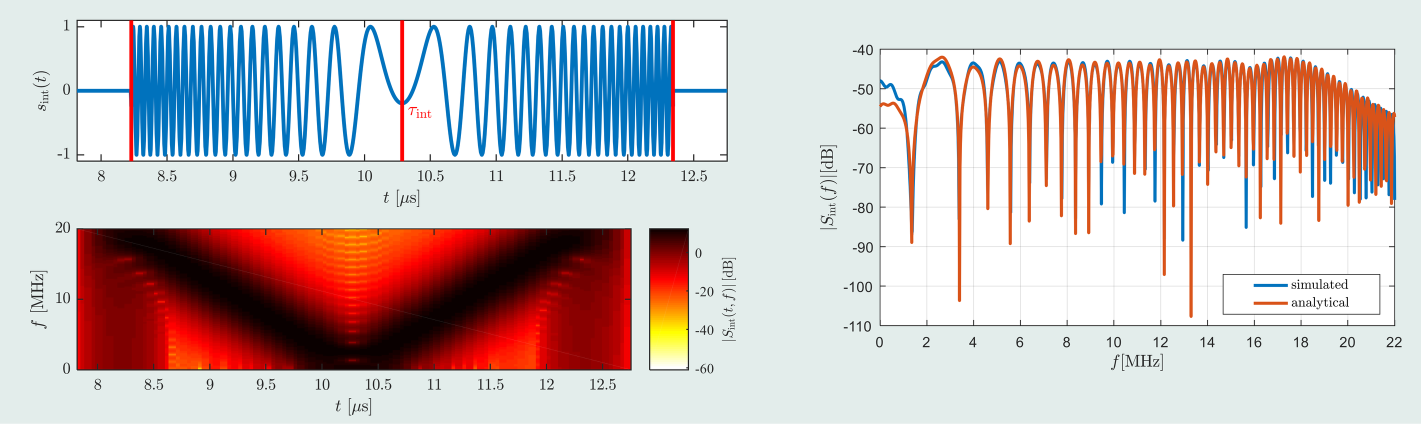
Figure: Corresponding distance measurement example.

Interference Modeling

- Interference arrival random, highly unpredictable
- FMCW/Chirp sequence radar: manifest as sequence of "chirp bursts"
- Mix of deterministic and statistical models

$s_{\text{int}}(t) = \cos(-2\pi k_{\text{int}}\tau_{\text{int}}t + \pi k_{\text{int}}t^2 + \varphi_{0,\text{int}})$

$S_{\text{int}}(f) = 2\,|S_{up}(f)|\,|\cos(\phi_{up}(f) + 2\pi f\tau_{\text{int}})|e^{-j2\pi f\tau_{\text{int}}}$



Mitigation Methods

- Classification of state-of-the-art algorithms according to processing principles and requirements
- Statistical performance comparison according to useful application-oriented metrics

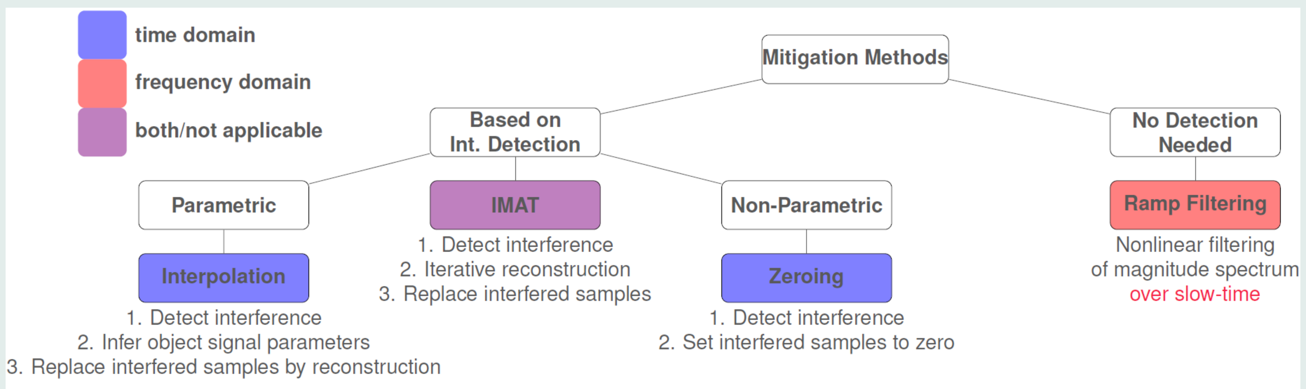


Figure: Classification of selected interferenc mitigation algorithms.

Some Results & Further Work

- Extensive simulation framework with 12 mitigation algorithms, out of which 6 developed by our group

- Ongoing work includes continuing novel algorithm development, validation by measurement, and inclusion of system & scenario models

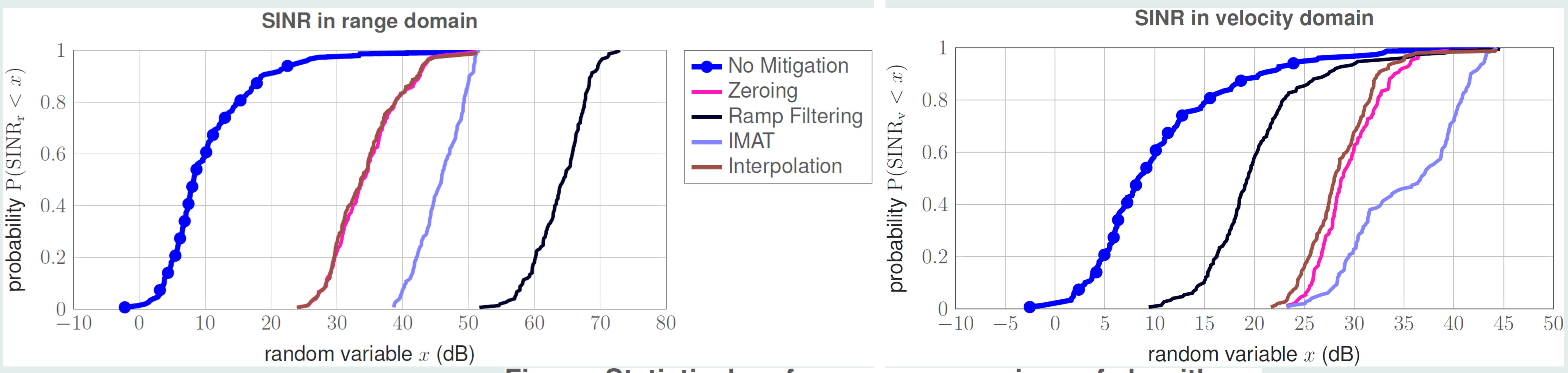


Figure: Statistical performance comparison of algorithms.

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Application

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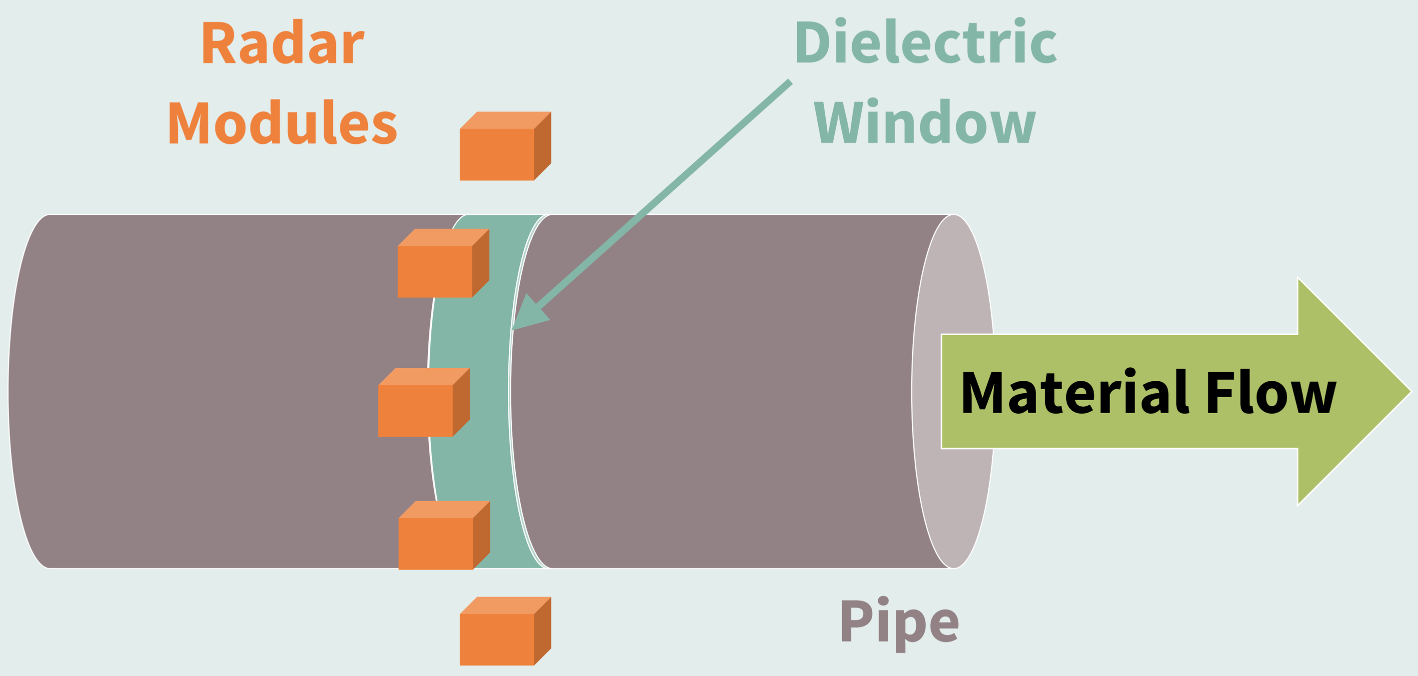
High-Resolution Tomographic Radar

Introduction

Advanced industrial process control requires **detailed real-time information about material parameters** classical sensors often cannot provide.
A novel high-resolution **radar tomography** system for **non-destructive material characterization** will enable insights into otherwise hidden process states.
Multiple **Infineon 77 GHz radar** modules are employed to realize a **low cost** and **low complexity** solution.
Highly accurate sensor synchronization is key to detect small deviations inside the material.

System Concept



Theory

Time of Flight: Propagation speed depends on material

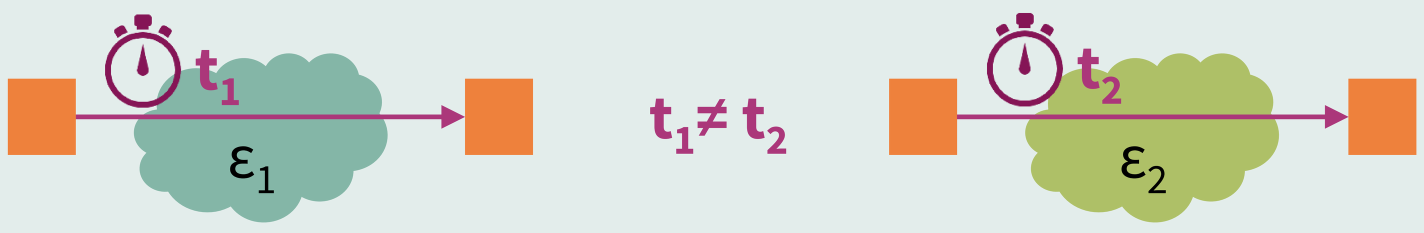
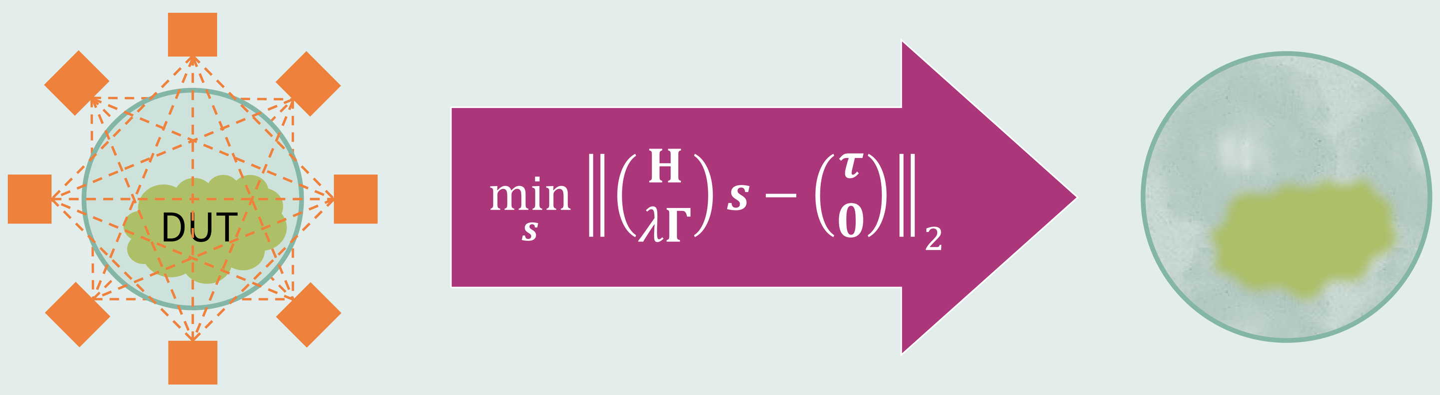


Image reconstruction from multiple measurements



Methodology

Ill-posed & underdetermined **inverse problem**
→ incorporate prior knowledge via **regularization**

Tikhonov: Smooth distributions, analytical solution

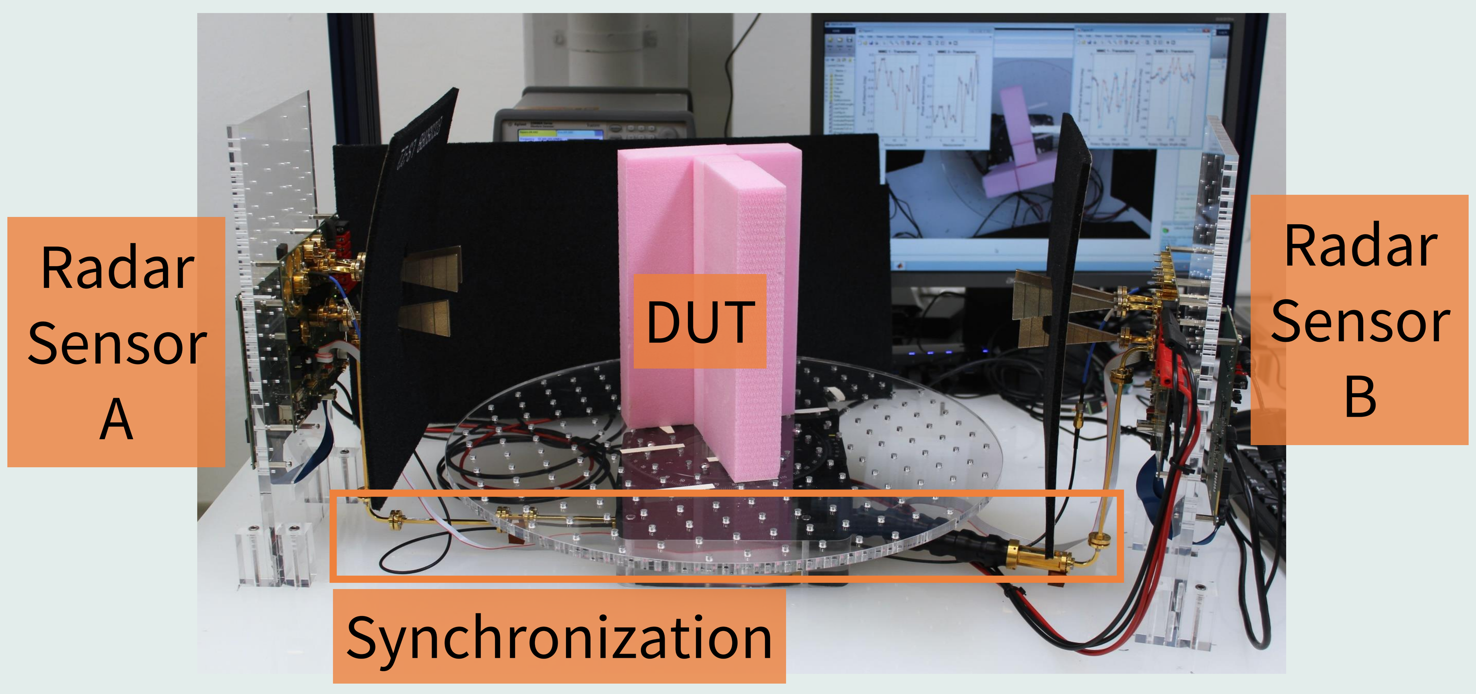
$$\min_s \left\{ \|\mathbf{H}s - \check{\tau}\|_2^2 + \lambda^2 \|\mathbf{\Gamma}s\|_2^2 \right\}$$

Least-squares solution | Weighting | Penalty term

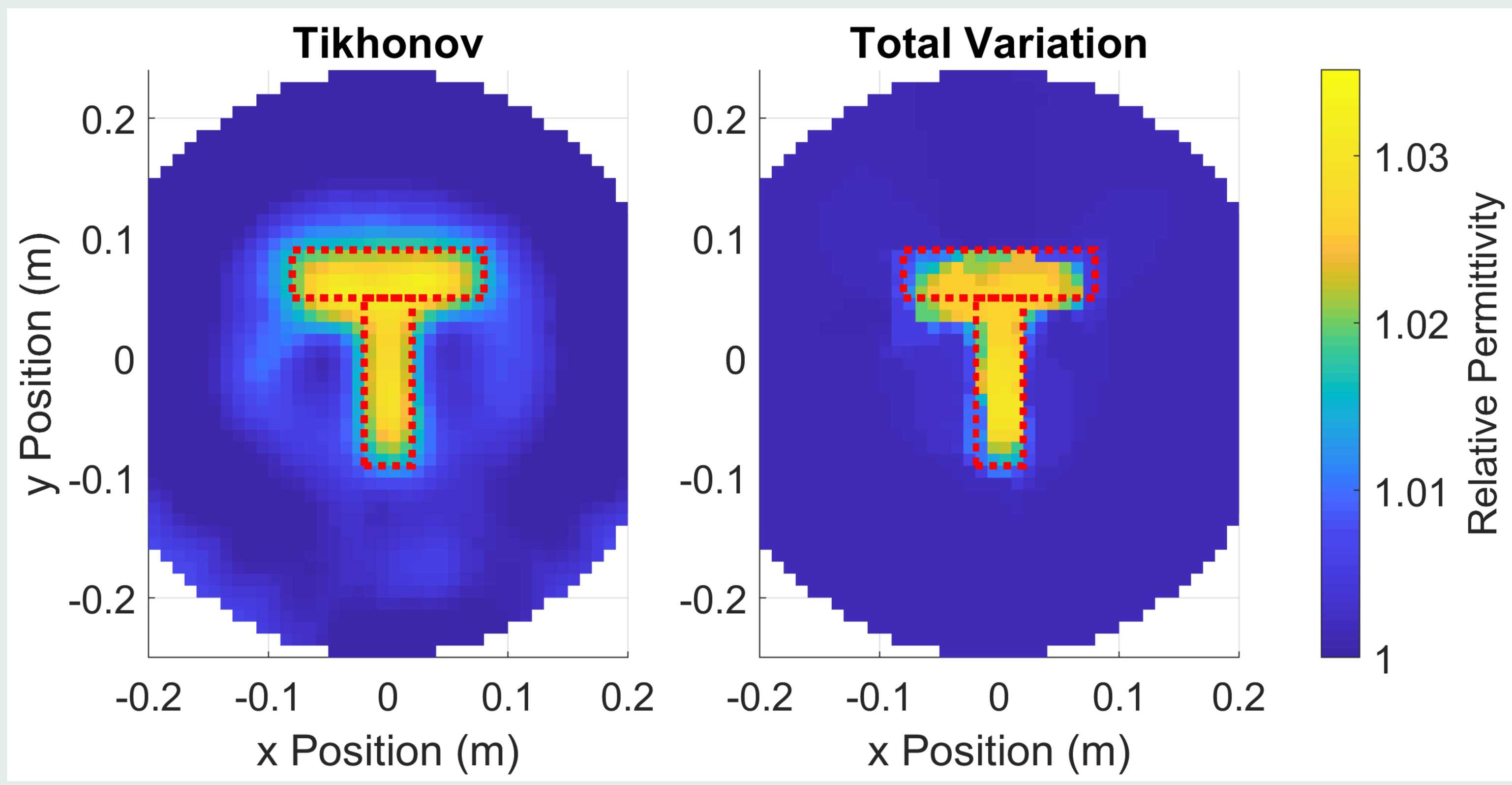
Alternative: **Total Variation**
Discrete distributions, only iterative approximation

Measurement Setup & Scenario

XPS foam (common in house insulation) with $\varepsilon_r \approx 1.04$



Results



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Application

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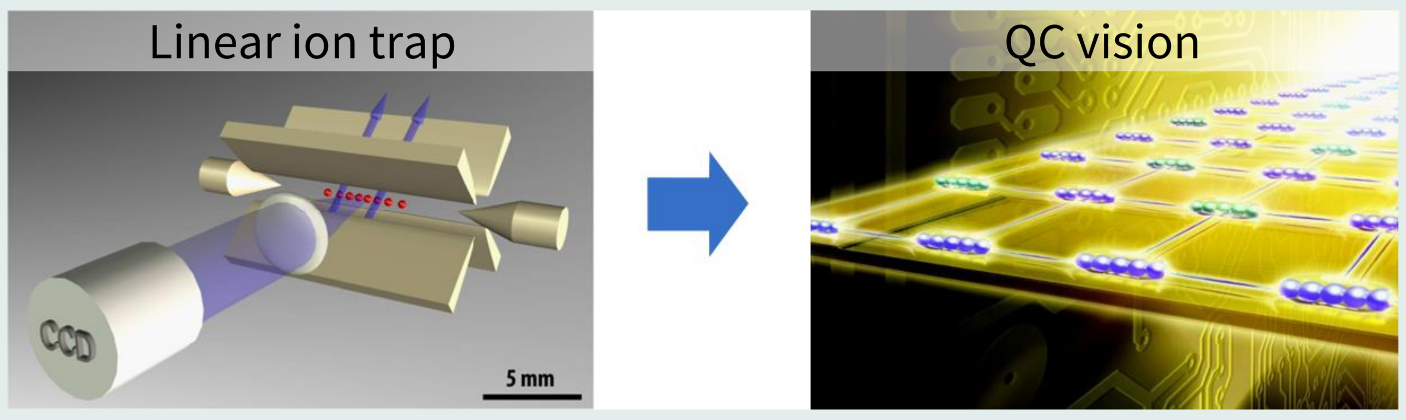
Supervisor
Clemens Rössler

Single trapped ions for quantum computing

Introduction

- Ion traps are one major technological modality for quantum computing
- But: academic fabrication is limited in terms of reliability & scalability
  ⇨ industrialization needed



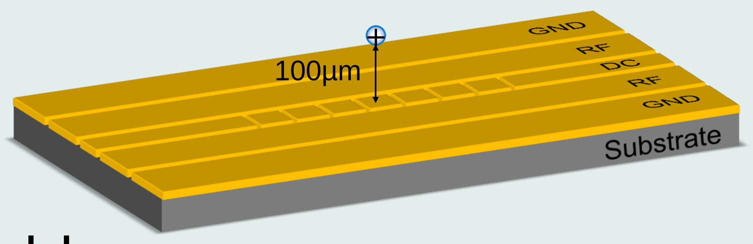
PIEDMONS:
Portable **I**on **E**ntangling **D**evices for **M**obile **O**riented **N**ext-generation **S**emiconductor-technologies

- Design, fabrication and characterization of a scalable 3D ion trap for room temperature operation
- Fabrication at Infineon facilities ensures high precision and reproducibility

Concept

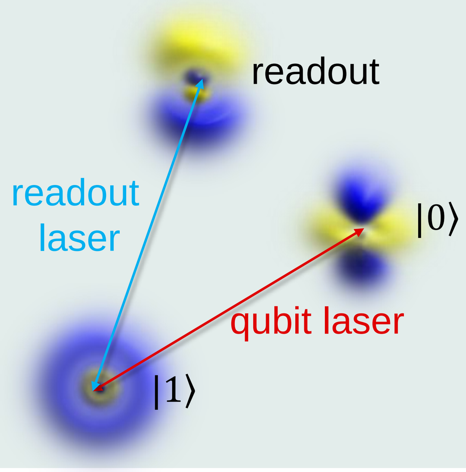
Trapped Ions:

- Trap in cryo vacuum
- Atom ionized mid-flight
- Ion captured by DC- & RF-fields



Qubit Operation:

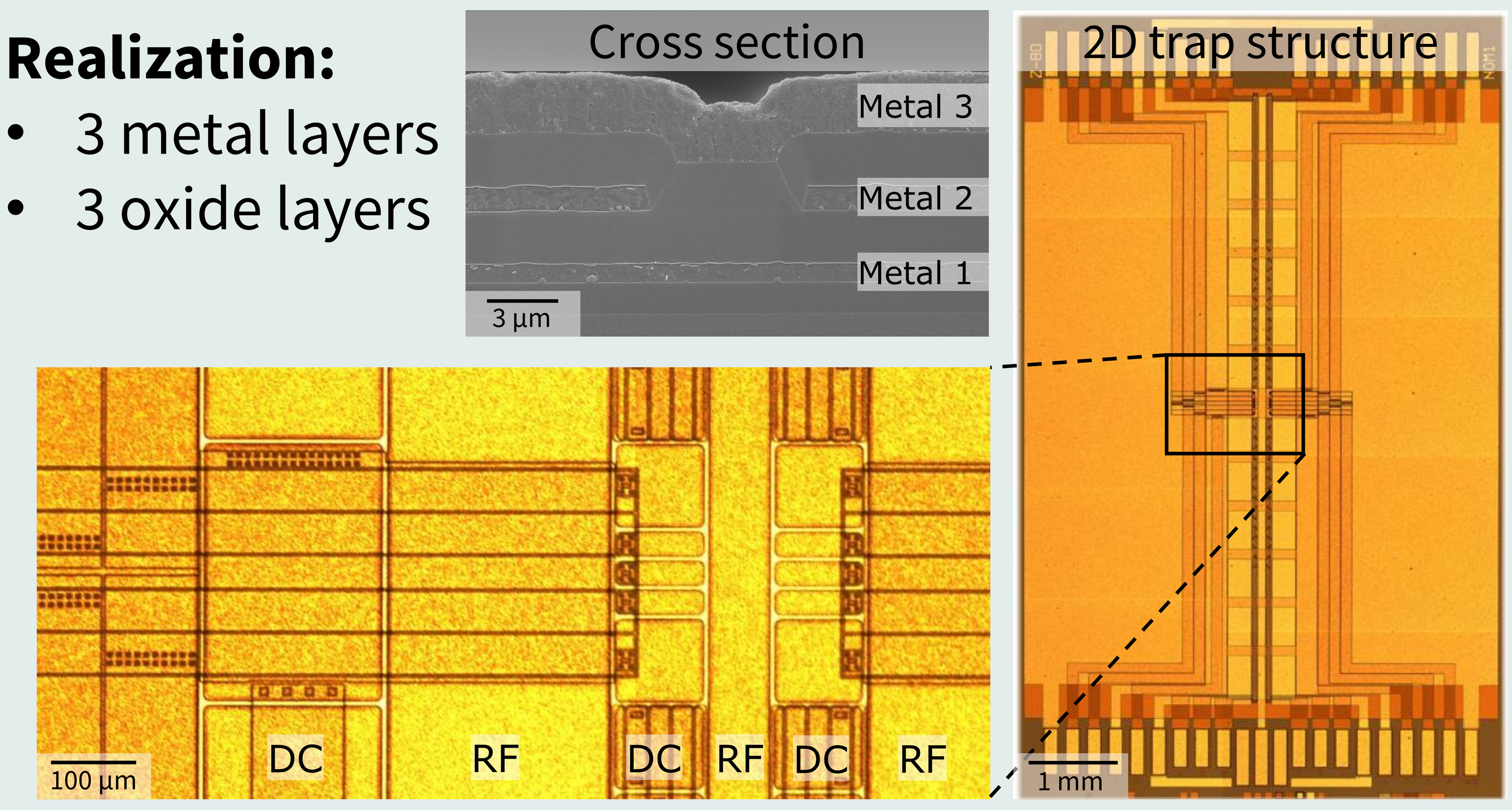
- Lasers manipulate electron orbits
- Red laser for gate operations
- Blue laser readout



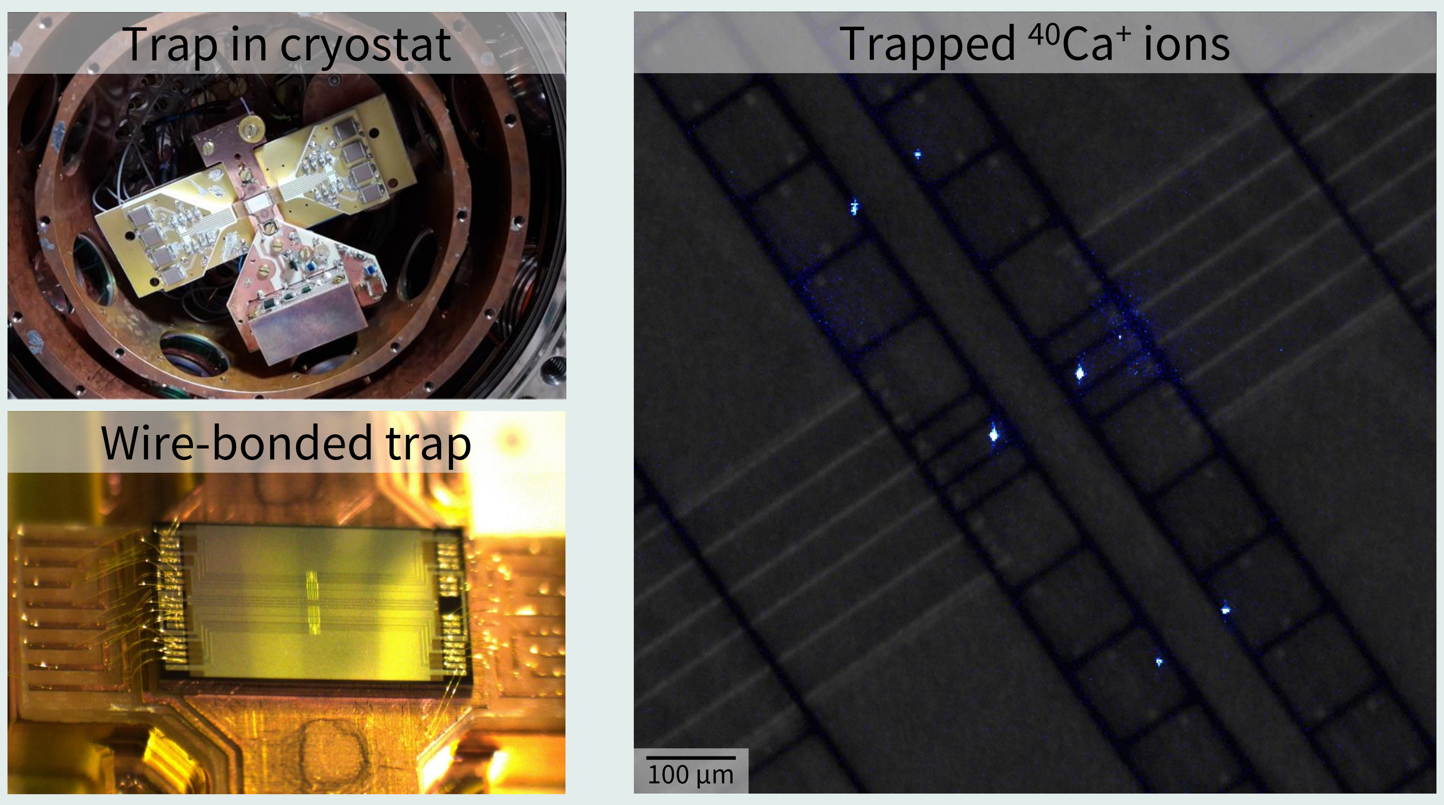
Methodology

Realization:

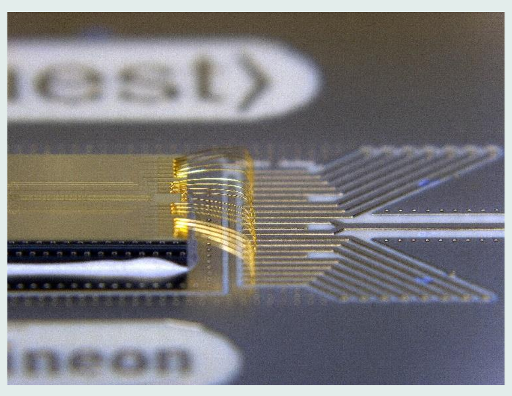
- 3 metal layers
- 3 oxide layers



Results



Next steps:



- Industrial package & assembly of Infineon ion trap
- Transfer to dielectric substrate for better RF performance
- Fabrication of a 3D MEMS ion trap for room temperature operation

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Infineon

universität innsbruck

PIEDMONS

This project has received funding from the European Union's Horizon 2020 research and innovation programme under agreement No. 801285.

Application

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Supervisor
Mirhad Memic

FMEA – ASSISTANT

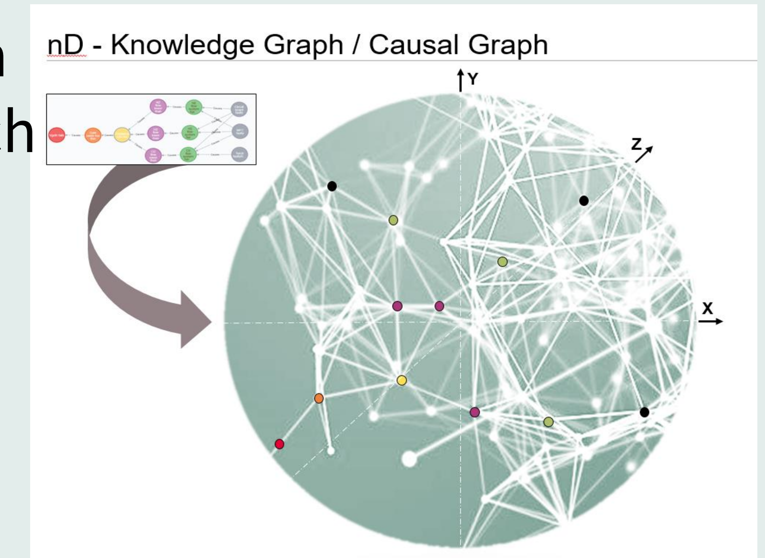
Introduction

Scientific issue

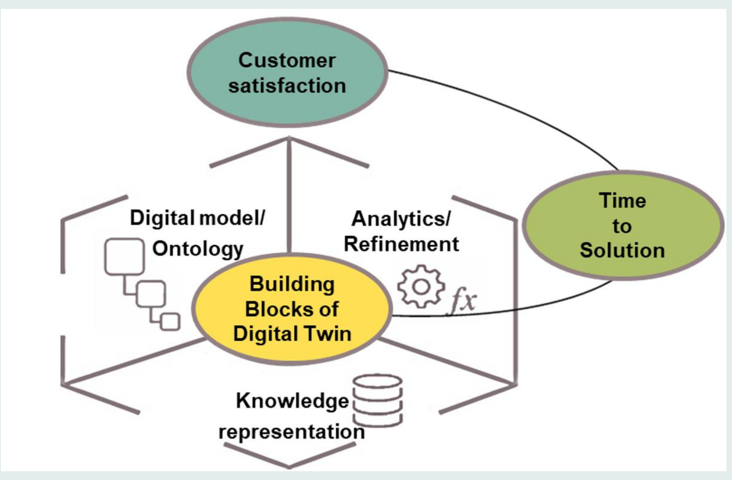
- **Root cause analysis** and **risk assessment** are **critical** and **complex** processes in industry.
- Experts rely on previse experiences which are documented in a **heterogeneous** data sources .
- Explore root cause analysis and risk assessment methods using **artificial intelligence** approaches**.**
- Focus on semiconductor industry and the corresponding challenges such as **domain-specific** terms and data **complexity**

Theories

Generating causal graphs from risk assessment document such as FMEAs would allow the use of **refinement** algorithms to generate **hypotheses** about possible links, which are **not present** in the datasets.

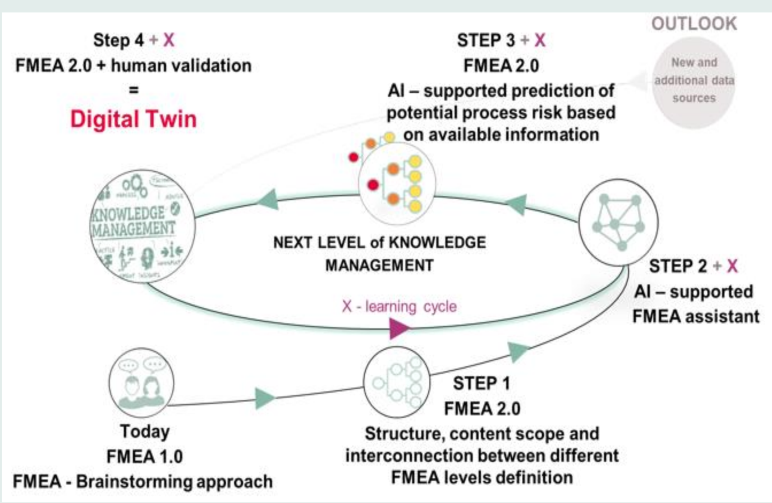


Utilizing topic related reports to train language models would allow leveraging of **sematic features** of entities' **text**.

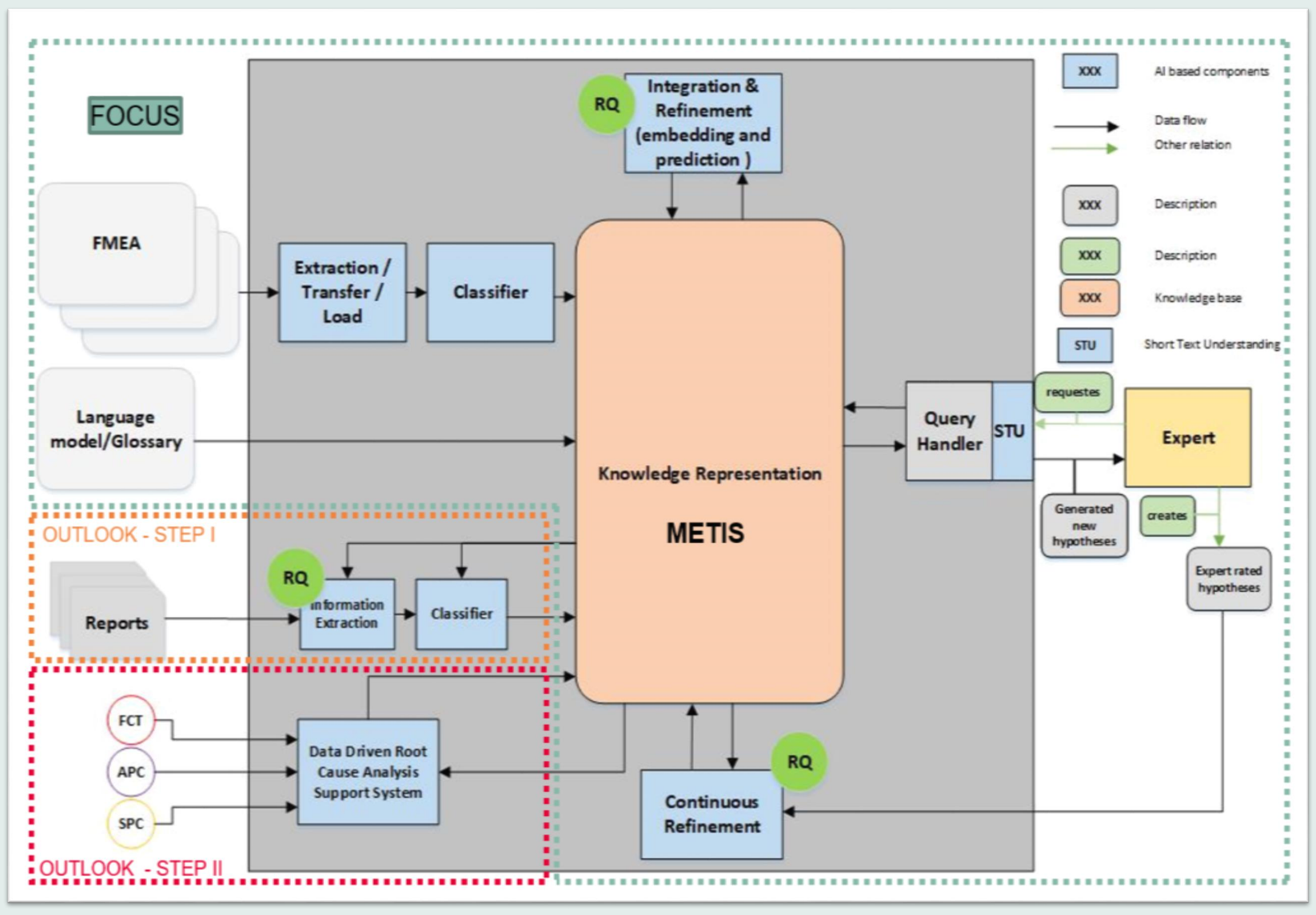


Using the user feedback as source of information to the refinement algorithm would allow a dynamic knowledge management system for **further learning** depending on the **user input.**

Extending **information extraction** methods on topic related reports would allow for more **completed** knowledge representation. Combining the knowledge representation with domain specific (**FMEA**) **ontology** would allow for **automated** support or reject of the generated hypotheses depending on corresponding **inline measurements**



Methodology



Current Results / Next Steps

- **Concepts and relation** for more comprehensive semi-structured dataset.
- AI based method for **improving consistency** in semi-structured knowledge bases of domains specific language.

Next Steps :

- **Hypotheses generation** method for knowledge completion
- Data driven **hypotheses ranking** method for complexity reduction of root cause analysis tasks

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Application

Sensor Data Fusion System for Optimization of Human/Robotic Collaboration

Feryel Zoghlami

H. Heinrich
G. Schneider

Introduction

Background and problem statement, why is the research necessary

In the industry 4.0 both humans and robots are working side-by-side in a hybrid automated workplace. The collaboration seems to be difficult sometimes because of the lack of a continuous bidirectional interaction between both parts. The lack of enough information from the environment including humans leads to lack of intelligence for robots in dealing with unexpected situation during the production.

What are the research questions you want to explore in your dissertation?

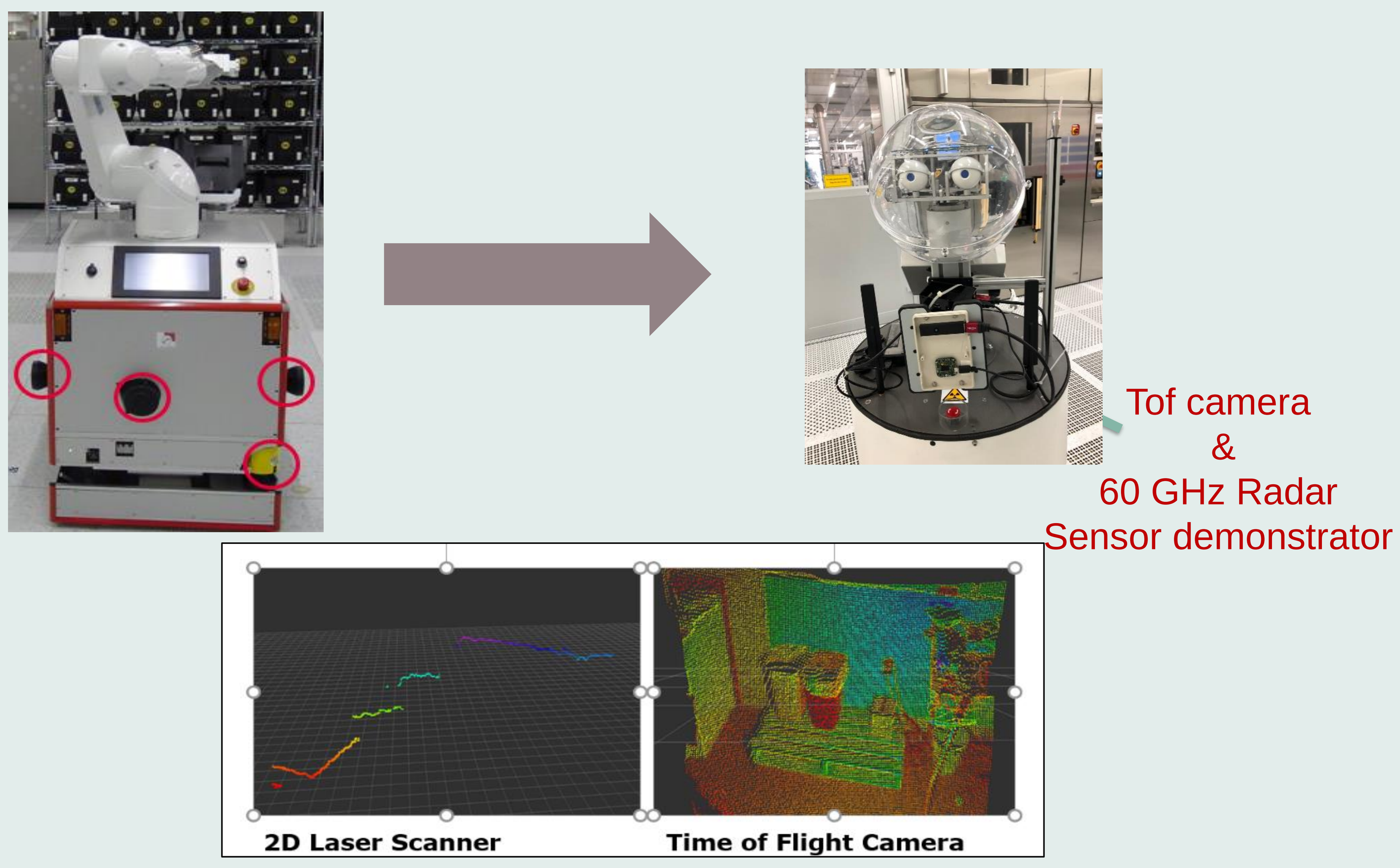
- Sensor data fusion based system installed in a hybrid workplaces inside the factory.
- Object classification with focus on human detection and tracking.
- Better perception of the surrounding environment for enhancement of the human–robotic collaboration.

Theories

Main theories in one or two sentences

- 2D laser scanners implemented in different directions -> 3D sensor technologies + AI.
- Continuous stops due to safety regulations -> Get rid of passive use of sensor data/ Data filtering/ Relevant features extraction/ Smart decision making by robotic systems.
- Human behavior understanding and prediction.

Methodology

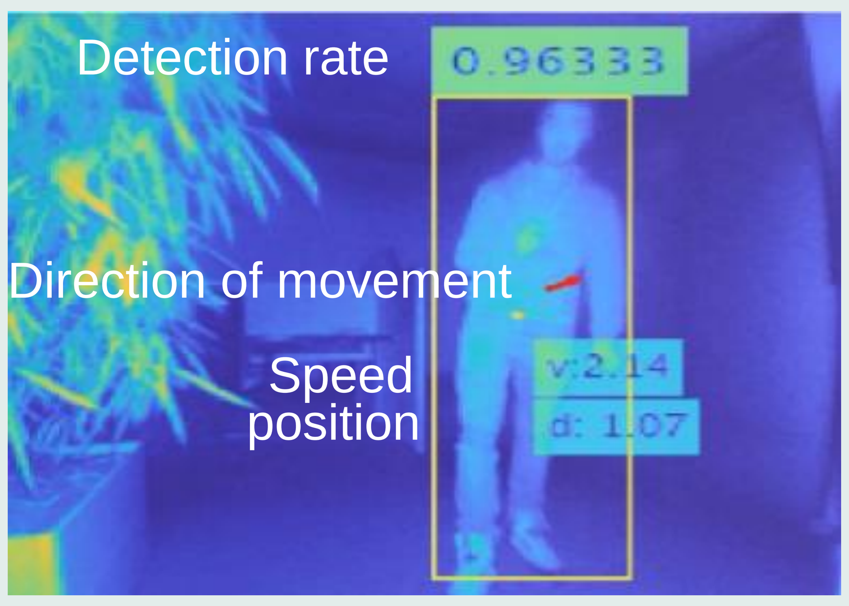


Results

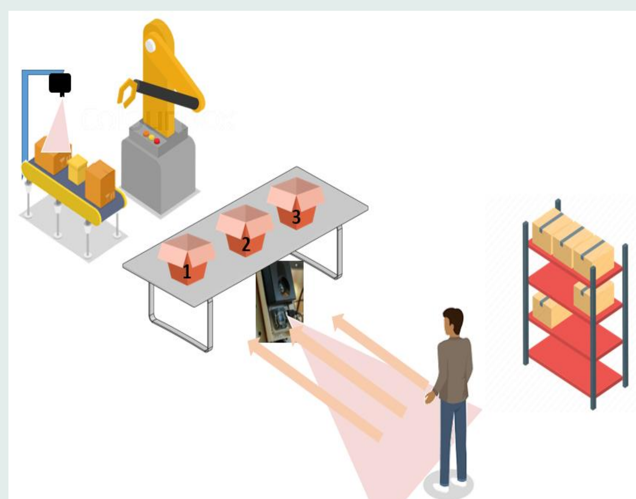
➧ A first demo has been developed and tested: ToF/Radar fusion system used for human detection and tracking able to:

- Detect and recognize with high confidence humans present in the system's field of view.
- Locate detected humans in the 3D space and send their live positions.
- Calculate the speed of movement of each detected person
- Track in real time the direction of movement of each detected person

➧ Outputs will be transferred in real time to a robotic system => A real use case which shows a proactive robotic reaction in a hybrid collaborative workplace.



System view & outputs visualization



Human/robotic collaboration with proactive robotic reaction

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ECSEL JU

GEFÖRDERT VOM Bundesministerium für Bildung und Forschung

HOCHSCHULE MITTWEIDA University of Applied Sciences

ARROWHEAD TOOLS

Infineon

Application

Dynamic Pulse Test Methods for Discrete High Power Semiconductors

Konstantinos Patmanidis

Michael Glavanovics

Introduction

Power devices fail because they are exposed to various stressors, which in turn stimulate certain failure mechanisms. Temperature stresses have major influence on the wear-out of the power devices. Thus, precise knowledge of the failure mechanisms is of vital importance in terms of reliability assessment and enhancement.

Previous stress test systems have been developed, aiming to emulate real operating conditions or to isolate a specific failure mechanism. However, further system level design effort is needed, to operate numerous DUTs (Device Under Test) in parallel mode with sophisticated data acquisition unit for accurate failure analysis and diagnosis.

The primary focus of this thesis is to implement a reliability stress test system for high power discrete semiconductors, targeting on modularity, scalability, and redundancy. The major objective is the incorporation of different stress test concepts within a unified stress test apparatus by retaining most of the stress system modules constant and merely change the DUT for a variety of power devices and stress patterns. Simultaneously, an appropriate amount of data of various DUT parameters should be recorded in situ for post failure analysis.

Prototype Design Phase

Version 1

- Proof of electrical performance
- Voltages up to 1.2 kV – Current up to 250 A in a single shot

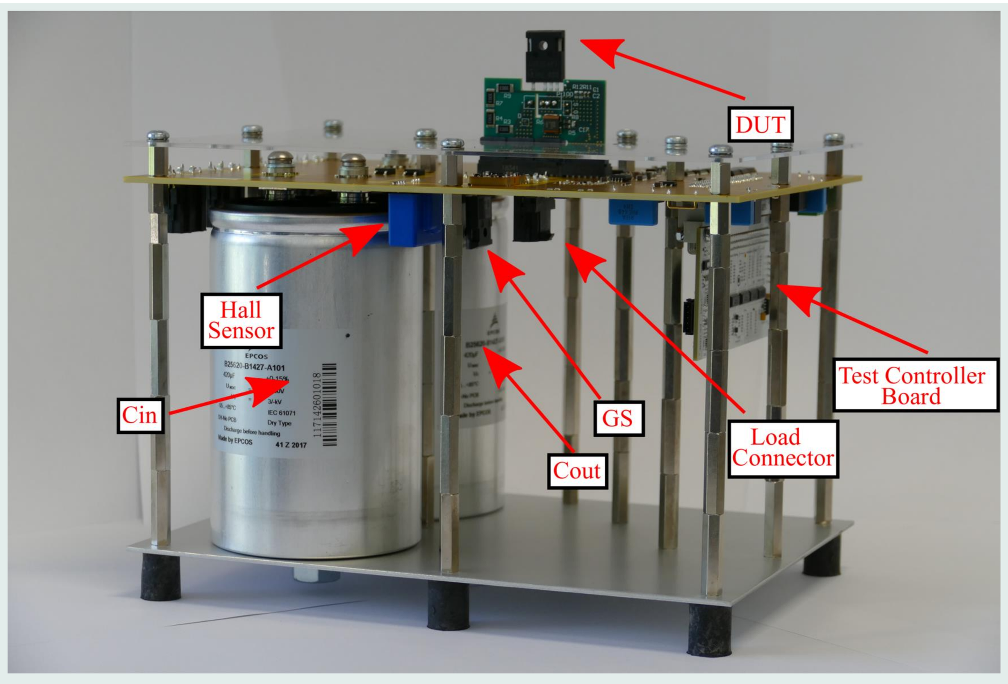


Figure : Single Channel of the first prototype

Version 2

- Smaller board size
- Voltages up to 1.5 kV – Current up to 400 A in a repetitive mode

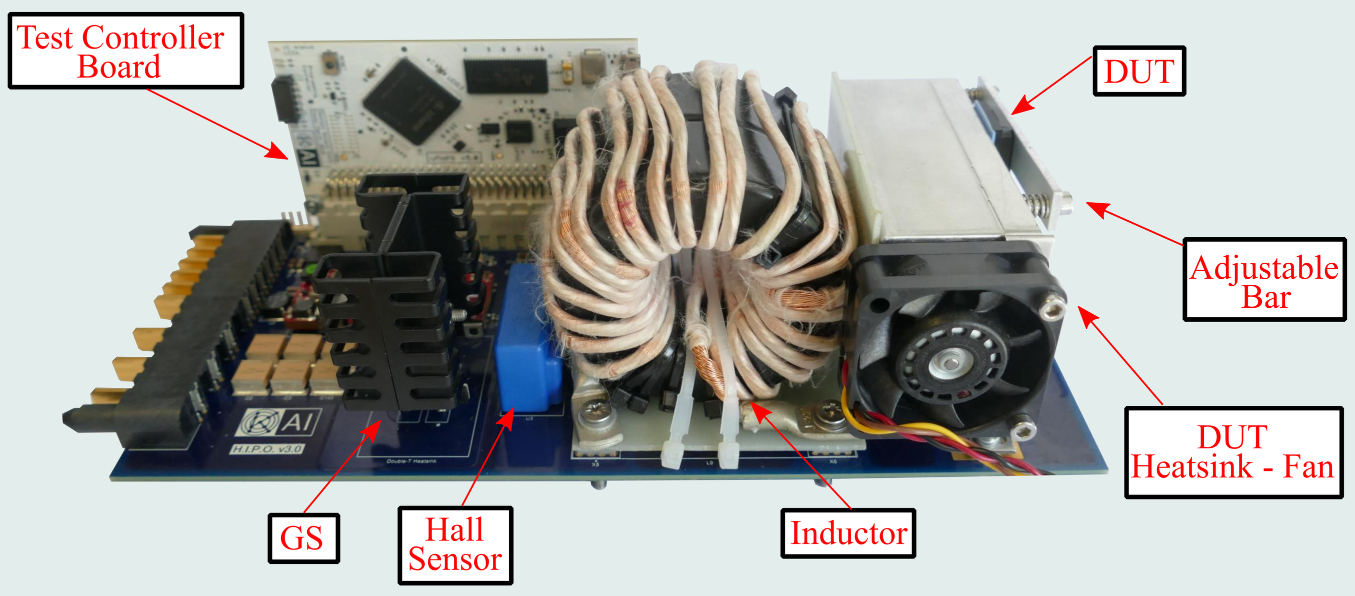


Figure : Single Channel of Base Board

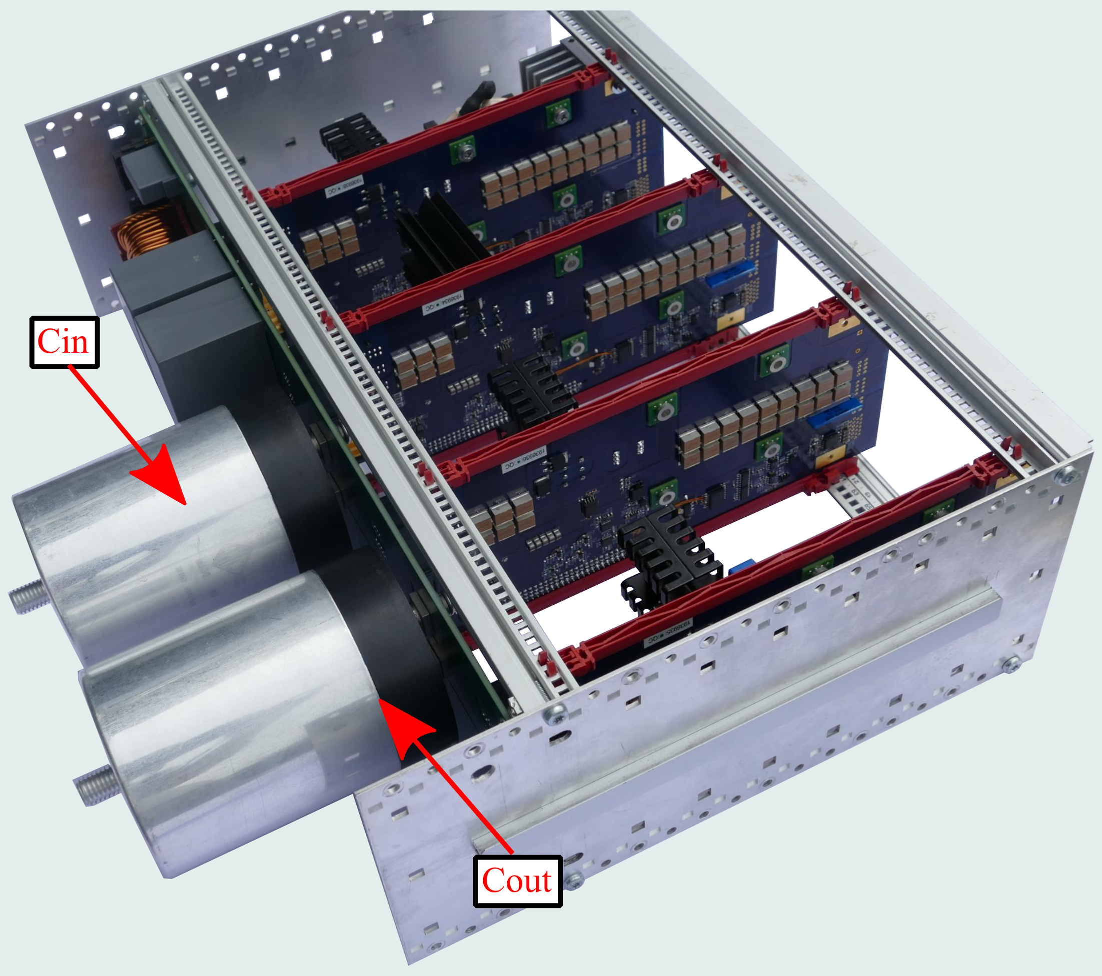
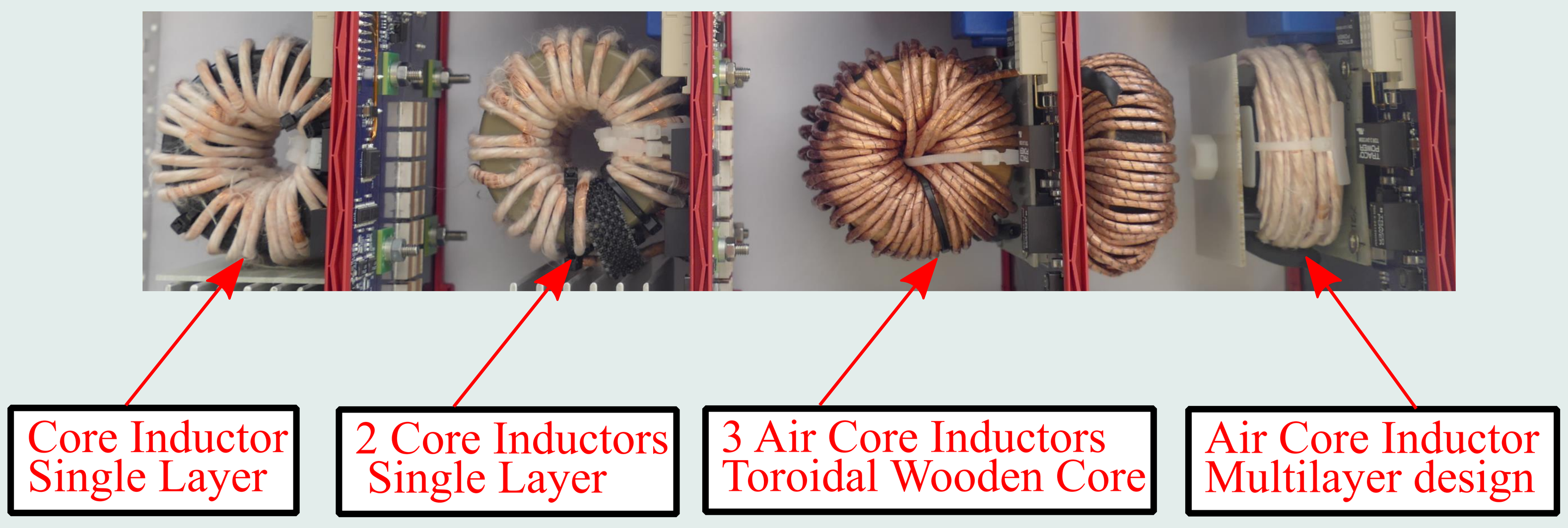


Figure : Subrack Multichannel Setup

Inductor – Prototype Implementation



Construction of 50 µH inductor with various techniques – for goal accomplishments

Future Work

- Evaluating the thermal performance of the system
- Analyzing the interlinked dynamics of the multichannel system
- Assessing the inductor's performance both electrically and thermally
- Identifying the limits of the latest version

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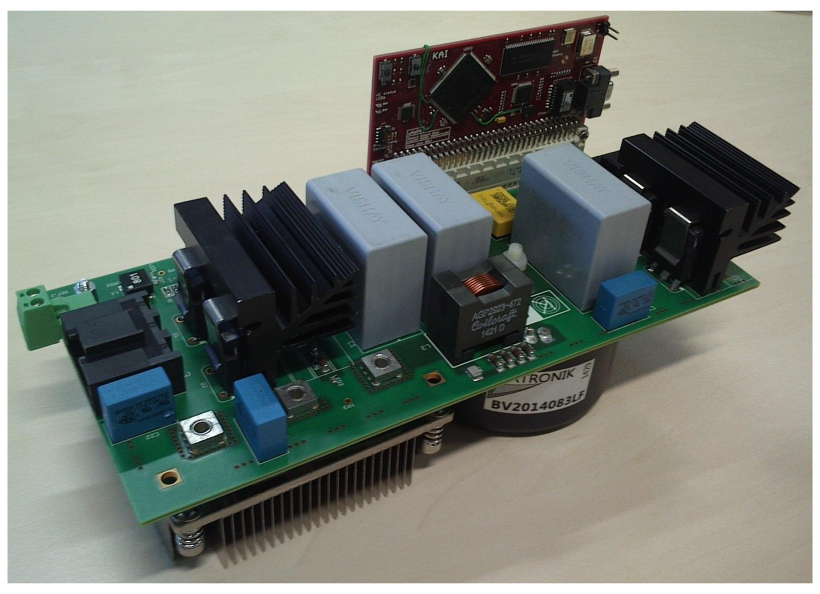
Application

GaN switching locus curve determination for application related reliability test system

PhD Student: *Ofner Sybille*

Supervisor: *Glavanovics Michael*



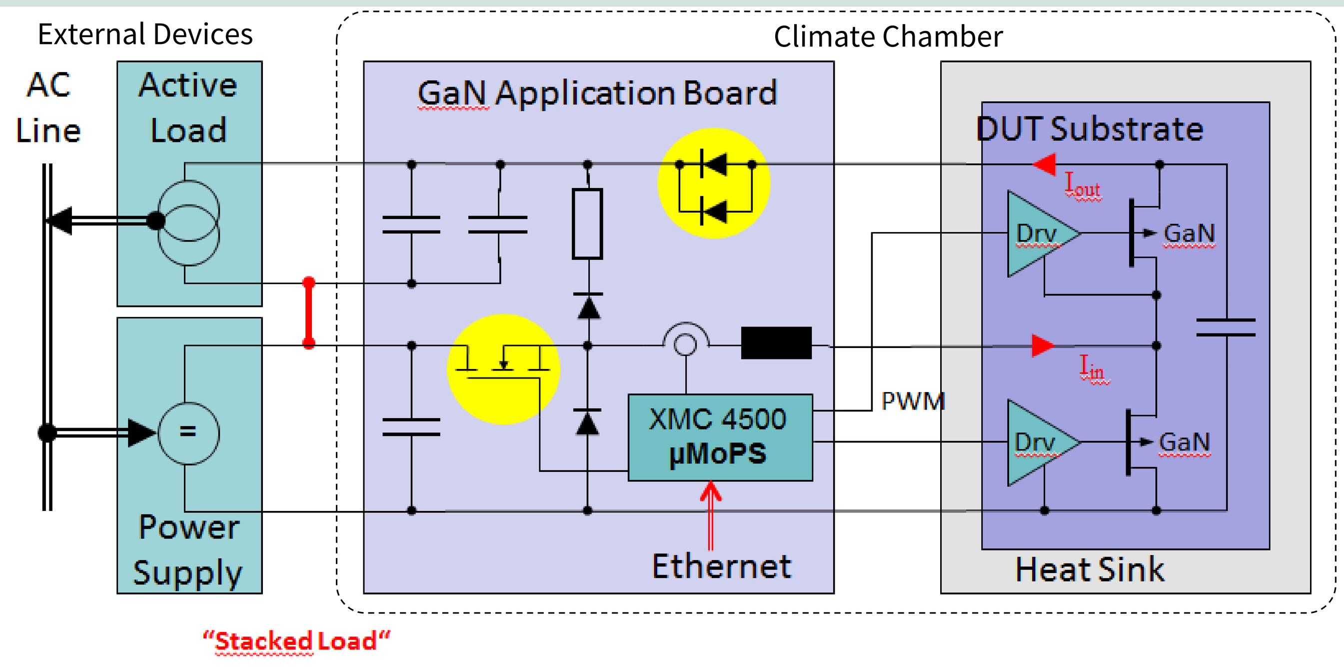
3x

- 3x 15 kW / 500 V / 90 A power supplies
- 3x 10.5kW / 500 V / 90 A active loads
- 3x 8 application test slots (48 GaN devices)
- 3 independently controlled test settings
- Climate chamber for ambient Temp. control

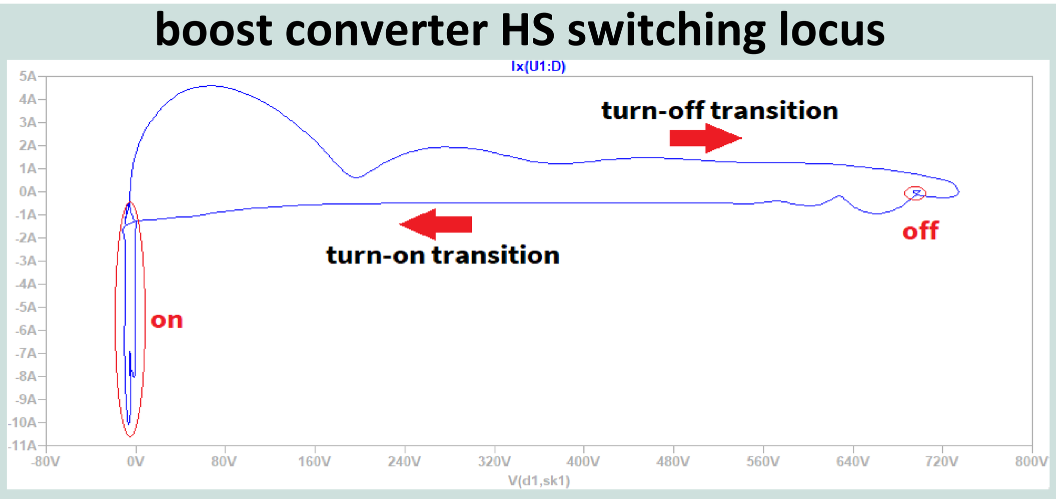
Introduction

Switching reliability testing is done to test the **reliability** and **robustness** of **GaN devices**. To support the research of GaN devices a **multipurpose application related reliability test system** was introduced by KAI.

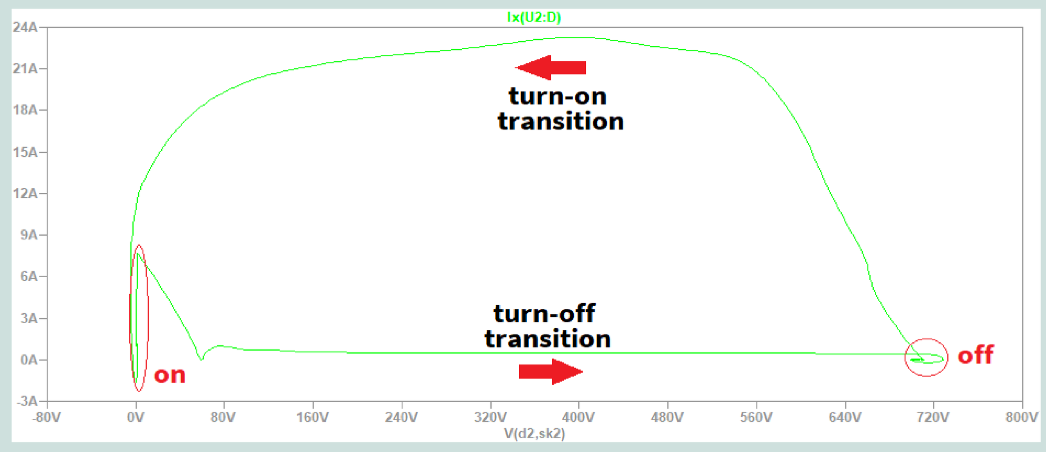
In line with the **JEDEC JEP180** guideline the **switching locus curve** is used to determine the level and type of switching stress applied to the device.

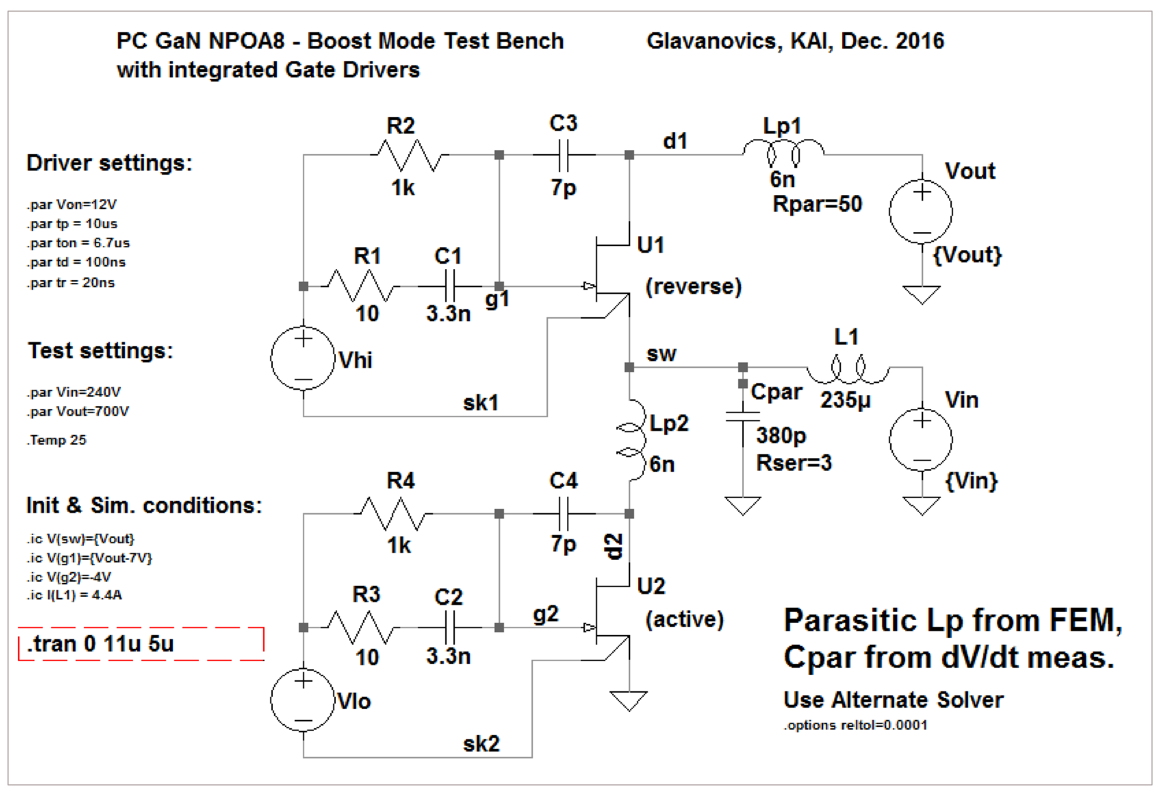


boost converter HS switching locus

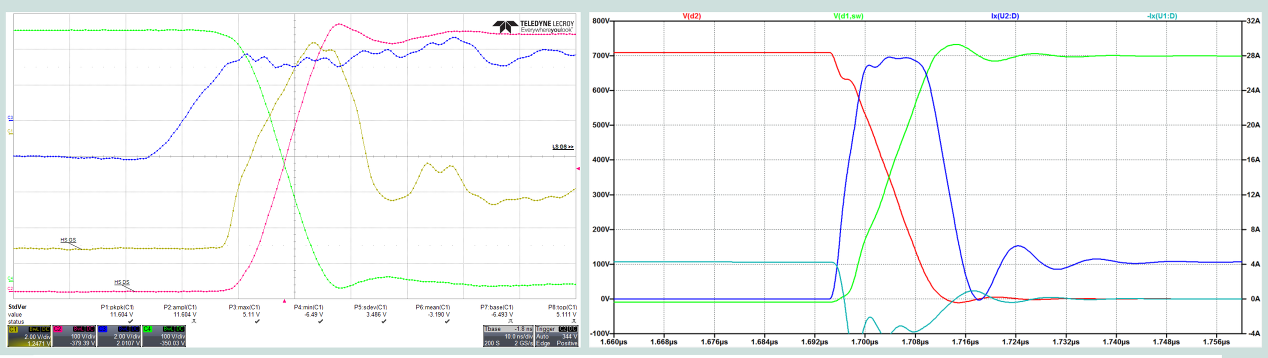


boost converter LS switching locus





low side turn on measurement vs. simulation



Methodology

- Simulations of the GaN device stress test circuit are done in **SPICE**
- parameter extracted from **lab characterization** (Cpar) and **FEM** simulations (Lp1, Lp2)
- Rpar, Rser adjusted for proper damping
- Cp adjusted for proper turn-on dV/dt
- Vds is verified with **scope measurement**

Research Topics

- hard/ soft switching **circuit topologies**
- **sensing techniques** for in-situ dynamic measurements with real time acquisition of relevant stress quantities
- **protection concepts** for a fast malfunction detection to prevent destruction of any part of the test system
- **Electromagnetic compatibility** needs to be checked due to the high switching frequencies, the high voltages and the interaction between the DUTs

Next Steps

- design of **application board** which can be a step up or step down converter
- **soft switching** circuit concepts **lab set up**
- redesign of the **MV DUT substrate** with **smaller** commutation loop **inductance** and gate driver with **smaller dead time**
- **publication** of results

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Application

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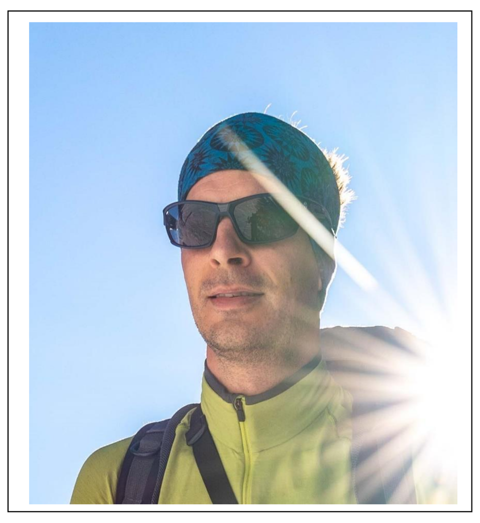
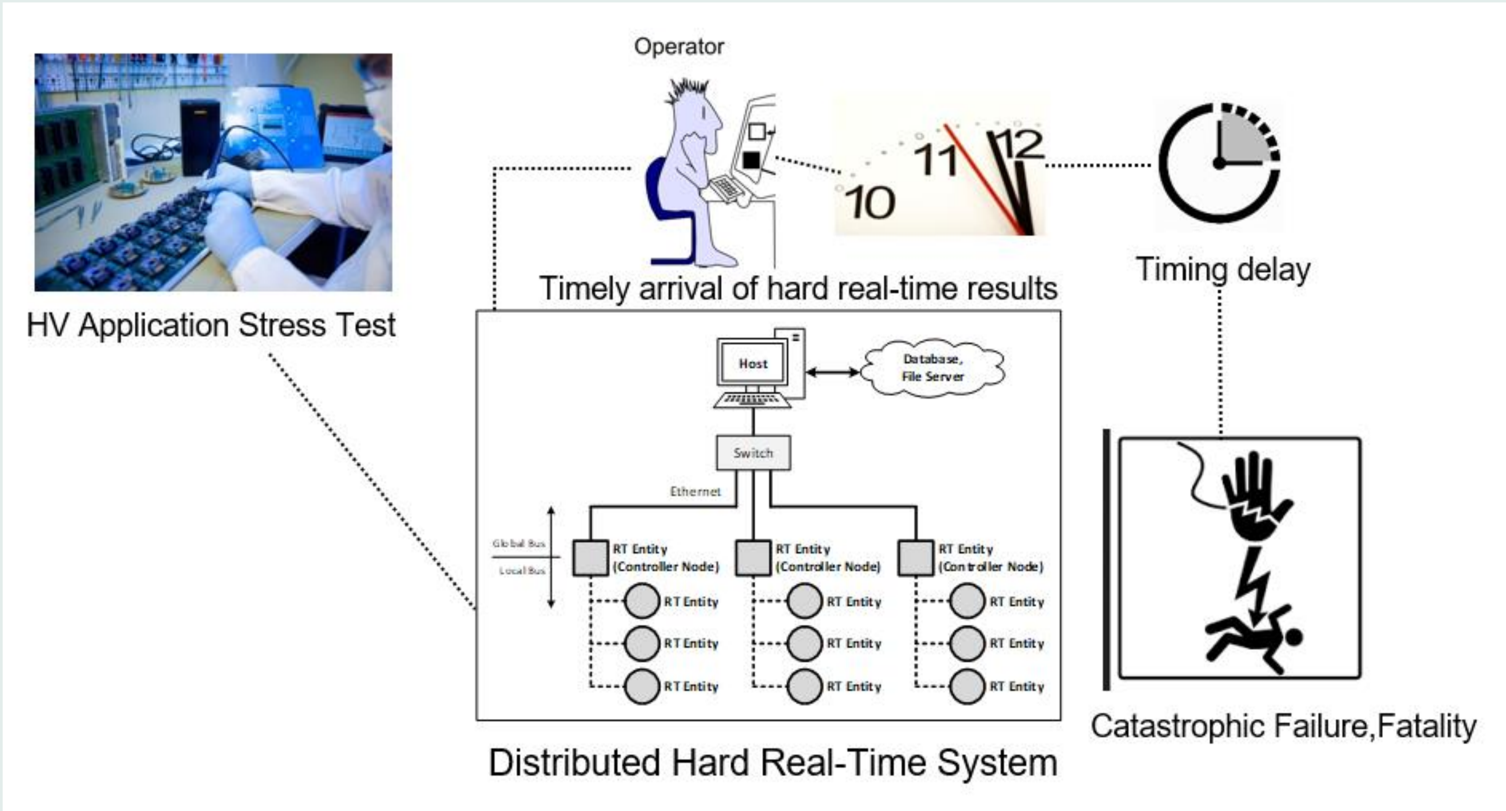


Temporal Fault Analysis of a Distributed Hard Real-Time System for Application-oriented Stress Tests

Introduction



Research Questions

RQ.1. What are the faults that affect the temporal behaviour of the distributed hard real-time system?

RQ.1.1. How to detect and handle the timing faults ?

RQ.2. How to achieve efficient measurement data transmission from the real-time entities to the controlling node during timing failure?

RQ.2.1. How to identify the failed nodes and which approach suits to handle the timing failure ?

RQ.3. How to improve the user control over the measurement data to access the application stress test ?

Methodology

Measurement Campaign
↓
Identify Distribution
↓
Estimate WCET bound
↓
Execution Time Schedule
↓
Statistical Timing Fault Model

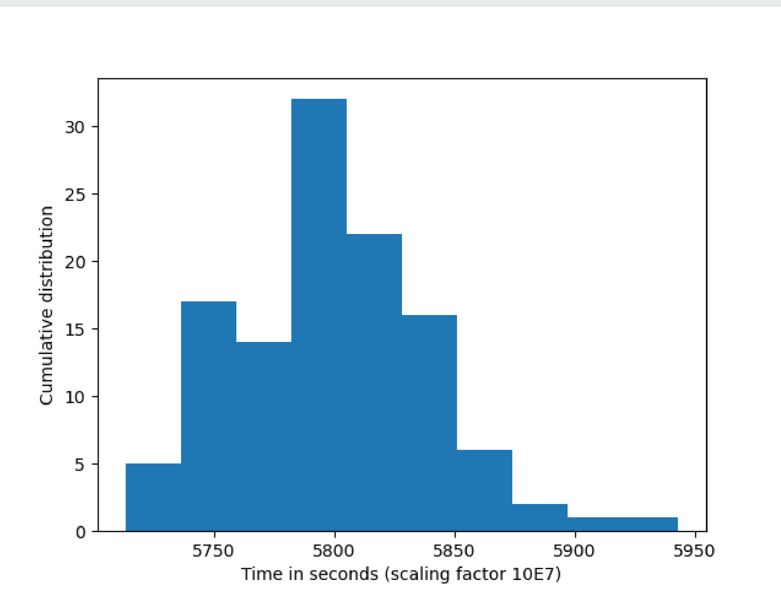
- Schedulability improvement from the WCET bound estimate
- Event control and Message protocol service using global determinism
- Implementation of temporal redundancy and self-checking mechanism
- Fail-silent strategy to counteract the unit of failed nodes

Results-I: Measurement Campaign

Events	Time with Load (µs)	Time without Load (Tiny Host) (µs)
Config	1.277 – 1.306	-N.A-
Temp	5.7134 – 5.9423	5.557-5.61

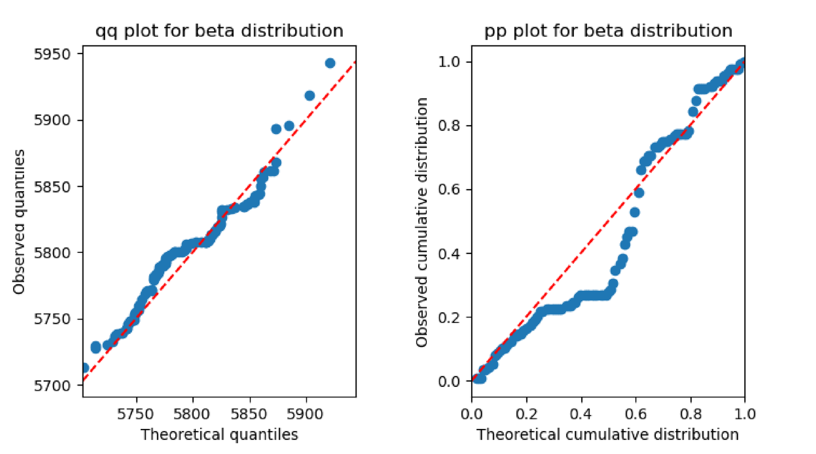
Software Functions	Time (in µs)	Bound Estimates (in µs)
handle_FSM	Net Time from i-system Trace: 5.43187	-N.A-
Temp	5.7134 – 5.9423	BCET bound – 5.7384 WCET bound – 5.8732

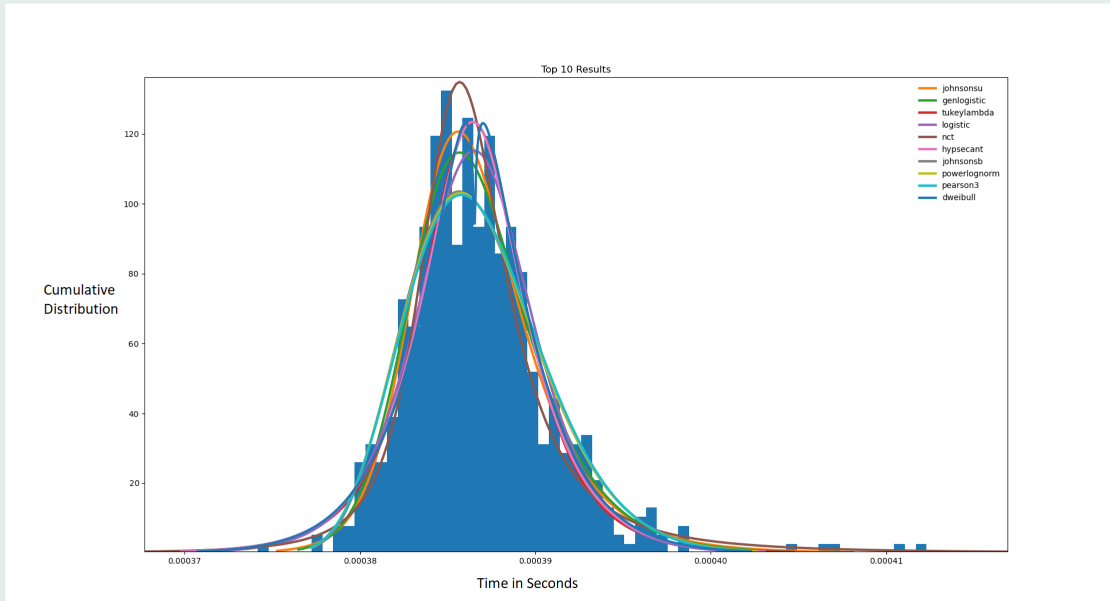
Results-II: Data Visualization



- QQ plots to validate plot data to theoretical quantiles

- PP plots to compare observed cumulative proportions to the expected probabilities





- Goodness of the fit for the distribution of the execution time values is determined by chi-squared test
- BCET bound and WCET bound obtained by process capability calculations

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