IPextreme

Product Brief

TriCore

Licensable 32Bit Microcontroller Core

The ***Infineon TriCore™*** is an innovative, award-winning processor solution unifying the features of real-time microcontrollers, computational power of DSP and the price/performance benefits of a superscalar RISC. TriCore's modular system architecture facilitates the design of true system-on-chip solutions by enabling flexible integration with on-chip high-density memories, application specific peripherals and customer logic.

TC1MP-S is the synthesizable implementation of the TriCore architecture and is now available as an XPack from IPextreme. The XPack is a complete configurable subsystem (available in either VHDL or Verilog) with an industry standard AMBA AHB interface, enabling simple integration into the wider platform, saving engineering time and effort to market.

MCU Features

- Fast context switch & low interrupt latency
- 16-bit and 32-bit instruction formats
- Powerful bit manipulation support

DSP Features

- Sustained throughput of two 16x16 MACs per clock
- SIMD packed arithmetic and zero overhead loops
- DSP addressing modes and saturated math

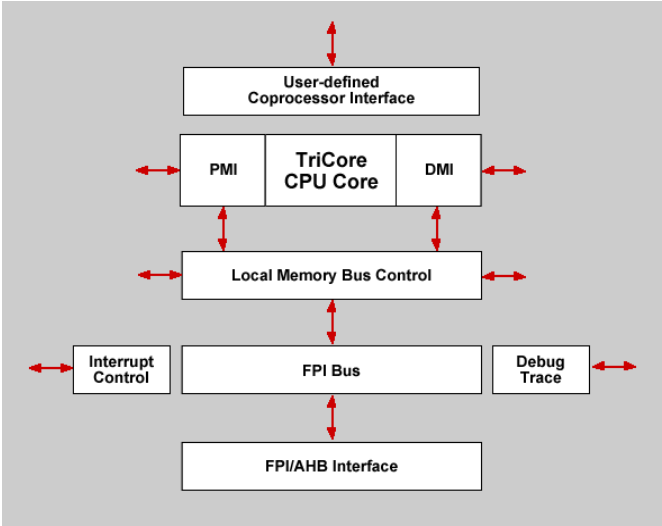
Processor Features

- 32-bit load-store Harvard architecture
- Superscalar execution
- 16 address and 16 data registers

TriCore Benefits

- Integrated MCU-DSP instructions in one core
- Fast and efficient processing of multiple tasks on one engine
- Low code size and inherent high level language support
- One development toolset for both MCU and DSP tasks
- Higher flexibility and lower cost

Block Diagram



TriCore Units & Interfaces

Superscalar Four-Stage Pipelined CPU

- 32-bit Load/Store Harvard Architecture
- 3 pipelines: Arithmetic, Load-Store, & Loop
- Single instruction Multiple Data capability

Control Features

- Single-bit addressing and manipulation
- Extract and insert data field instructions
- Fast context switching (from 4 cycles)
- 16 & 32-bit instructions, intermixable without boundary penalty

DSP Features

- Dual 16-bit Multiplier Accumulators
- Zero overhead loops
- Addressing: Circular, bit-reverse, register indirect with post & pre-increment
- Rounding, truncation, saturation, signed fraction support

Memory Protection

- Native protection scheme
- Optional MMU Coprocessor Interface
- Up to 3 coprocessor available
- Floating Point coprocessor available

Program Memory Interface (PMI)

- 64-bit interface for up to 64KB of configurable, tightly coupled cache/scratchpad memory

Data Memory Interface (DMI)

- 128-bit interface for up to 64KB of configurable, tightly coupled cache/scratchpad memory

Local Memory Bus (LMB)

- 64-bit data, 32-bit address
- Runs at CPU clock speed and supports 8, 16, 32 and 64-bit transfers
- Support for dual external interfaces Flexible Peripheral Interface (FPI) Bus
- 32-bit address and data de-multiplexed
- Single and multiple transfers: 8, 16 and 32-bit

Interrupt Controller

- Programmable: Up to 255 Interrupt priorities/sources

Debug Interface for Advanced Emulation

- Access to internal registers and memory through JTAG port
- Hardware, software and external breakpoints
- Support for trace functionality

— Tricore XPack —

XPack is a new innovative technology from IPextreme for packaging IP cores which enables customers to integrate IP as quickly and easily into their designs as possible. The new IPextreme lightweight technology for packaging IP is based on the familiar metaphor of a datasheet which contains all the descriptions and diagrams one would expect from a datasheet, but in reality, it is the cockpit by which users interact with the IP. Customers change configuration parameters or modify timing information by updating fields on the interactive datasheet.

IPextreme packages all its products using this technology.

XPack Features

- Automatic configuration source code based on user selectable options for both hardware and software parameters
- Generation of a instantiation template based on user configuration for the SoC design
- Generation of synthesis scripts and constraints for major EDA synthesis tools.

Tricore XPack Contents

- RTL source code the baseband controller
- Integration test bench
- Self-checking integration tests
- Extensive user documentation

For More Information:

IPextreme - Silicon Valley Headquarters
300 Orchard City Drive
Suite 102
Campbell, CA 95008 USA

Phone: (800) 619-0618 Fax: (408) 850-4902
Email: info@ip-extreme.com

IPextreme, Inc.,
300 Orchard City Drive
Suite 102
Campbell, CA 95008
USA
(800) 619-0618