Technical Presentation

November 2002

TriCore™
32-bit Unified Processor
TriCore Value Proposition

TriCore™ is a 32-bit superscalar unified MCU-DSP processor architecture, with fast interrupt response, optimized for cost sensitive, real-time embedded systems. It is available as a licensable core in both VHDL and Verilog.
Best-in Class Performance

TriCore™ is ONE core that offers:

- Best-in-class microprocessor performance – 1.5 MIPS/MHz
- Best in class controller performance - 2 cycles context switching
- Best-in-class DSP performance - 2 taps/cycle for FIR filters

www.infineon.com/tricore
Unified Processor Reduces Complexity & Cost

- 1 processor does the work of 2. No need for inter-processor communication
- Dynamic assignment of DSP vs. controller code in response to changes in the system requirements
- Fast context switch is the key
- Reduced number of resources (no duplications)
- Smaller, simpler silicon

RTOS + DSP + App

TriCore™

Memory | I/O

OEM Product

1 CPU
1 OS
1 Toolset

• Faster to Market
• Higher Flexibility
• Lower Cost
Target Segments

Automotive
- Engine Management
- Transmission Control
- ABS
- Active Suspension
- Infotainment
- X-by Wire

Industrial Control
- Robotics
- PLC’s
- Servo-Drives
- Motor Control
- Power-Inverters
- Machine-Tool Control (CNC)

Data Storage & Processing
- Hard Disk Drives
- Tape Drives
- Scanners
- Digital Copiers
- FAX Machines

Telecom/Datacom
- Communication Boards (LAN)
- Modems
- Mobile Communication
- Switches
- Routers

Consumer
- DVD / CD-ROM
- HDTV
- Set Top Boxes
- Games
- Printers
TriCore™
Unique 3-in-1 Feature Set!

Microcontroller
• Fast interrupt response
• Fast context switch
• Low code size through use of 16-bit & 32-bit instructions
• Powerful bit manipulation unit
• Powerful comparison instructions
• Integrated peripheral support

DSP
• Sustainable single-cycle dual MAC
• Packed/SIMD instructions
• DSP addressing modes
• Zero overhead loops
• Saturation
• Rounding
• Q-Math

RISC Processor
• 32-bit load/store Harvard architecture
• Super-scalar execution
• Shallow 4-stage pipeline
• Uniform register set
• Single data-memory model
• Memory protection
• C/C++ and RTOS support
TriCore™ Core Roadmap

Performance

TC 3
1500MIPS

TC 2
600MIPS

TC 1 v1.3
250MIPS

TC 1 v1.2
100MIPS

2000 2001 2002 2003

Compatibility

TC1Modular
Softmacro Available

Performance / Power Enhancements

TC1ML
Low Power Small Footprint
The Infineon Open Licensing Program (OLP)

Infineon has created a licensing program which allows semiconductor companies, OEMs and design houses to gain access to Infineon IP.

This program will ensure that Infineon Cores become industry standards with:

- A broad tool partner base
- A wide range of application software
- A choice of world wide design partners
- Multiple foundries

www.infineon.com/olp
SOC Design Trend: Step-up on a Platform!

Q. Why a platform?
A. Because Designers need a fast, easy and reliable way to complete their system

- Complete, silicon tested system based on one or more open standard buses
- Configurability to allow optimisation for both performance & cost
- Extensive library of tested and proven building blocks in the form of synthesizable IP products
- Complete set of powerful, easy to learn and use tools for configuration, simulation, verification and implementation
- Process-Independence
Basic TC1MP-S Configuration

TC1M = CPU + PMI + DMI
Verified in >10 Silicon Implementations

PMI: Program Memory Interface

DMI: Data Memory Interface

LMBh: Local Memory Bus hub
Fast local bus operating at CPU speed

FPI: Flexible Peripheral Interface
Large number of pre-verified peripherals available from Infineon

LFI: LMB to FPI Interface

ICU: Interrupt Control Unit
Interrupt controller (255 sources)

Debug: Debug/Trace Interface Support

BCU: Bus Control Unit
FPI Arbiter

FPI2AHB: FPI to AMBA Bridge

- Standard Interfaces to the FPI bus are provided free for SOC implementations
- Program Memory (P_MEM) & Data memory (D_MEM) configurable at build-time in respect to the amount of used memory and its partition as cache &/or scratch-pad RAM
- The Memory Management Unit (MMU) &/or Floating Point Unit (FPU), &/or FPI2AHB Bridge, is selectable at build time
Structure of a TriCore-based SOC

Key
- required
- optional

- TC1M
  - CPU + PMI + DMI

- TC1MP-S
  - configurable

- AMBA Bridge

- User-defined Coprocessor

- P-Tag
- D-Tag
- MMU
- ICU
- LMBh
- BCU
- LFI
- EBU
- D-RAM
- P-RAM
- PLL
- STM
- UDL
- ASL
TC1MP-S: General View & Connections

Data Tag Interface

Program Tag Interface

MMU Interface

Program Memory Interface

Memory BIST Interface

Interrupt Interface

FPI Bus

Debug Interface

Clock Reset & Control

Coprocessor Interface

Data Memory Interface

Local Memory Bus Interface

FPI Bus Interface

TC1MP-S

P-TAG  MMU  D-TAG

PMI  CPU  DMI

FPU  LMBh  CPS

TC1M
TC1MP-S: Silicon Proven Softmacro

SOFTMACRO

TC1MP-S

P-TAG  MMU  D-TAG
PMI  CPU  DMI
FPU  LMBh  LFI  CPS
FPI Bus

TC1M

MEMORY

24K P-SPRAM
24K D-SPRAM
8K P-cache
8k D-cache

HARDMACRO

10.3 mm² - 0.18µm
150 MHz w/c

SILICON

TC11IB

PXF 4225

TriCore

Infineon Technologies
Accelerating Implementation

- TriCore TC1MP-S based Hardmacro
  
  TC1M = CPU + PMI + DMI

- 32kBytes total memory
  
  16k Data, with 8k Cache
  
  16k Program, with 8k Cache

- MMU

- LMBH, LFI, ICU, Debug

- Area ~ 8.44 mm² (0.18µm)

- Frequency: 200 MHz
  
  (1.62V, 125C, typical 0.18µm process)

- From spec freeze to tape/out in 4 weeks

ARM922T, which has only 8K caches on each side and no protection mechanism, no DSP extensions nor the equivalent of ICU, Debug and LFI is listed at 8.1 mm²

TriCore TC1MP-S: Points of Interest

- **TC1M**
  
  *The heart of the system*

- **LMBh, LFI**
  
  *The glue that binds the system*

- **Memory**
  
  *Have it your way!*

- **Exceptions**
  
  *Simply the best system available*

- **Floating Point Unit (FPU)**
  
  *IEEE 754 Compatible*

- **MMU**
  
  *Memory Management Unit*

- **FPI**
  
  *The gateway to a wealth of pre-verified IP’s*

- **Debug System**
  
  *Easy & Powerful*

- **Software Development Tools**
  
  *Many to choose from*

- **Benchmarks**
  
  *We are better and we can prove it!*
TC1M: Block Diagram

- 32-bit Load/Store Harvard Architecture
- Superscalar Execution - Issue Up To 3 Instructions Simultaneously
- Add Customized Instructions Using Coprocessors
- 32, 32-bit General Purpose Registers (GPRs)
- Powerful Bit Manipulation Unit
- Fast Interrupt Response
- SIMD Capabilities
- Built-in Protection System
- Built-in Multiprocessing Capabilities
TC1M: The Pipelines

- TriCore is the only 32-bit Superscalar Licensable Core
- Superscalar Processing means the ability to issue more than 1 instruction per clock cycle – TriCore can issue up to 3 instructions in parallel with automatic data resource hazard checking and handling.
TC1M: Code Size

- 32-bit & 16-bit Instruction Formats
- 30% - 40% Code Size Reduction Over 32-bit Format Only
- Two Formats Can Be Freely Intermixed - No Mode To Change
- 16-bit Instructions Are Subset Of 32-bit Instructions & Are Automatically Generated During Compilation
- Many 3-Operand Instructions Available

![Code size - Lower is better](chart)

**Infineon internally generated benchmark for a general storage application**

- ARM7TDMI
- TC1M Compiler Settings Code Optimised
- TC1M Compiler Setting Speed Optimised
TC1M: Power Management

The Power Management is under software control.

TC1M implements 3 power management modes:

- RUN Mode
  The system is fully operational, all clocks are enabled

- IDLE Mode
  The CPU & memories clock is disabled

- DEEP SLEEP Mode
  All the clocks are turned-off
LMBh, LFI & CPS

- **LMBh**
  - Synchronous, pipelined bus with variable block transfer support
  - 32-bit address, 64-bit data
  - Central, simple per cycle arbitration
  - Address pipelining

- **LFI**
  - Bi-directional bridge between the LMB and the FPI bus
  - Address decoding and translation
  - Flexible LMB/FPI clock ratio support

- **CPS**
  - Provides emulation and trace support
  - Provides a complete Interrupt Controller
TriCore TC1MP-S Memory

- TriCore’s 4GB of address space is divided into 16 regions or segments (0 through to 15), each of 256MB

- TriCore implements a hierarchical, linear memory model using the Little Endian convention

- The memory can be located at 3 levels:
  - **Internal**
    Harvard-type, 1 cycle access memory for time-critical applications
  - **Local**
    unified memory, connected directly to the LMBh for improved performance
  - **External**
    unified memory (connected through an External Bus Unit (EBU))

• EBU & External Memory can be connected to the LMBh if necessary.
• The Harvard architecture can be extended to the local and/or external memory
TriCore TC1MP-S Exceptions

There are 3 categories of exceptions:

– Interrupts (handled by the ICU)
  - Selectable number 3 / 15 / 63 / 255, each with its own priority
  - Arbitration independent from CPU operation
  - Vector interrupt support

– Traps
  - Allows the CPU to service conditions that are critical and that must not be postponed

– Calls

All exceptions have in common a fast context switch mechanism, that takes advantage of a wide 128b bus to data memory.
TriCore TC1MP-S FPU

- IEEE 754 compatible
- Supports only single precision
  - Small area: 0.3 mm$^2$ in 0.13µm process
- It is closely coupled to the Coprocessor interface
- Implements a pipelined design for fast execution
- The design scales to the same clock frequency as TC1M
TriCore TC1MP-S MMU

- 4 GByte virtual address space

- Addressing by direct translation or via Page Table Entries (PTE)

- Two addressing modes:
  - Physical
  - Virtual
  
  Physical page attributes override Virtual page attributes

- Implements 2 Translation Lookaside Buffers (TLB)
  - Supports 4 page sizes: 1KB, 4KB, 16KB and 64KB
  - Supports 4 to 128 table entries per TLB
FPI Bus Features

- Internal bus that connects TriCore core & internal peripherals
- Multimaster capability (up to 16 masters)
- Demultiplexed operation
- Clock synchronous
- Peak transfer rate of up to 400 MBytes/s (@ 100 MHz bus clock & 32-bit data bus)
- 32-bit wide address & data buses
- 8, 16 & 32-bit data transfers
- Single to multiple data transfers
Debug System

OCDS Level 1

- Embedded emulation: OCDS (On-Chip Debug Support)
  - Low cost concept
  - Available on all production chip
  - Controlled via a JTAG link

Features:
- Run Control
- Program breakpoint / trigger (4 channels)
- Read/Write on the fly
- Break on data access

OCDS Level 2 = OCDS Level 1 + Expansion

- OCDS + Trace expansion:
  - Enhanced concept

Features:
- Run Control
- Program breakpoint / trigger also in internal FLASH (4 channels)
- Read/Write on the fly
- Break on data access
- Triggered real-time trace of program flow
- Performance analysis
Debug System: OCDS Overview

- Breakpoints; Single Stepping
- Read/Write Access to the whole Address Space
- Connection to the Debugger including JTAG and Break-Interface
- Fast Tracing through transfers to External Bus
- Multi-Core Debugging possible across a single JTAG Interface
Infineon TriCore 32-bit Architecture

Applications / Boards / Software Modeling Tools / Training / Consulting

Software Generation, Debug & Calibration Tools

Operating Systems
Language Tools

- Optimized C/C++ Cross Compiler
- Full TriCore 2 Architecture support
- Enhanced DSP code generation
- Misra C code checking support
- Peripheral Control Processor support
- ANSI/IEEE-754 Floating Point Libraries
- Macro Assembler / Linker / Locator
- EDE, Debugger, Simulator
- Intuitive, fully Graphical User Interface
- Windows & Solaris support

www.tasking.com
Language Tools - Continued

- Optimized C/C++ Cross Compiler
- Japanese Automotive C extensions
- PCP support
- Macro Assembler/Linker/Locator
- Run-Time Error Checking
- Multi IDE, Debugger, Simulator
- Version Control System
- Intuitive, fully Graphical User Interface
- Windows & Solaris support

www.ghs.com
Language Tools - continued

- GNU based C/C++ Cross Compiler
- Macro Assembler / Linker / Locator
- Debugger, Simulator
- PXROS support
- Windows, Solaris & Linux support
- GNU source level debugger with GUI
- Virtual I/O file based support
- TGDB graphical user interface for
- Solaris & Linux

www.hitec-rt.com
## Hardware Tools

<table>
<thead>
<tr>
<th>Hardware Tool</th>
<th>Website</th>
<th>TriCore Support</th>
</tr>
</thead>
</table>
| **TRACE32-ICD**   | [www.lauterbach.com](http://www.lauterbach.com) | - High-speed link via Ethernet, ISA bus or LPT  
- Universal hardware for all supported debuggers  
- 64K frame trace extension up to 60 MHz for program flow reconstruction  
- Full OCDS Level 1 & HITEX Development Tools |
| **TANTO**         | [www.hitex.com](http://www.hitex.com)           | - USB (V1.1), Serial (115k Baud), Ethernet (10BaseT)  
- Highly Modular, Configurable  
- Up to 133MHz (200MHz in preparation)  
- Full OCDS Level 1 & Level 2 support |
| **VITRA**         | [www.ashling.com](http://www.ashling.com)        | - RS232 Serial Port (115Kbits/s), Ethernet (RJ45/10BaseT) & highspeed USB Interfaces  
- Powerful Real-Time Trace for TriCore program execution  
- User defined Debug mode priorities  
- OCDS Level 1 & Level 2 support |
Hardware Tools - continued

JDSnet / ET-TriCore

- Multi-threaded Windows application – Chameleon Debugger
- JDSnet/ET is a real-time, Transparent in-circuit JTAG boundary scan based emulator
- Serial, parallel or Ethernet connection

Universal Debug Engine

- High-speed CAN in a ROM or BSL-RAM monitor version with up to 1Mbps
- 400Mbps Communication Speed
- Serial, parallel or Ethernet connection
- Full JTAG / OCDS Level 1 support

www.signum.com

www.pls-mc.com

www.tektronix.com

www.agilent.com

• Inverse assembler support based on the TriCore Microprocessor Architecture

www.agilent.com
Expert Systems:
DAvE (Digital Application Engineer)

• Helps program Infineon microcontrollers that you want to use in your project. DAvE offers:
  • Intelligent wizards
  • Chip configuration
  • Automatic C-level templates generation (on-chip peripherals)
  • Interrupt controls

• Helps you compare and evaluate the different members of the Infineon C500 (8-Bit), C166 (16-Bit) and TriCore (32-Bit) families of microcontrollers.

• Access point to all standard knowledge associated with Infineon embedded technology expertise, by offering you context sensitive access in your development environment, to:
  • User's manuals
  • Data sheets
  • Application notes, etc.

• Connects and interacts directly with compilers to offer a fully programmable software interface and even come with an SDK Tool-chain, enabling you to add your own plugins!
Tooling Certification & Partner Programs

Certification & Test

TriCore Development Tools are supported by the Infineon Certification & Test Programme to ensure integrated tooling solution operation with vendor tool-chains.

Partner Programs

Infineon Development Tools information, updates, new releases and support is also available from the SPACETools program and web-page (www.spacetools.com). SPACETools is a database of all Infineon Development Tools, a buyers guide for developers.
TriCore DSP Library

TriLib

- Assist Application developers with standard algorithms
- Provide benchmarks for DSP applications
- Significantly reduce DSP application development time
- Compiler support
  - Implementation of common DSP algorithms which are delivered in source code
  - Hand-coded and optimized assembly modules
  - C/C++ callable compiler functions
  - Bit-exact reference C Codes for easy understanding and verification of the algorithms
  - Assembly implementation tested for bit exactness against C model
  - Workarounds implemented to take care of known core errors
  - Examples to demonstrate the usage of functions
  - Example input test vectors and the output test data for verification
  - Comprehensive Users manual covering many aspects of implementation
# Real-Time Operating Systems

<table>
<thead>
<tr>
<th>RTOS</th>
<th>SUPPLIER</th>
<th>PORT TOOLCHAIN</th>
<th>TRICORE PRODUCT</th>
<th>CODE SIZE (BYTES)</th>
<th>DISTRIBUTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>MicroC/OS- II</td>
<td>Infineon</td>
<td><img src="image" alt="Green Hills Software" /></td>
<td>✓</td>
<td>Not planned</td>
<td>5k-15k</td>
</tr>
<tr>
<td>CMX-RTX</td>
<td>CMX Company</td>
<td><img src="image" alt="TASKING" /></td>
<td>✓</td>
<td>On demand</td>
<td>~5k</td>
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<tr>
<td>Nucleus PLUS</td>
<td><img src="image" alt="Green Hills Software" /></td>
<td><img src="image" alt="TASKING" /></td>
<td>✓</td>
<td>On demand</td>
<td>25k-40k</td>
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<tr>
<td>OSE</td>
<td>OSE</td>
<td><img src="image" alt="TASKING" /></td>
<td>✓</td>
<td>On demand</td>
<td>?</td>
</tr>
<tr>
<td>PXROS</td>
<td>High Tec</td>
<td>GNU</td>
<td>✓</td>
<td>On demand</td>
<td>Application dependent</td>
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<tr>
<td>VxWorks</td>
<td>WindRiver</td>
<td>GNU</td>
<td>✓</td>
<td>On demand</td>
<td>60K-250K</td>
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<tr>
<td>Linux</td>
<td>Infineon</td>
<td>GNU</td>
<td>No</td>
<td>On demand</td>
<td>?</td>
</tr>
</tbody>
</table>
Linux – Project Goals

• Port Embedded Linux with real-time extensions to TriCore
• Provide a means for distributing, maintaining, and supporting the port once completed.
• Provide sample applications to validate the port.
• Provide a board support package for a TriCore evaluation board.
• Provide capability to extend the port and applications to future products based on the TC1M core & TC2.
Linux Port Project Deliverables

- Boot loader
- Low level device drivers
- Embedded Linux kernel with TCP/IP
- Standard Linux library
- Real-Time extensions
- Memory protection and MMU support
- Performance data
- File system support
- Utility box
- Shell and standard UNIX utilities
- Documentation
## System Comparison: TC1MP-S Vs. ARM1020E

<table>
<thead>
<tr>
<th>Feature</th>
<th>ARM1020E</th>
<th>TCMP-S</th>
</tr>
</thead>
<tbody>
<tr>
<td>Core</td>
<td>ARM10E</td>
<td>TC1M</td>
</tr>
<tr>
<td>I-Cache</td>
<td>32K</td>
<td>8K</td>
</tr>
<tr>
<td>D-Cache</td>
<td>32K</td>
<td>8K</td>
</tr>
<tr>
<td>I-SPR</td>
<td>0K</td>
<td>24K</td>
</tr>
<tr>
<td>D-SPR</td>
<td>0K</td>
<td>24K</td>
</tr>
<tr>
<td>64b internal I-mem I/F</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>64b internal D-mem I/F</td>
<td>Yes</td>
<td>128b I/F</td>
</tr>
<tr>
<td>MMU</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>Dual 64b bus I/F</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>Support for trace</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>Interrupts</td>
<td>2</td>
<td>255</td>
</tr>
<tr>
<td>Local-to-peripheral bridge</td>
<td>No</td>
<td>Yes</td>
</tr>
<tr>
<td>Coprocessor I/F</td>
<td>Yes</td>
<td>Yes</td>
</tr>
</tbody>
</table>
System Area Comparison

(mm² in 0.13µm process)
Using data from the EEMBC telecom benchmark (out-of-box)

http://www.eembc.org/

*Note: TC1M data based on existing silicon (TC11IB)*
TriCore TC1MP-S: Summary of Benefits

- 64-bit performance with 32-bit area / power / cost
- Compact Code Size (16b/32b mix)
- Powerful built-in DSP capabilities
- Outstanding Real-Time Performance
- Not only CPU Core, but also System IP & Peripheral Library
- Tested on a variety of Process Technologies
- Hardware Assisted Debug Support
- Soft Core, easy Process Migration
- Silicon proven
- Solid Roadmap
Never Stop Thinking.