

Trilith IC 3G - H-Bridge Demo Board

Version 1.1

Demo Board Description

V1.0, 2011-10-18

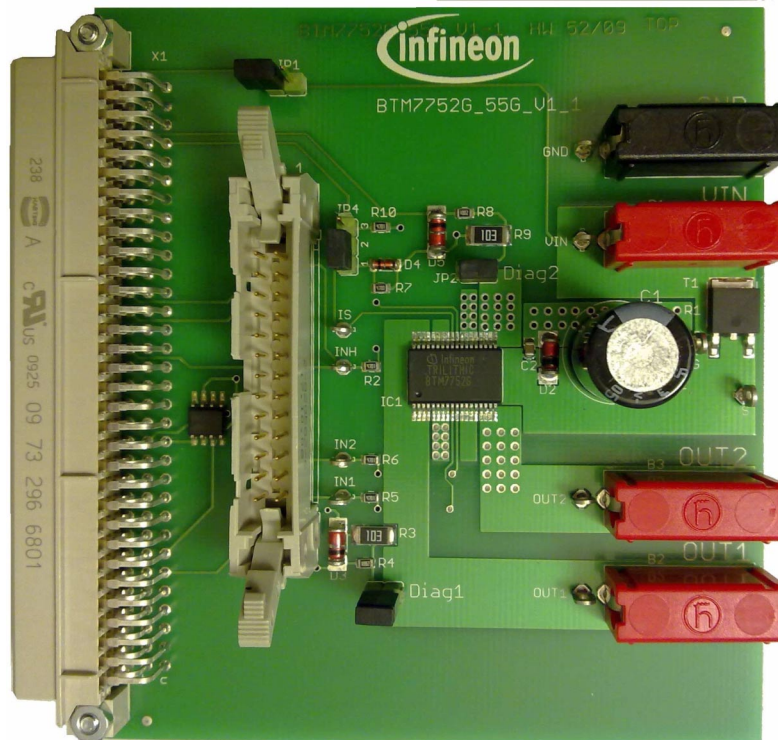


Figure 1 Demo board (top view)

1 General Description

The Trilith IC 3G - H-Bridge Demo Board contains one Trilith IC in a typical H-bridge configuration including peripheral components and reverse polarity protection. Control signals can be supplied via a 26 pin header connector or a 96 pin board connector. The board is compatible to all members of the Trilith IC 3G family in a PG-DSO36 package (like BTM7752G and BTM7755G).

1.1 Layout Considerations

Special care has been taken to the PCB layout to minimize stray inductances in the power bridge design as it is necessary in all switched high power bridges. The Trilith IC has no separate pin for power ground and logic ground. Therefore it is recommended to assure that the offset between the ground connection of the slew rate resistor, the current sense resistor and ground pins of the device is minimized. In this board this is achieved by routing the high current traces from the 470 μ F supply capacitor to the bridge so that the area spanned by the loop is as small as possible. In addition a ceramic capacitor from VS to GND close to the device is implemented to provide current for the switching phase via a low impedant path and therefore reducing noise and ground bounce.

It also needs to be assured that all supply pins are shorted and the voltage offset between the supply pins on both sides of the package is as small as possible. This was done on this board by a direct connection of the supply pins (VS) via a wide trace below the package and mid-tap to the supply capacitor.

The digital inputs are protected from excess currents (e.g. caused by induced voltage spikes) by 10 k Ω series resistors.

1.2 Connector Pin Assignment

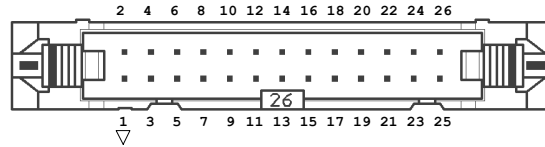


Figure 2 26 pin header connector (top view)

Pin	Signal	Description
1	IN1	Input of half-bridge 1
2	INH	Inhibit
3	IN2	Input of half-bridge 2
18	GND	GND
20	GND	GND
23	IS / ST	Current sense output or Status output (can be connected by jumper JP4 via sense resistor R7 to GND or via pull-down R10 to external Vdd (5V))
25	GND	GND
26	GND	GND
others	NC	Not connected

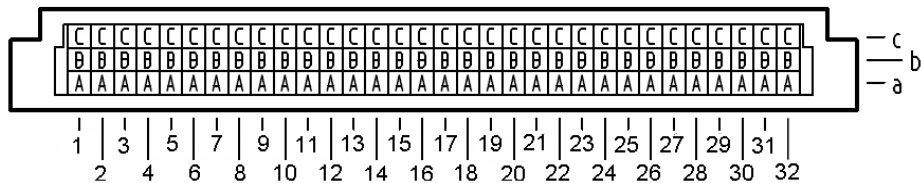


Figure 3 96 pin board connector (front view)

Pin	Signal	Description
A1	VBAT/vIN	VBAT going to external control board / starter kit
B1	GND	GND
C1	VDD	Vdd (5V) coming from external control board / starter kit
A4	OUT1	Output of halfbridge 1 - control signal going to external control board (clamped to 5V by on-board zener diode)
B4	OUT2	Output of halfbridge 2 - control signal going to external control board (clamped to 5V by on-board zener diode)
C4	IS / ST	Status output connected via JP4 (for use of BTM77x5G)
A12	IN1	Input of half-bridge 1
A13	IN2	Input of half-bridge 2
A15	INH	Inhibit
B20	SCL	Serail Clock Input of "board ID" EEPROM
C20	SDA	Serial Data Output of "board ID" EEPROM
C26	GND	GND
C27	IS	Current sense output connected via JP4 (for us of BTM77x2G)
others	NC	Not connected

1.3 Jumper Settings

Jumper	Description
JP1	Connects VIN (VBAT, supply voltage) to external control board / starter kit Default: not connected
JP2 (Diag2)	Connects OUT 2 (output of halfbridge 2) to pull-down resistor R3 and connector pin B4 Default: connected
JP3 (Diag1)	Connects OUT 1 (output of halfbridge 1) to pull-down resistor R9 and connector pin A4 Default: connected
JP4	Current sense output or Status output Pos.1 (pin 1-2): IS/ST connected to pull-down (sense) resistor (for BTM77x2G with current sense) Pos.2 (pin 2-3): IS/ST connected via pull-up resistor to external Vdd (for BTM77x5G with open-drain status) Default: Pos. 1 (BTM77x2G) Pos. 2 (BTM77x5G)

1.4 Board ID

The Trilith IC H-Bridge Demo Board features a two wire serial EEPROM (IC2) including a board ID to distinguish between different types of demo boards. The supply voltage VDD for this EEPROM (pin C1 front board connector) has to be supplied by the control board or starter kit. The serial clock input SCL (pin B20) has to be provided by the control board (microcontroller). The serial data output (pin C20) can be connected to an I/O of the microcontroller to read the board ID.

2 Schematic

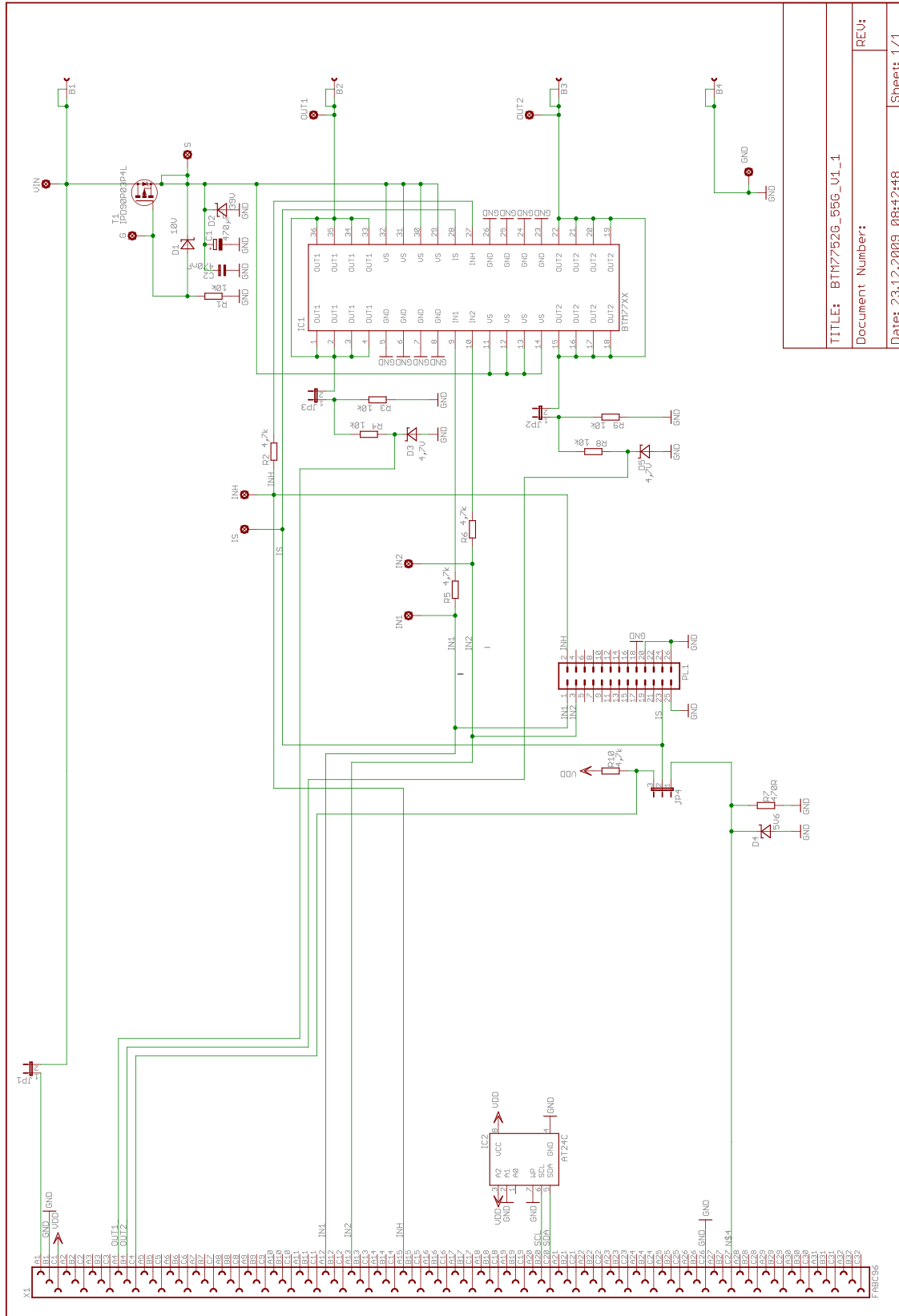


Figure 4 Schematic

3 Top Layer

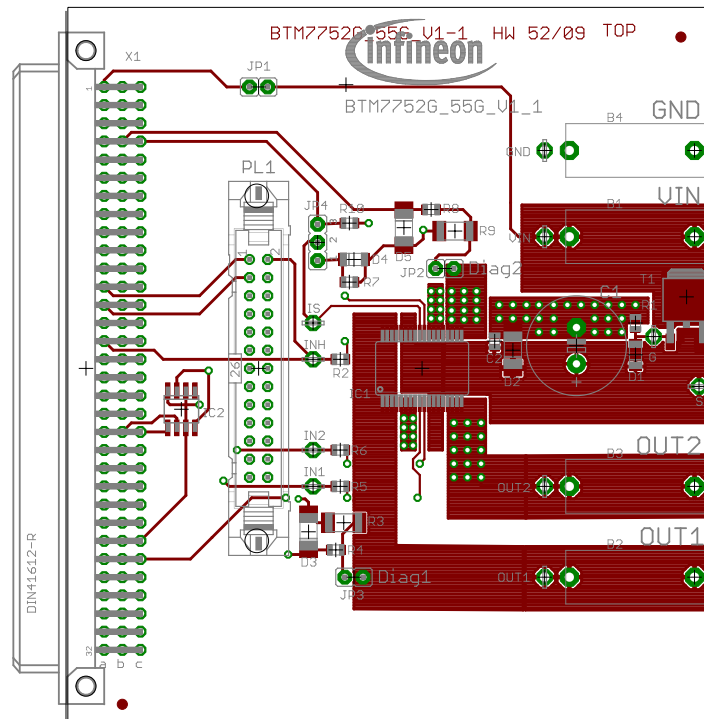


Figure 5 **Top layer**

4 Bottom Layer

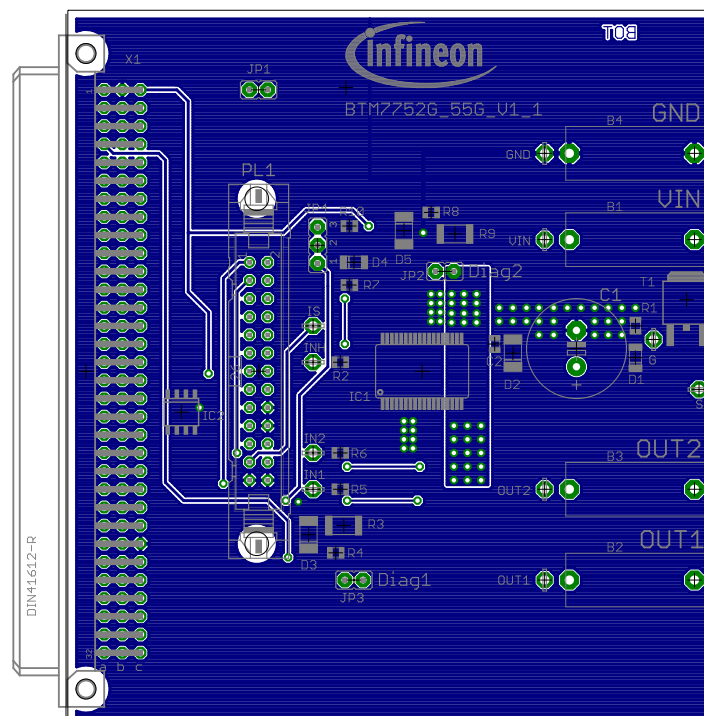


Figure 6 Bottom layer

5 Revision History

Trilith IC 3G - H-Bridge Demo Board

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Revision History Document: V1.0, 2011-10-18

Previous Version(s): -

Page	Subjects (major changes since last demo board revision V1.0)
	- changed T1 (reverse polarity MOSFET) to IPD90P03P4L - changed R3 and R9
	initial version of documentation

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