SmartLEWIS™ TRX

TDA5340

Migration from a TDA5240/35 design to a TDA5340 design

Application Note

Revision 1.1, 2012-06-20

Wireless Sense & Control

Edition 2012-06-20

Published by
Infineon Technologies AG
81726 Munich, Germany

Legal Disclaimer

The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics. With respect to any examples or hints given herein, any typical values stated herein and/or any information regarding the application of the device, Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind, including without limitation, warranties of non-infringement of intellectual property rights of any third party.

Information

For further information on technology, delivery terms and conditions and prices, please contact the nearest Infineon Technologies Office (**www.infineon.com**).

Warnings

Due to technical requirements, components may contain dangerous substances. For information on the types in question, please contact the nearest Infineon Technologies Office.

Infineon Technologies components may be used in life-support devices or systems only with the express written approval of Infineon Technologies, if a failure of such components can reasonably be expected to cause the failure of that life-support device or system or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.

TDA5340 Enhanced Sensitivity Transceiver TDA5340

Revision History: 2012-06-20, Revision 1.1

Previous Revision:

Page	Subjects (major changes since last revision)
	Register Content update to final TDA5340 design

Table of Contents

Table of Contents 4

1 Introduction 5

2 PCB Hardware Differences 5

3 Software Considerations 6

3.1 Power On Reset 6

3.2 SPI Communication 6

3.3 FIFO Handling 7

3.4 Interrupt Handling 7

3.5 Operating Modes 7

3.6 SFR Register Map 7

3.6.1 Registers Overview 8

1 Introduction

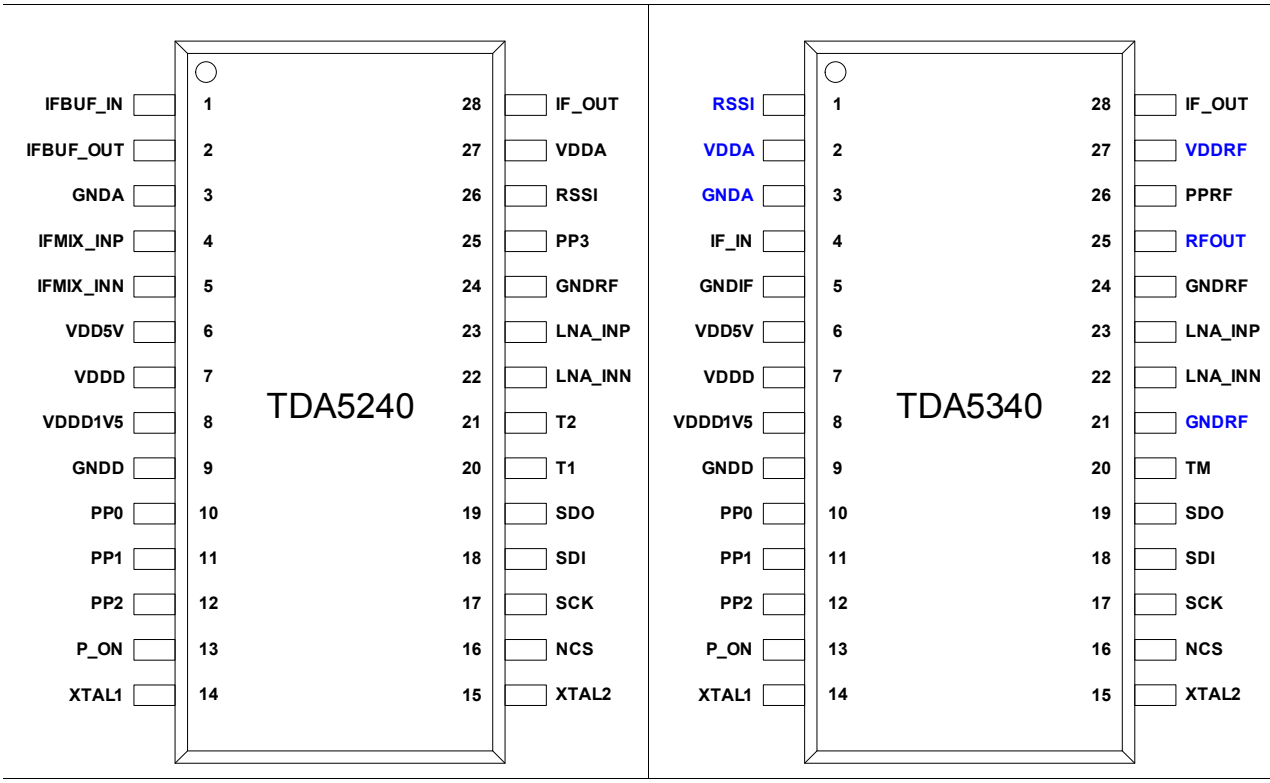
The TDA5340 transceiver is based on the TDA5240/35 receiver design and provides the same functionality on the receiver side except of some improvements like Antenna Diversity and Multiband frontend switching. The pinout of the TDA5340 allows a PCB design which can be used for the TDA5240/35 receiver as well as for the TDA5340 transceiver.

This application note describes the main differences of the TDA5340 transceiver compared to the TDA5240/35 receiver and explains the main topics which have to be considered to migrate from a TDA5240/35 receiver design to a TDA5340 transceiver design.

2 PCB Hardware Differences

As already mentioned the pinout of the TDA5340 transceiver allows a PCB design which can be either populated with a TDA5240/35 receiver or with a TDA5340 transceiver.

Table 1 Pin Out Comparison



Hardware trade-off and considerations when doing an universal PCB design for TDA5240/35 and TDA5340

- The analog RSSI pin of the TDA5240/35 is replaced by the PPRF pin in the TDA5340 and moved to Pin1.
  - An external solder jumper needs to be introduced if the analog RSSI is used by the application controller
  - Access to digital RSSI (which is anyhow recommended) via SPI with no trade-off
- 2nd external IF Filter pins removed
  - The TDA5340 does not support a second external IF Filter
  - The input for the IF signal has to be adjusted to the IFMIX_INP pin for the TDA5240/35.
- The output pin for the external IF Filter is used within the TDA5340 as additional supply input.
  - A solder jumper for VDDA has to be foreseen in the TDA5240/35 receiver design
- The PP3 pin of the TDA5240/35 receiver is on the TDA5340 transceiver used as the power amplifier output pin

  - Usage of an external LNA with enable of the PP3 pin must be done with the PPRF pin in the TDA5340 transceiver design.
- External load Capacitors for the Crystal circuitry
  - The TDA5340 transceiver has the permanently connected load capacitor integrated
  - Depending on the application, either the external capacitors can be removed completely (use only the internal load capacitors) or only the tighter tolerated external capacitors can be used (internal load capacitors are switched out of the circuit)
  - Crystal load capacitors has to be foreseen on the layout in case of the receiver design and can be saved (not populated) in the TDA5340 transceiver design.
- Antenna Matching
  - The TDA5340 transceiver supports an antenna switch by shorting the LNA input pins to ground which allows a quite easy migration from a receiver design to a transceiver design.
  - The matching components have to be changed
  - By using a SAW filter in the RX path only, the simple LNA input switches can not be used. A design with an external Antenna switch must be considered.

3 Software Considerations

The TDA5340 has of course different modes compared to the TDA5240/35 receiver due to the additional features within the TDA5340. The main differences are in the location and positioning of the register and bit positions.

3.1 Power On Reset

The Power on Reset procedure of the TDA5340 transceiver has not changed compared to the TDA5240/35 receiver.

3.2 SPI Communication

The SPI communication interface of the TDA5340 is compatible with the TDA5240/35 receiver. Of course additional functions needs to be implemented for the TX portion.

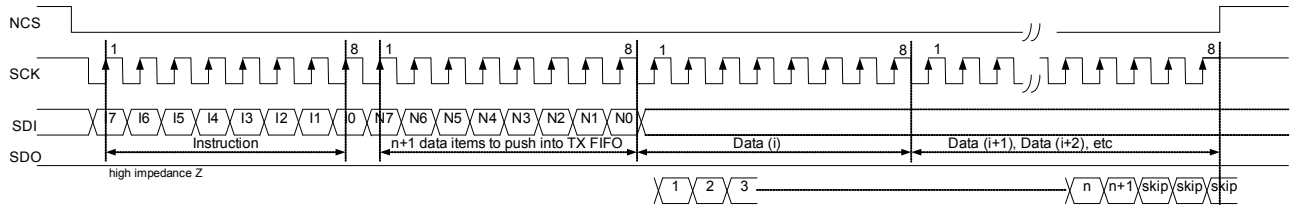


Figure 1 TX FIFO write

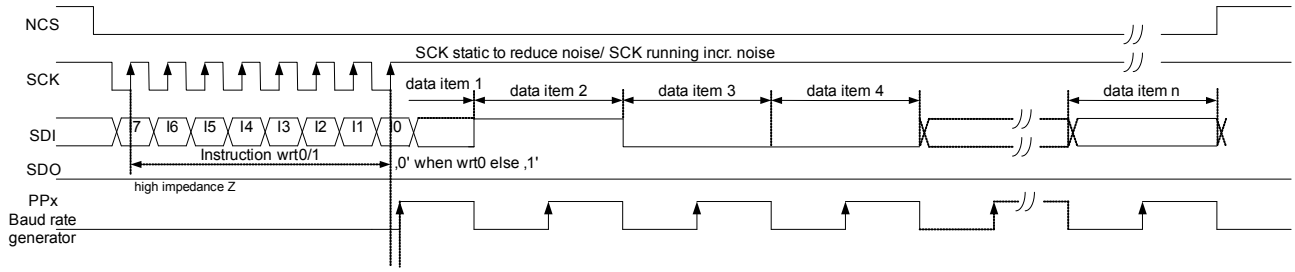


Figure 2 TX transparent command

3.3 FIFO Handling

The TDA5340 provides additional almost full and almost empty interrupts which enables easier FIFO handling. The FIFO size of the TDA5340 is increased from 256 bits to 288 bits.

3.4 Interrupt Handling

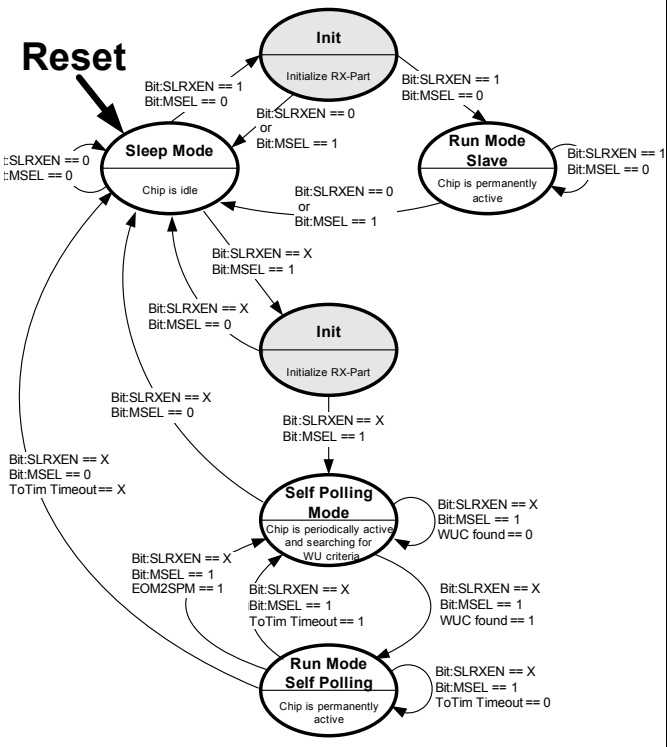
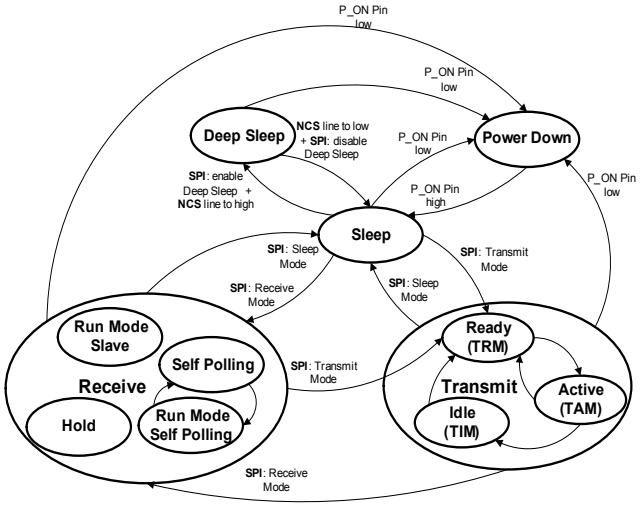
The TDA5340 has one additional interrupt status register which covers the additional transmit functionality together with the RX/TX FIFO fill interrupts and the new deep sleep mode information.

3.5 Operating Modes

The Self Polling Mode and the Run Mode Slave from the TDA5240/35 receiver are unchanged in the TDA5340 transceiver.To implement the transmit functionality of course the existing implementation of the TDA5240/35 operating modes needs to be adopted accordingly.

Within **Table 2**, the two different main state diagrams for the TDA5240/35 receiver and the TDA5340 transceiver are depicted.

Table 2 Mode Comparison

TDA5240/35	TDA5340
	

3.6 SFR Register Map

The following section shows the differences of the SFR registers between TDA5240/35 and TDA5340. Within the yellow marked registers some bits and functions are changed.

3.6.1 Registers Overview

Table 3 Registers Overview

Register Short Name	Register Long Name	TDA5340		TDA5240/35		Register Bit/Function Changes
		Offset Address	Reset Value	Offset Address	Reset Value	
A_MID0	Message ID Register 0	000_H	00_H	000_H	00_H	No
A_MID1	Message ID Register 1	001_H	00_H	001_H	00_H	No
A_MID2	Message ID Register 2	002_H	00_H	002_H	00_H	No
A_MID3	Message ID Register 3	003_H	00_H	003_H	00_H	No
A_MID4	Message ID Register 4	004_H	00_H	004_H	00_H	No
A_MID5	Message ID Register 5	005_H	00_H	005_H	00_H	No
A_MID6	Message ID Register 6	006_H	00_H	006_H	00_H	No
A_MID7	Message ID Register 7	007_H	00_H	007_H	00_H	No
A_MID8	Message ID Register 8	008_H	00_H	008_H	00_H	No
A_MID9	Message ID Register 9	009_H	00_H	009_H	00_H	No
A_MID10	Message ID Register 10	$00A_H$	00_H	$00A_H$	00_H	No
A_MID11	Message ID Register 11	$00B_H$	00_H	$00B_H$	00_H	No
A_MID12	Message ID Register 12	$00C_H$	00_H	$00C_H$	00_H	No
A_MID13	Message ID Register 13	$00D_H$	00_H	$00D_H$	00_H	No
A_MID14	Message ID Register 14	$00E_H$	00_H	$00E_H$	00_H	No
A_MID15	Message ID Register 15	$00F_H$	00_H	$00F_H$	00_H	No
A_MID16	Message ID Register 16	010_H	00_H	010_H	00_H	No
A_MID17	Message ID Register 17	011_H	00_H	011_H	00_H	No
A_MID18	Message ID Register 18	012_H	00_H	012_H	00_H	No
A_MID19	Message ID Register 19	013_H	00_H	013_H	00_H	No
A_MIDC0	Message ID Control Register 0	014_H	00_H	014_H	00_H	No
A_MIDC1	Message ID Control Register 1	015_H	00_H	015_H	00_H	No
A_IF1	IF1 Register	016_H	$A3_H$	016_H	20_H	Yes
A_WUC	Wake-Up Control Register	017_H	04_H	017_H	04_H	Yes
A_WUPAT0	Wake-Up Pattern Register 0	018_H	00_H	018_H	00_H	No
A_WUPAT1	Wake-Up Pattern Register 1	019_H	00_H	019_H	00_H	No
A_WUBCNT	Wake-Up Bit or Chip Count Register	$01A_H$	00_H	$01A_H$	00_H	No
A_WURSSITH1	RSSI Wake-Up Threshold for Channel 1 Register	$01B_H$	00_H	$01B_H$	00_H	No
A_WURSSIBL1	RSSI Wake-Up Blocking Level Low Channel 1 Register	$01C_H$	FF_H	$01C_H$	FF_H	No

Table 3 Registers Overview

Register Short Name	Register Long Name	TDA5340		TDA5240/35		Register Bit/Function Changes
		Offset Address	Reset Value	Offset Address	Reset Value	
A_WURSSIBH1	RSSI Wake-Up Blocking Level High Channel 1 Register	$01D_H$	00_H	$01D_H$	00_H	No
A_WURSSITH2	RSSI Wake-Up Threshold for Channel 2 Register	$01E_H$	00_H	$01E_H$	00_H	No
A_WURSSIBL2	RSSI Wake-Up Blocking Level Low Channel 2 Register	$01F_H$	FF_H	$01F_H$	FF_H	No
A_WURSSIBH2	RSSI Wake-Up Blocking Level High Channel 2 Register	020_H	00_H	020_H	00_H	No
A_WURSSITH3	RSSI Wake-Up Threshold for Channel 3 Register	021_H	00_H	021_H	00_H	No
A_WURSSIBL3	RSSI Wake-Up Blocking Level Low Channel 3 Register	022_H	FF_H	022_H	FF_H	No
A_WURSSIBH3	RSSI Wake-Up Blocking Level High Channel 3 Register	023_H	00_H	023_H	00_H	No
A_WURSSITH4	RSSI Wake-Up Threshold for Channel 4 Register	024_H	00_H	n.a	n.a	n.a
A_WURSSIBL4	RSSI Wake-Up Blocking Level Low Channel 4 Register	025_H	FF_H	n.a	n.a	n.a
A_WURSSIBH4	RSSI Wake-Up Blocking Level High Channel 4 Register	026_H	00_H	n.a	n.a	n.a
A_SRTHR	Signal Recognition Threshold Register	027_H	10_H	$01D_H$;020_H;023_H	00_H	No
A_SIGDETSAT	Signal Detector Saturation Threshold Register	028_H	FF_H	024_H	10_H	No
A_WULOT	Wake-up on Level Observation Time Register	029_H	00_H	025_H	00_H	No
A_SYSRCTO	Synchronization Search Time-Out Register	$02A_H$	87_H	026_H	87_H	No
A_TOTIM0	Timeout Timer Register 0	$02B_H$	FF_H	n.a	n.a	No
A_TOTIM1	Timeout Timer Register 1	$02C_H$	$0F_H$	n.a	n.a	No
A_TOTIM_SYNC	SYNC Timeout Timer Register	$02D_H$	FF_H	027_H	FF_H	No
A_TOTIM_TSI	TSI Timeout Timer Register	$02E_H$	00_H	028_H	00_H	No
A_TOTIM_EOM	EOM Timeout Timer Register	$02F_H$	00_H	029_H	00_H	No
A_AFCLIMIT	AFC Limit Configuration Register	030_H	02_H	$02A_H$	02_H	Yes
A_AFCAGCD	AFC/AGC Freeze Delay Register	031_H	00_H	$02B_H$	00_H	Yes
A_AFCSFCFG	AFC Start/Freeze Configuration Register	032_H	00_H	$02C_H$	00_H	Yes

Table 3 Registers Overview

Register Short Name	Register Long Name	TDA5340		TDA5240/35		Register Bit/Function Changes
		Offset Address	Reset Value	Offset Address	Reset Value	
A_AFCKCFG0	AFC Integrators Gain Coefficients Register 0	033_H	00_H	$02D_H$;02 E_H	00_H	Yes
A_AFCKCFG1	AFC Integrators Gain Coefficients Register 1	034_H	00_H	$02F_H$;030 H	00_H	Yes
A_PMFUDSF	Peak Memory Filter Up-Down Factor Register	035_H	42_H	031_H	42_H	No
A_AGCSFCFG	AGC Start/Freeze Configuration Register	036_H	00_H	032_H	00_H	No
A_AGCCFG0	AGC Configuration Register 0	037_H	$0B_H$	033_H	$2B_H$	Yes
A_AGCCFG1	AGC Configuration Register 1	038_H	$2F_H$	034_H	03_H	Yes
A_AGCTHR	AGC Threshold Register	039_H	08_H	035_H	08_H	No
A_DIGRXC	Digital Receiver Configuration Register	$03A_H$	40_H	036_H	40_H	No
A_PKBITPOS	RSSI Peak Detector Bit Position Register	$03B_H$	00_H	037_H	00_H	No
A_PDFMFC	PD Filter and Matched Filter Configuration Register	$03C_H$	77_H	$03C_H$; 038_H	07_H; 07_H	Yes
A_PDECF	Pre Decimation Factor Register	$03D_H$	00_H	039_H	00_H	No
A_PDECSCFSK	Pre Decimation Scaling Register FSK Mode	$03E_H$	00_H	$03A_H$	00_H	No
A_PDECSCASK	Pre Decimation Scaling Register ASK Mode	$03F_H$	20_H	$03B_H$	20_H	No
A_SRC	Sampe Rate Converter NCO Tune	040_H	00_H	$03D_H$	00_H	No
A_EXTSLC0	Externel Data Slicer Configuration Register 0	041_H	02_H	$03E_H$	02_H	No
A_EXTSLC1	Externel Data Slicer Configuration Register 1	042_H	00_H	n.a	n.a	n.a
A_EXTSLC2	External Data Slicer Configuration Register 2	043_H	00_H	n.a	n.a	n.a
A_EXTSLTHR0	Externel Data Slicer BW Switching Threshold Register 0	044_H	00_H	n.a	n.a	n.a
A_EXTSLTHR1	Externel Data Slicer BW Switching Threshold Register 1	045_H	00_H	n.a	n.a	n.a
A_SIGDET0	Signal Detector Threshold Level Register - Run Mode	046_H	00_H	$03F_H$	00_H	No
A_SIGDET1	Signal Detector Threshold Level Register - Wakeup	047_H	00_H	040_H	00_H	No
A_SIGDETLO	Signal Detector Threshold Low Level Register	048_H	00_H	041_H	00_H	No

Table 3 Registers Overview

Register Short Name	Register Long Name	TDA5340		TDA5240/35		Register Bit/Function Changes
		Offset Address	Reset Value	Offset Address	Reset Value	
A_SIGDETSEL	Signal Detector Range Selection Register	049_H	$7F_H$	042_H	$7F_H$	No
A_SIGDETCFG	Signal Detector Configuration Register	$04A_H$	00_H	043_H	00_H	No
A_NDTHRES	FSK Noise Detector Threshold Register	$04B_H$	00_H	044_H	00_H	No
A_NDCONFIG	FSK Noise Detector Configuration Register	$04C_H$	07_H	045_H	07_H	No
A_CDRP	Clock and Data Recovery P Configuration Register	$04D_H$	$E6_H$	046_H	$E6_H$	No
A_CDRI	Clock and Data Recovery Configuration Register	$04E_H$	45_H	047_H	65_H	No
A_CDRCFG0	CDR Configuration Register 0	$04F_H$	$4C_H$	049_H; 048_H	$0C_H$; 01_H	Yes
A_CDRCFG1	CDR Configuration Register 1	050_H	$1E_H$	$04A_H$; 048_H	$1E_H$; 01_H	Yes
A_TVWIN	Timing Violation Window Register	051_H	28_H	$04B_H$	28_H	No
A_SLCCFG	Slicer Configuration Register	052_H	90_H	$04C_H$	90_H	Yes
A_TSIMODE	TSI Detection Mode Register	053_H	80_H	$04D_H$	80_H	No
A_TSILENA	TSI Length Register A	054_H	00_H	$04E_H$	00_H	No
A_TSILENB	TSI Length Register B	055_H	00_H	$04F_H$	00_H	No
A_TSIGAP	TSI Gap Length Register	056_H	00_H	050_H	00_H	No
A_TSIPTA0	TSI Pattern Data Reference A Register 0	057_H	00_H	051_H	00_H	No
A_TSIPTA1	TSI Pattern Data Reference A Register 1	058_H	00_H	052_H	00_H	No
A_TSIPTB0	TSI Pattern Data Reference B Register 0	059_H	00_H	053_H	00_H	No
A_TSIPTB1	TSI Pattern Data Reference B Register 1	$05A_H$	00_H	054_H	00_H	No
A_EOMC	End Of Message Control Register	$05B_H$	05_H	055_H	05_H	No
A_EOMDLEN	EOM Data Length Limit Register	$05C_H$	00_H	056_H	00_H	No
A_EOMDLENP	EOM Data Length Limit Parallel Mode Register	$05D_H$	00_H	057_H	00_H	No
A_CHCFG	Channel Configuration Register	$05E_H$	00_H	058_H	04_H	Yes
A_TXRF	TX RF Configuration Register	$05F_H$	04_H	n.a	n.a	n.a

Table 3 Registers Overview

Register Short Name	Register Long Name	TDA5340		TDA5240/35		Register Bit/Function Changes
		Offset Address	Reset Value	Offset Address	Reset Value	
A_TXCFG	TX Configuration Regsiter	060_H	05_H	n.a	n.a	n.a
A_TXCHOFFS0	TX Channel Offset Register 0	061_H	00_H	n.a	n.a	n.a
A_TXCHOFFS1	TX Channel Offset Register 1	062_H	00_H	n.a	n.a	n.a
A_TXBDRDIV0	TX Baudrate Divider Register 0	063_H	00_H	n.a	n.a	n.a
A_TXBDRDIV1	TX Baudrate Divider Register 1	064_H	00_H	n.a	n.a	n.a
A_TXDSHCFG0	TX Data Shaping Configuration Register 0	065_H	00_H	n.a	n.a	n.a
A_TXDSHCFG1	TX Data Shaping Configuration Register 1	066_H	00_H	n.a	n.a	n.a
A_TXDSHCFG2	TX Data Shaping Configuration Register 2	067_H	00_H	n.a	n.a	n.a
A_TXPOWER0	TX Power Configuration Register 0	068_H	00_H	n.a	n.a	n.a
A_TXPOWER1	TX Power Configuration Register 1	069_H	00_H	n.a	n.a	n.a
A_TXFDEV	TX Frequency Deviation Register	$06A_H$	00_H	n.a	n.a	n.a
A_PLLINTC1	PLL MMD Integer Value Register Channel 1	$06B_H$	93_H	059_H	93_H	No
A_PLLFRAC0C1	PLL Fractional Division Ratio Register 0 Channel 1	$06C_H$	$F3_H$	$05A_H$	$F3_H$	No
A_PLLFRAC1C1	PLL Fractional Division Ratio Register 1 Channel 1	$06D_H$	07_H	$05B_H$	07_H	No
A_PLLFRAC2C1	PLL Fractional Division Ratio Register 2 Channel 1	$06E_H$	09_H	$05C_H$	09_H	No
A_PLLINTC2	PLL MMD Integer Value Register Channel 2	$06F_H$	13_H	$05D_H$	13_H	No
A_PLLFRAC0C2	PLL Fractional Division Ratio Register 0 Channel 2	070_H	$F3_H$	$05E_H$	$F3_H$	No
A_PLLFRAC1C2	PLL Fractional Division Ratio Register 1 Channel 2	071_H	07_H	$05F_H$	07_H	No
A_PLLFRAC2C2	PLL Fractional Division Ratio Register 2 Channel 2	072_H	09_H	060_H	09_H	No
A_PLLINTC3	PLL MMD Integer Value Register Channel 3	073_H	13_H	061_H	13_H	No
A_PLLFRAC0C3	PLL Fractional Division Ratio Register 0 Channel 3	074_H	$F3_H$	062_H	$F3_H$	No
A_PLLFRAC1C3	PLL Fractional Division Ratio Register 1 Channel 3	075_H	07_H	063_H	07_H	No

Table 3 Registers Overview

Register Short Name	Register Long Name	TDA5340		TDA5240/35		Register Bit/Function Changes
		Offset Address	Reset Value	Offset Address	Reset Value	
A_PLLFRAC2C3	PLL Fractional Division Ratio Register 2 Channel 3	076_H	09_H	064_H	09_H	No
A_PLLINTC4	PLL MMD Integer Value Register Channel 4	077_H	13_H	n.a	n.a	n.a
A_PLLFRAC0C4	PLL Fractional Division Ratio Register 0 Channel 4	078_H	$F3_H$	n.a	n.a	n.a
A_PLLFRAC1C4	PLL Fractional Division Ratio Register 1 Channel 4	079_H	07_H	n.a	n.a	n.a
A_PLLFRAC2C4	PLL Fractional Division Ratio Register 2 Channel 4	$07A_H$	09_H	n.a	n.a	n.a
A_RXPLLBW	PLL Bandwidth Selection Register for RX Mode	$07B_H$	$0C_H$	n.a	n.a	n.a
A_TXPLLBW	PLL Bandwidth Selection Register for TX Mode	$07C_H$	27_H	n.a	n.a	n.a
A_PLLTST	PLL Startup Time Register	$07D_H$	$5B_H$	n.a	n.a	n.a
A_ANTSW	Antenna Switch Configuration Register	$07E_H$	22_H	n.a	n.a	n.a
A_ADRSFCFG	ADR Start/Freeze Configuration Register	$07F_H$	00_H	n.a	n.a	n.a
A_ADRTCFG0	ADR Timeout Configuration Register 0	080_H	40_H	n.a	n.a	n.a
A_ADRTCFG1	ADR Timeout Configuration Register 1	081_H	40_H	n.a	n.a	n.a
A_ADRTCFG2	ADR Timeout Configuration Register 2	082_H	00_H	n.a	n.a	n.a
A_ADRTHR0	ADR Threshold Register 0	083_H	05_H	n.a	n.a	n.a
A_ADRTHR1	ADR Threshold Register 1	084_H	84_H	n.a	n.a	n.a
SFRPAGE	Special Function Register Page Register	$0A0_H$	00_H	080_H	00_H	No
PPCFG0	PP0 and PP1 Configuration Register	$0A1_H$	50_H	081_H	50_H	Yes
PPCFG1	PP2 and PPRF Configuration Register	$0A2_H$	$F2_H$	082_H	12_H	Yes
PPCFG2	PPx Port Configuration Register	$0A3_H$	00_H	083_H	00_H	Yes
PPCFG3	PPRF_RSSI Configuration Register	$0A4_H$	$0F_H$	n.a	n.a	n.a
RXRUNCFG0	RX RUN Configuration Register 0	$0A5_H$	FF_H	084_H	FF_H	No
RXRUNCFG1	RX RUN Configuration Register 1	$0A6_H$	FF_H	085_H	FF_H	No

Table 3 Registers Overview

Register Short Name	Register Long Name	TDA5340		TDA5240/35		Register Bit/Function Changes
		Offset Address	Reset Value	Offset Address	Reset Value	
CLKOUT0	Clock Divider Register 0	$0A7_H$	$0B_H$	086_H	$0B_H$	No
CLKOUT1	Clock Divider Register 1	$0A8_H$	00_H	087_H	00_H	No
CLKOUT2	Clock Divider Register 2	$0A9_H$	10_H	088_H	00_H	No
ANTSW	Antenna Switch Configuration Register	$0AA_H$	$1D_H$	n.a	n.a	No
RFC	RF Control Register	$0AB_H$	$E7_H$	089_H	07_H	No
BPFCALCFG0	BPF Calibration Configuration Register 0	$0AC_H$	07_H	$08A_H$	07_H	No
BPFCALCFG1	BPF Calibration Configuration Register 1	$0AD_H$	04_H	$08B_H$	04_H	No
XTALCAL0	XTAL Coarse Calibration Register	$0AE_H$	90_H	$08C_H$	10_H	No
XTALCAL1	XTAL Fine Calibration Register	$0AF_H$	00_H	$08D_H$	00_H	No
RSSICFG	RSSI Configuration Register	$0B0_H$	11_H	$08E_H$	01_H	No
ADCINSEL	ADC Input Selection Register	$0B1_H$	00_H	$08F_H$	00_H	No
RSSIOFFS	RSSI Offset Register	$0B2_H$	80_H	090_H	80_H	No
RSSISLOPE	RSSI Slope Register	$0B3_H$	80_H	091_H	80_H	No
DELOGSFT	DELOG Shift Register	$0B4_H$	00_H	n.a	n.a	n.a
CDRDRTHRP	CDR Data Rate Acceptance Positive Threshold Register	$0B5_H$	$1E_H$	092_H	$1E_H$	No
CDRDRTHRN	CDR Data Rate Acceptance Negative Threshold Register	$0B6_H$	23_H	093_H	23_H	No
IM0	Interrupt Mask Register 0	$0B7_H$	00_H	094_H	00_H	No
IM1	Interrupt Mask Register 1	$0B8_H$	00_H	095_H	00_H	No
IM2	Interrupt Mask Register 2	$0B9_H$	00_H	n.a	n.a	n.a
SPMIP	Self Polling Mode Idle Periods Register	$0BA_H$	01_H	097_H	01_H	No
SPMC	Self Polling Mode Control Register	$0BB_H$	08_H	098_H	00_H	Yes
SPMRT	Self Polling Mode Reference Timer Register	$0BC_H$	01_H	099_H	01_H	No
SPMOFFT0	Self Polling Mode Off Time Register 0	$0BD_H$	01_H	$09A_H$	01_H	No
SPMOFFT1	Self Polling Mode Off Time Register 1	$0BE_H$	00_H	$09B_H$	00_H	No
SPMONTA0	Self Polling Mode On Time Config A Register 0	$0BF_H$	01_H	$09C_H$	01_H	No
SPMONTA1	Self Polling Mode On Time Config A Register 1	$0C0_H$	00_H	$09D_H$	00_H	No

Table 3 Registers Overview

Register Short Name	Register Long Name	TDA5340		TDA5240/35		Register Bit/Function Changes
		Offset Address	Reset Value	Offset Address	Reset Value	
SPMONTB0	Self Polling Mode On Time Config B Register 0	$0C1_H$	01_H	$09E_H$	01_H	No
SPMONTB1	Self Polling Mode On Time Config B Register 1	$0C2_H$	00_H	$09F_H$	00_H	No
SPMONTC0	Self Polling Mode On Time Config C Register 0	$0C3_H$	01_H	$0A0_H$	01_H	No
SPMONTC1	Self Polling Mode On Time Config C Register 1	$0C4_H$	00_H	$0A1_H$	00_H	No
SPMONTD0	Self Polling Mode On Time Config D Register 0	$0C5_H$	01_H	$0A2_H$	01_H	No
SPMONTD1	Self Polling Mode On Time Config D Register 1	$0C6_H$	00_H	$0A3_H$	00_H	No
EXTPCMD	External Processing Command Register	$0C7_H$	00_H	$0A4_H$	00_H	Yes
TXC	TX Control Register	$0C8_H$	00_H	n.a	n.a	n.a
RXC	RX Control Register	$0C9_H$	84_H	$0A5_H$	04_H	Yes
CMC	Chip Mode Control Register	$0CA_H$	10_H	$0A6_H$	10_H	Yes
TXCHNL	TX Channel Configuration Register	$0CB_H$	00_H	n.a	n.a	n.a
PLLCFG	PLL Configuration Register	$0CC_H$	08_H	n.a	n.a	n.a
VACERRTH	VCO Autocalibration Error Threshold	$0CD_H$	00_H	n.a	n.a	n.a
PRBS	PRBS Starting Value Register	$0CE_H$	50_H	n.a	n.a	n.a
TXFIFOAEL	TX FIFO Almost Empty Level Register	$0CF_H$	00_H	n.a	n.a	n.a
TXFIFOAFL	TX FIFO Almost Full Level Register	$0D0_H$	00_H	n.a	n.a	n.a
RXFIFOAFL	RX FIFO Almost Full Level Register	$0D1_H$	00_H	n.a	n.a	n.a
PLLSTAT	PLL Status Register	$0D2_H$	00_H	n.a	n.a	n.a
IS2	Interrupt Status Register 2	$0D3_H$	FF_H	n.a	n.a	n.a
IS0	Interrupt Status Register 0	$0D4_H$	FF_H	$0A8_H$	FF_H	No
IS1	Interrupt Status Register 1	$0D5_H$	FF_H	$0A9_H$	FF_H	No
RFPLLACC	RF PLL Actual Channel and Configuration Register	$0D6_H$	00_H	$0AA_H$	00_H	Yes
RSSIPWU	Wakeup Peak Detector Readout Register	$0D7_H$	00_H	$0A7_H$	00_H	No
RSSIPRX	RSSI Peak Detector Readout Register	$0D8_H$	00_H	$0AB_H$	00_H	No

Table 3 Registers Overview

Register Short Name	Register Long Name	TDA5340		TDA5240/35		Register Bit/Function Changes
		Offset Address	Reset Value	Offset Address	Reset Value	
RSSIPPL	RSSI Payload Peak Detector Readout Register	$0D9_H$	00_H	$0AC_H$	00_H	No
PLDLEN	Payload Data Length Register	$0DA_H$	00_H	$0AD_H$	00_H	No
ADCRESH	ADC Result High Byte Register	$0DB_H$	00_H	$0AE_H$	00_H	No
ADCRESL	ADC Result Low Byte Register	$0DC_H$	00_H	$0AF_H$	00_H	No
AFCOFFSET	AFC Offset Read Register	$0DD_H$	00_H	$0B1_H$	00_H	No
AGCGAINR	AGC Gain Readout Register	$0DE_H$	00_H	$0B2_H$	00_H	No
SPIAT	SPI Address Tracer Register	$0DF_H$	00_H	$0B3_H$	00_H	No
SPIDT	SPI Data Tracer Register	$0E0_H$	00_H	$0B4_H$	00_H	No
SPICHKSUM	SPI Checksum Register	$0E1_H$	00_H	$0B5_H$	00_H	No
SN0	Serial Number Register 0	$0E2_H$	00_H	$0B6_H$	00_H	No
SN1	Serial Number Register 1	$0E3_H$	00_H	$0B7_H$	00_H	No
SN2	Serial Number Register 2	$0E4_H$	00_H	$0B8_H$	00_H	No
SN3	Serial Number Register 3	$0E5_H$	00_H	$0B9_H$	00_H	No
CHIPID	Chip ID Register	$0E6_H$	00_H	n.a	n.a	n.a
RSSIRX	RSSI Readout Register	$0E7_H$	00_H	$0BA_H$	00_H	No
RSSIPMF	RSSI Peak Memory Filter Readout Register	$0E8_H$	00_H	$0BB_H$	00_H	No
SPWR	Signal Power Readout Register	$0E9_H$	00_H	$0BC_H$	00_H	No
NPWR	Noise Power Readout Register	$0EA_H$	00_H	$0BD_H$	00_H	No

w w w . i n f i n e o n . c o m

Published by Infineon Technologies AG