

FAQs for SmartLEWIS RX+ family: TDA5240, TDA5235, TDA5225

Version 1.7, 23rd of July 2013

History info: V1.7 (Items 21 and 22 added compared to V1.5)

Info: All FAQs are valid for all products of the SmartLEWIS RX+ family, unless otherwise noted.

1. The default levels of the PPx output pins after successful reset are as following:

- PP0 (CLK_OUT): Delivers an output signal with approximately 1MHz
- PP1 (DATA): DATA output is always LOW after reset
- PP2 (NINT): Behaves as described in the data sheet in Chapter „2.4.9.2 Chip Reset“. So after reset this signal/pin is set to LOW.
- PP3 (RX_RUN): After reset TDA5240/35/25 is in SLEEP Mode, therefore RX_RUN is set to LOW.

2. The default levels of the PPx output pins during reset are as following:

- PP0 (CLK_OUT): Tristate
- PP1 (DATA): Tristate
- PP2 (NINT): Behaves as described in the data sheet in Chapter „2.4.9.2 Chip Reset“. So during reset this signal/pin is set to HIGH.
- PP3 (RX_RUN): Tristate

3. The output pins (PPx and SDO) are in tristate during power-down

4. The input pins (NCS, SCK and SDI) show following behavior during power-down:

In general, all CMOS input pins require a well defined input level in order to avoid floating.

Input logic levels between VIH and VIL (see datasheet) are not allowed also in power-down mode (P_ON=0)

4.1 Case 1: Chip is permanently supplied, P_ON = LOW

The VDD5V rail stays further supplied. The ESD structures of the pads are supplied with VDD5V/GNDD. No increased leakage current in this case.

4.2 Case 2: Power supply is switched off via external switch.

a) In case all digital input pins are set to LOW → Everything's fine

b) At least one digital input pin is set to HIGH, e.g. NCS → The chip would be supplied via the ESD structures. Even in case P_ON = LOW, the power-down current is delivered by the signal line(s).

At P_ON = HIGH it's even worse, as here the chip is in SLEEP Mode (XOSC is active, digital core is waiting for SPI command). Depending on temperature, here even higher „undesired“ current will be drawn.

5. **How is XTAL trimming used for centering the receive frequency?**

As a general rule we recommend to set the receiver center frequency exactly to the transmitted center frequency. On slightly changing the internal trim capacitors (registers XTALCAL0 and XTALCAL1), this can be done very easy, when applying a centered RF constant wave (CW) signal and measuring at the external 10.7 MHz ceramic filter (pin 28 – IF_OUT) while the receiver is in Run Mode Slave using DDC mode (Double Down Conversion). Tune the trimming caps so that you get exactly 10.700 MHz at pin 28. For sure, AFC needs to be deactivated during this centering process.

Alternatively the crystal frequency can be measured as well (Do not directly contact the High Frequency probe with the crystal circuitry – Just put the RF probe close to the crystal). Then tune the internal trim capacitors (registers XTALCAL0 and XTALCAL1) until the crystal frequency is exactly at 21.948717MHz while the receiver is in Run Mode Slave.

6. **Frequency offset detectable on the 10.7 MHz IF_OUT pin (pin 28) when AFC (Automatic frequency control) is activated and RF frequency was swept about +/- 300 .. 400 kHz around the RF center frequency. What caused this behavior when using TDA5235 or TDA5240?**

AFC is activated and the AFC limit is set to a standard value of e.g. 42 kHz. In TDA5235 and TDA5240 a detected TSI (Telegram Start Identifier, means a start sequence) triggers writing data into the FIFO, whereas an EOM stops this writing process into FIFO. TDA5235 and TDA5240 have the baseband processing feature “Lock Data FIFO at EOM”. This means, the data FIFO (and the digital receive chain, including digital control unit of AFC) are locked after an EOM (End of Message) was detected (Note, a complete FIFO read releases this lock state). When now applying an RF signal with a frequency offset in the range of +/- 400kHz, this signal is noisy and can be interpreted as TSI, later an EOM is generated and the FIFO lock state is reached. When now applying an RF signal at the real center frequency, then the previously locked AFC offset value is still active and therefore a frequency offset of AFCLIMIT can be observed on the 10.7 MHz IF_OUT pin. This behavior can occur in case the Signal Recognition Thresholds are not set properly.

Remember, the Signal Recognition Mode and the appropriate Threshold settings must be set correctly (see Application Note for setting Signal and Noise Detector Thresholds → Using FSK requires “Signal and noise detection simultaneously + SIGDETLO”). Then no wrong TSI will be detected and no wrong EOM will be generated, which can initiate locking the data FIFO and therefore also locking the digital receive chain (including the AFC control circuitry).

7. **When using TDA5235's or TDA5240's 8bit Parallel mode or 8bit Extended mode, but only having a single TSI in the transmit frame, sometimes wrong data can be readout from the FIFO. What can cause this behavior?**

Remember, when having only 1 single TSI within the transmit frame, then the 16bit TSI mode needs to be used. When using 8bit Parallel mode or 8bit Extended mode, then also both TSI's on the receiver side would need to be configured. Otherwise the un-configured second TSI can lead to an FSYNC, so that data after this FSYNC are written into the FIFO, and this data is definitely not the expected data. So use 16bit TSI mode and the receiver works fine in this case.

8. Why is there an RC low-pass required at VDD5V pin in case of 5V supply usage?

The 5V-to-3.3V regulator needs a slew rate limitation at power-up. Steep slew rates at VDD5V in 5V supply mode cannot be regulated and therefore higher voltages than allowed could result across voltage regulator. For avoiding this, slew rate limitation can be applied with an RC low-pass (220 Ω + 1 μ F) as shown in the datasheet.

The time constant of the 220 Ω resistor together with the 1 μ F capacitor has to be kept constant. That means a 4.70 Ω resistor together with 4.7 μ F capacitor can be used as well to overcome possible voltage drop across this resistor, which could reduce the supply voltage seen by TDA5225/35/40.

Also keep in mind that if P_ON is switched together with VDD5V in 5V supply mode, then P_ON needs to be taken after this RC low-pass as well (same reason as for VDD5V pin, see above). In case P_ON and VDD5V are not connected in 5V supply mode, and P_ON is switched to 5V before VDD5V, then P_ON needs its own RC low-pass (same time constant as for VDD5V, see above).

9. What to take care when using Data Rate Acceptance Limitation (DRAL) function of TDA5240 or TDA5235?

In Self Polling Mode (SPM) the DRAL function (CDRDRTHRP and CDRDRTHRN registers) of TDA5235/40 can be used to narrow the acceptance range of the received data rate.

In Run Mode Slave (RMS) the DRAL function shall not be used, but the Valid Pulse Width criterion (x_CDRTOLB and x_CDRTOLC registers) can be used to narrow the accepted range of the received data rate in RMS.

To achieve rejection of unwanted data rate of an interfering signal:

- the functional blocks “DRAL” and “CDRTOL valid pulse width” can be used in SelfPollingMode
- the functional block “CDRTOL valid pulse width” ONLY can be used in RunModeSlave

Further details are summarized in the Application Note “Usage and Limitations of DRAL “Data Rate Acceptance Limitation” Function”.

However, the Signal Recognition thresholds (SigRec = x_SIGDET0/1, x_NDTHRES, x_SIGDETLO) need to be set properly according to our Application Note “Signal Noise Detector Settings” for both RMS and SPM.

10. Why is there a minimum value for the RSSI load resistance specified in the data sheet?

RSSI pin should not see less than 100k Ω (see datasheet). At RSSI pin, there is a chip-internal series resistor of typ. 1.5k Ω , which can vary by about 50%. In case the external series resistor is lower than 100k Ω , the internal series resistor gets more influence and is distorting the resulting RSSI output voltage (due to voltage drop at the chip-internal resistor).

11. Which Signal Recognition setting is required for an application using an ASK wake-up and FSK payload frame with TDA5240 or TDA5235?

Such ASK/FSK application can be handled using Self Polling Mode and selecting “Signal Recognition” mode “Signal and noise detection simultaneously + SIGDETLO”. “Signal Detector Threshold – Wakeup Level” needs to be used for ASK. “Signal Detector Threshold – RunMode Level” needs to be used for FSK together with “Noise Detector” and “SIGDETLO”. Please note to select the corresponding modulation type for the threshold determination (e.g. using [Wizard page 1 + 5](#) and [Explore page – Power Readout Statistic](#) on TDA5240 Explorer Family).

12. Do I need to take special care (in terms of crystal startup time and TDA Reset time), when using the crystal given in the Datasheet of TDA5240/35/25?

When using the crystal, noted in the datasheet, then everything is fine, because the crystal startup time (see Reference item H5 in Datasheet) is smaller than the Reset time (see Reference item C9 in Datasheet).

A HIGH=>LOW edge on NINT signal (see Figure “Reset Behavior” in the Datasheet) indicates that Reset is already finished and can be used for the Reset procedure initiated by the application controller. This NINT indication can occur before the maximum Reset time given in Reference item C9. This all is valid for the crystal given in the Datasheet.

13. What do I need to take care, when crystal startup time is longer than Reset time of TDA5240/35/25?

In case another crystal is used (e.g. smaller size, like NX3225) and the external trimming capacitors use large values (e.g. 18pF on each side of the crystal, which are present during crystal startup), then the crystal startup time is expected to be higher. In case the crystal startup time is now larger than the Reset time, then the first SPI communication is allowed only after the worst case crystal startup time is already elapsed. This means TDA can be programmed via SPI only after the largest value out of a) maximum reset time and b) worst-case crystal startup time (NINT indication will most probably not be usable anymore in this case).

Also take into account that CLKOUT frequency is only stable after the worst-case crystal startup time.

14. Are the same Brownout detector thresholds (item C8) valid for both supply voltage domains (5.0V / 3.3V) of TDA5240/35/25?

The Brownout detector threshold voltage given in the datasheet (item C8) is valid for VDDD (3.3V supply domain). In 5V supply mode (VDD5V) the Brownout detector threshold will occur at VDD5V = 3.0V (typical) and VDD5V = 3.25V (max).

15. Do you have any recommendation for unused input pins IFBUF_IN (1) and IFMIX_INP (4) of TDA5240/35/25?

Please note, that IFMIX_INN (pin5) needs to be tied to GND in any case.

Both IFBUF_IN (pin1) and IFMIX_INP (pin4) input pins are biased at 1.65V (=3.3V/2). DDC (Double Down Conversion) and only 1 external CER filter used is the chip reset state. Therefore IFBUF_IN (pin1) needs to be left open, even in case SDC (Single Down Conversion) is used in the application. An unused IFBUF_IN pin should only have the PCB footprint soldering connection, but no additional copper line, which could act as antenna.

IFMIX_INP (pin4) is not used after chip reset and can be tied to GND (same GND as IFMIX_INN) in case this pin is not used in the application (including chip register configuration) for achieving better EMC behavior. In case there are separated analog and digital ground areas on the PCB, then the unused IF input pins should be tied to analog GND.

16. Do you have any recommendation for unused output pins IF_OUT (28), IFBUF_OUT (2), RSSI (26) and unused PPx (10, 11, 12 and/or 25) of TDA5240/35/25?

IFBUF is not activated after a chip reset, so IFBUF_OUT (pin2) can be tied to GND in case this pin is not used in the application (including chip register configuration => IFBUF off). In case pin 2 is tied to GND and IFBUF gets activated accidentally, then an unwanted current of 4.5mA will flow. In case someone wants to leave IFBUF_OUT open, this is OK as well. In that case IFBUF_OUT pin should only have the PCB footprint soldering connection, but no additional copper line, which could act as antenna.

IF_OUT (pin28) provides an output signal after chip reset, so this pin needs to be left open in case pin is not used in the application. An unused IF_OUT pin should only have the PCB footprint soldering connection, but no additional copper line, which could act as antenna.

RSSI (pin26) provides an output signal after chip reset, so this pin needs to be left open in case pin is not used in the application. An unused RSSI pin should only have the PCB footprint soldering connection, but no additional copper line, which could act as antenna.

All PPx output lines (pin10, 11, 12, 25) provide an output signal after chip reset, therefore unused PPx pins need to be left open. Unused PPx pins should only have the PCB footprint soldering connections, but no additional copper lines, which could act as antenna.

17. Can I read-back the content of a write register in a TDA5240/35/25?

No, this is not possible.

Write registers are marked with “w” (Type) in the register list and can only be written (no read-back of the actual value possible). Read registers are marked with “r” (Type) in the register list and can only be read (no writing to these registers possible).

There are also read registers, which are cleared after read-out – these are marked with “rc” (read-clear) in the register list. Finally there is also a write register, which is cleared after write (like a trigger) – this is marked with “wc” (write-clear) in the register list.

18. Should I use P_ON pin in my TDA5240/35/25 application?

Yes, indeed. We recommend the usage of P_ON pin, which needs to be controlled by the application controller for resetting the receiver IC. The reason is very simple, because unintentional SPI communication (1. Bug in application controller firmware generating wrong address, wrong data or wrong command; 2. SPI clock glitch (digital noise on SCK) in case NCS is kept low) can generate wrong data on SPI bus. Usage of SPICHSUM read register can detect wrong SPI communication, but it does not indicate the affected register. Therefore a chip reset using P_ON (“1” → “0” → “1”; setting all register bits to their predefined reset value) followed by a re-configuration of the registers used in the application is strongly recommended in such an error case.

Info: P_ON reset initializes not only the SFR flip-flops, but also all flip-flops of internal state machines. For mission-critical stand-alone applications it is recommended (as for all digital circuits) to implement a periodical reset and to renew the device configuration. Take care that device is not functional until configuration is completed, thus the “reconfiguration period” will depend on requested service availability timing (e.g.: RKE/TPMS protocol), application state (Sleep/Run) and SPI speed.

19. Can I use SIB interface board 2.0 together with an evaluation/application board, which is adapted to 5V supply mode of TDA5240/35/25?

No, this is not allowed.

SIB interface connection is working in 3.3V domain. In order to avoid electrical over-stress, DO NOT CONNECT a TDA5240/35/25 in 5V SUPPLY MODE DIRECTLY to the SIB Board! TDA5240/35/25 in 5V mode would require level shifter, when using SIB Board.

20. I use “Wakeup on Equal Bits” criterion in SelfPollingMode and I’m wondering why even a transmission of a random bit sequence generates a Wakeup interrupt in TDA5240/35. I used “External Data Processing” mode = “Chip Data”, is this allowed in that case?

No, usage of “External Data Processing” mode = “Chip Data” is not allowed in SelfPollingMode.

When using SelfPollingMode (SPM), then “External Data Processing” mode = “No Deactivation of Functional Blocks” needs to be used (“External Data Processing” mode can be selected on Explorer Wizard page 1).

Keep in mind: In case “External Data Processing” mode = “Chip Data” is selected accidentally in SPM, then the WU criteria “WU on Random/Equal/Pattern” (strong criteria) are automatically mapped to “WU on Sync” (weak criterion). This weak Wakeup criterion can lead to false alarms (Wakeup interrupt is generated by TDA5240/35 and application controller gets activated) and will increase the average current consumption.

21. Can I use AFC during ASK reception?

No, AFC shall not be used, when receiver is configured to ASK reception (AFC behaves unpredictable during ASK "ZERO"-chips, since there is no wanted signal available to tune to proper RX frequency).

22. PLLFCOMPC1 bit is noted in register x_PLLFRAC2Cy. Can this bit be used?

The originally intended idea of this function is not working properly. Therefore the reset value of this bit (“0” ... disabled) needs to be used. This usage of the fixed value “0” is implemented in the Explorer tool as well.