Wireless Components

ASK Single Conversion Receiver

TDA 5200

Application Note

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2 Product Overview

Contents of this Chapter

2.1 Abstract

This application note describes the operation of the TDA 5200 evaluation board. It demonstrates the design of a low-cost receiver for applications in wireless I.S.M. data communication systems. Various application considerations are presented to assist system designers in implementing the device.

The application board can be operated in one of the assigned frequency bands for short-range devices (SRD) at either 434MHz or 869MHz. The receiver has been optimized for single-channel operation in systems using amplitude shift key (ASK) modulation. The board complies with the I-ETS 300 220 regulations.

2.2 Product Description

The TDA 5200 has been implemented in a 25GHz silicon bipolar process (Infineon “B6HF” process). It supports all low-power device (LPD) wireless applications with ASK modulated signals with data rates of up to 120kb/s.

As can be seen from the block diagram in Figure 2-1, the basic concept of the TDA5200 is a single conversion receiver with an on-chip fully integrated PLL frequency synthesizer and an IF of nominal 10.7MHz. The 10.7MHz IF was selected because of the availability of low-cost ceramic filters in a variety of bandwidths between 60kHz and 280kHz. The user is free to select other IFs and/or filters that are compatible with the 3MHz - 25MHz bandwidth provided by the 90dB limiting IF. The IF provides over 80dB of received signal strength indication (RSSI). The RSSI output is used as the demodulator for the ASK signals. The output of the ASK demodulator is DC-coupled internally to the data slicer. An on-chip 2nd order low-pass filter is provided at the demodulator output. Its upper frequency limit should be set to meet the baseband system requirements. The data slicer is an one-bit analog-to-digital converter that makes the bit decision and provides a rail-to-rail output. In accordance with the code being used for modulation, there is a choice between two different internal analog-to-digital converters. The conventional adaptive data slicer utilizes a large capacitor to provide DC reference for the bit decision. It should be used for the digital conversion of coded signals with no or only a small DC component. The alternate clamping data slicer references its bit decision on the positive peak level of the data signal. It can be used with all unsymmetrical codes of high DC content. Since the clamping data slicer does not have to charge a large capacitor, it requires a shorter preamble and exhibits a nearly instantaneous response time with some slight loss of sensitivity. The local oscillator (LO) is a single-channel PLL frequency synthesizer. It is fully integrated on the chip.

Table 2-1 Summary of the Key Parameters of the Device
Selectable frequency range 433-435 MHz and 868-870 MHz
Fully integrated VCO and PLL frequency synthesizer
ASK demodulation at data rates up to 120kbit/s
Supply voltage range 5.0 V ± 10%
Supply current 4.8 mA typ.
Reference frequency 6.7 MHz or 13.4 MHz
IF frequency range 3 - 25MHz
Power down mode
Input sensitivity typ. -110 dBm at 2.4kbit/s
Adaptive and peak data slicer
Low-pass filter with selectable cutoff frequency

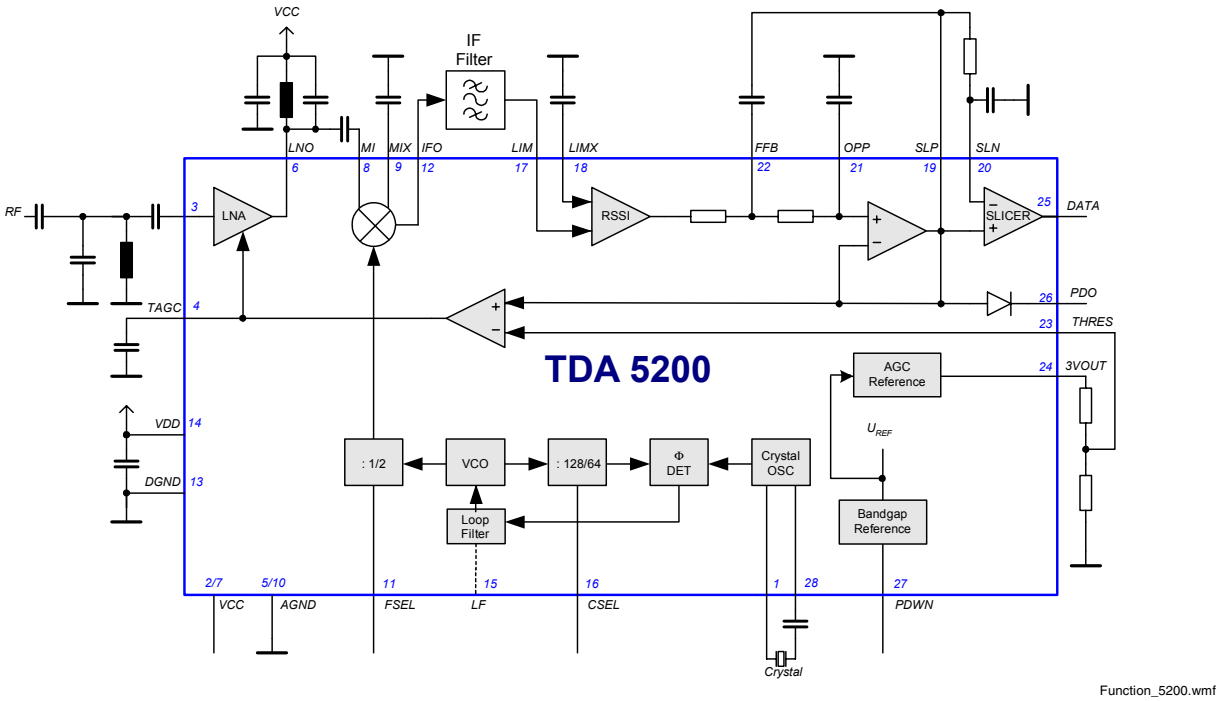

Figure 2-1 Functional Block Diagram

2.3 Package Outlines

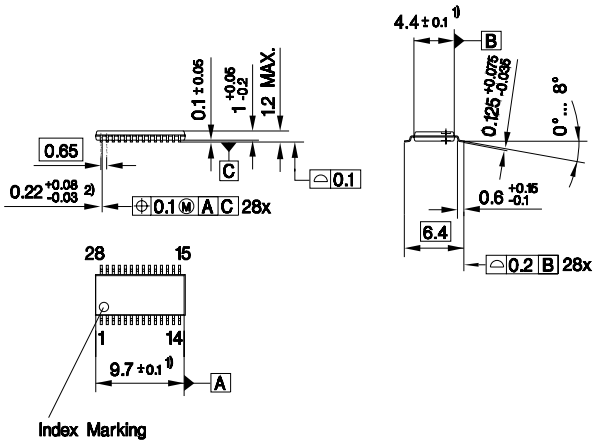

Figure 2-2 P-TSSOP-28-1 package outlines

3 Pin Configuration and Function

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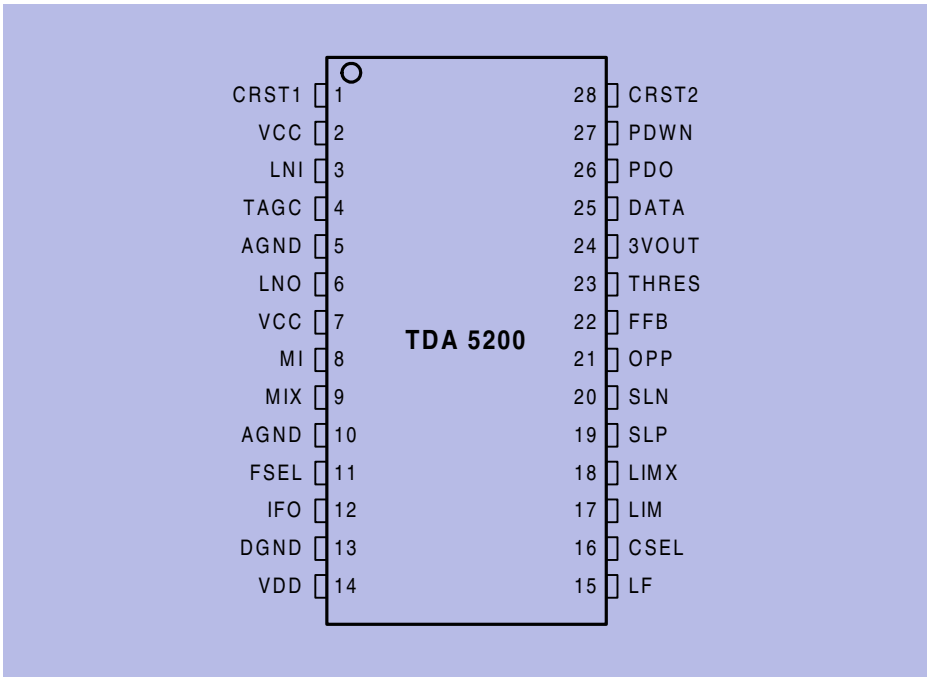
3.1 Pin Configuration

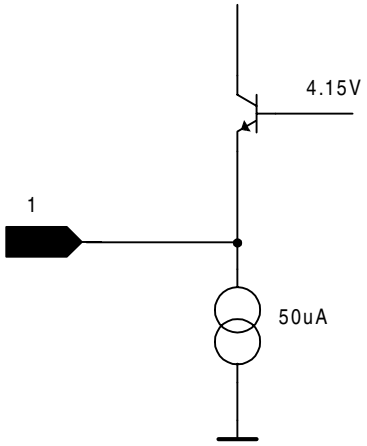
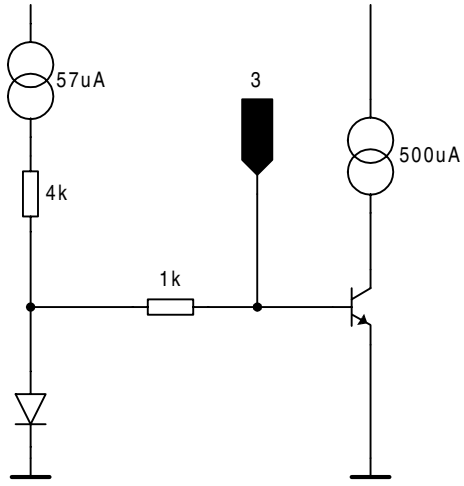


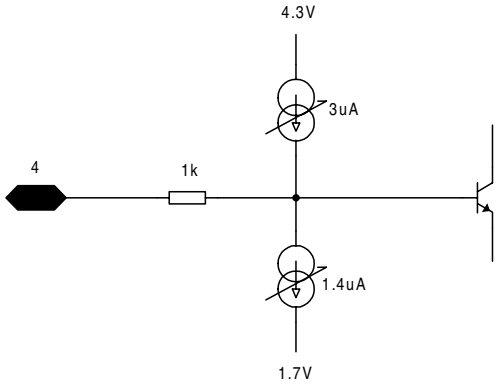
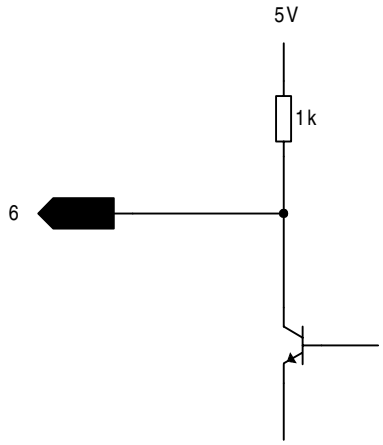
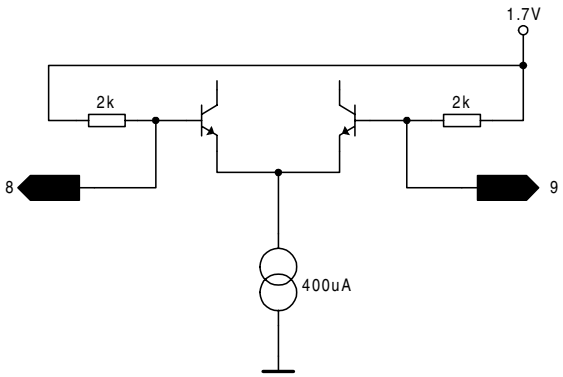
Pin_Configuration.wmf

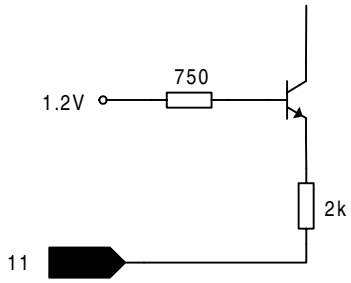
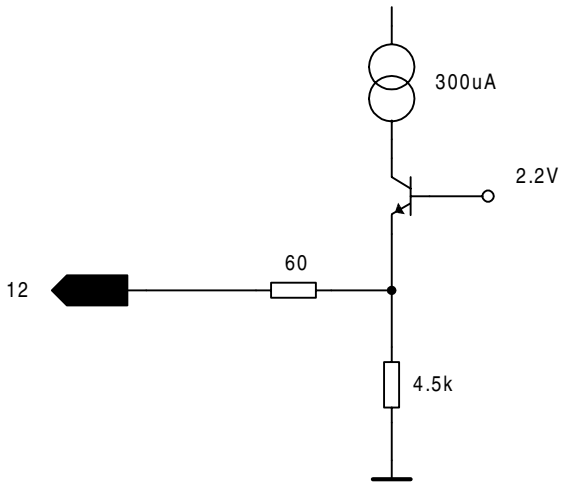
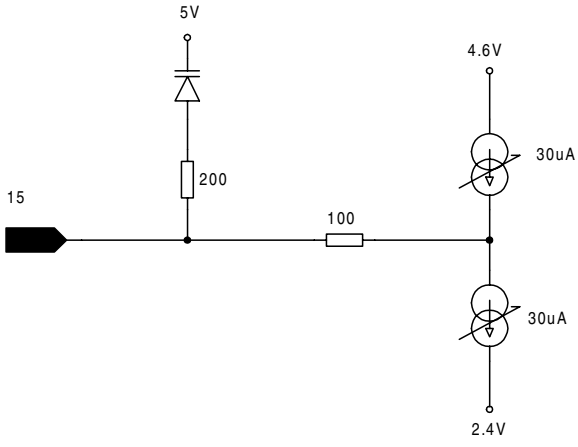
Figure 3-1 IC Pin Configuration

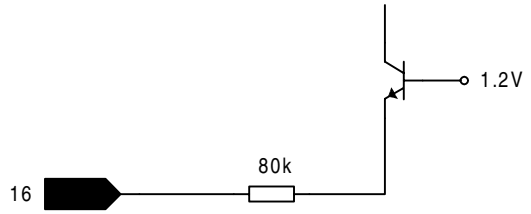
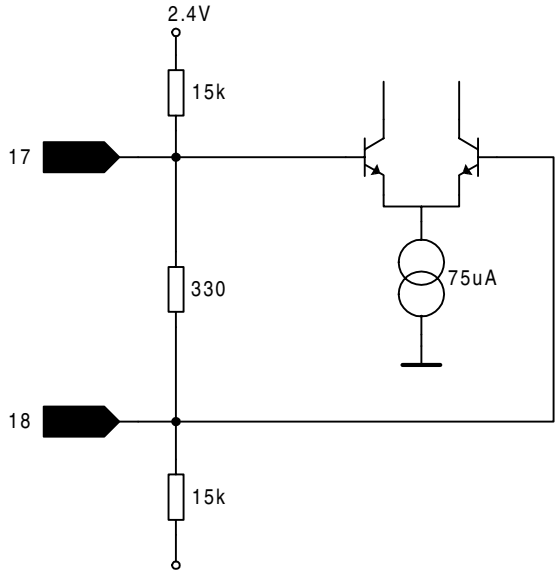
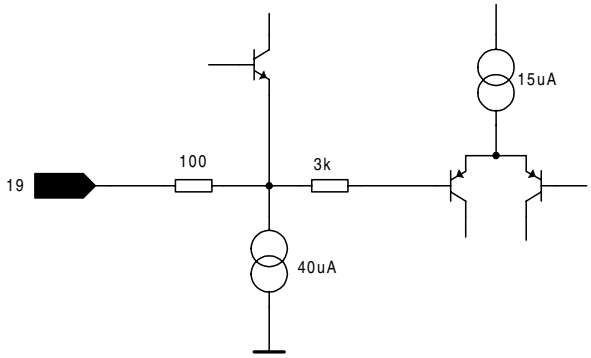
3.2 Pin Definition and Function

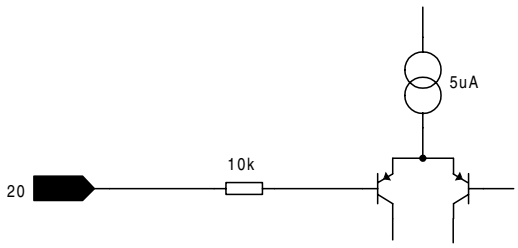
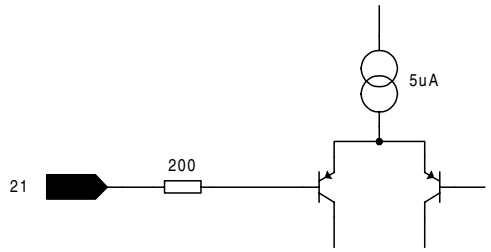
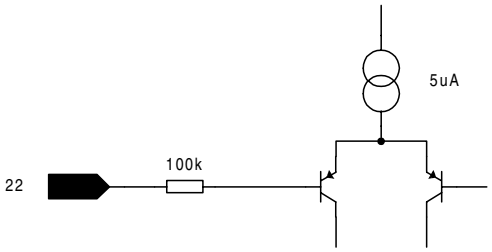
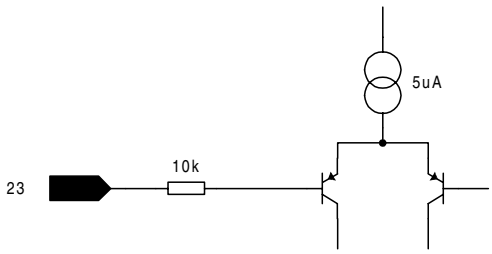
Table 3-1 Pin Definition and Function

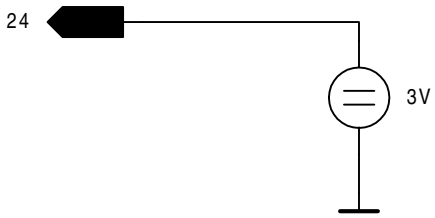
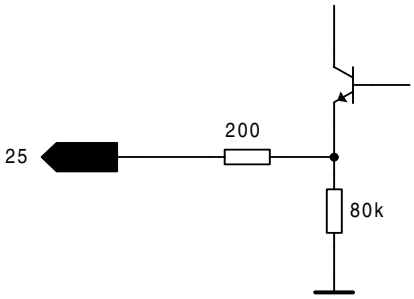
Pin No.	Symbol	Equivalent I/O-Schematic	Function
1	CRST1		Connection 1 to the symmetrical reference oscillator circuit. The reference oscillator is of the negative impedance converter type. It represents a negative resistor connected in series to an inductor between the CRSTL1 and CRSTL2 pins.
2	VCC		5V DC bias supply.
3	LNI		RF input to the LNA. This input is DC-coupled to the base of the common emitter input stage of the LNA cascade configuration.

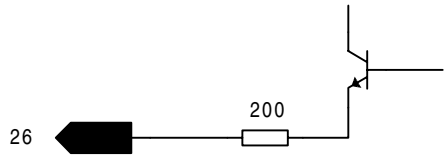
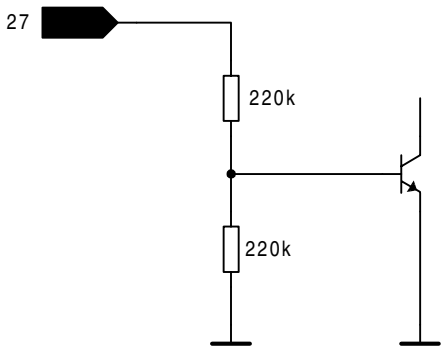
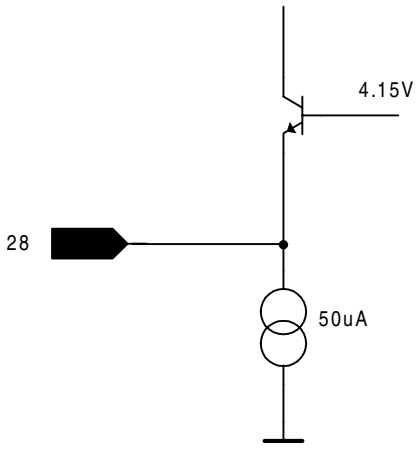
4	TAGC		This pin is used for the gain control of the LNA. The gain of the LNA can be reduced by approx.18dB. The threshold voltage for the gain control function is 1.3V. The control sensitivity is -1dB/8mV See Section 4.1
5	AGND		Ground connection for the analog section
6	LNO		Output of the receiver RF low-noise amplifier (LNA). Collector of the common base output stage of a cas-cade configuration. A DC path to VCC can be sup-plied by the output matching network.
7	VCC		5V DC bias supply.
8 9	MI MIX		Symmetrical input to the mixer. The inputs are DC-coupled to the base of the input stage of a Gilbert Cell mixer configuration.
10	AGND		Ground connection for the analog section

11	FSEL		This pin is used to select the desired operating frequency range of the receiver. FSEL ≤ 0.2V will give access to the 869MHz frequency range. FSEL ≥ 1.4V or an open will set the receiver to the 434MHz mode.
12	IFO		RF mixer output. This pin is the single-ended IF output of the mixer. The output impedance is set internally to 330Ω. It interfaces directly with 10.7MHz standard ceramic IF filters.
13	DGND		Ground connection for digital electronics.
14	VDD		DC bias supply to the digital section
15	LF		Output of the charge pump and input to the VCO control. An internal loop filter (not shown) has been designed for a loop bandwidth of 150kHz. The loop bandwidth may be reduced by applying an external RC network to VCC.

16	CSEL		A logic low (CSEL< 0.2V) applied at this pin sets the internal frequency divider for a reference frequency of 13.xx MHz. A logic high (CSEL > 1.4V) or an open will be applied for a reference frequency of 6.xx MHz.
17 18	LIM LIMX		Input to the IF amplifier/limiter. The input is DC-coupled to the base of the first differential stage of the IFF amplifier strip. The differential input impedance is set internally to 330Ω to meet standard 10.7MHz ceramic filter requirements.
19	SLP		Output of the low-pass filter, directly coupled to the non-inverting input of the data slicer. An external RC low-pass filter connected to the inverting input SLN, pin 20 of the data slicer sets the reference level for the data slicer/comparator to the average DC level of the data bit stream.

20	SLN		This pin is used for setting the data slicer reference level. A RC low-pass filter from the filter output SLP, pin19 provides the comparator with an average DC level of the data bit stream. When applying the peak detector interface, the peak voltage of the data signal at PDO, pin 26 is tapped to determine the bit decision threshold voltage.
21	OPP		Non inverting input of the low-pass filter operational amplifier. A capacitor to ground will be applied as part of a second order Sallen-Key low-pass filter.
22	FFB		Access point to place a capacitor to the output of the low-pass filter. This capacitor is part of the network building the Sallen-Key low-pass filter.
23	THRES		The voltage at this pin sets the receiver input level to a value where the AGC circuit comes into operation. THRES is the inverting input of a differential operational transimpedance amplifier that is used to compare the internal RSSI voltage of the IF amplifier with the voltage applied to THRES. The voltage at THRES can be set by a voltage divider attached to the reference voltage at 3VOUT, Pin 24.

24	3VOUT		Highly stable 3.0V voltage source. This voltage reference output is derived internally from a band gap voltage reference. It is held constant over variations in supply voltage and operating temperature. A resistive voltage divider will be used to precisely set the trigger level at THRES, Pin 23 for the AGC access point
25	DATA		Data output from the demodulator. The output level is TTL/CMOS-compatible. The fall and the rise time of the output pulse will be approx. 3µs when loaded with 10pF.

26	PDO		An external capacitor at this pin will be charged to the peak level of the data filter output voltage. The decision threshold of the data slicer will be set below this voltage by an amount given by the division ratio of the voltage divider coupled to this output. An external time constant at the PDO output determines the decay time of the reference voltage. It should be set in accordance with the lowest signal component within the data string.
27	PDWN		Enable pin for the receiver circuit. PDWN ≤ 0.8V or an open turns off all receiver functions. PDWN ≥ 2.8V powers up all receiver functions
28	CRST2		Connection 2 to the symmetrical reference oscillator circuit.The reference oscillator is of the negative impedance converter type. It represents a negative resistor in series to an inductor between the CRSTL 1 and CRSTL2 pins.

4 Functional Description

Contents of this Chapter

4.1 Low-Noise Amplifier (LNA)

The low-noise amplifier is an on-chip high-gain cascade amplifier operating at a current of 0.5mA. The gain can be reduced by approx. 18dB by applying a high state to the TAGC input, pin 4. The S-parameters of the LNA and the input to the mixer are shown in the following table.

Table 4-1 S-Parameters of the LNA

Parameter	434 MHz			869 MHz	
S11 LNA, high gain	0.873	-34.689deg		0.738	-73.509deg
S11 LNA, low gain	0.899	-35.367deg		0.772	-80.222deg
S21 LNA, high gain	1.509	138.196deg		1.419	101.712deg
S21 LNA, low gain	0.183	140.598deg		0.179	109.069deg
S12 LNA, high gain	0.003	128.233deg		0.023	172.333deg
S12 LNA, low gain	0.001	-153.515deg		0.022	173.381deg
S22 LNA, high gain	0.886	-12.903deg		0.866	-24.222deg
S22 LNA, low gain	0.897	-13.644deg		0.868	-26.328deg
S11 MIX	0.942	-14.429deg		0.918	-28.142deg

Matching the LNA input to the generator and matching the LNA output to the mixer input has been done imparting a LC network. Both the networks have been designed to achieve best selectivity at a designed loss of 2 to 3dB for each filter. The low-loss and hence low Q design is mandatory in order to keep the circuit tuning-free. This low-loss design achieves a high voltage gain of the LNA and hence a good sensitivity of the receiver. Higher losses result in better selectivity at the expense of gain and sensitivity.

It is good practice to design such a network utilizing an appropriate linear CAE design tool. Even a very simple version can be used very efficiently. A very practical way to design the network will be shown below.

As an example, the design of the input-matching network for an 869MHz application will be demonstrated in detail.

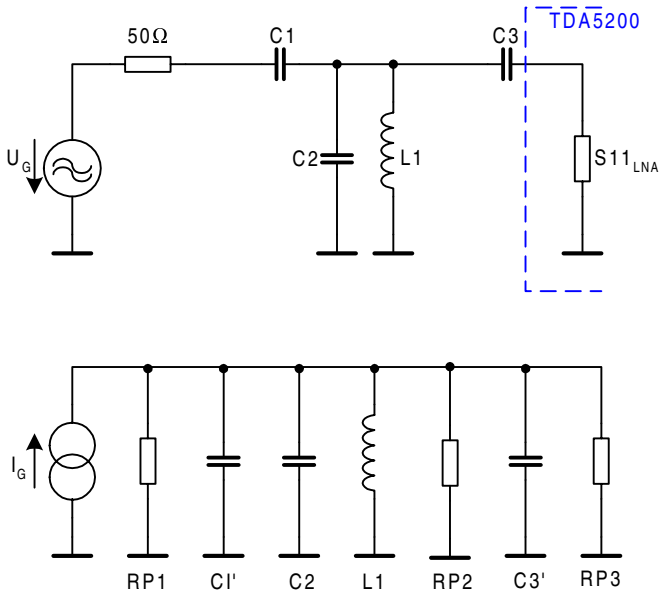


Figure 4-1 LNA input matching network

As shown in the circuit diagram in Figure 4-1, the input filter represents a single tuned parallel resonance circuit loaded by three resistors: RP1, the generator resistor transformed to the circuit, RP2, which collects the filter component losses, and RP3, the mixer input resistor transformed to the circuit.

By dimensioning

$$RP1 = RP3 \quad (1)$$

the overall performance of the filter will be optimized: the best selectivity will be achieved at lowest losses. The design example will be done for assumed filter losses of 2-3 dB.

The power efficiency of the network in Figure 4-1 is:

$$\eta = (1 - Q_L/Q_U)^2 \quad (2)$$

The unloaded Q_U of the circuit is:

$$Q_U = RP2 / Z \quad (3)$$

The characteristic impedance of the circuit is:

$$Z = (L/C)^{1/2} = \omega_0 L = 1 / \omega_0 C_{tot} \quad (4)$$

The effective total capacitance adds up to:

$$C_{tot} = C1' + C2 + C3'. \quad (5)$$

The resonance frequency f_o is

$$\omega_0 = 2\pi f_o$$

The loaded Q_L of the circuit will be:

$$Q_L = (RP1//RP2//RP3) / Z \quad (6)$$

The 3dB bandwidth B for the single tuned LC network can be calculated from:

$$Q_L = f_o / B \quad (7)$$

A tuning-free design is required on grounds of cost. In order to minimize the complexity of the circuit, the application example uses a single tuned LC parallel circuit for both the antenna input matching network and the matching network between the LNA output and the mixer input.

The requirement for a tuning-free implementation provides the basis for dimensioning the networks.

Due to component and manufacturing tolerances, the frequency of the resonance circuit may vary by Δf from the designed frequency. This will result in loss of gain of the LNA, and therefore in reduced sensitivity of the receiver. In order to limit this sensitivity loss, the two circuits in the application example are dimensioned in such a way that each of them exhibits a maximum additional loss of 3 dB under worst-case tolerance conditions.

Typical relevant tolerance values are:

Table 4-2 Tolerance Values of the LNA Input Matching Circuit

		$\Delta f/f$
Tolerance of C	± 2%	± 1%
Tolerance of L	± 2%	± 1%
Manuf. tolerance	Board Placing the components on the pads	± 2% ± 2%
Total frequency tolerance		± 6%

Detuning losses will be low for a higher 3dB bandwidth and hence for a low loaded Q_L of the circuit. With an assumed drop in gain by max. 3 dB per circuit, the required Q_L is:

$$Q_L \leq f_r / 2\Delta f = 8.3 \quad (8)$$

Q_L : loaded Q of resonance circuit

f_r : operating frequency

Δf : frequency offset of resonance circuit

Using chip inductors of size 0805, an unloaded Q_U of

$$Qu \approx \begin{matrix} 30 & (434MHz) \\ 40 & (869MHz) \end{matrix} \qquad (9)$$

can be achieved for the resonance circuits. The Q of the capacitors are greater by at least a factor of 5, so their losses are not taken into account.

The filter losses for each circuit at the LNA input and output will be:

$$a = (1 - Q_L/Q_u)^2 = \begin{matrix} .523 \cong -2.8dB & (434MHz) \\ .628 \cong -2.0dB & (869MHz) \end{matrix} \qquad (10)$$

This value applies to optimum dimensioning, where the generator resistance and the load resistance are both transformed into an equal conductance of RP1 = RP3 in parallel to the resonance circuit.

The selectivity of these circuits is not impressive due to their low loaded QL. In the example, the image frequency rejection for $\Delta f = 2 * f_{IF} = 21.4MHz$ is therefore only

$$a_{if} = \begin{matrix} 2 * 2.2dB = 4.4dB & (434MHz) \\ 2 * 0.6dB = 1.2dB & (869MHz). \end{matrix} \qquad (11)$$

This result can be improved (still with a tuning-free design) by using high Q, pretuned resonators, e.g. based on SAW structures or ceramic filters.

It is rather unusual to design an LC filter for a specified loaded Q_L. The following description outlines a very practical method for the design of such a filter. This procedure is not as attractive as a CAE design but it is very effective. The example applies for the input matching circuit of the LNA with a frequency of 869MHz.

As a first step, a convenient combination of C1 and C3 has to be found to transform the generator resistance and the LNA input resistance to the same conductance RP1=RP3 across the parallel resonance circuit. This can be very elegantly done on the PCB by use of a VNA. This method offers the advantage that all parasitic elements of the board are captured.

In the next step, the equations (3), (4), (7), (8) and (9) are used to calculate the inductance value of L1.

Experimental values of C1 and C3 have been found on the evaluation board with a frequency of 869MHz as:

C1 = 1pF

C3 = 5.6pF

The resultant value of the conductance has been measured as:

RP1 = RP3 = 300Ω

Applying (3), (7), (8) and (9) results in

$Q_U / Q_L = 40 / 8.3 = 4.8 = RP2 / (RP1//RP2//RP3)$

and

$RP2 = 570\Omega$

The inductance L1 is calculated using (3) and (4) to give

$Z \geq \omega_o L = RP2 / Q_U = 570\Omega / 40 = 14.25\Omega$

and

$L1 \geq Z / \omega_o = 2.6nH$

The (standard) value selected is

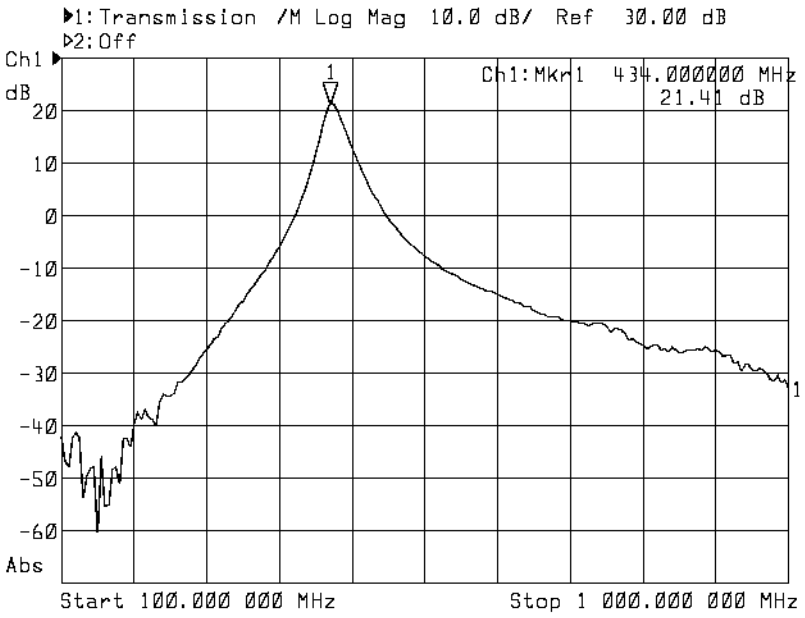
$L1 = 3.3nH$

The size of the capacitor C2 required to set the circuit to resonance is once again most easily found empirically. The resonant frequency in general will not be hit accurately enough with standard component values. There is still some room for adjustment by changing the positions of L1 and C3 on the board and by changing the orientation of L1 (!). If these variation options are not satisfactory, then C1 or C3 can be changed slightly, violating rule (1). The resultant slight loss of receiver sensitivity can be tolerated.

The values of the components imparted in the circuit should fall within a range where they can be handled electrically. The circuit itself gives some freedom in the determination of the characteristic impedance Z and hence in the component values. The component values may be selected to conform to certain criteria.

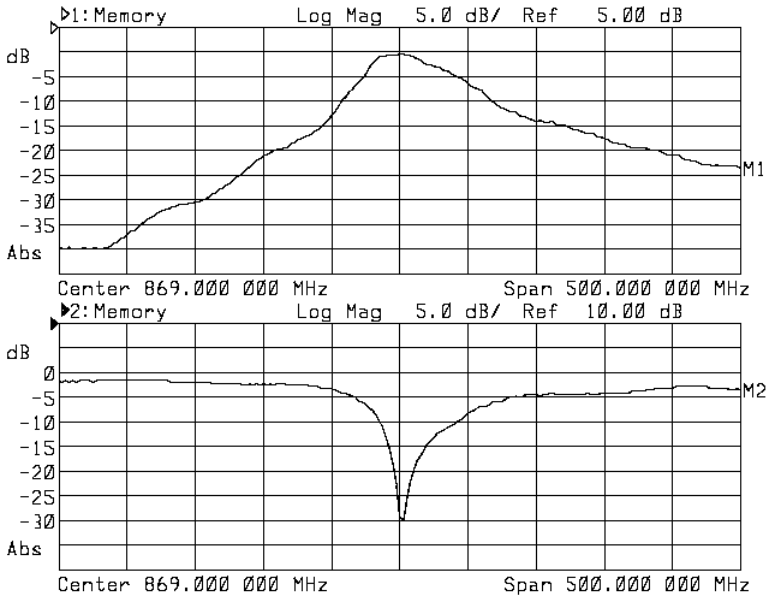
One selection criterion for the filter components is that their value remains within technically manageable limits. For example, it may be specified that the C values should not exceed 10pF. Up to this value they are available with absolute tolerances of ± 0.1pF. Frequency-determining C's should not fall below 2.2pF because of the ± 0.1pF tolerance specification. Inductances below 3.3nH also pose problems due to the increasing influence of lead inductances. Once the inductance value exceeds approximately 33nH with a frequency of 869MHz, their effective impedance is capacitive due to their self-resonance.

The overall frequency response of the LNA is shown in Figure 4-2. The midband voltage gain from the receiver input to the mixer input is +21dB/+18dB with a frequency of 434/868 MHz.



LNAvoltage_vsfreq.wmf

Figure 4-2 LNA voltage gain vs. frequency of 434MHz receiver



Inputref_vsfreq.wmf

Figure 4-3 Input reflection and relative gain of the LNA vs. frequency at 869MHz

4.2 AGC

The receiver incorporates an “automatic gain control” (AGC) function to change its gain in accordance with the RF input level. Applying this function will improve the power handling capability of the receiver by almost 20dB. Increasing the voltage at the TAGC control input (Pin 4) beyond a level of approx. 1.3V will reduce the gain of the LNA by 19dB/18dB with 434/869 MHz by shifting the bias point to a low-level current. The low gain mode of the LNA will result in a power handling capability of the receiver for input levels up to 0dBm without degradation. A low signal or an open at TAGC sets the LNA to the high gain mode.

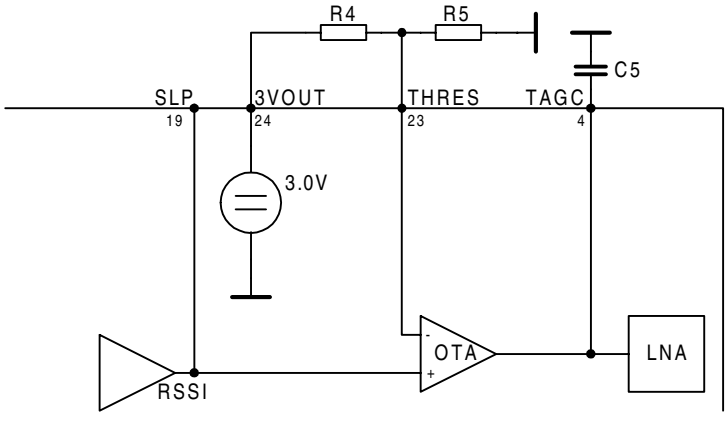


Figure 4-4 AGC circuit

The AGC function is controlled by a comparator connected to the RSSI voltage. The decision threshold for the start of the AGC function is set by the comparator reference voltage. This voltage is tapped down from the precision 3.0V voltage source at the 3VOUT port (Pin 24) via the R4-R5 voltage divider. If the RSSI voltage reaches the comparator threshold voltage, then the TAGC voltage is pulled up by the transconductance comparator output current. The LNA passes over to the low gain mode.

The threshold of the AGC should be set to the lowest possible receiver input level, in order to optimize the large-signal response of the receiver for the widest possible input level range. However, it must be set higher than the receiver sensitivity limit by at least the value of the gain reduction, so that the mixer does not operate at its sensitivity threshold. With the specified LNA gain reduction of approx. 18 dB, it is recommended that the threshold be dimensioned to a receiver input level of at least 25...30 dB higher than the sensitivity limit value. Figure 4-5 shows the AGC function for a transition level set to -85dBm by a combination of R4=330kΩ and R5=330kΩ.

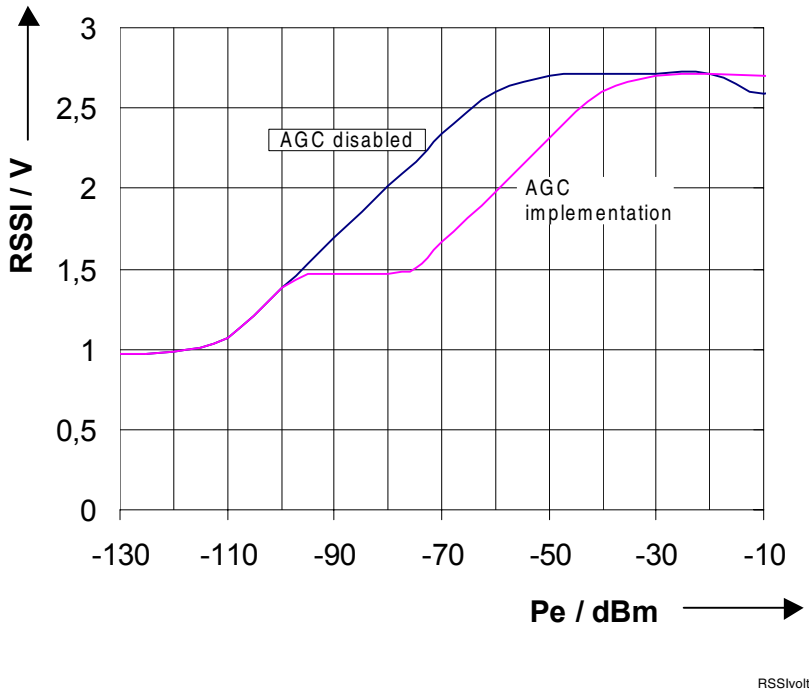


Figure 4-5 RSSI voltage as a function of input level for AGC implementation

The AGC function is filtered via C5. C5 is charged by the current source at the comparator output by a 4.2µA source and a 1.5µA sink current for a fast attack and slow decay time. The AGC operation should not be triggered by the data signal. Since the AGC operates in a linear mode without any hysteresis, there always is some range of the receiver input level, where the AGC will be affected by the data signal.

The AGC gain at TAGC is 10dB/80mV. Due to the very high total gain within the AGC, the loop will only be stable for

$C5 \geq 10nF$

A recommended value for C5 is 47nF

For a receiver input level above the static AGC threshold level, the RSSI data signal at SLP, Pin19 will show a characteristic overshoot at the positive pulse edge. It is caused by the AGC loop trying to level down the RSSI signal to the preset threshold value. The amplitude and duration of the overshoot is directly related to C5. In order to keep the overshoot below 30% of the signal amplitude, C5 should be designed for a value as shown in the subsequent table.

Table 4-3 Dependence of T_L Value on C5	
T_L	C5
0.25ms	10nF
1ms	47nF
2ms	150nF

where T_L is the longest period of no signal change within the data sequence.

The design of the data slicer has to consider the distorted pulse shape. This will be quite unproblematic when applying the adaptive data slicer. For most coding schemes, C5 can even be set to 1/5 of the above value then without a significant degradation of performance.

When applying the peak data slicer, however, the threshold has to be reduced to cover the overshoot voltage. A combination of R2=100kΩ and R3=390kΩ should be imparted then. Setting the threshold to this lower level will reduce the receiver sensitivity by approx. 6dB, however.

4.3 Mixer

The Double Balanced Mixer is based on a Gilbert Cell configuration with a symmetrical input and a single-ended output. The output presents a 330Ω termination which directly interfaces to 10.7MHz ceramic filters. A LC matching network is used to connect the LNO to the MI or the MIX input. The conversion voltage gain of the mixer with the internal load of 330Ω is 21dB. The receiver uses low-side LO injection. This avoids interference caused by signals at the image frequency range when operated with high-side injection.

4.4 Overall Performance of the Front End

Table 4-4 shows the overall performance of the LNA and of the mixer at a frequency of 434MHz. Table 4-5 summarizes the same results for the evaluation board operated at 869 MHz.

Table 4-4 Measured Mixer Performance at 434 MHz

Parameter	LNA		LNA&Mixer	
	low gain	high gain	low gain	high gain
Gain	1 dB	21dB	22 dB	42 dB
Receiver sensitivity			- 95 dBm	- 112 dBm
IIP3	-10 dBm	- 10 dBm	-20 dBm	-40 dBm
1dB compression	- 18 dBm	- 15 dBm	- 31 dBm	- 53 dBm

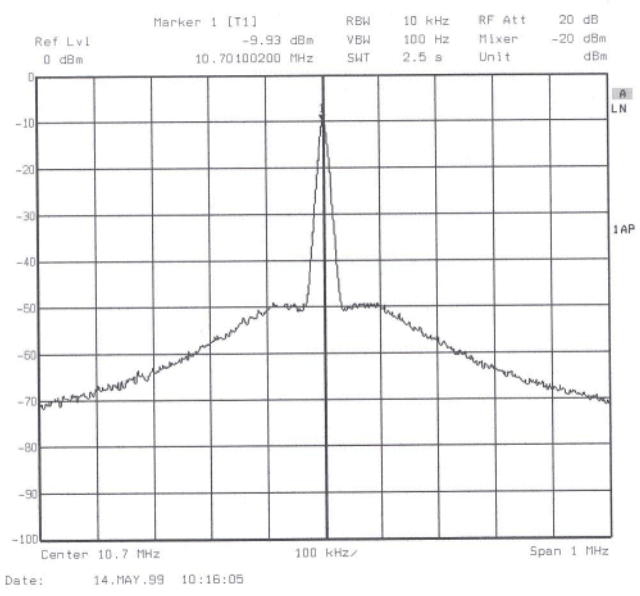
Table 4-5 Measured Mixer Performance at 869 MHz

Parameter	LNA		LNA&Mixer	
	low gain	high gain	low gain	high gain
Gain	0 dB	19 dB	19 dB	40 dB
Receiver sensitivity			- 95 dBm	- 112 dBm
IIP3	-5 dBm	- 14 dBm	-17 dBm	-37 dBm
1dB compression	- 6 dBm	- 9 dBm	- 34 dBm	- 55 dBm

4.5 PLL Synthesizer

The basic circuit of the PLL frequency synthesizer consists of a VCO operating at a nominal frequency of 852MHz, a frequency divider with a division ratio of either 64 or 128, a frequency/phase discriminator and a reference oscillator operating at either 13.5MHz or 6.7MHz. In case of operation at 868.3 MHz the VCO operates at 857.6MHz, for example, This frequency is divided by 64 for operation at a reference frequency of 13.4MHz or by 128 at a reference frequency of 6.7MHz.

The VCO signal is directly applied to the mixer stage when operating the receiver at 869MHz. For operation at 434MHz, the VCO signal is divided by two to build the injection signal to the mixer. The VCO frequency covers the range of 750MHz to 900Mhz at the limits of the tuning voltage of 4.7V and 2.2V. The phase noise spectrum of the VCO signal is shown in Figure 4-6. It has been measured with a resolution bandwidth of 10kHz. It shows the characteristic noise suppression within the loop bandwidth of 150kHz. Sideband noise outside the loop bandwidth at a frequency offset of ±200kHz can be specified at -87dBc/Hz. This noise sets the limit of the adjacent channel suppression of the receiver.The selectivity of the IF filter is bypassed this way.



Phasenoise.wmf

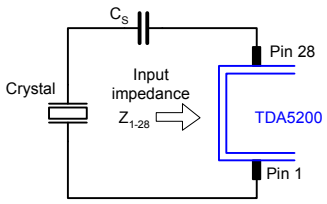
Figure 4-6 Phase noise spectrum of local oscillator

4.6 Reference Oscillator

The receiving frequency and its stability are determined by the reference crystal and the associated oscillator circuit.

The oscillator is a symmetrical configuration of the negative impedance converter type. A resistor and a capacitor are “sign-inverted” to give a negative resistance in series with an inductance between the oscillator ports CRST1 and CRST2, pin1 and pin28. The equivalent impedance parameters of the oscillator presented in Section 5.1.3 of the Specification have been taken between pin1 and pin28 of the TDA5200 on the evaluation board.

The value of the capacitor necessary to achieve that the oscillator is operating at the intended frequency is determined by the reactive (inductive) part of the negative resistance of the oscillator circuit and by the crystal specifications given by the crystal manufacturer.



Quartz_load.wmf

Figure 4-7 Determination of Series Capacitance Value for the Quartz Oscillator

A crystal is specified with a load capacitance C_l. The series capacitor C_S needed to achieve the wanted oscillation frequency in presence of the above mentioned series reactance imposed by the oscillator circuit can be calculated according to the following formula.

$$C_S = \frac{1}{\frac{1}{C_l} + 2\pi f X_L}$$

with C_l the load capacitance (refer to the quartz crystal specification).

Examples:

6.7 MHz:	C_L = 12 pF	X_L=750 Ω	C_S = 8.7 pF
13.401 MHz:	C_L = 12 pF	X_L=1250 Ω	C_S = 5.3 pF

These values may be obtained in high accuracy by putting two capacitors in series to the quartz, such as 20pF and 15pF in the 6.7MHz case and 15pF and 8.2pF in the 13.401MHz case.

The frequency stabilities of both the receiver and the transmitter and the modulation bandwidth set the limit for the bandwidth of the IF filter. To achieve a high receiver sensitivity and efficient suppression of adjacent interference signals, the narrowest possible IF bandwidth should be realized.

The frequency stability of the center frequency of the receiver is affected by a number of factors:

- Tuning tolerance of the crystal
- Temperature stability of the crystal
- Aging of the crystal
- Tuning tolerance of the oscillator circuit
- Temperature stability of the oscillator circuit

In the following table an assessment of the worst case overall frequency spread to be expected in case of operation at 868MHz with a 13.4MHz Jauch reference crystal as denoted in the Bill of Materials in Table 5-1 is shown. The calculation is taking into account the tolerance of the crystal and of the components in the oscillator circuit which are determining the tuning tolerance and temperature stability of the circuit. Note that the result is a sum of the squares of the indivual terms.

A spreadsheet[1] may be obtained from Infineon which can be used to predict the total frequency error under worst-case conditions by simply entering the crystal specification.

Table 4-6 Assessment of the Worst Case Frequency Error of the Crystal Oscillator

Tolerance of the crystal	tuning ± 10ppm	± 10ppm
	temperature stability ±20ppm	± 20ppm
Tolerance of the circuit	tolerance of the series load capacitor ±2%	±11ppm
	tolerance of the oscillator circuit (3 σ spread of internal component values assumed), calculated with spreadsheet	±56ppm
	Total frequency error under worst-case conditions	± 65ppm

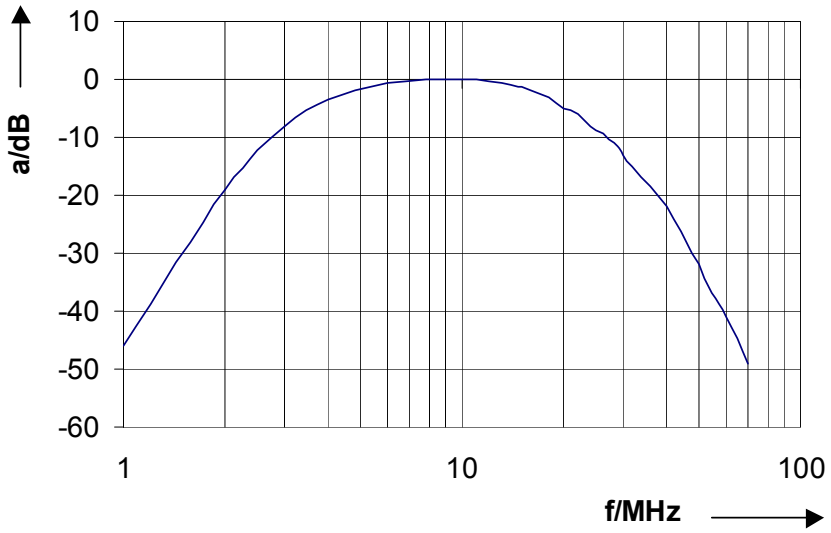
1.available for download on the Infineon RKE Webpage www.infineon.com/rke, also included on evalkit CD-ROM

4.7 IF Section

4.7.1 IF Amplifier

The IF section is an AC-coupled high-gain differential input, single-ended output amplifier. It utilizes three identical gain stages each with a Received Signal Strength Indicator detector. The RSSI signal of the IF amplifier is obtained by summing the individual detector signals. The differential input resistance has been set internally to 330Ω. Single-ended operation of the amplifier presents the nominal load to the ceramic IF filter.

Figure 4-8 shows the frequency response of the IF amplifier. It can be used at all IF frequencies within the range of 3MHz and 25MHz without significant degradation of the overall performance of the receiver.



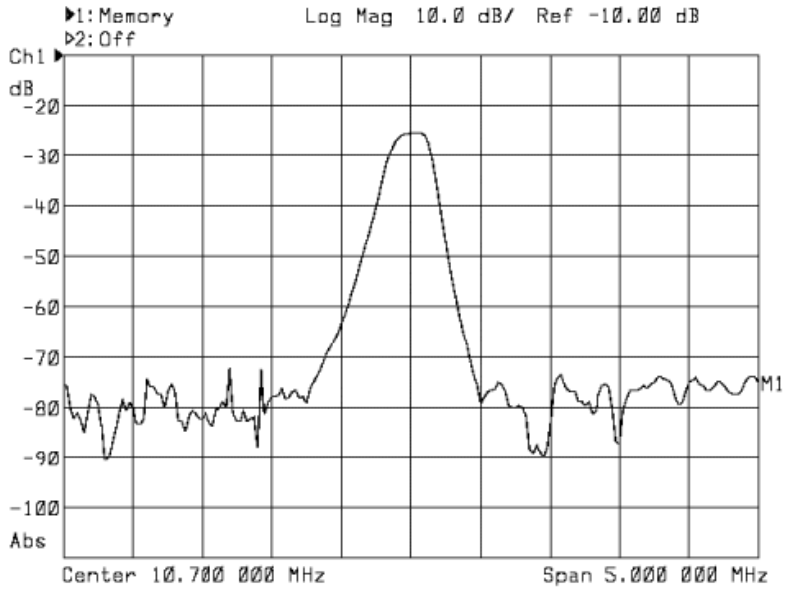
Freqresp.wmf

Figure 4-8 Frequency response of the IF amplifier.

4.7.2 IF Filtering

The TDA 5200 has been designed to be used with a low-cost ceramic IF filter. Those filters are supplied with a wide variety of bandwidth between 60kHz and 300kHz. The nominal input and output impedance is specified at 330Ω. The frequency response of such a filter with a nominal bandwidth of 230kHz imparted to the evaluation board is shown in Figure 4-9. The filter characteristic may be

degraded by oscillator and signal feed-through to the input of the IF amplifier. Both signals may convert to the IF frequency at the IF amplifier, bypassing the IF filter. This effect can be clearly demonstrated at high input levels. A simple low-pass filter in front of the IF amplifier may keep the RF signals from entering. In most cases a careful layout of the board gives adequate decoupling.



Frequencyresponse.wmf

Figure 4-9 IF frequency response

The bandwidth of the IF filter should be set to a value where the modulation signal is reliably transferred under the influence of the frequency tolerance of the transmitter and the receiver.

Table 4-7 Design Example: IF Bandwidth Calculation Under Worst-Case Conditions		
Transmit frequency	434.4MHz	
Modulation ASK4kbit/s	4kbit/s	
Frequency tolerance of the transmitter		± 63ppm
Frequency tolerance of the receiver		± 65ppm
Spectrum of modulation	±1.5*4kbit/s = ± 6kHz	±14ppm
Tolerance of the center frequency of the IF filter	± 30kHz	± 69ppm
Total tolerance		±211ppm

The IF bandwidth therefore should be:

$$B_{IF} \geq \pm 211\text{ppm} * 434\text{MHz} = \pm 91.5\text{kHz} = 183\text{kHz}$$

4.8 Demodulation

After passing the IF filter, the IF signal is fed to the limiter. The limiter serves two functions: amplification and demodulation of the filtered IF signal. The limiter rectifies the IF in order to demodulate the received signal. The demodulated signal is referred to as the RSSI signal. Figure 4-10 shows the relation between the RSSI voltage level and the limiter input IF level at LIM, pin17. As can be seen, the RSSI function is linear to the log. of the limiter input level over a range of 80dB. The receiver can detect a modulated carrier over an input signal dynamic range of more than 80dB. Applying the integrated AGC function, this range will be extended by another 18dB to a total dynamic range of 95dB. The maximum input level that can be detected by the receiver is approx. 0dBm. This value greatly depends on the depth of modulation of the transmitter signal

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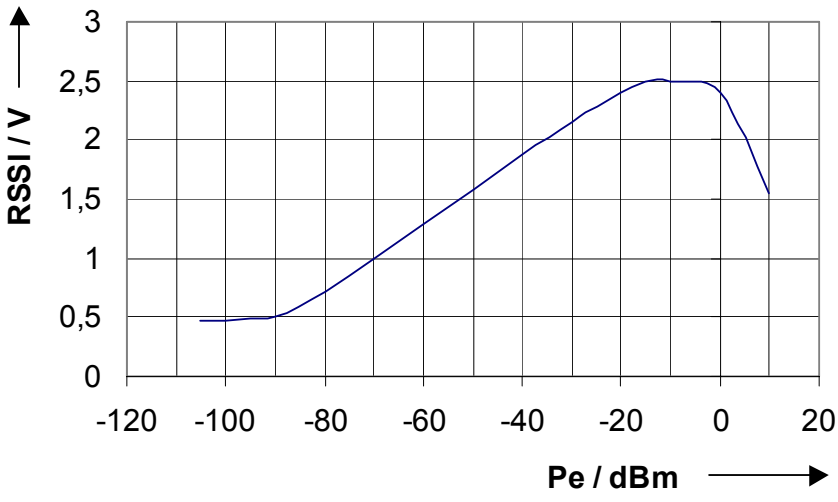
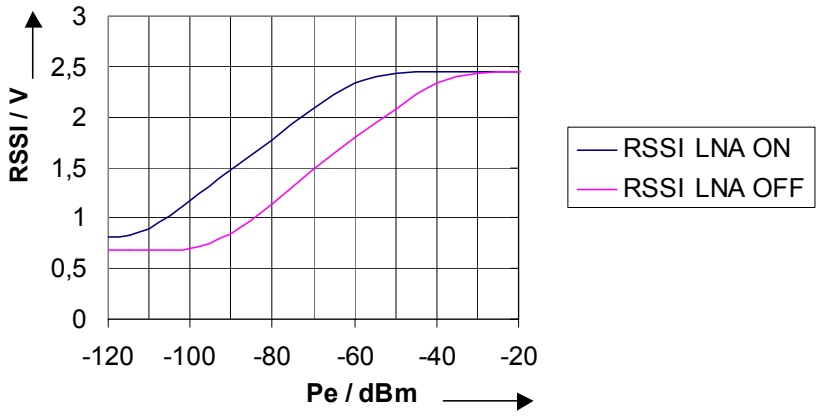


Limiterdemod.wmf

Figure 4-10 Limiter demodulator characteristics



RSSIvolt.wmf

Figure 4-11 RSSI Voltage vs. Receiver Input Level

Figure 4-9, Figure 4-10 and Figure 4-11 give some interesting information about the interaction of the different gain blocks of the receiver.

The voltage gain between the antenna input and the limiter input is 40dB.

The LNA block adds approx. 7dB of noise at the mixer input to the receiver.

Following the formula for the noise figure NF_c of cascaded blocks with individual noise figures NF1 and NF2 and the gain G1

$$NF_c = NF1 + (NF2-1)G1$$

it is quite evident that the given factor of $7dB \cong 5$ is the factor between the two terms of the above formula. Applying this formula, it can be concluded that the LNA gain, G_{LNA} can be reduced by 3dB without degrading the overall noise characteristics of the receiver significantly. The factor between the two terms in the formula will then be $4dB \cong 2.5$, then resulting in a total noise figure of

$$NF_c = NF_{LNA} + (NF_{MX} - 1)/G_{LNA} = NF_{LNA} (1 + 1/2.5) = 1.4\ NF_{LNA}$$

The noise of the LNA (having a noise figure of NF_{LNA}) will then contribute just

$1.4 \cong 1.4dB$ to the total noise of the receiver.

The converter block (LNA in cascade with the mixer stage) adds approx. 10dB of noise to the receiver at the input of the limiter. Applying the above formula for the cascaded noise figure again, it can be concluded that the converter gain could be reduced by 6dB without reducing the overall sensitivity of the receiver significantly. The receiver sensitivity will drop by 1.4dB.

The circuit thus gives some margin to apply filters with higher losses at the IF and at the LNA output.

4.9 Data Filtering

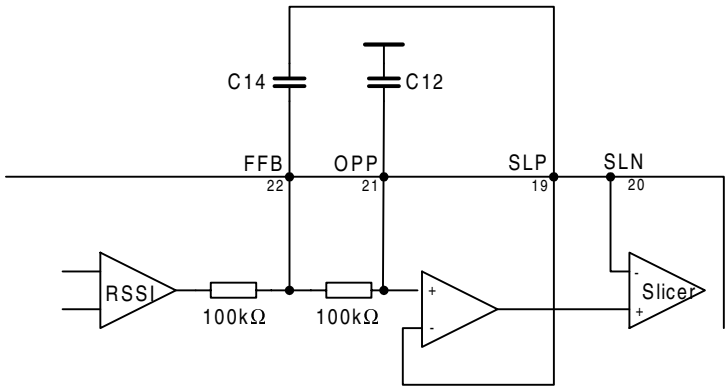
Data filtering is provided by means of a 2nd order Sallen-Key low-pass filter. This filter is DC coupled to the RSSI output of the IF amplifier. As can be seen from Figure 4-12, the cutoff frequency can be set by the external components C12 and C14. The data filter bandwidth should be set according to the highest frequency component of the baseband signal received. For example a 4.8kbit/s signal may correspond to a 2.4kHz square wave tone, depending on the code being used. The bandwidth of the filter should be set to $f_C \approx 1.5\ f_{max} = 3.6$kHz then to recover the transmitted pulse shape as far as possible. A wider data filter bandwidth does reduce the sensitivity by passing a wider spectrum of noise to the data slicer. Applying a Bessel characteristic filter will result in a good pulse shape of the band-limited signal.

Bessel Characteristic

C12= 1.362 / 4πRfc

C14= 1.33 C12

R = 100kΩ



Lowpass.wmf

Figure 4-12 Low-pass filter

As a design example a cutoff frequency of fc = 3.6 kHz will result in

C14 = 401pF

C12 = 301pF

4.10 Data Slicer

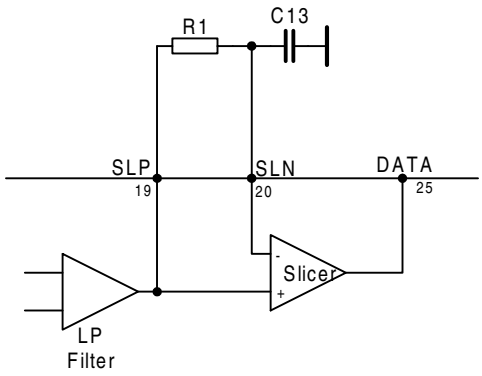
The filtered data signal is fed to the data slicer. This is a one-bit analog-to-digital converter that makes the bit decision and provides a rail-to-rail output. There are two different internal analog-to-digital converters. They differ in how to generate the slice reference.

As can be seen from Figure 4-13, the first circuit is the conventional adaptive data slicer deriving the threshold by means of a separate low-pass filter. This data slicer should be used for digital conversion of coded signals with no or only small DC components. The low-pass filter is designed for a long time constant in order to derive the average RSSI value (DC component of data) as an adaptive reference for the data slicer. As a design rule, the time constant T_A should be at least 3 times the longest period T_L of no signal change within the data sequence

$$T_A = R1 * C13 \geq 3 * T_L$$

This will result in a momentary shift of the reference level by -3.5dB of the data signal amplitude.

The time constant selected directly affects the data slicer run-in time and as a result the receiver settling time.



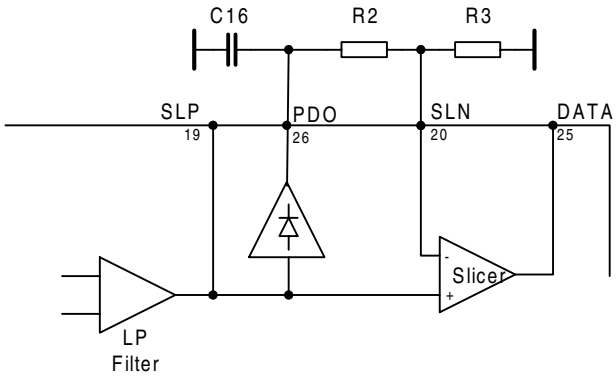
Dataslicer.wmf

Figure 4-13 Data slicer with adaptive slice reference

Figure 4-14 shows the alternate clamping data slicer which references its bit decision to the positive peak level of the data signal. This data slicer can be used with coding schemes employing high DC content. The decay time constant T_P of the peak detector should be designed to hold the detector voltage level well above the decision threshold of the comparator for a time long enough to bridge the longest time T_L with no level change within the data stream. This is most important for low data levels at the sensitivity threshold of the receiver. On the other hand T_P should be short enough to follow the variations of the received signal level. As a design rule, the time constant should be

$$T_P = (R2+R3) * C15 \geq 20 * T_L$$

The comparator threshold will be set by the division ratio of the voltage divider R2 /R3. The voltage drop across R2 acts like an additional offset voltage across the comparator input. It should be set to a value just big enough for a glitch-free decoding of a noisy signal at the receiver sensitivity threshold. Setting the threshold beyond the noise level of the receiver will give an operation similar to a squelch function. The data output will be held in a high state without a signal at the receiver input then. There will be some degradation in receiver sensitivity when applying the clamping data slicer.



Dataslicerclamp.wmf

Figure 4-14 Data slicer with clamping slice reference

The data output DATA, pin25 is a common collector stage utilizing an internal pull-down resistor of 80kΩ. The bandwidth of this output is limited to approx. 60kHz when loaded by 1MΩ//10pF. This limits the data rate to a maximum of 120kbit/s. Higher capacitive loading at the data output will further reduce the bandwidth. The bandwidth of the RSSI decoder, the low-pass filter and the data slicer are internally limited to >100kHz.

The evaluation board has been designed for

$$T_A = R1^* C13 = 100k\Omega * 47nF = 4.7ms$$

The longest uncompensated DC component of the decoded data stream therefore should not exceed 1.5ms. The lower frequency of the data stream is limited to 330Hz this way.

When using the peak data slicer, T_P has been designed for

$$T_P = (R2+R3) * C15 = (100k\Omega+820k\Omega) * 47nH = 43ms$$

The longest uncompensated DC component of the data stream is limited to 2.1ms now. The lower frequency limit of the data slicer has been extended down to 250Hz.

4.11 Decoder

For demonstration purposes, a standalone decoder device has been added to the receiver board. The HCS 515 (Microchip) is a decoder capable of responding to the code-hopping sequences sent by the encoder device HCS 360 (Microchip) at the transmitter side. Both devices, the encoder and the decoder, must be programmed with an identical customer code. Each decoder can undergo a learning process with up to 5 individual transmitters. Synchronization will be established following a defined learning sequence. Closing the “learn” contact will light up the LED for approx. 2s. Opening the contact after the LED has turned off sets the decoder to the learn mode. Activating the transmitter then will transfer the synchronization data. This completes the learning process. The LED will then light up for 500ms each time a synchronized transmitter signal is received.

4.12 Settling Time

Some receiver applications target an average supply current of 1mA and less. If an intermittent receiver operation is allowed, the supply current may easily be reduced from the typical value of 4.6mA to less than 1mA. The pulsed operation of the receiver can be controlled by a signal applied to the PDWN, pin27 input. A high state will enable the receiver. For pulsed receiver operation, a number of parameters need to be considered, such as receiver settling time, system response time and on-off duration.

The receiver settling time depends on a number of application parameters:

- Power up signal slew rate
- Data slicer design
- RF settling time

The RF settling time depends on the start-up time of the reference oscillator, the settling time of the PLL loop and the settling time of the bias of the receiver blocks. Due to the high excessive gain of the reference oscillator and the wide bandwidth of the PLL loop filter of 150kHz, the VCO will lock within a time of less than 1ms. The settling time of the receiver bias depends primarily on the size of the blocking capacitor C11. The impedance of capacitor C11 has, however, to be low compared to the input impedance of the IF amplifier at the IF frequency of 10.7MHz. A capacitor of 100pF gives a 1dB loss of IFgain at the input impedance of 330Ω. Applying C11=10nF will give a bias settling time of the IF amplifier of only 200µs.

The settling time of the data slicer is given by the low-pass characteristic of the imparted filter functions.

The adaptive data slicer is dominated by the $T_A = R1 * C13$ time constant. The settling time for a valid data signal will be:

$$T_{SA} \approx 3\ T_A$$

The peak data slicer will settle within a much shorter time. The hold capacitor C15 on the application board is charged by the output resistor R_L of the peak detector during each positive cycle of the data signal. The charging process may therefore take several cycles of the data signal. It is influenced by the shape of the data signal. A symmetrical signal will result in an access time T_{SP} of the peak detector of

$$T_{SP} \approx 6 * R_L * C15$$

All the individual settling times have to be considered in finding the total settling time of the receiver. On the evaluation board they are

- Bias settling time 0.2ms
- Start-up time of the reference oscillator 0.6ms
- Power supply slew rate < 1ms
- T_{SA} 14ms
- T_{SP} 0.3ms

As can be seen, T_{SA} is the dominant time. All the other functions have settled before the low-pass R1 - C13 has been charged. The settling time of the evaluation receiver will be approx. 15ms, utilizing the sliding data slicer and it will be below 1ms when the peak data slicer is applied.

4.13 Spurious Radiation

The receiver has to meet the European Telecommunications Standards Institute ETS 300 220 requirements. Other requirements may apply for other countries.

According to ETS 300 220, the limits for spurious radiation on the receiver side are:

-57 dBm in the range of 25MHz to 1GHz

-30 dBm in the range of 1GHz to 40GHz

Two different types of emission have to be considered, conducted (antenna port) and board radiation. Conducted emission is defined as the spurious power level at the antenna port. Radiated emission is defined as the “effective radiated power” (ERP) emitted by the board.

The most important spurious signal is the LO signal. The low power design of the VCO and a careful PCB layout keep the spurious radiation well below the limits. The spurious levels measured at the evaluation board can be summarized as:

Table 4-8 Spurious Radiation Levels

Source of emission		Receiver Frequency		Limit
		434 MHz	869 MHz	ETS 300 220
Antenna port VCO	858MHz	-90dBm	-73dBm	-57dBm
VCO/2	423MHz	-102dBm	<-120dBm	-57dBm
Radiated ERP VCO	858MHz	-73dBm	-67dBm	-57dBm
VCO/2	423MHz	<-120dBm	<-100dBm	-57dBm

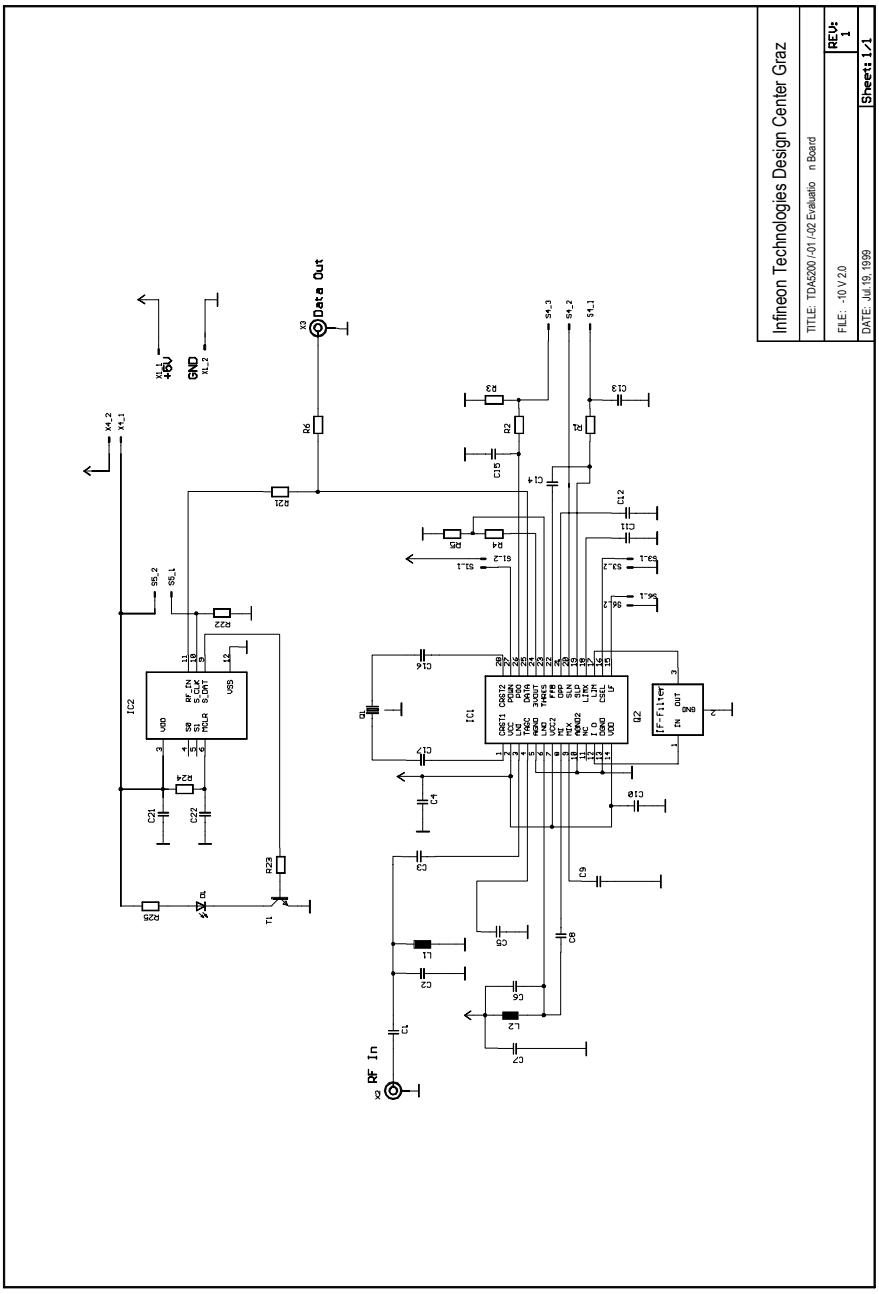
The TDA 5200 conforms to the ETS 300 220 requirements

5 Reference

Contents of this Chapter

5.1 Test Circuit

The device performance parameters were measured on an Infineon evaluation board. This evaluation board can be obtained together with evaluation boards of the accompanying transmitter device TDA5100 in an evaluation kit that may be ordered on the INFINEON RKE Webpage www.infineon.com/rke



Test_circuit.wmf

Figure 5-1 Schematic of the Evaluation Board

5.2 Test Board Layouts

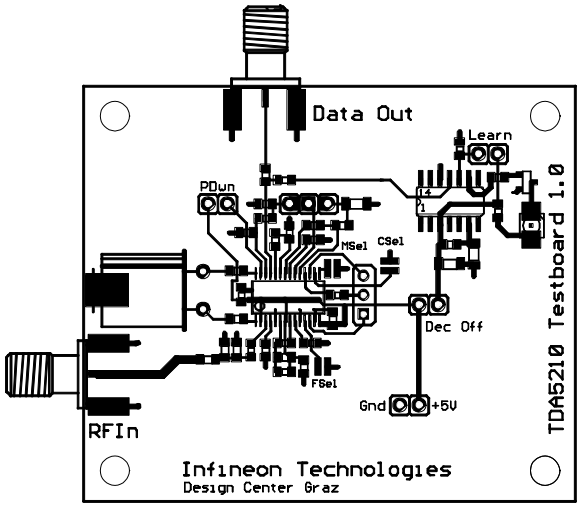


Figure 5-2 Top Side of the Evaluation Board

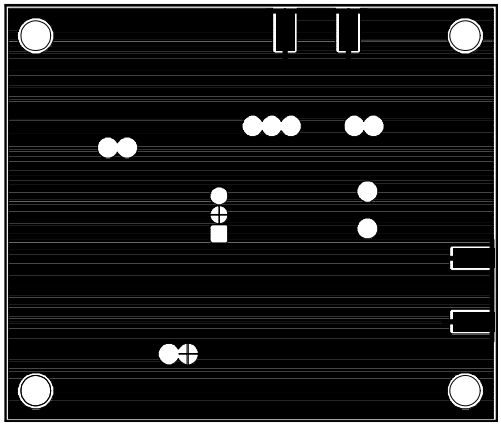


Figure 5-3 Bottom Side of the Evaluation Board

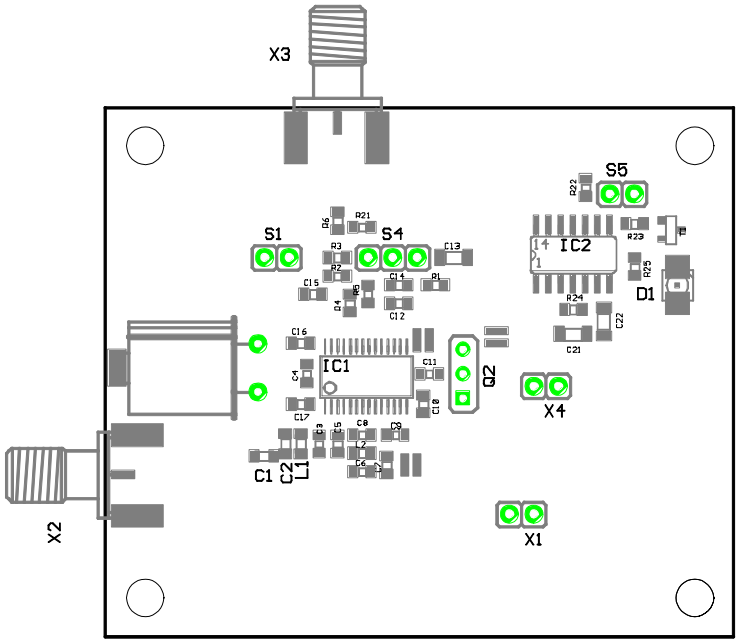


Figure 5-4 Component Placement on the Evaluation Board

5.3 Bill of Materials

The following components are necessary for evaluation of the TDA5200 without use of a Microchip HCS515 decoder.

Table 5-1 Bill of Materials

Ref	Value	Specification
R1	100kΩ	0805, ± 5%
R2	100kΩ	0805, ± 5%
R3	820kΩ	0805, ± 5%
R4	120kΩ	0805, ± 5%
R5	180kΩ	0805, ± 5%
R6	10kΩ	0805, ± 5%
L1	434 MHz: 15nH 869 MHz: 3.3nH	Toko, PTL2012-F15N0G Toko, PTL2012-F3N3C
L2	434 MHz: 8.2pF 869 MHz: 3.9nH	0805, COG, ± 0.1pF Toko, PTL2012-F3N9C
C1	1pF	0805, COG, ± 0.1pF
C2	434 MHz: 4.7pF 869 MHz: 3.9pF	0805, COG, ± 0.1pF 0805, COG, ± 0.1pF
C3	434 MHz: 6.8pF 869 MHz: 5.6pF	0805, COG, ± 0.1pF 0805, COG, ± 0.1pF
C4	100pF	0805, COG, ± 5%
C5	47nF	1206, X7R, ± 10%
C6	434 MHz: 10nH 869 MHz: 3.9pF	Toko, PTL2012-F10N0G 0805, COG, ± 0.1pF
C7	100pF	0805, COG, ± 5%
C8	434 MHz: 33pF 869 MHz: 22pF	0805, COG, ± 5% 0805, COG, ± 5%
C9	100pF	0805, COG, ± 5%
C10	10nF	0805, X7R, ± 10%
C11	10nF	0805, X7R, ± 10%
C12	220pF	0805, COG, ± 5%
C13	47nF	0805, X7R, ± 10%
C14	470pF	0805, COG, ± 5%
C15	47nF	0805, X7R, ± 5%
C16	15pF	0805, COG, ± 1%
C17	8.2pF	0805, COG, ± 0.1pF
Q2	(f_{RF} – 10.7MHz)/32 or (f_{RF} – 10.7MHz)/64	HC49/U, fundamental mode, CL = 12pF, e.g. 434.2MHz: Jauch Q 13,23437-S11-1323-12-10/20 e.g. 868.4MHz: Jauch Q 13,40155-S11-1323-12-10/20

Table 5-1 Bill of materials (continued)		
Ref	**Value**	**Specification**
F1	SFE10.7MA5-A or SKM107M1-A20-10	Murata Toko
X2, X3	142-0701-801	Johnson
X1, X4, S1, S5		2-pole pin connector
S4		3-pole pin connector, or not equipped
IC1	TDA 5200	Infineon

Please note that in case of operation at 434 MHz a capacitor has to be soldered in place of L2 and an inductor in place of C6.

The following components are necessary in addition to the above mentioned ones for evaluation of the TDA5200 in conjunction with a Microchip HCS515 decoder.

Table 5-2 Bill of Materials Addendum		
Ref	**Value**	**Specification**
R21	22kΩ	0805, ± 5%
R22	100kΩ	0805, ± 5%
R23	22kΩ	0805, ± 5%
R24	820kΩ	0805, ± 5%
R25	560kΩ	0805, ± 5%
C21	100nF	1206, X7R, ± 10%
C22	100nF	1206, X7R, ± 10%
IC2	HCS515	Microchip
T1	BC 847B	Infineon
D1	LS T670-JL	Infineon

6 List of Figures

7 List of Tables