FAQs for SmartLEWIS transmitter TDA5150

Version 1.0, January, 17th 2012

Info: All FAQs are valid for TDA5150 transmitter, unless otherwise noted.

1. Question: May virtually any crystal within the specified frequency range of the reference oscillator (12..14 MHz) be used?

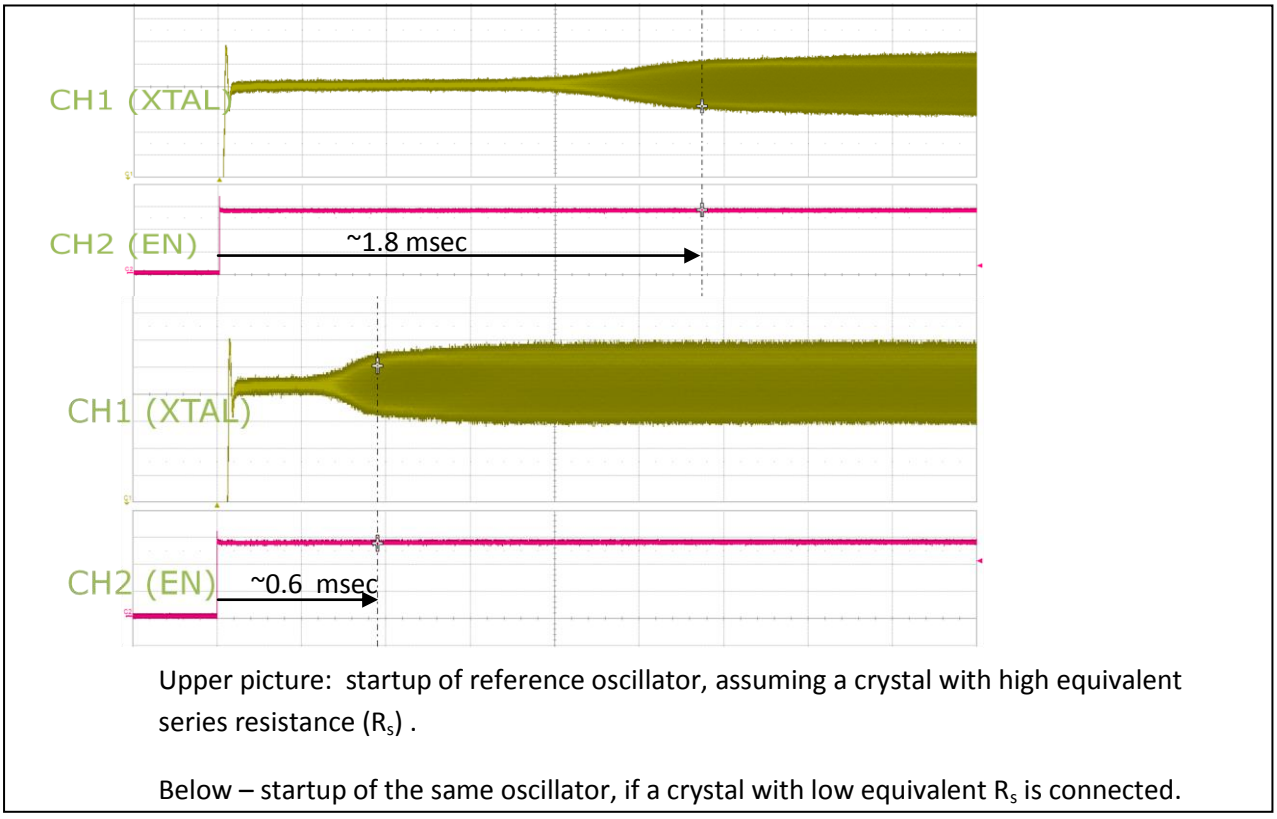
Answer At the 1st glance the answer would be an unconditional yes, as the fractional synthesizer accepts any frequency value in the specified range, as reference signal.
However following aspects have to be considered – startup time, relative level of fractional spurs as well as the crystal's short- and long term frequency stability (related to temperature and ageing).

1.1 The startup time of the reference oscillator, which at its turn is determined mainly by the crystal parameters (R_s; C_0; L_1 and at less extent also C_1 of crystal).
It is worth to note that:

- Crystals with high motional inductance (L_1) tend to start slower as those with low inductance.
- The same is true for the equivalent series resistance. As higher the value of this parameter (R_s) as longer the startup time will be.

The figure below depicts the startup time achieved with two different crystals, but in the same TDA5150 application circuit.
The component with higher motional inductance and resistance (in upper screenshot) achieves a startup time which is at least twice as long as that of the version with lower equivalent inductance and resistance (shown in lower part of screenshot).

***Note**: the above statement does not mean that crystals with low equivalent inductance are always the best choice. They tend to expose a "soft" behavior , are more suitable to be frequency-pulled versus the "stiff" crystals, which expose high equivalent inductance (referenced for the same frequency, of course).*
Consider also long-term stability of specific crystals if tight tolerances are part of the system specification and performance requirements.



Upper picture: startup of reference oscillator, assuming a crystal with high equivalent series resistance (R_s) .

Below – startup of the same oscillator, if a crystal with low equivalent R_s is connected.

1.2 The relation between transmit frequency (f_{TX}) and reference frequency(f_{XTAL}) can be put in following form:

$$\frac{fTX}{fXTAL} = N + r; \quad where\ \boldsymbol{N}\ is\ an\ integer\ and\ \boldsymbol{r}\ the\ fractional\ part\ of\ the\ division,\ 0 \leq r < 1 \quad [\mathbf{1}]$$

In order to avoid fractional spurs , the crystal frequency have to be chosen in such way, to fulfill the following relation:

$$0{,}1 < r\ < 0{,}9 \qquad \textbf{[2]}$$

The check is trivial for a system operating on a single frequency, but if the final target is a multichannel or frequency hopping system , relation [2] have to be fulfilled for each, individual frequency used by system.

1.3 The third aspect is related to the programmable frequency shift, a feature of TDA5150 (for FSK and GFSK modulation modes). Frequency modulation is achieved in the TDA5150 by means of a sigma-delta modulator.

- If the transmit frequency(f_{TX}) would be very close to an integer multiple of the reference frequency (f_{XTAL}), a scenario which in fact is a violation of the rule described by equation **[2]**, and at the same time
- A large enough value for the frequency shift would be programmed, the sigma-delta modulator subpart would “roll” over an integer-N division ratio number, and the generated spectrum may be very different from the expected one.

However , if the equation **[2]** is fulfilled, the normal operating conditions for the sigma-delta modulator are also fulfilled, automatically.

Final conclusions:

- Any crystal frequency within the allowed range (of 12..14 MHz) may be chosen, provided that the relation [2] is fulfilled for each transmit channel which is intended to be used
- The negative resistance of the reference oscillator (R_{NEG}) and the motional parameters of the crystal (C_0; R_s; L) are the main factors which determine the oscillator’s startup time.
- Provide sufficient settling time for the oscillator to reach stationary mode before starting an RF-transmission. However the special function registers (SFR) may be read and written before the startup time elapsed, the timing limitation refers only to start of an RF-transmission (as the on-chip synthesizer shall be fed with the reference frequency signal from a stable source).

2. Question: What is the total variation of the RF signal power?

Answer As for the most of C-class, low power RF amplifiers, the output power is influenced mainly by:

- Supply voltage level
- Impedance of the load

Of course the variation of the RF output power is subjected to the variation of the above listed main factors.
As secondary factors, temperature dependent variation of the RF power gain of the power amplifier and process conditioned parameter variations may be taken in account.

Over the full supply voltage range (of 1,9V..3,6V) an ideal (non-saturating) amplifier would have a power variation of 6dB (2*3dB). The total power variation of the TDA5150, including temperature conditioned variations, between the minima and maxima of supply voltage (1,9..3,6V) is of 5 dB.

A downloadable Application Note is dealing with stabilization techniques of the RF-power.

3. Question: Referring to TDA5150, which are the recommended methods for controlling the RF-power?

Answer The output RF power can be controlled over the following means:

3.1 The duty cycle of the signal driving the RF power amplifier (in four steps of 27%, 33%, 39% and 44%). The control is accomplished over the bits 5 and 4 of Special Function Register (0x1F).
This mechanism is effective in the 434 MHz; 868 MHz and 915 MHz bands (ISMB = 1/2/3, according to notation system used in the TDA5150 Datasheet).
The duty –cycle control is deactivated in the 315 MHz band (ISMB = 0).The detailed description is to be found in **SFR Detailed Descriptions** part of the **TDA5150 Datasheet.**

ADDR 0x1F		**ANTTDCC—Antenna Tuning and Duty Cycle Configurations**					
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
reserved	DCC DISABLE	DCCCONF	DCCCONF	TUNETOP	TUNETOP	TUNETOP	TUNETOP
w/0	w/0	w/1	w/0	w/0	w/0	w/0	w/0

Bit 7	reserved		Reserved, set to 0
Bit 6	DCCDISABLE		Duty cycle control disable
Bit <5:4>	DCCCONF		Duty cycle control delay configuration bit <1:0>
Bit 3:0	TUNETOP		Antenna tuning top (PAOUT pin) bit <3:0>

DCCDISABLE	Duty cycle control disable (must be 0 for ISMB=0)					
	0 enabled			1 disabled (delay = 0ps)		
DCCCONF	Duty cycle control delay configuration (ISMB = 1/2/3, for ISMB = 0 => delay = 0 ps)					
	00: 43% (69/35/33 ps)	01: 39% (207/104/98 ps)	10: 35% (346/173/164 ps)	11: 31% (484/242/230 ps)		
TUNETOP	Antenna tuning top capacitor selection (4-bits):					
	Individual switch of capacitor banks		**0**: switched off		**1**: switched on	
	Bit(0) ==> 60 fF	Bit(1) ==> 120 fF	Bit(2) ==> 240 fF	Bit(3) ==> 480 fF		

3.2 The number of active RF power amplifier stages, as the RF PA comprises a total of 11 elementary cells, connected in parallel. Each one is a class-C amplifier. The cells are grouped in three blocks.
PA Block 0 is composed of 9 elementary stages, **PA Block 1** and **PA Block 2** are strong single stages. Each PA Block can be individually enabled and disabled to optimize power consumption and efficiency in an output power subrange.
The 3 PA Blocks are enabled by PA_PS1 and PA_PS2 bits contained in Special Function Register (0x1A).
Enabling the 3 PA Blocks offers following typical PA ranges (note that the PA output power depends also on the external matching circuit, at a quite large extent):

- PA_PS bit0=1 +5 dBm matched; Pout = +5dBm down to -10dBm, 9 PA Stages
- PA_PS bit1=1 +8 dBm matched; Pout = +8dBm down to -10dBm, 10 PA Stages
- PA_PS bit2=1 +10 dBm matched; Pout = +10dBm down to -10dBm, 11 PA Stages

In addition to enabling the PA Blocks, the 11 PA stages have to be configured. This is accomplished by setting the bit-fields POUT1 (0x1B.3:0) for Output Power Setting #1 and POUT2 (0x1B.7:4) for Output Power Setting #2 in Special Function Register (0x1B).

ADDR 0x1A		POWCFG0—PA Output Power Configuration Register 0					
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PA_PS2	PA_PS2	PA_PS2	PA_PS1	PA_PS1	PA_PS1	SLOPEDIV	SLOPEDIV
w/0	w/0	w/0	w/0	w/0	w/0	w/0	w/0

Bit <7:5>	PA_PS2		PA output blocks setting 2 bit <2:0>
Bit <4:2>	PA_PS1		PA output blocks setting 1 bit <2:0>
Bit <1:0>	SLOPEDIV		ASK sloping clock divider bit <9:8>

PA_PS2	Individual control of the 3 PA blocks, setting 2 (3-bits)					
	0: disabled	**1**: enabled	Bit(0) ==> PA block 0	Bit(1) ==> PA block 1	Bit(2) ==> PA block 2	
PA_PS1	Individual control of the 3 PA blocks, setting 1(3-bits)					
	0: disabled	**1**: enabled	Bit(0) ==> PA block 0	Bit(1) ==> PA block 1	Bit(2) ==> PA block 2	
SLOPEDIV	ASK sloping clock division ratio (10 bits, bits < 9:8 >), defines the frequency of the ASK signal shaping using PA power stage switching					
	Range:		from **0x000**: SLOPEDIV = 1		to **0x3FF**: SLOPEDIV = 1024	

ADDR 0x1B		POWCFG1—PA Output Power Configuration Register 1					
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
POUT2	POUT2	POUT2	POUT2	POUT1	POUT1	POUT1	POUT1
w/0	w/0	w/0	w/0	w/0	w/0	w/0	w/0

Bit <7:4>	POUT2		Output power setting 2 bit <3:0>
Bit <3:0>	POUT1		Output power setting 1 bit <3:0>

POUT2	PA output power setting 2 (4 bits), defines the number of enabled PA stages		
	Range:	from **0x0**: POUT2 = 0	to **0xB**: POUT2 = 11 > **0xB**: POUT2 = 11
POUT1	PA output power setting 1 (4 bits), defines the number of enabled PA stages		
	Range:	from **0x0**: POUT1 = 0	to **0xB**: POUT1 = 11 > **0xB**: POUT1 = 11

Note: $POUT_n$ = 0 means that the PA is effectively OFF).

The detailed description of steps for RF power programming is to be found in **PA Output Power Programming** part of the **TDA5150 Datasheet.**

Final conclusions: By taking in account the effects of RF output power variation over

- programmable duty cycle value and
- number of active RF power amplifiers

a bi-dimensional RF power control field is obtained.
Further, it is worth to note that

- The variation of the RF power amplifier's supply voltage does influence the output power, as explained by answer to **Question: #2**, and
- The available maximum power is limited by the load impedance, as "perceived" by the RF power amplifier (as the load is connected usually over a matching network to the RF PA).

4. **Question: Are there any special routing rules, which have to be considered by layout?**

Answer Beyond the rules which are generally valid for boards operating with radio frequency signals please take in account the followings:

- the components of the impedance matching network, found between the RF power amplifier and load (this last is usually the antenna) shall be connected to the RF return ground (Pin7, GNDPA) in such way, which yields:
  - Short tracks in the RF ground network and consequently low impedance of the lines belonging to it
  - If possible, use a star-like topology instead of a ladder-like in the RF-ground network
  - Avoid loops (or at least long loops) as those may form (parasitic) loop antenna(s). If the resonant frequency of such a structure is close to a harmonic of the carrier, the loop may radiate the respective harmonic with increased efficiency, leading to high level of unwanted (out of band) signal.
  - For decoupling of the RF power amplifier's supply voltage use capacitors with low ESR value, or, at best two capacitors, one of high capacity (as rule of thumb in the 22..100 nF range) and one in the 6.8..33 pF range, yielding an efficient, broadband decoupling. Place the decoupling capacitors close to the DC-feed coil connection and to RF return ground (Pin7).
  - In order to minimize coupling between antenna and reference oscillator circuit (over EM-field), connect the crystal and the load capacitor associated to it to the reference oscillator (Pin 2, XTAL) over short track(s). If EM simulation is used during board design and layout work, check and make sure that components and tracks belonging to the reference oscillator are not exposed to intensive EM field. As the VCO is operating on significantly higher frequency as the transmit frequency (4, 3 or 2 times the Tx-frequency, depending on selected band) the risk of load pulling over back-radiation is low, but even so, if excessive levels of RF signal are injected into the reference oscillator, this may have adverse effects on signal spectrum.

5. **Question: Is the TDA5150 suitable for frequency hopping? If yes, what is the maximum dead-time between two hops?**

Answer The TDA5150 has four PLL setting banks, which may be pre-programmed for different transmit frequencies. If this technique is used for hopping, the switchover time can be kept short, as before starting a transmission it is required to indicate just which bank shall be used, instead of downloading all the frequency information. The dead time between hops is in this case is typically 20 µsec if the hop is below 1 MHz, relative to previously used channel, and in any case less than 100 µsec, between band-ends (f_{min} /f_{max}).
If a higher number of channels is required (>4) the PLL frequency information may be downloaded into the associated Special Function Registers in burst mode, in order to shorten the duration of data transfer and after completion of this operation the transmission may be started.
In this case the dead time between hops will be the sum of:
-Time consumed to download the PLL channel data and

- Time, required by PLL to achieve lock (which is, again typically 20 µsec or 100 µsec, depending on "size" of the frequency hop)

6. **Question: Which is the best procedure to check the communication protocol at hardware level?**

Answer The traffic on the SPI-bus can be monitored. the data decoded and interpreted.
A downloadable Application Note (Programming the TDA5150) gives in-depth description the programming of the transmitter and contains hints about debugging procedures and an overview of relations between modulation parameters and generated signal spectrum.

7. Question: What happens if the supply voltage drops under the allowed minima?

Answer the chip-internal low voltage /brownout detector block of the TDA5150 has two distinct functions:

- Low supply voltage warning (whereas the supply voltage is still higher as the minimum of safe operating voltage).
  Two trigger levels, of nominal 2.4V and 2.1V give an “early” and a “close” warning, if the supply voltage value decreases toward the reliable operational) minima of 1.9V

- A brownout detector, which stops transmissions if the supply voltage drops below the minima of operating value, followed by a forced (brownout) reset. The nominal value of brownout trigger is of 1.75V, which is below the nominal minima for supply voltage (1.9V)

All the 3 events listed above do set designated flags in the status register (0x01). By reading the respective register warning about the low (but still reliable) supply voltage and / or abnormal transmission termination can be detected by Host and appropriate reaction shall be triggered.

Note: *reading the TXSTAT register (0x01) clears the previously set flag(s).*
If the register is red twice, consecutively, the 1st reading will deliver the correct content, but the 2nd may be erroneous, as it will show an “all clear” state, indicating no error, and thus information may be lost.
Thus it is indicated to read the status register after a transmission ends up, to achieve information about successful termination (or failure) of the transmission.

ADDR 0x01	**TXSTAT—Transmitter Status Register**						
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	n.u.	LBD_2V1	LBD_2V4	VAC_FAIL	BROUTERR	PARERR	PLLLDER
/	/	r/0	r/0	c/0	c/1	c/0	c/0

Bit 7	1		Set to 1, mandatory
Bit 5	LBD_2V1		battery low detected, threshold at 2.1 V -
Bit 4	LBD_2V4		battery low detected, threshold at 2.4 V
Bit 3	reserved		Don’t care
Bit 2	BROUTERR		Brown out event
Bit 1	PARERR		Parity error
Bit 0	PLLLDER		PLL lock detector error

LBD_2V1	Battery voltage drop below 2.1 V detected if **1** - in standby mode, bit is invalid
LBD_2V4	Battery voltage drop below 2.4 V detected if **1** - in standby mode, bit is invalid
BROUTERR	Brownout event detected if **1**
PARERR	Parity error detected if **1**
PLLLDERR	PLL lock error detected if **1**

8. Question: A strong sideband lobe occurred sporadically in the lower one sideband during transmission. What is the root cause of this phenomenon?

Answer

8.1 If the spur is

- present in both the lower and upper sideband, and
- the offset from carrier is the same (in absolute value, as one spur is below and the other above the carrier frequency) the likelihood for upmixing product is high.

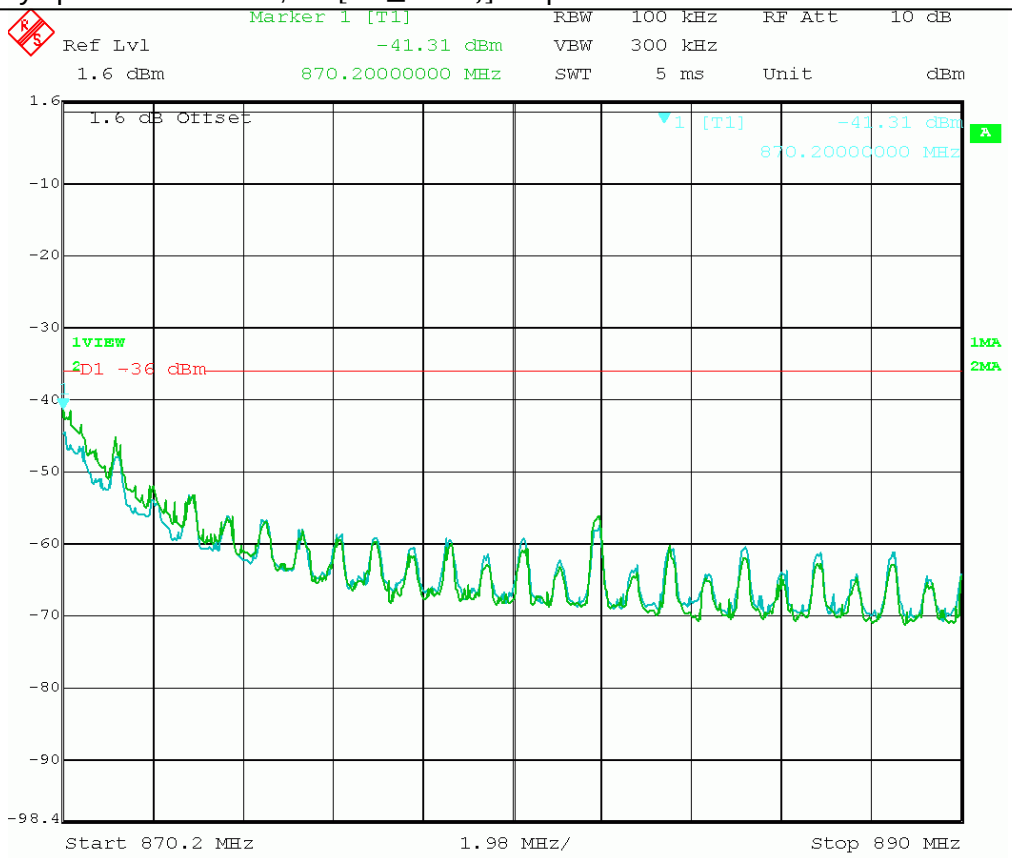
It may originate from crosstalk between a clock or data line with the reference oscillator's input for instance, or ripple generated by an external part, coupling into the TDA5150, over poorly decoupled supply line.

The upmixing product (P_m) can be expressed as

$$Pm = A\sin(2\pi f_T + \varphi_T) * I\cos(2\pi f_J + \varphi_J) \quad \textbf{[3]}$$

where f_T respectively φ_T are the frequency and initial phase of transmit channel signal and f_J respectively φ_J the frequency and initial phase of the interferer.

Due to upmixing, which may be associated also with intermodulation, the mentioned products may be found – if any spur is observable, at $[f_T \pm N * f_J]$ frequencies.



Example for spurs generated by crosstalk between a GPIO line of Host and reference frequency input (XOSC) of TDA5150.
The spurs are placed 800 kHz apart, which equals the frequency of signal on the mentioned GPIO line (used to scan a key matrix).
This kind of crosstalk could be minimized if reasonable layout rules are followed, and even with the original layout, if during the RF transmission the Host avoids activity leading to to state – change of GPIO lines.

8.2 If the spur is observable only in one sideband (as the example below shows) the probable origin of interferer is from outside the system containing the TDA5150, or – quite seldom, a tendency for self-oscillation in the system.

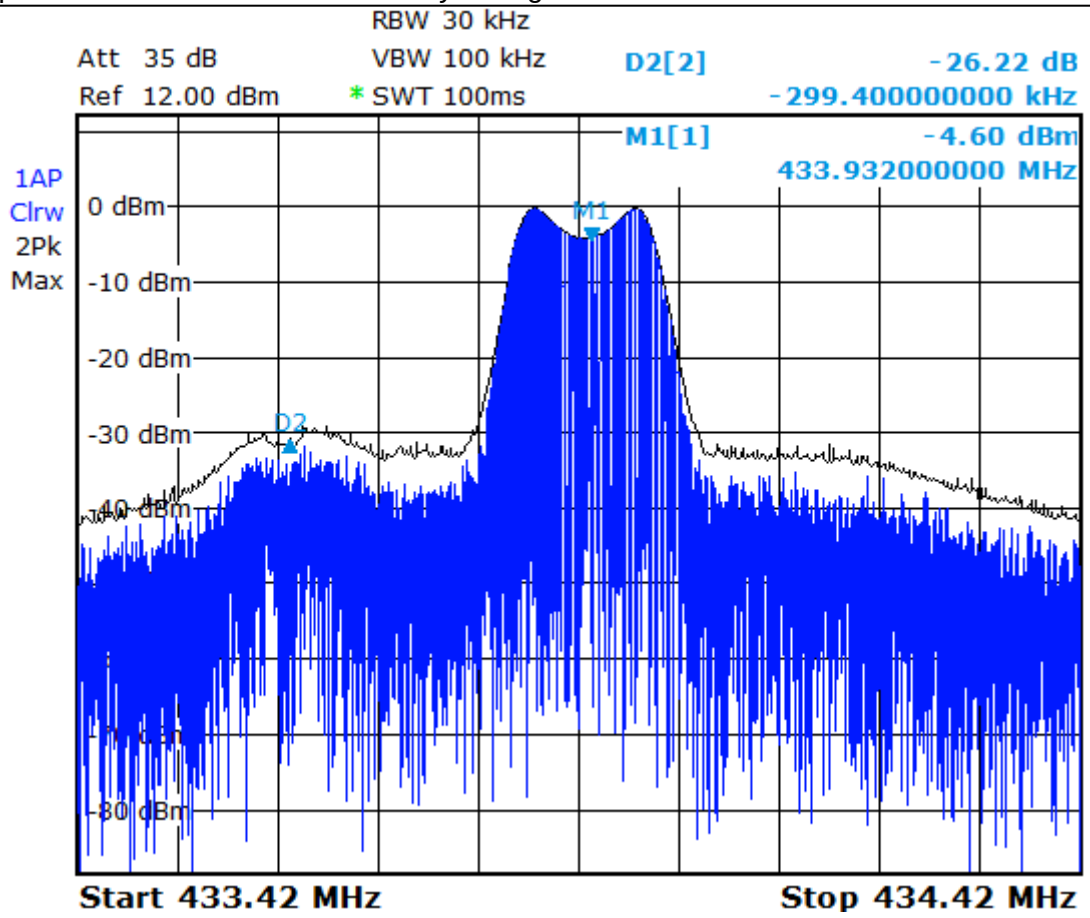
To track back for root cause:

- During measurements use a shielded chamber (or box) containing the device under test (DUT) If the shielding enhances the behavior, and the spur decreases or does vanish, the source of interferer is probably an external one.

- If the shielding does not enhance the situation, but the frequency of the spur does “slide” by variation of the supply voltage and/ or variation of load impedance, (i.e. the frequency of the spur does change) it is likely a tendency toward self-oscillation.

  ***Note**: the driver and RF power amplifier of the TDA5150 are practically speaking unconditionally stable, but for the unlikely case that self-oscillation occurs, decrease of the equivalent Q of the matching network (found between RF PA output and load) may solve the issue.*

The example shows the effects of a relatively strong external interferer in the lower sideband.



Transmission on 433.920 MHz and a strong interferer in the lower sideband (marked by differential marker D2).
Black trace recorded using MaxHold mode, blue trace in normal (Clear/Write) mode.

9. The TDA5150s Special Function Register map list is rather long (0x00..0x27H). If only transmissions according to ASK (OOK) modulation scheme are intended, is it necessary to program all those registers?

Answer Only the **Special Function Registers** which contain data and setting parameters relevant for the particular transmission mode have to be programmed.
For instance if only one transmission frequency is used , say PLL Channel A, the SFRs (0x09)..(0x0C) have to be programmed (as those contain the integer and fractional part of frequency information) but the SFR range (0x0D)..(0x18) could be skipped, as that block is related to PLL Channels B; C and D.

Hint: using the freely downloadable TESEUS tool to generate a particular setup (even multichannel, with transmission parameters differing not only in term of Tx-frequency, but Tx- power and used modulation scheme) can shorten significantly the initial project setup time.
The setup can be edited, modified , saved for later usage and be exported as ASCII (text) file or as C header and source, as well.