

High-Performance DrMOS

6 mm x 6 mm x 0.8 mm IQFN

TDA21220

Data Sheet

Revision 2.5, 2013-01-07

Power Management and Multimarket

Edition 2013-01-07

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Revision History

Page or Item	Subjects (major changes since previous revision)
Revision 2.5, 2013-01-07	
	Updated page 4

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1 Applications

- Desktop and Server VR11.X and VR12.X buck-converter
- Network and Telecom processor VR
- Single Phase and Multiphase POL
- CPU/GPU Regulation in Notebook, Desktop Graphics Cards, DDR Memory, Graphic Memory
- High Power Density Voltage Regulator Modules (VRM).

2 Features

- Compliant to Intel® VR12.X Driver and Mosfets Module (DrMOS) for Desktop/Server Applications
- For synchronous Buck step down voltage applications
- Maximum average current of 50 A
- Power MOSFETs rated 25 V for safe operation under all conditions
- Extremely fast switching technology for improved performance at high switching frequencies (> 1 MHz)
- Remote driver disable function
- Switch modulation (SMOD#) of low side MOSFET
- Includes bootstrap diode
- Undervoltage lockout
- Shoot through protection
- +5 V high side and low side MOSFETs driving voltage
- Compatible to standard +3.3 V PWM controller integrated circuits
- Tri-state PWM input functionality
- Small package: IQFN40 (6 x 6 x 0.8 mm³)
- RoHS compliant

Table 1 Product Identification

Part Number	Temp Range	Package	Marking
TDA21220	-25 to 125 °C	6 x 6 x 0.8 mm ³ PG-IQFN-40-1	TDA21220



Figure 1 Picture of the product

3 Description

3.1 Pinout

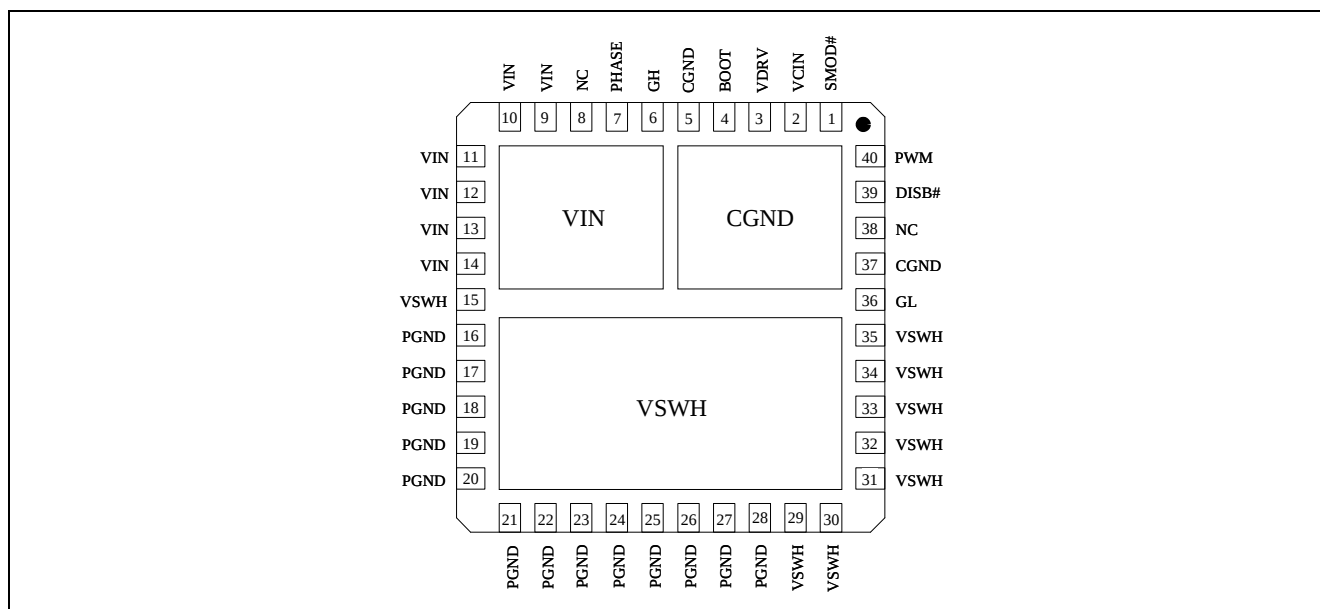


Figure 2 Pinout, numbering and name of pins (transparent top view)

Note: Signals marked with “#” at the end are active low signals.

Table 2 I/O Signals

Pin No.	Name	Pin Type	Buffer Type	Function
1	SMOD#	I	+3.3 V logic	Low Side gate disable When SMOD# is “low” the GL is “off”
6	GH	O	Analog	High side gate signal Monitoring of high side MOSFET gate
7	PHASE	I	Analog	Switch node (reference for Boot voltage) internally connected to VSWH pin, connect to BOOT capacitor
4	BOOT	I	Analog	Bootstrap voltage pin Connect to BOOT capacitor
15, 29 to 35, VSWH pad	VSWH	O	Analog	Switch node output High current output switching node
36	GL	O	Analog	Low side gate signal Monitoring of low side MOSFET gate
39	DISB#	I	+3.3 V logic	Disable signal (active low) Connect to GND to disable the IC.
40	PWM	I	+3.3 V logic	PWM drive logic input The tri-state PWM input is compatible with 3.3 V.

Table 3 Power Supply

Pin No.	Name	Pin Type	Buffer Type	Function
2	VCIN	POWER	–	Logic supply voltage 5 V bias voltage for the internal logic
3	VDRV	POWER	–	FET gate supply voltage High and low side MOSFETs gate drive supply
9 to 14, Vin pad	VIN	POWER	–	Input voltage Supply of the drain of the high side MOSFET

Table 4 Ground Pins

Pin No.	Name	Pin Type	Buffer Type	Function
5, 37, CGND pad	CGND	GND	–	Control signal ground Should be connected to PGND externally
16 to 28	PGND	GND	–	Power ground All these pins must be connected to the power GND plane through multiple low inductance vias.

Table 5 Not Connected

Pin No.	Name	Pin Type	Buffer Type	Function
8, 38	NC	–	–	No internal connection Leave pin floating or tie to GND.

3.2 General Description

The Infineon TDA21220 is a multichip module that incorporates Infineon's premier MOSFET technology for a single high side and a single low side MOSFET coupled with a robust, high performance, high switching frequency gate driver in a single 40 pin QFN package. The optimized gate timing allows for significant light load efficiency improvements over discrete solutions. State of the art MOSFET technology provides exceptional full load performance.

When combined with the Infineon's family of digital multiphase controllers, the TDA21220 forms a complete core-voltage regulator solution for advanced micro and graphics processors as well as point-of-load applications.

The TDA21220 is pin to pin compatible and compliant with the Intel 6x6 DrMOS specification. The device package height is only 0.8 mm, and is an excellent choice for applications with critical height limitations.

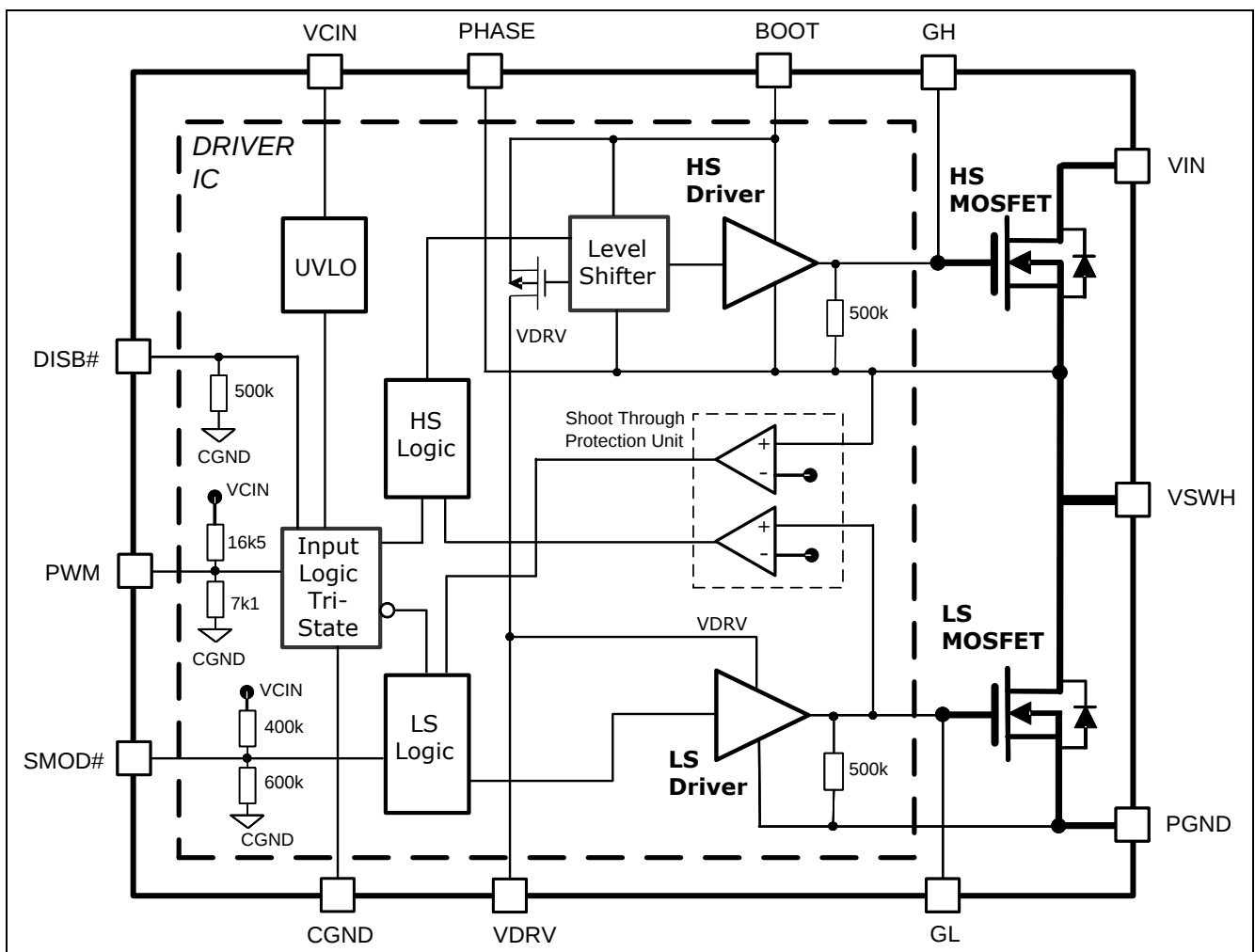


Figure 3 Simplified Block Diagram

4 Electrical Specification

4.1 Absolute Maximum Ratings

Note: $T_{Ambient} = 25^{\circ}C$

Stresses above those listed in Table 6 “Absolute Maximum Ratings” may cause permanent damage to the device. These are absolute stress ratings only and operation of the device is not implied or recommended at these or any other conditions in excess of those given in the operational sections of this specification. Exposure to the absolute maximum ratings for extended periods may adversely affect the operation and reliability of the device.

Table 6 Absolute Maximum Ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Frequency of the PWM input	f_{SW}	–	–	1.2	MHz	–
Maximum average load current	I_{OUT}	–	–	50	A	–
Input Voltage	V_{IN} (DC)	-0.30	–	25	V	–
Logic supply voltage	V_{CIN} (DC)	-0.30	–	6.0		–
High and Low side driver voltage	V_{DRV} (DC)	-0.30	–	6.0		–
Switch node voltage	V_{SWH} (DC)	-1	–	25		–
	V_{SWH} (AC)	-10 ¹	–	25		–
PHASE node voltage	V_{PHASE} (DC)	-1	–	25		–
	V_{PHASE} (AC)	-10	–	25		–
BOOT voltage	V_{BOOT} (DC)	-0.3	–	31.5		–
	V_{BOOT} (AC)	-1 ¹	–	31.5		–
	$V_{BOOT-PHASE}$ (DC)	-1	–	6.0		–
SMOD# voltage	$V_{SMOD\#}$ (DC)	-0.3	–	5.5		–
DISB# voltage	V_{DISB}^2	-0.3	–	5.5		–
PWM voltage	V_{PWM}^2	-0.3	–	5.5		–
Junction temperature	T_{Jmax}	-40	–	150	°C	–
Storage temperature	T_{STG}	-55	–	150		–

Note: All rated voltages are relative to voltages on the CGND and PGND pins unless otherwise specified.

¹ AC is limited to 10 ns

² Latch Up class II- Level B (Jedec 78). Please refer to Quality Report for details.

4.2 Thermal Characteristics

Table 7 Thermal Characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction-soldering point ¹	θ_{JS}	–	5	–	K/W	–
Thermal resistance, junction-top of package	θ_{Jtop}	–	20	–		–

4.3 Recommended Operating Conditions and Electrical Characteristics

Note: $V_{DRV} = V_{CIN} = 5\text{ V}$, $T_{Ambient} = 25^{\circ}\text{C}$ (conditions for table 8 through table 12 unless otherwise specified)

Table 8 Recommended Operating Conditions

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input voltage	V_{IN}	5	–	16	V	–
MOSFET driver voltage	V_{DRV}	4.5	5	5.5		–
Logic supply voltage	V_{CIN}	4.5	5	5.5		V_{CIN} rising, 3.3V to 3.9V: $dv_{CIN}/dt > 300\text{V/s}$
Junction temperature	T_{JOP}	-25	–	125	$^{\circ}\text{C}$	–

Table 9 Voltage Supply And Biasing Current

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Driver current	I_{VDRV_300kHz}	–	10	–	mA	DISB# = 5 V, $f_{SW} = 300\text{ kHz}$
	I_{VDRV_PWML}	–	25	–	μA	DISB# = 5 V, PWM = 0 V
IC current (control)	I_{VCIN_PWML}	–	400	–		DISB# = 5 V, PWM = 0 V SMOD# = Open
	I_{VCIN_O}	–	500	–		DISB# = 5 V, PWM = Open SMOD# = Open
IC quiescent	$I_{VCIN} + I_{VDRV}$	–	–	550		DISB# = 0 V
UVLO rising	V_{UVLO_R}	2.9	3.5	3.9	V	V_{CIN} rising, 3.3V to 3.9V: $dv_{CIN}/dt > 300\text{V/s}$
UVLO falling	V_{UVLO_F}	2.5	3.1	3.3		VCIN falling

¹ The junction-soldering point is referred to the VSWH bottom exposed pad.

Table 10 Logic Inputs And Threshold

Parameter		Symbol	Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
DISB#	Input low	V_{DISB_L}	0.7	1.1	1.3	V	V_{DISB} falling
	Input high	V_{DISB_H}	1.9	2.1	2.4		V_{DISB} rising
	Sink current	I_{DISB}	–	2	–	μA	$V_{DISB} = 1\text{ V}$
SMOD#	Input low	$V_{SMOD\#_L}$	0.7	1.1	1.3	V	$V_{SMOD\#}$ falling
	Input high	$V_{SMOD\#_H}$	1.9	2.1	2.4		$V_{SMOD\#}$ rising
	Open voltage	$V_{SMOD\#_O}$	–	3.0	–		–
	Sink current	$I_{SMOD\#}$	–	-8	–	μA	$V_{SMOD\#} = 1\text{ V}$
PWM	Input low	V_{PWM_L}	–	–	0.7	V	V_{PWM} falling
	Input high	V_{PWM_H}	2.4	–	–		V_{PWM} rising
	Input resistance	R_{IN-PWM}	3	5	7	$k\Omega$	$V_{PWM} = 1\text{ V}$
	Open voltage	V_{PWM_O}	–	1.5	–	V	V_{PWM_O}
	Tristate shutdown window ¹	V_{PWM_S}	1.2	–	1.9		–

Table 11 Timing Characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Tri-State to GL/GH rising delay	t_{pts}	–	15	–	ns	GH, GL unloaded
GL Shutdown Hold-Off time	t_{GLtssh}	–	150	–		
GH Shutdown Hold-Off time	t_{GHTssh}	–	85	–		
GH Turn-on propagation delay	t_{pdhu}	–	15	–		
GH Turn-off propagation delay	t_{pdlu}	–	20	–		
GL Turn-on propagation delay	t_{pdhl}	–	20	–		
GL Turn-off propagation delay	t_{pdll}	–	10	–		
DISB# Turn-off propagation delay falling	t_{pdl_DISB}	–	20	–		
DISB# Turn-on propagation delay rising	t_{pdh_DISB}	–	20	–		
PWM minimum pulse width high side	$t_{on_min_PWM}$	–	25	–		
PWM minimum off time	$t_{off_min_PWM}$	65	–	–		

¹ Maximum voltage range for tri-state

Table 12 Recommended Operation Timing

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test conditions
SMOD# rising to PWM rising edge set-up time	t_surll	-	20	-	ns	
SMOD# falling to PWM falling edge hold time	t_hfll	-	20	-		

Time t_surll is a recommended maximum time between SMOD# disabling and PWM going high to prevent the LS-MOSFET from turning on prior to its immediate turn-off.

Time t_hfll is a recommended maximum time between PWM falling and SMOD# enabling to prevent the LS-MOSFET from turning on prior to its immediate turn-off.

5 Theory of Operation

The TDA21220 incorporates a high performance gate driver, one high side power MOSFET and one low side power MOSFET in a single 40 lead QFN package. The advantages of this arrangement are found in the areas of increased performance, increased efficiency and lower overall package and layout inductance. This module is ideal for use in Synchronous Buck Regulators.

The power MOSFETs are optimized for 5 V gate drive enabling excellent high load and light load efficiency. The gate driver is a robust high-performance driver rated at the switching node for DC voltages ranging from -1 V to +25 V. The power density for transmitted power of this approach is approximately 40 W within a 36 mm² area.

5.1 Driver Characteristics

The gate driver of the TDA21220 has two voltage inputs, VCIN and VDRV. VCIN is the logic supply for the driver. VDRV sets the driving voltage for the high side and low side MOSFETs. The reference for the gate driver control circuit (VCIN) is CGND. To decouple the sensitive control circuitry (logic supply) from a noisy environment a ceramic capacitor must be placed between VCIN and CGND close to the pins. VDRV also needs to be decoupled using a ceramic capacitor (MLCC) between VDRV and PGND in close proximity to the pins. PGND serves as reference for the power circuitry including the driver output stage.

Referring to Figure 3 (Block Diagram), VCIN is internally connected to the UVLO (undervoltage-lockout) circuit and for VCIN voltages less than required for proper circuit operation will provide shut-down. VDRV supplies the floating high side drive – consisting of an active boot circuit - and the low-side drive circuit. A second UVLO circuitry, sensing the BOOT voltage level, is implemented to prevent false GH turn on during insufficient power supply level condition (BOOT cap charging/discharging sequence). During an undervoltage event GH and GL will both be driven low. In addition, a 500 kΩ pull-down resistor is placed from gate to source at both FETs.

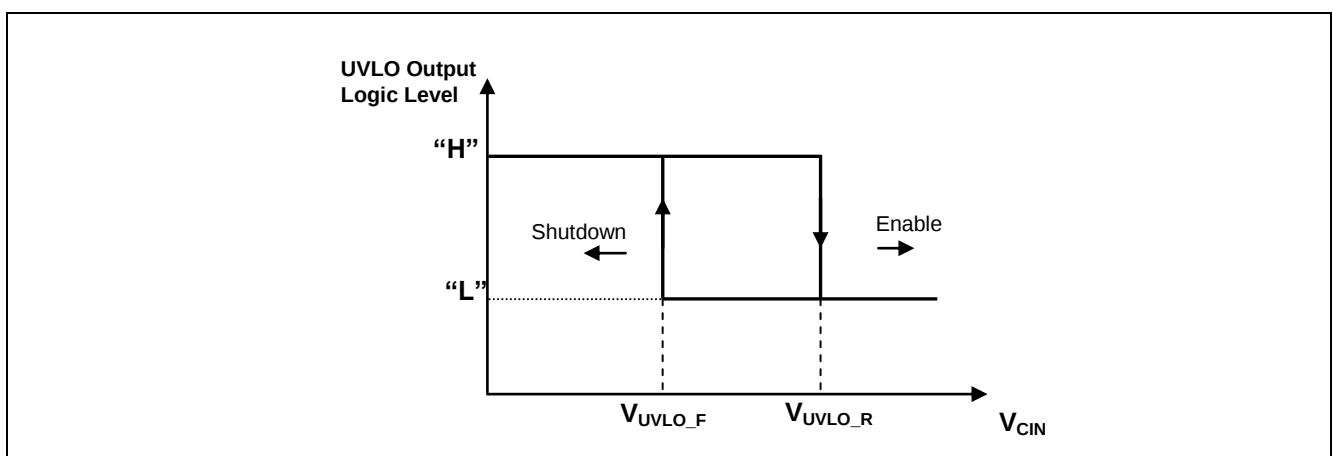


Figure 4 Internal output signal from UVLO unit

5.2 Inputs to the Internal Control Circuits

The **PWM** is the control input to the IC from an external PWM controller and is compatible with 3.3 V.

The PWM input has tri-state functionality. When the voltage remains in the specified PWM-shutdown-window for at least the PWM-shutdown-holdoff time (t_{GLtssh} , t_{GHTssh}) the operation will be suspended by keeping both MOSFET gate outputs low. Once left open, the pin is held internally at a level of $V_{PWM_O} = 1.5$ V level.

Table 13 PWM Pin Functionality

PWM logic level	Driver output
Low	GL = High, GH = Low
High	GL = Low, GH = High
Open (left floating, or high impedance)	GL = Low, GH = Low

Once a logic “high” spike has been captured the PWM logic will prolongate the logic “high” state to the minimum of $t_{on_min_PWM}$. Equivalently, once a logic “low” spike has been captured the PWM logic will prolongate the logic “low” state to the minimum of $t_{off_min_PWM}$.

Using a wide range VCIN power supply (from 4.5 V to 5.5 V) causes a shifting in the threshold voltages for the following parameters: V_{PWM_O} , V_{PWM_H} , V_{PWM_L} , V_{PWM_S} . The typical behavior of these thresholds over VCIN voltage variation is shown in the following graph:

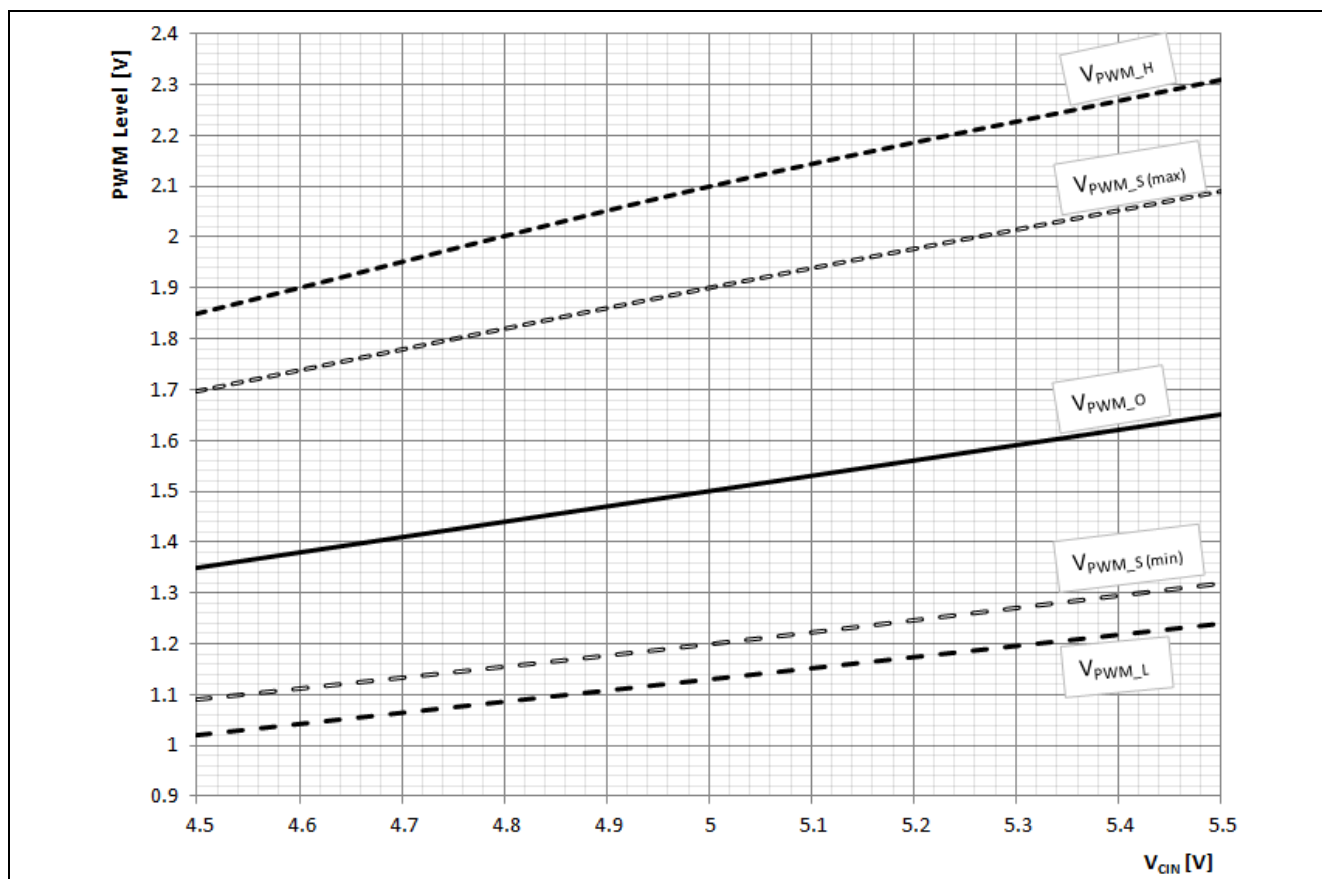


Figure 5 Variation of PWM Levels versus VCIN Logic Supply Voltage

VCIN requires a minimum dv/dt of 300V/s in the vicinity of the UVLO threshold to prevent the driver logic from emitting any gate drive glitches.

The **DISB#** is an active low signal. When pulled low, the power stage is disabled. The disable pin is being held low internally during the thermal shut down condition.

Table 14 DISB# Pin Functionality

DISB# logic level	Driver output
Low	Shutdown : GL = GH = Low
High	Enable : GL = GH = Active
Open (left floating, or high impedance)	Shutdown : GL = GH = Low

The **SMOD#** feature is provided to disable the low-side MOSFET during active operation. When synchronized with the PWM signal, **SMOD#** can be used to improve light load efficiency by saving the gate charge loss of the low-side MOSFET. Once left open, the pin is internally fixed to $V_{SMOD\#_O} = 3\text{ V}$ level.

Table 15 SMOD# Pin Functionality

SMOD# logic level	Driver output
Low	Shutdown : GL = Low, GH = PWM
High	Enable : GL = GH = Active
Open (left floating, or High impedance)	Enable : GL = GH = Active

5.3 Shoot Through Protection

The TDA21220 driver includes gate drive functionality to protect against shoot through. In order to protect the power stage from overlap, both high side and low side MOSFETs being on at the same time, the adaptive control circuitry monitors the voltage at the “VSWH” pin. When the PWM signal transitions to low, the high side MOSFET will begin to turn off after the propagation delay time t_{pdlu} . When V_{GS} of the high side MOSFET is discharged below 1 V (a threshold below which the high side MOSFET is off), a secondary delay t_{pdhl} is initiated. After that delay the low side MOSFET turns on regardless of the state of the “VSWH” pin. It ensures that the converter can sink current efficiently and the bootstrap capacitor will be refreshed appropriately during each switching cycle. See Figure 9 for more detail.

GH and GL are monitoring pins to check the internal gate drive signals.

5.4 Safe Operating Area

The maximum load current versus the temperature of the PCB (below the device) is given below:

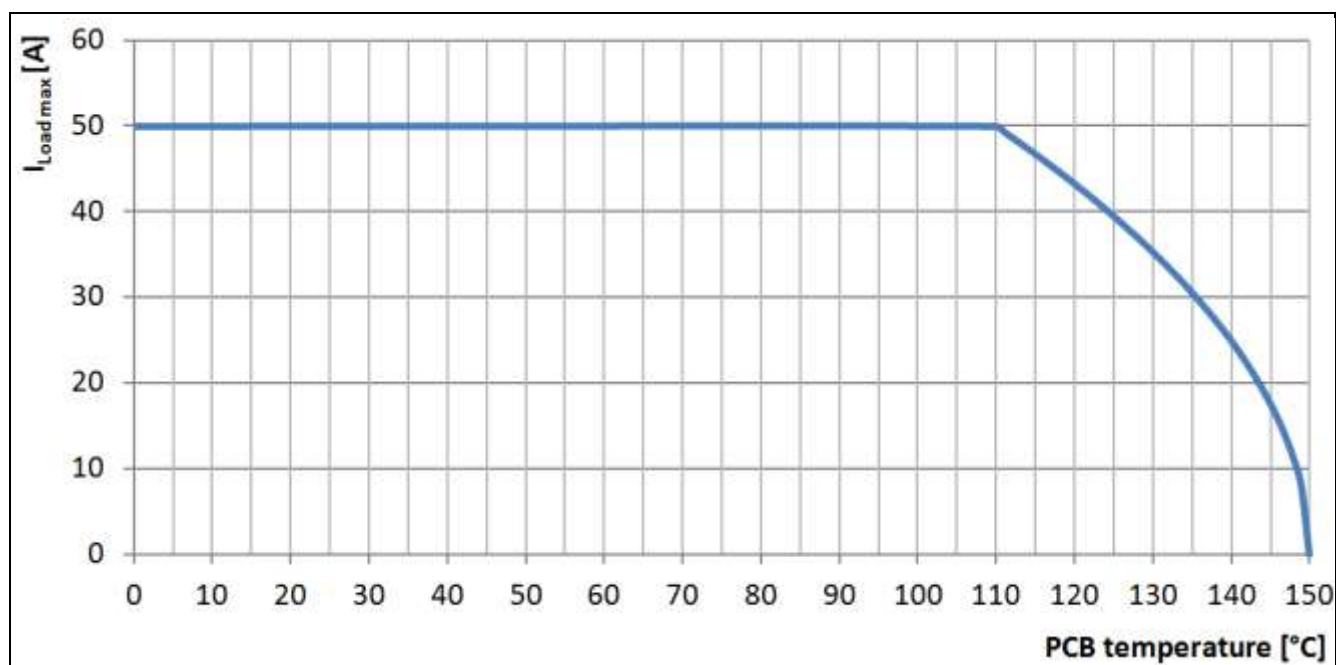


Figure 6 Safe Operating Area (Condition: $V_{IN} = 12\ V$, $V_{OUT} = 1.2\ V$, $f_{SW} = 362\ kHz$)

6 Application

6.1 Implementation

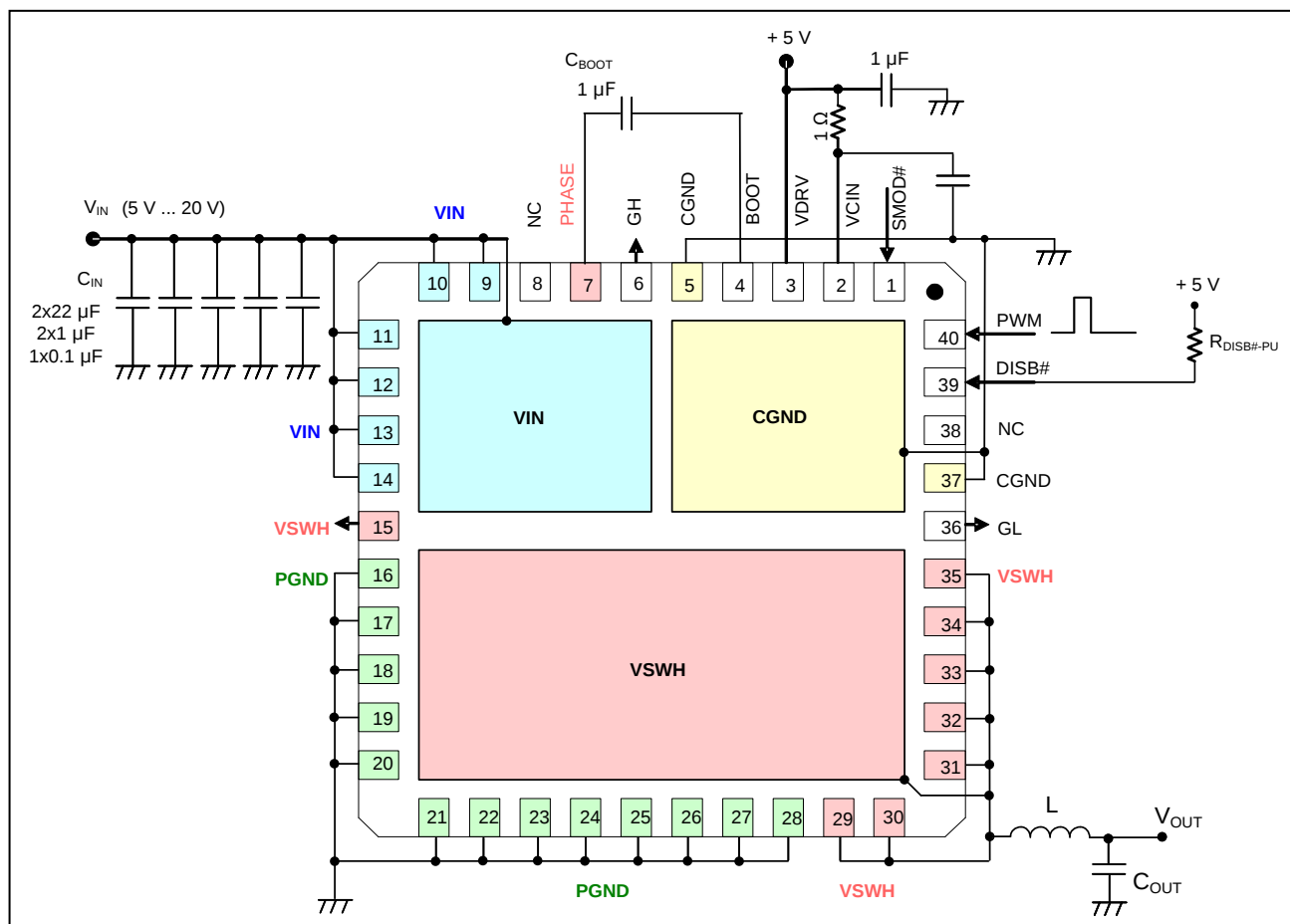


Figure 7 Pin Interconnection Outline (transparent top view)

Note:

1. Pin PHASE is internally connected to VSWH node
2. It is recommended to place a RC filter between VCIN and VDRV as shown.
3. During power-up and down sequences, the PWM signal must be either low or tri-state (open voltage), but never high, in order to avoid uncontrolled output voltage.

7 Gate Driver Timing Diagram

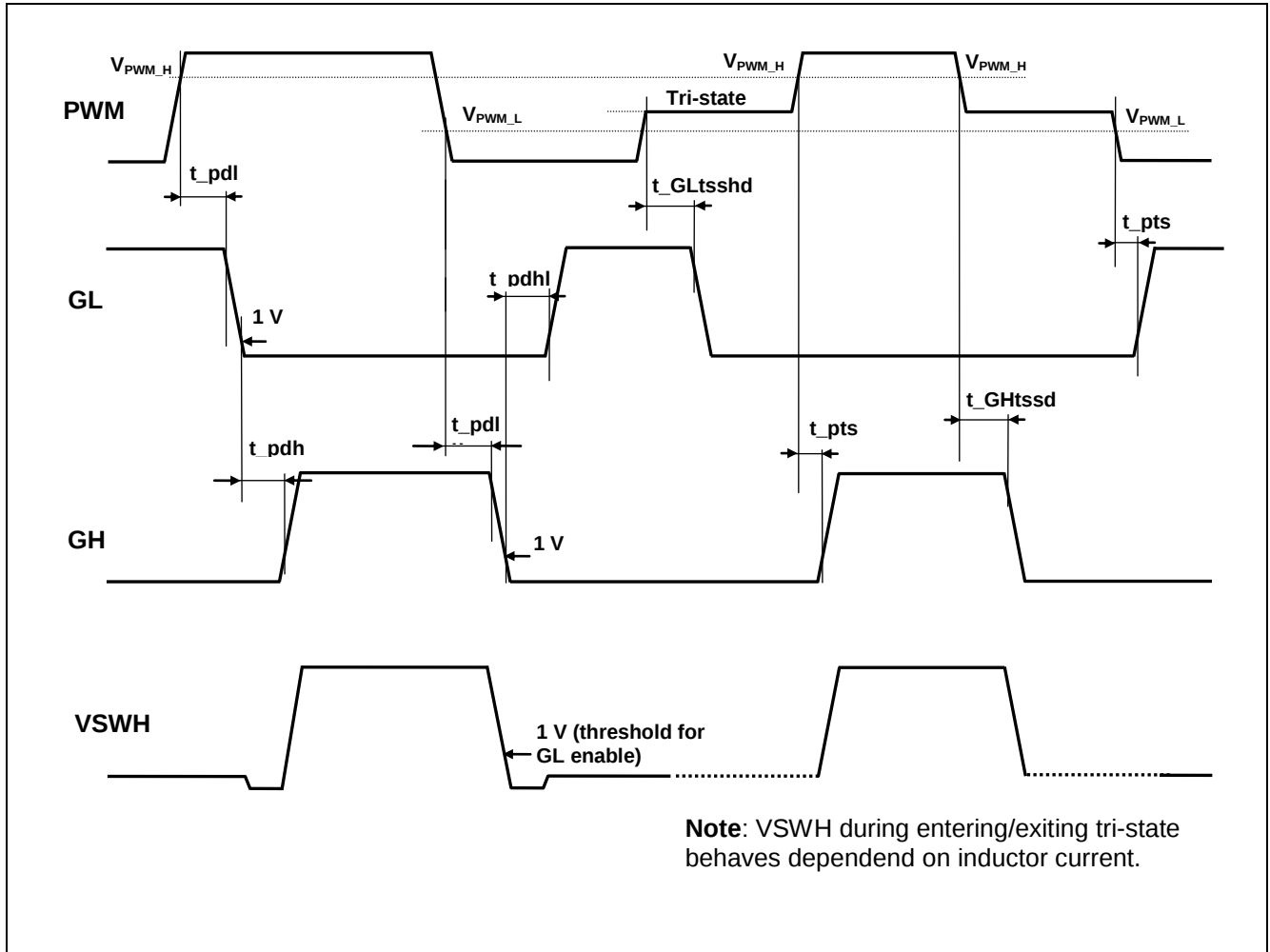


Figure 9 Adaptive Gate Driver Timing Diagram

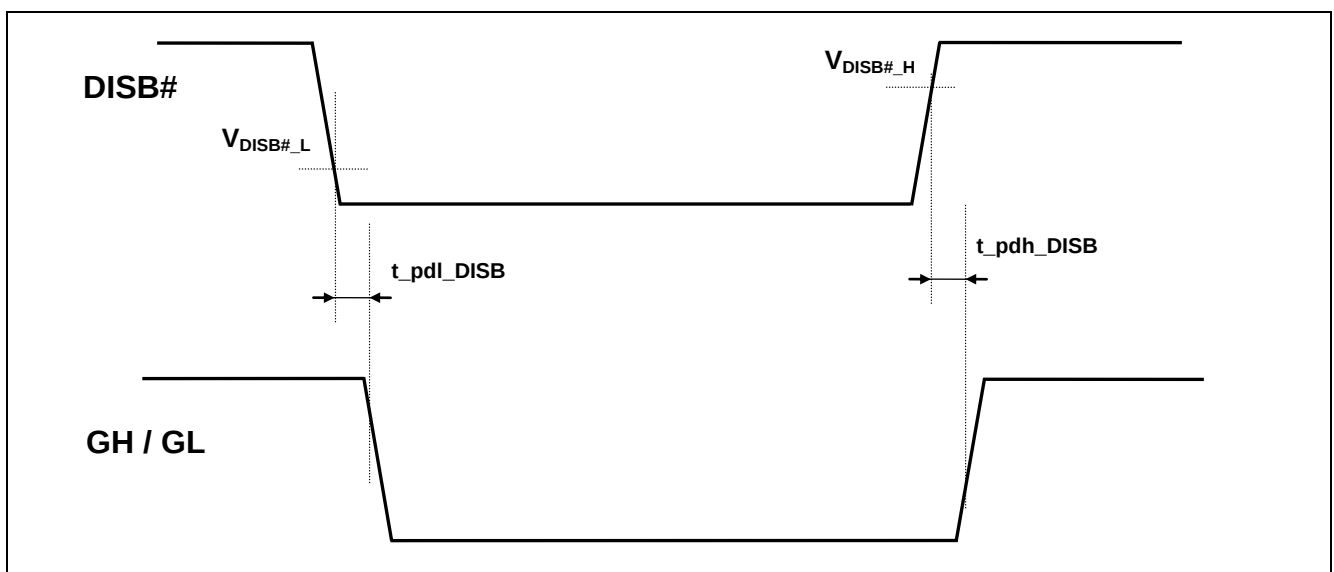


Figure 10 DISB# Timing Diagram

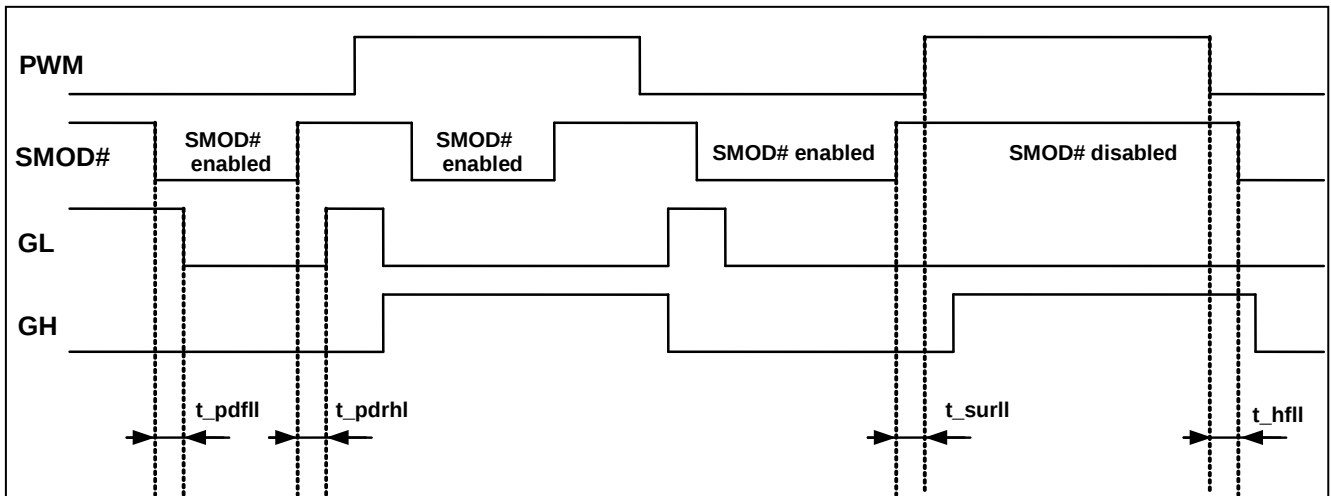


Figure 11 SMOD# Timing Diagram

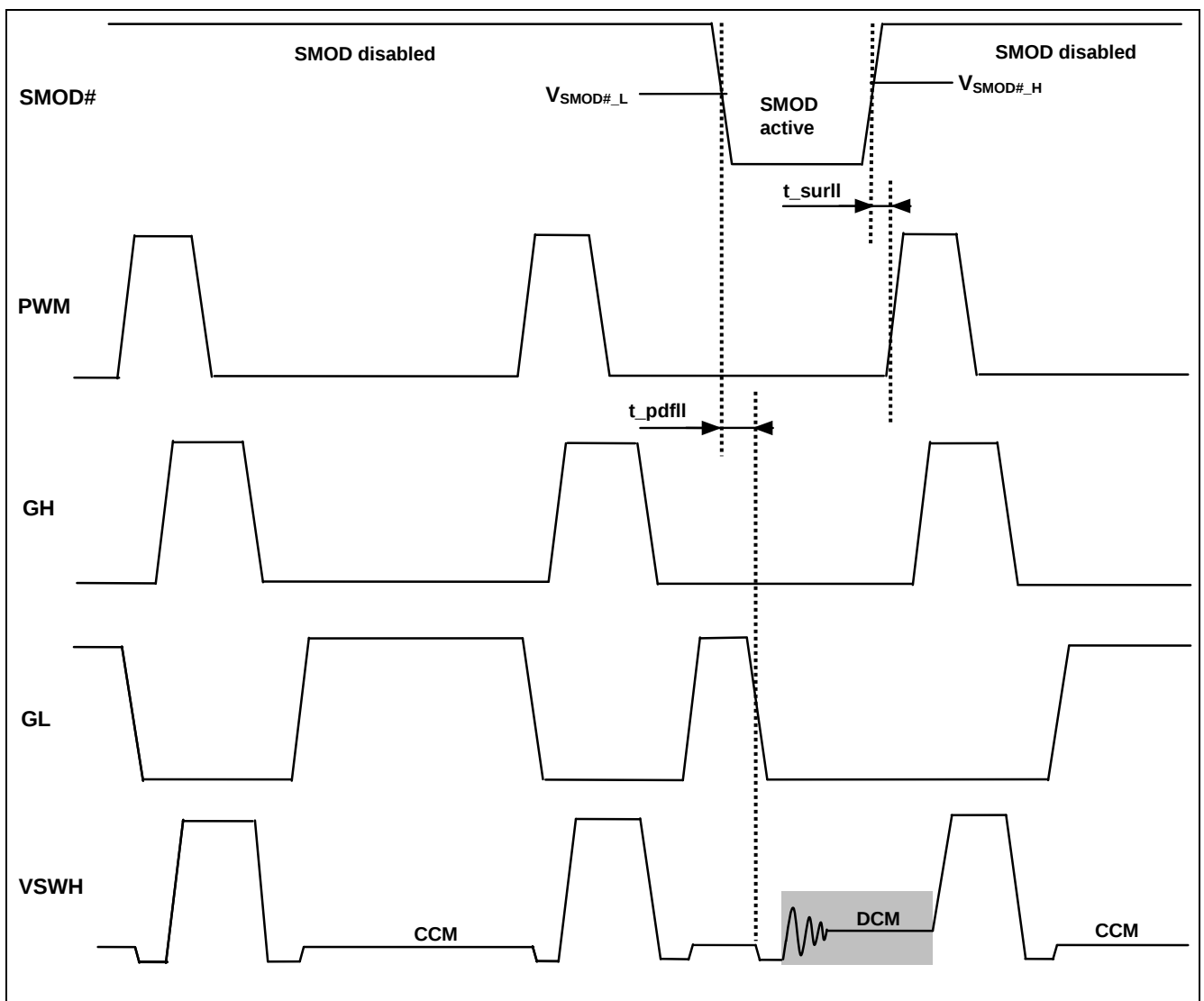


Figure 12 SMOD# Timing Diagram

8 Performance Curves – Typical Data

8.1 Efficiency and Power Loss versus VOUT

Operating conditions (unless otherwise specified): $V_{IN} = +12\text{ V}$, $V_{CIN} = V_{DRV} = +5\text{ V}$, $V_{OUT} = 0.8\text{ V to } 1.6\text{ V}$, $f_{SW} = 362\text{ kHz}$, 210 nH inductor (Cooper-FPI1108, $DCR(\text{typ.}) = 0.29\text{ m}\Omega$) $T_A = 25\text{ }^\circ\text{C}$, load line = $0\text{ m}\Omega$, airflow = 100 LFM , no heatsink. Efficiency and power loss reported herein include only TDA21220 losses. Data are taken after thermal equilibrium ($\sim 10\text{ min}$ for each current step) with unit in temperature chamber.

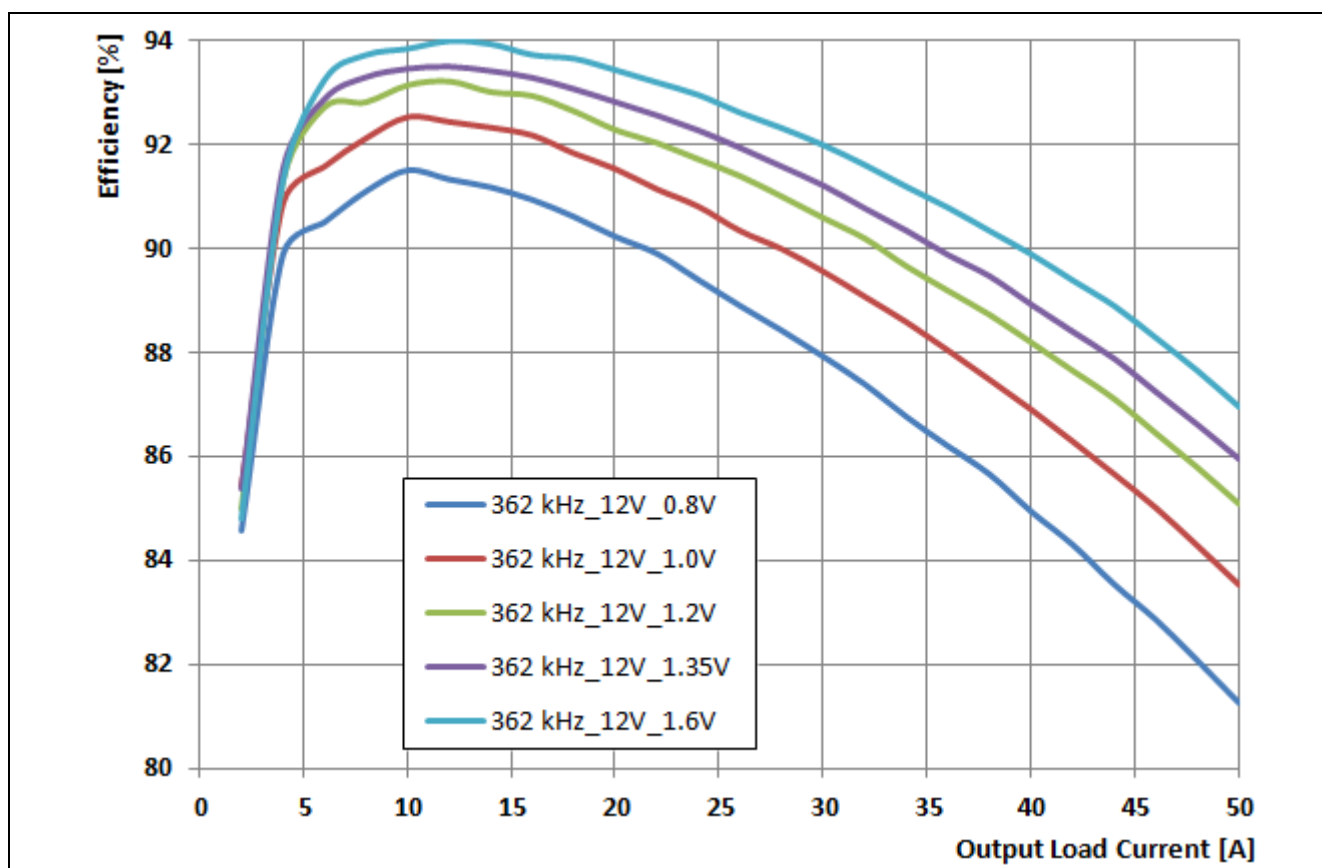


Figure 13 Efficiency vs. output current , VOUT as parameter

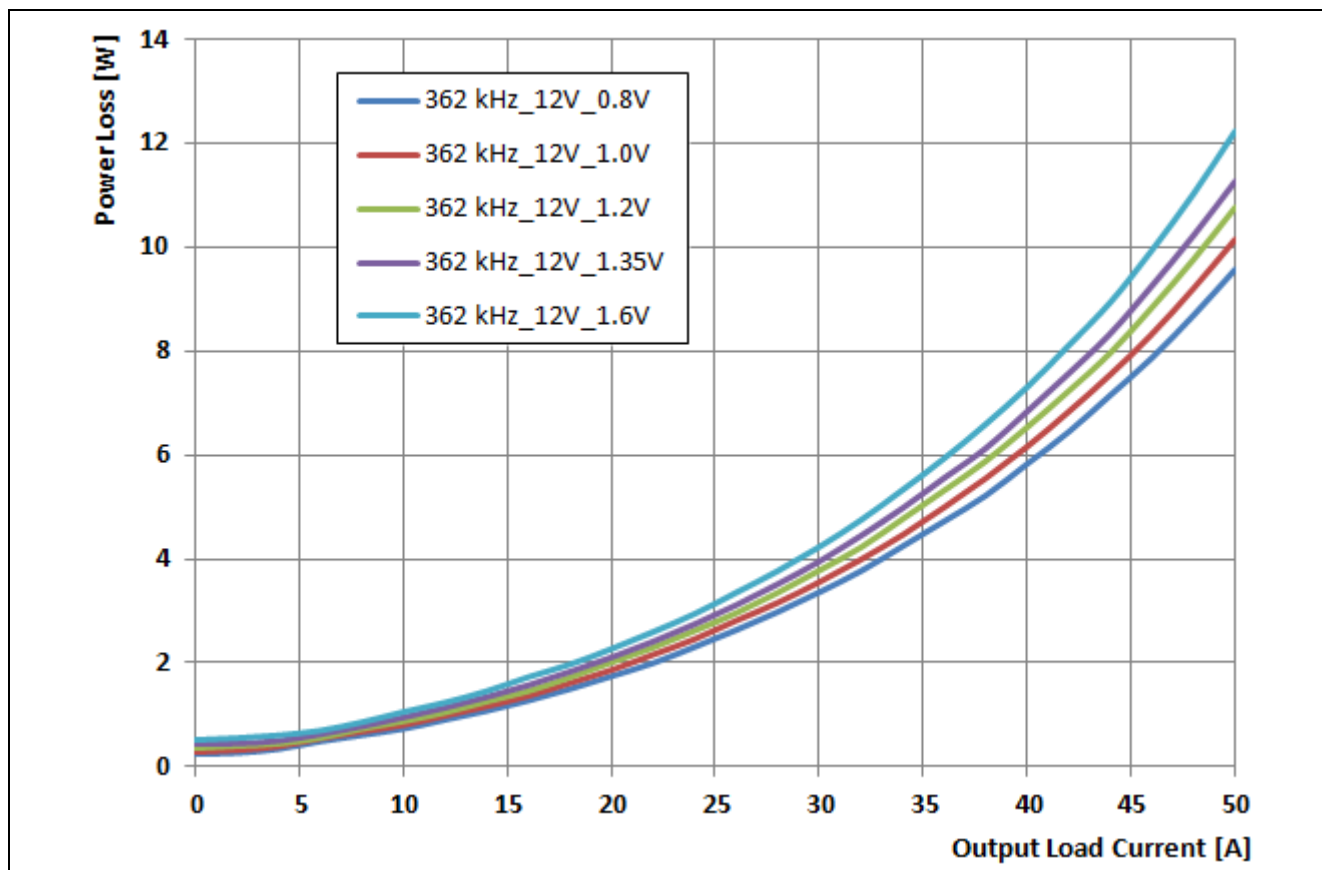


Figure 14 Power loss vs. output current , VOUT as parameter

8.2 Efficiency and Power Loss versus VIN

Operating conditions (unless otherwise specified): VIN = +10/12/14 V, VCIN = VDRV = +5 V, VOUT = 1.2 V, f_{SW} = 362 kHz, 210 nH inductor (Cooper-FPI1108, DCR (typ) = 0.29 mΩ) T_A = 25 °C, load line = 0 mΩ, airflow = 100 LFM, no heatsink. Efficiency and power loss reported herein include only TDA21220 losses. Data are taken after thermal equilibrium (~ 10 min for each current step) with unit in temperature chamber.

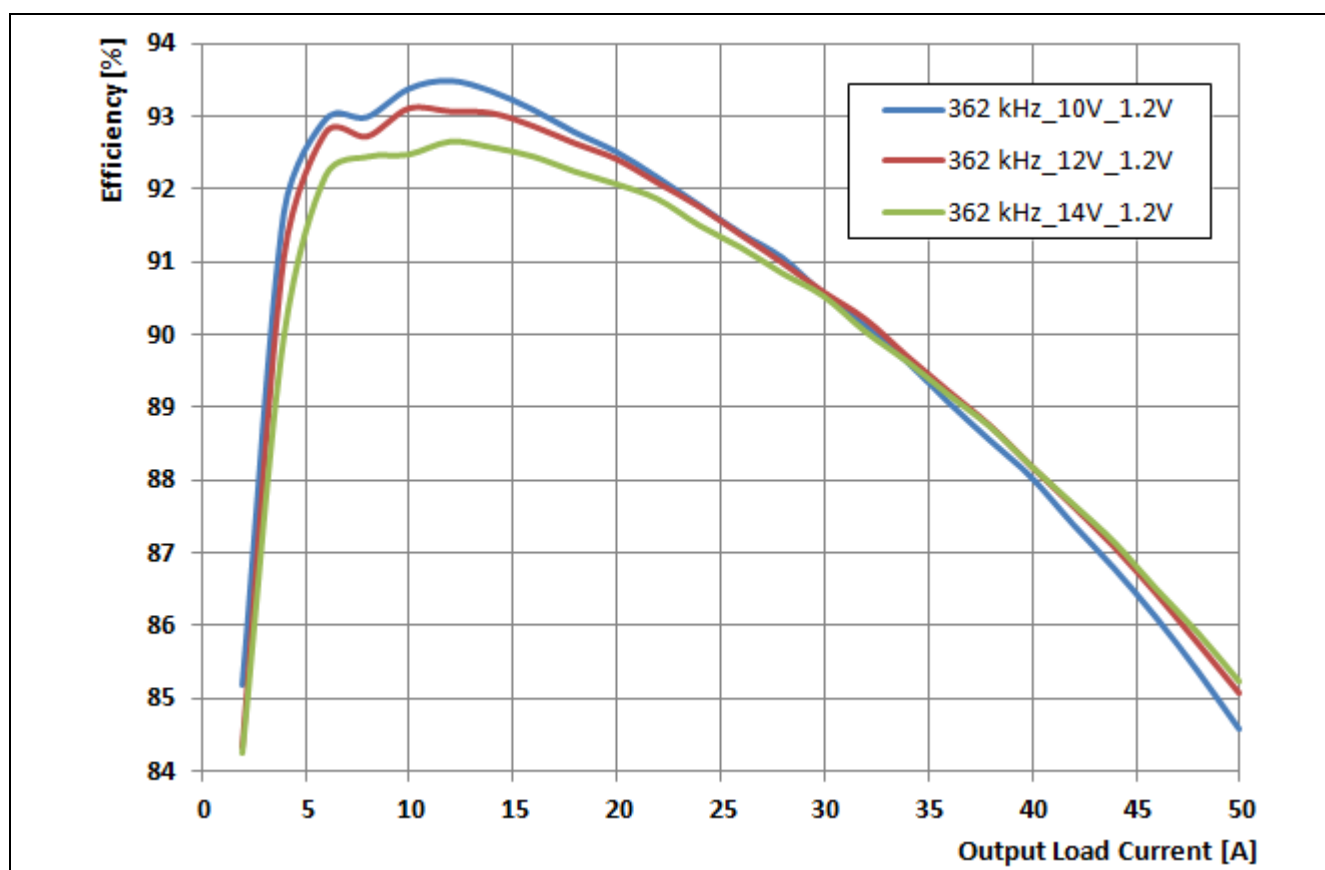


Figure 15 Efficiency vs. output current , VIN as parameter

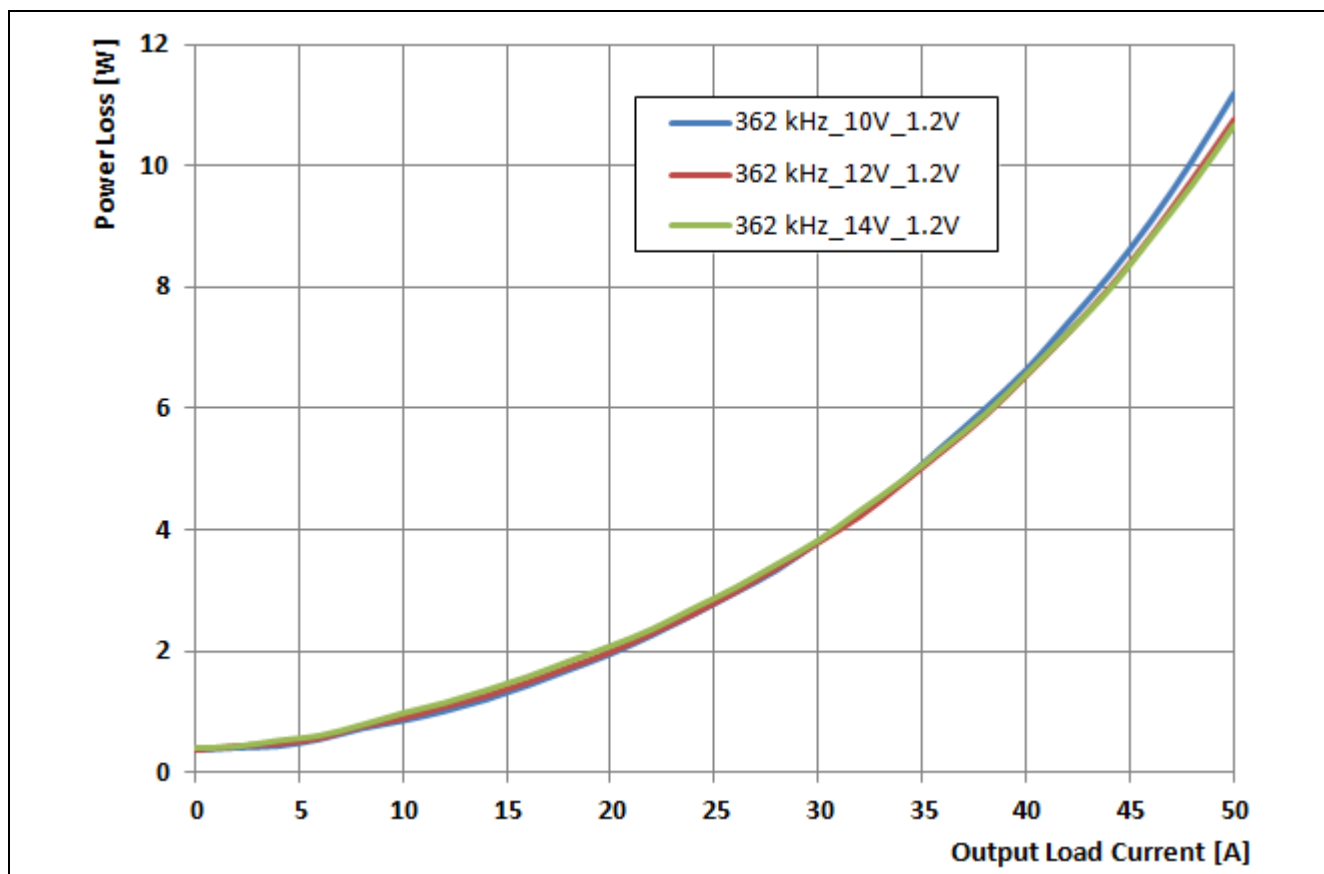


Figure 16 Power loss vs. output current with VIN as parameter

8.3 Efficiency and Power Loss versus Switching Frequency

Operating conditions (unless otherwise specified): $V_{IN} = +12\text{ V}$, $V_{CIN} = V_{DRV} = +5\text{ V}$, $V_{OUT} = 1.2\text{ V}$, $f_{SW} = 296\text{ kHz}$ to $f_{SW} = 592\text{ kHz}$, 210 nH inductor (Cooper-FPI1108, DCR (typ) $= 0.29\text{ m}\Omega$) $T_A = 25\text{ }^\circ\text{C}$, load line $= 0\text{ m}\Omega$, airflow $= 100\text{ LFM}$, no heatsink. Efficiency and power loss reported herein include only TDA21220 losses. Data are taken after thermal equilibrium ($\sim 10\text{ min}$ for each current step) with unit in temperature chamber.

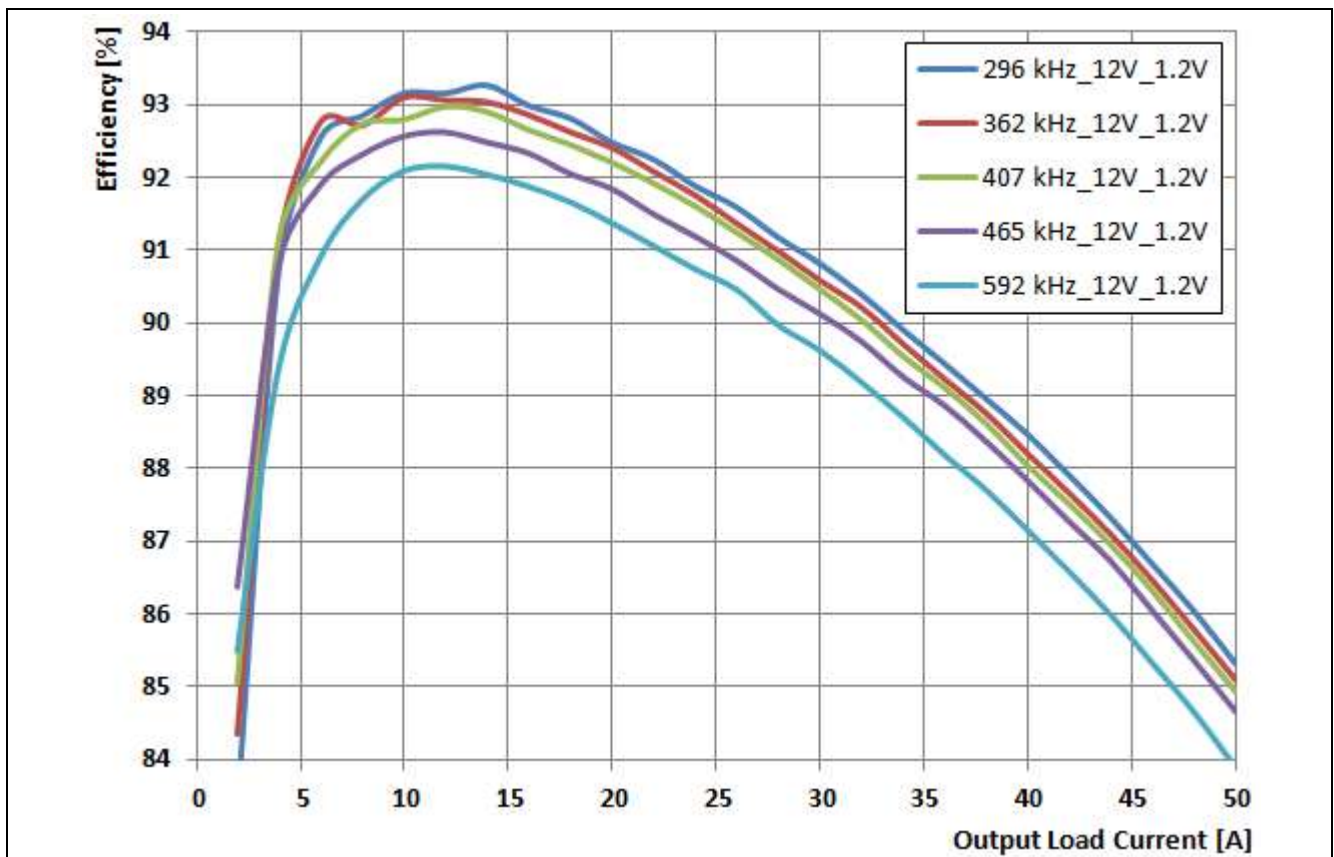


Figure 17 Efficiency vs. output current, switching frequency as parameter

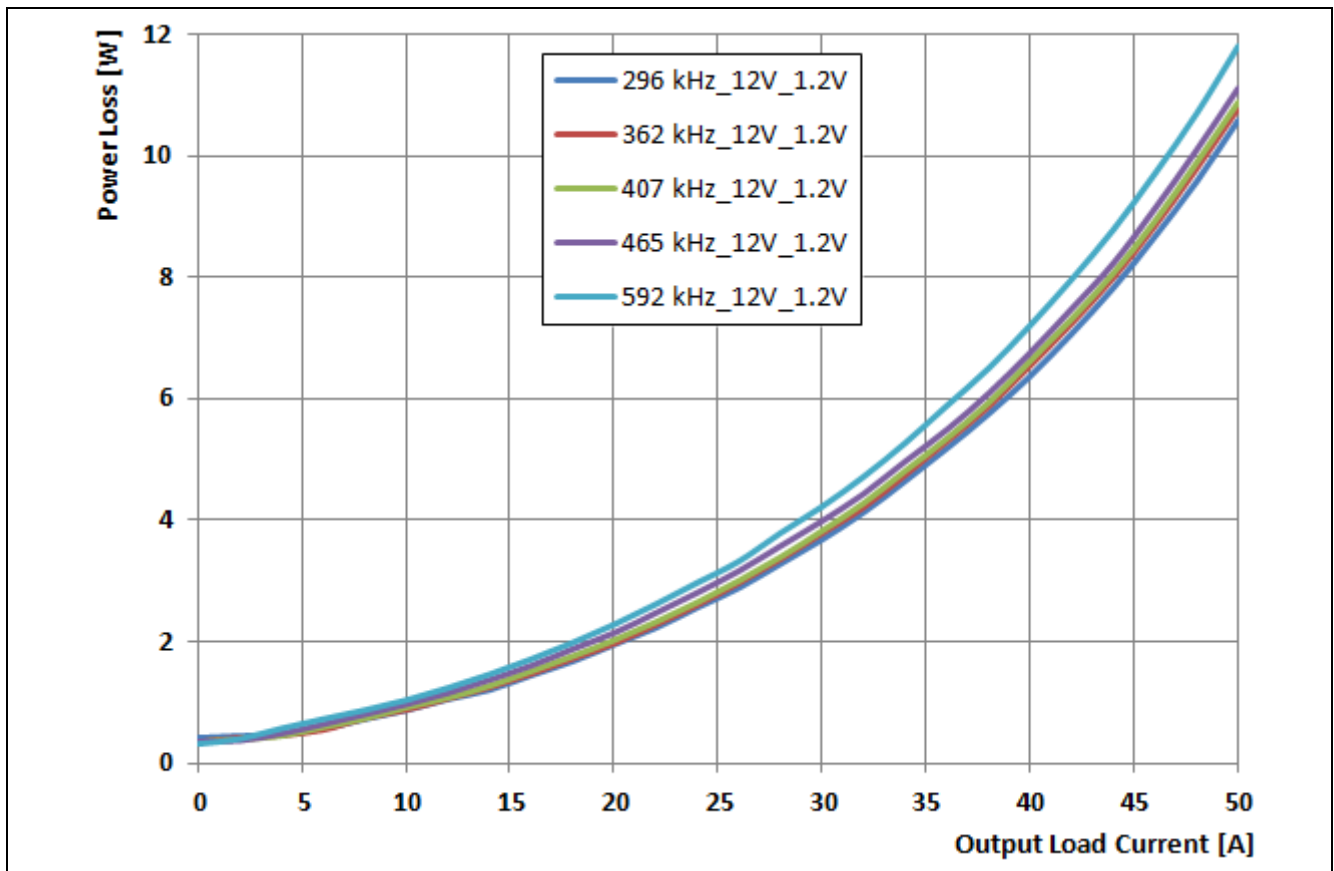


Figure 18 Power loss vs. output current, switching frequency as parameter

8.4 Driver Current versus Switching Frequency

Operating conditions (unless otherwise specified): $V_{IN} = +12\text{ V}$, $V_{CIN} = V_{DRV} = +5\text{ V}$, $V_{OUT} = 1.2\text{ V}$, from $f_{SW} = 296\text{ kHz}$ to $f_{SW} = 592\text{ kHz}$, 210 nH inductor (Cooper-FPI1108, $DCR(\text{typ}) = 0.29\text{ m}\Omega$) $T_A = 25\text{ }^\circ\text{C}$, load line = $0\text{ m}\Omega$, airflow = 100 LFM , no heatsink. Efficiency and power loss reported herein includes only TDA21220 losses. Data are taken after thermal equilibrium ($\sim 10\text{ min}$ for each current step) with unit in temperature chamber.

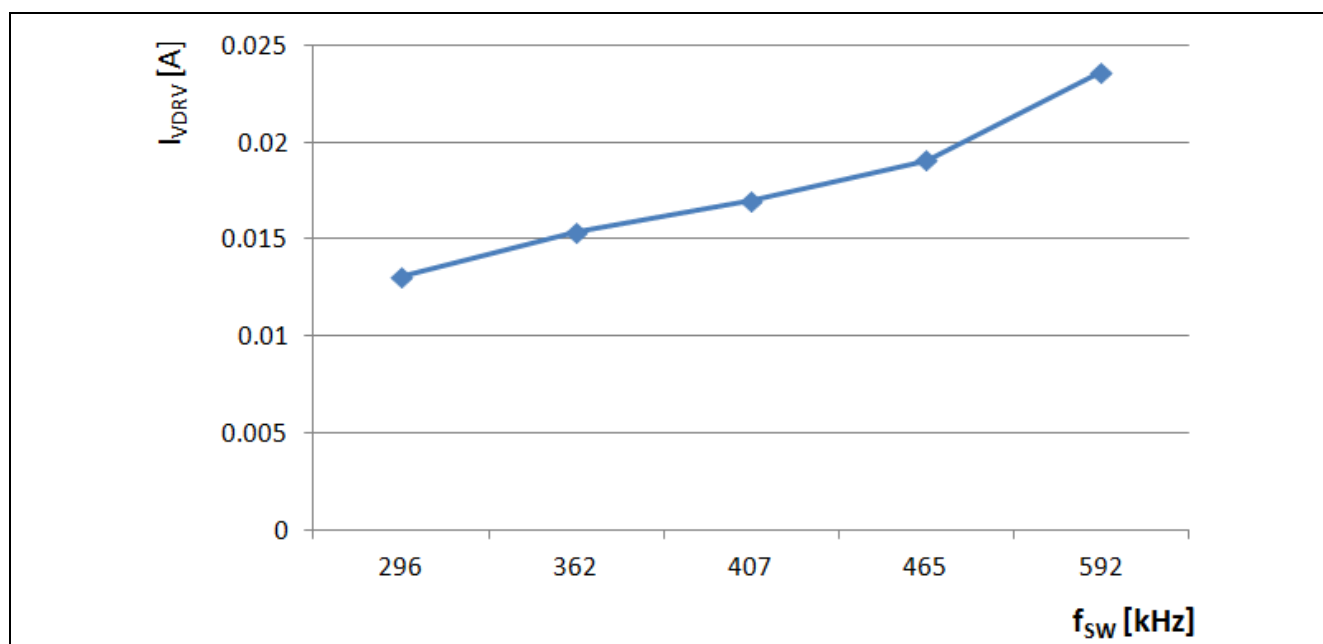
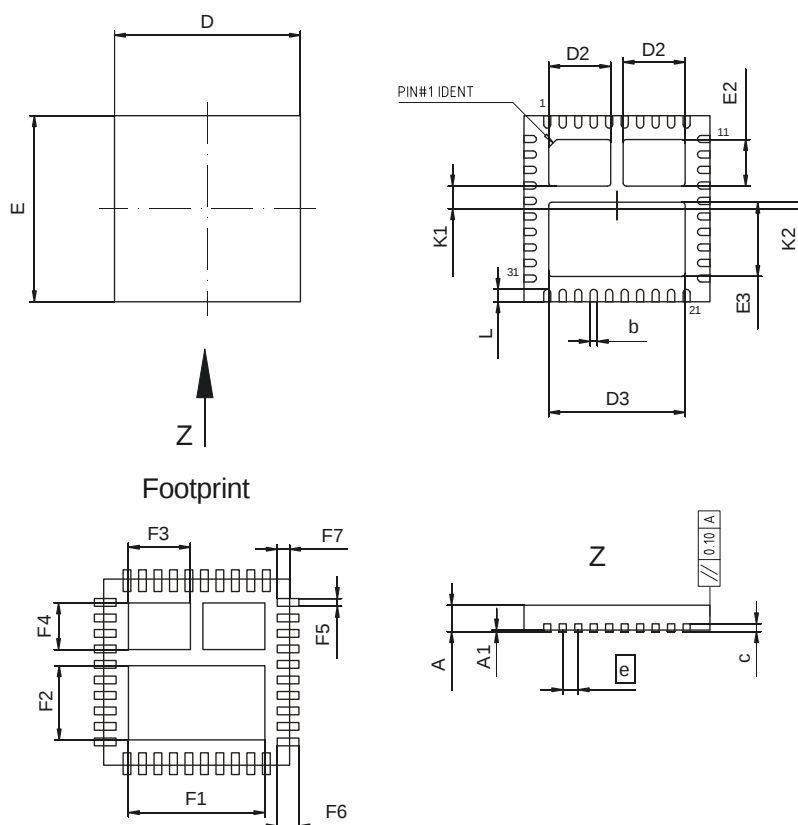


Figure 19 Driver current vs. switching frequency

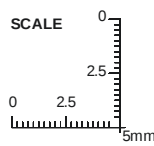
9 Mechanical Drawing



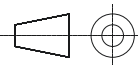
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.75	0.85	0.030	0.033
A1	0.00	0.05	0.000	0.002
b	0.18	0.28	0.007	0.011
c	0.10	0.30	0.004	0.012
D	5.90	6.10	0.232	0.240
D2	1.90	2.10	0.075	0.083
D3	4.30	4.50	0.169	0.177
E	5.90	6.10	0.232	0.240
E2	1.40	1.60	0.055	0.063
E3	2.30	2.50	0.091	0.098
e	0.50		0.020	
N	40		40	
L	0.30	0.50	0.012	0.020
K1	0.63	0.83	0.025	0.033
K2	0.11	0.31	0.004	0.012
F1	4.40		0.173	
F2	2.40		0.094	
F3	2.00		0.079	
F4	1.50		0.059	
F5	0.25		0.010	
F6	0.70		0.028	
F7	0.40		0.016	

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Figure 20 Mechanical Dimensions

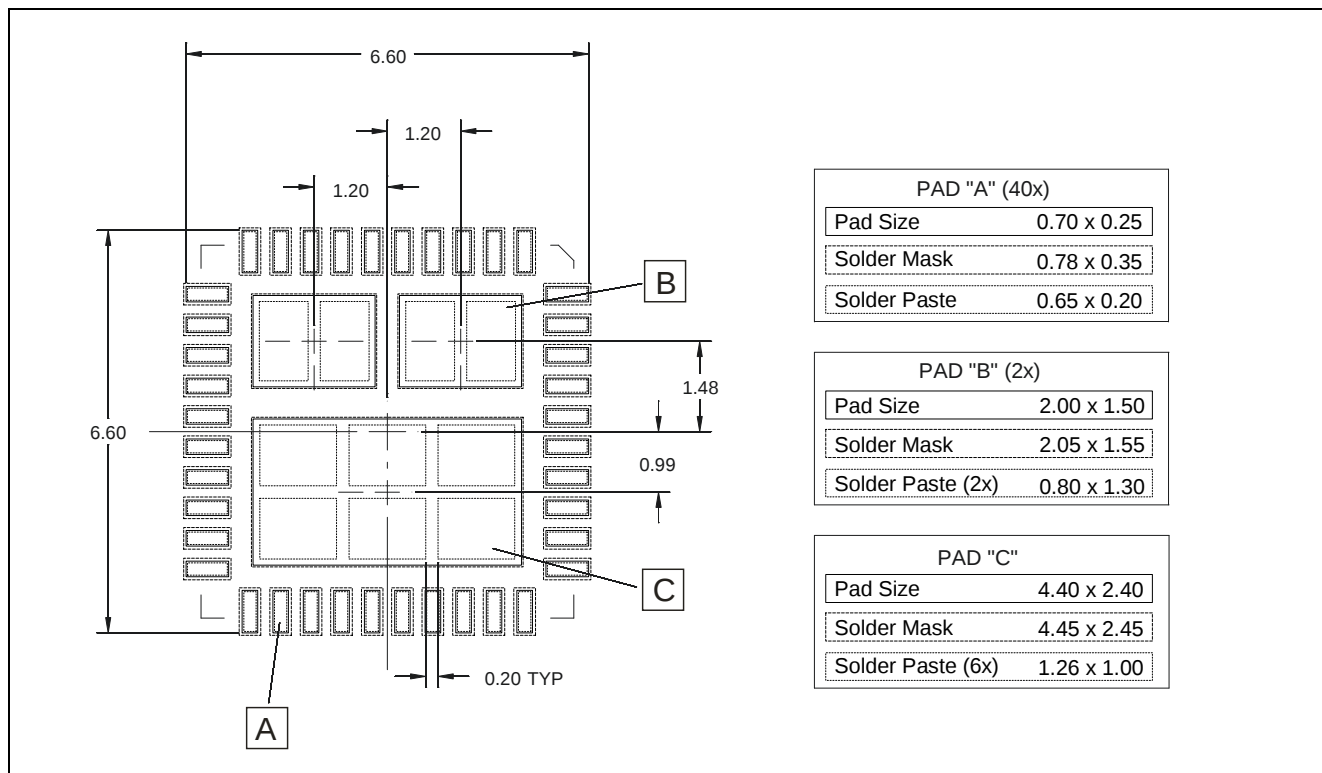


Figure 21 Footprint and solder stencil recommendations

Attention: The recommended stencil height is 120 µm.

Assembly recommendations can be found in this document:

"Recommendations for Printed Circuit Board Assembly of Infineon PG-IQFN Packages"

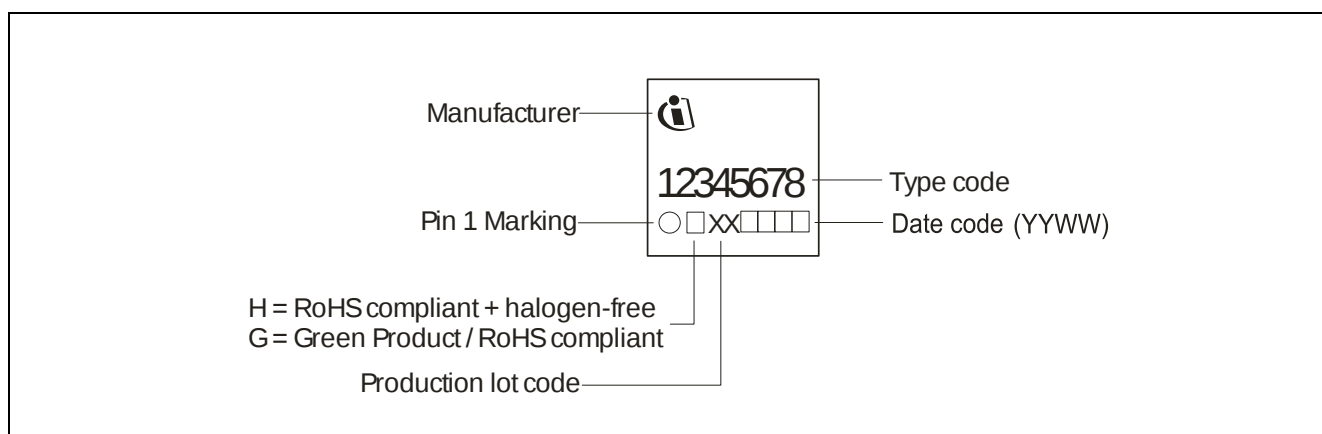


Figure 22 Marking definition

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