TC1796

32-Bit Single-Chip Microcontroller

Microcontrollers

Never stop thinking

Edition 2007-04

**Published by Infineon Technologies AG,
81726 München, Germany**

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TC1796 Documentation Addendum

Revision History: V1.2 2007-04

Previous Version: V1.1

Page	Subjects (major changes since last revision)
6	The register long name for MMU_CON is corrected.
7	The register long names for D11 to D15 are corrected.
8	The desription for CRC generation and error checking is improved; typos corrected for EICR0.REN0, EICR0.REN1, EICR1.REN2 and EICR1; typo of bit description GEEN1 corrected.
10	Figure 6-12 is corrected.
12	“CSRAM” is corrected into “SPRAM”.
13, 14	The bit name and access type is corrected for bit 5 of PCP_ES register; the instruction field definition of Table 11-12 is updated. Figure 11-14 is updated;
15	The typo in the syntax description of the ST.PI instruction of the PCP is corrected.
16	The typo in Figure 12-5 is corrected.
17	The description for Channel Reset Operation is improved.
18	The typo in Transaction Lost Interrupt section is corrected.
19	The typo in Move Engine Interrupt section is corrected.
21	Read and write access modes of MSC register are corrected.
22	MMUCON short register name is corrected.
23	Typo in Slave Select Output Control and the description for Slave Select Register Update section are corrected.
24	A new note is added for SSOC and SSOTC registers; a new footnote is added to SSOTC.LEAD, SSOTC.TRAIL and SSOTC.INACT bit description; â note paragraph at register SSOTC is updated;
25	A new paragraph is added to Receive FIFO section.
26	A new sentence is added to Transmit FIFO section; the description when LEC=111_B is improved; the CAN Bus State Information is updated in Table 22-8;
27, 28	MLI receive clock max. frequency is corrected.
32	The formula for the timer period is corrected.

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Table of Contents

1 Introduction

This document describes corrections, changes, and improvements for the two parts of the TC1796 User's Manual V1.0 2005-06, the System Units book (Volume 1) and the Peripheral Units book (Volume 2). These corrections will be considered with the next update of these User's Manual documents.

The referenced documents to this addendum are located at the Internet page:

- **www.infineon.com/audo-ng**
- TC1796 System Units User's Manual (Vol.1), V1.0, June 2005
- TC1796 Peripheral Units User's Manual (Vol.2), V1.0, June 2005

2 User's Manual - System Units Part (Volume 1)

This section describes corrections for the System Units part of the User's Manual.

Page 1-11

In the second bullet paragraph of section "Interrupt System" the number "256" must be corrected to "25**5**".

Page 1-20

The first "Dash" paragraph under the third bullet paragraph under "Features" must be changed into:

Baud rate: f_{MSC} divided by **4**, 8, 16, 32, 64, 128, or 256

Page 1-34

In the logic symbol of Figure 1-11, the 12 lines of Port 6 have no secondary functions for MSC0 and MSC1. The text right of the bracket in the drawing must be corrected into: "ASC0 / ASC1 / SSC1 / CAN".

Page 1-52

The pad driver class of pin $\overline{\text{HDRST}}$ is "A2" instead of "A1".

Page 1-56

The following section has to be added after section 1.4.2 at the bottom of page 1-55 (top of a new page 1-56):

1.4.3 Pull-Up/Pull-Down Behavior of the Pins

Table 2-1 List of Pull-Up/Pull-Down Reset Behavior of the Pins

Pins	$\overline{\text{PORST}}$ = 0	$\overline{\text{PORST}}$ = 1
$\overline{\text{NMI}}$, $\overline{\text{TDI}}$, TMS, $\overline{\text{TESTMODE}}$, BFCLKO	High-impedance (tri-state)	
$\overline{\text{HDRST}}$, BRKOUT, $\overline{\text{BRKIN}}$, BYPASS, all GPIOs, EBU except BFCLKO: $\overline{\text{BFCLKI}}$, $\overline{\text{RD}}$, RD/$\overline{\text{WR}}$, $\overline{\text{ADV}}$, $\overline{\text{BC}}$[3:0], MR/$\overline{\text{W}}$, $\overline{\text{WAIT}}$, $\overline{\text{BAA}}$, $\overline{\text{HOLD}}$, $\overline{\text{HLDA}}$, $\overline{\text{BREQ}}$, D[31:0], A[23,0], $\overline{\text{CS}}$[3:0], $\overline{\text{CSCOMB}}$	Weak pull-up device active	
$\overline{\text{PORST}}$	Weak pull-down device active	
TSTRES	High-impedance	Weak pull-up device active
$\overline{\text{TRST}}$, TCK		Weak pull-down device active
SLSO0, SLSO1, MTSR0, MRST0, SCLK0, SLSI0, TDO	Weak pull-up device active	High-impedance
-	Weak pull-down device active	

Page 2-12

The long register name of register MMU_CON must be changed into "MMU **Configuration** Register".

Page 2-14

The bit description of bit CPU_SRCn.TOS is wrong. For TOS = 1, the description must be changed from "Reserved" into "Service Provider = PCP".

Page 2-16

In Table 2-4, the register long name for D11, D12, D13, D14 and D15 must be changed to "Data Register 1**1**, Data Register 1**2**, Data Register 1**3**, Data Register 1**4** and Data Register 1**5**.

Page 2-22

The offset address for register CMP1 must be corrected in Table 2-6 from 2200_H into 2280_H.

Page 2-34

The access type for bit fields "DCSZ" and "DMEMSZ" in register DMI_CON must be changed in the register image and in the register description table from "rh" into "r".

Page 3-18

Section 3.2.2.5: Point 3) of the actions should be executed after point 5) and not after point 2).

Page 4-9

Section "4.2.6 Special Case: Tuning Protection Reset" must be completely deleted.

Page 4-23

This page with section "Timing Parameters" must be completely deleted.

Page 4-28

The paragraph below 4.4.3 must be replaced by the following paragraph:

Except **for** different connections to serial port lines of ASC0, the bootstrap loader mode 3 is identical with bootstrap loader mode **1**. The serial data input of the ASC0 is connected to RXD0B which **is** an alternate function of P6.8/RXDCAN0 and the serial data output of the ASC0 is connected to TXD0B which **is** an alternate function of P6.9/TXDCAN0.

Page 4-29

The first sentence of the note at the top of the page must be extended by "For CRC generation and error checking, the BootROM software uses the TC1796 on-chip memory checker module with an initial value of FFFF $FFFF_H$ for the memory checker result register before the checksum is generated."

Page 5-17

The bit description of case "1" for EICR0.REN0 must be replaced by " The detection of a **rising edge** of IN0 generates a trigger event (INTF0 becomes set)."

Page 5-19

The bit description of case "1" for EICR0.REN1 must be replaced by " The detection of a **rising edge** of IN1 generates a trigger event (INTF1 becomes set)."

Page 5-20

The bit description of case "1" for EICR1.REN2 must be replaced by " The detection of a **rising edge** of IN2 generates a trigger event (INTF2 becomes set)."

Page 5-21

The bit description of case "1" for EICR1.REN3 must be replaced by " The detection of a **rising edge** of IN3 generates a trigger event (INTF3 becomes set)."

Page 5-27

The first sentence of the bit description of GEEN1 must be replaced by "Bit **GEEN1** enables the generation of a trigger event for output channel 1 when the result of the pattern detection changes.".

Page 5-49

The first sentence on the top "In the TC1796, ..." must be replaced by the following sentence: "In the TC1796, the input line**s** IN1 of the **GPTA0,** GPTA1**, and LTCA2** module**s** can be used to measure the baud rate of an ASC0 or ASC1 receiver input signal." Additionally, Figure 5-11 must be corrected.

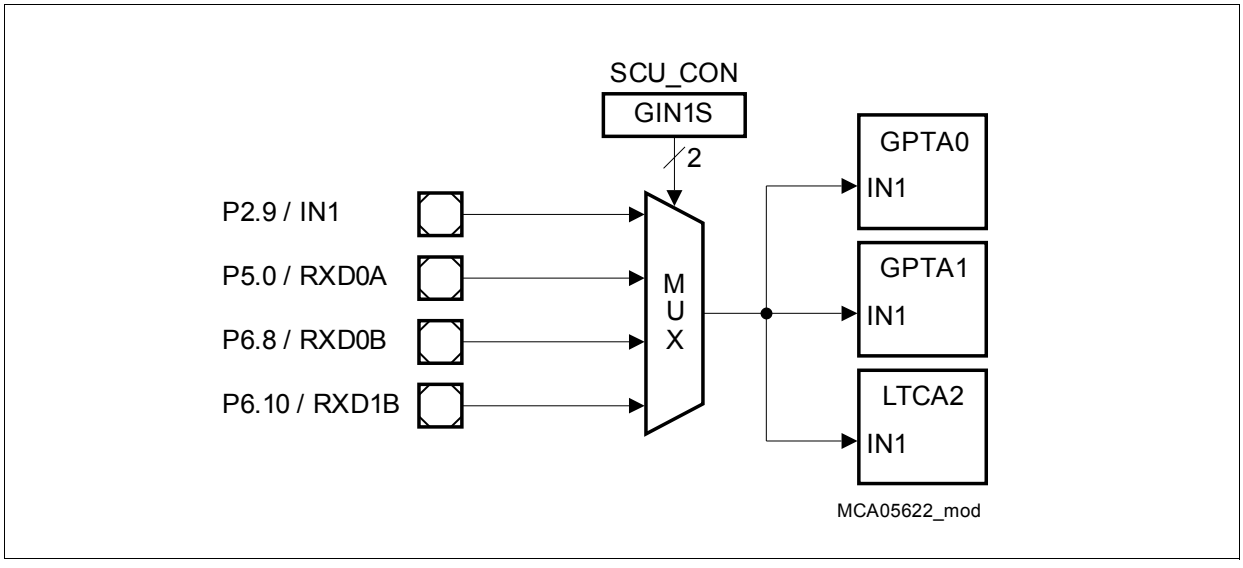

Figure 5-11 GPTA0/GPTA1/LTCA2 Input IN1 Control

Page 5-59

The bit description of ENON on the bottom of page 5-95 must be corrected into:
"1 Setting of EMSF by hardware is **enabled**."

Page 5-65

The sentence "This bit is set with any reset." in the description of bit PARAV must be changed into "This bit is set after a power-on reset".

Page 6-4

Figure 6-2 must be replaced with the below figure:

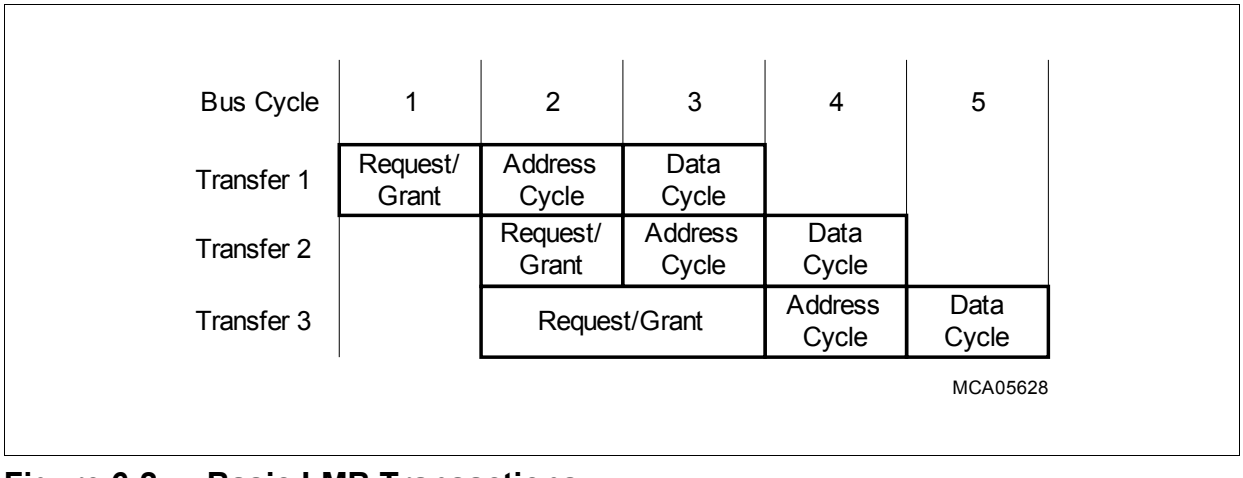

Figure 6-2 Basic LMB Transactions

Page 6-6

In the second bullet paragraph from the top, the register short name for the LMB Error Data Registers in brackets should be replaced with "**LEDATL/LEDATH**".

Page 6-8

In the bit description of bit LEC, the text "When writing a 0 to LEC" must be replaced by "When writing a **1** to LEC".

Page 6-13

In the register image, the access mode below bit 12 (SRE) must be changed into "rw".

Page 6-19

The second sentence of the first paragraph of Section 6.4.3 should be replaced with: "The requesting FPI Bus master releases the FPI Bus for one cycle after the FPI Bus transaction request, in order to allow the **FPI** Bus slave to indicate if it is ready to handle the requested **FPI** Bus transaction."

Page 6-20

Figure 6-7 must be replaced with the below figure:

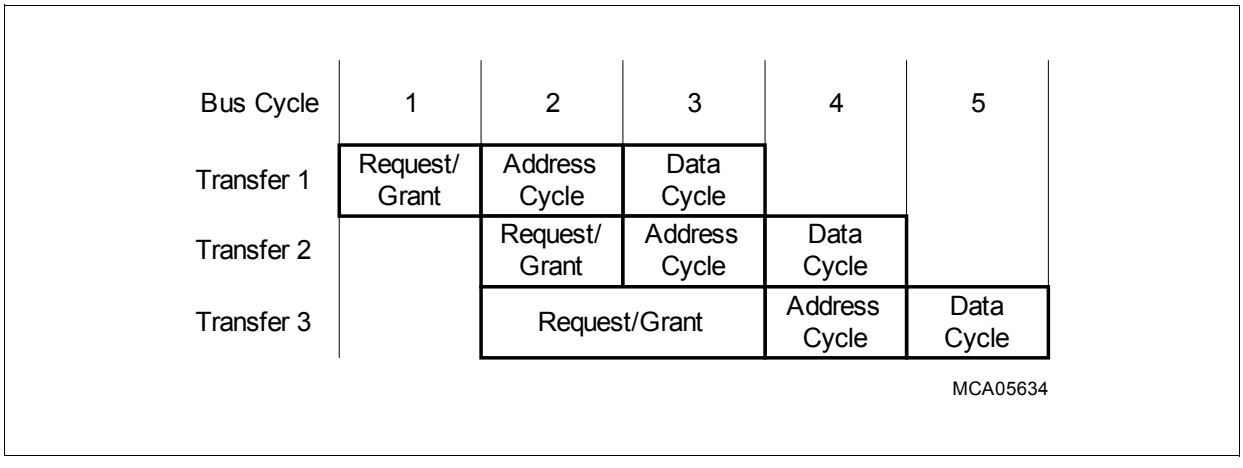

Figure 6-7 Basic FPI Bus Transactions

Page 6-28

Figure 6-12 must be replaced with the below figure:

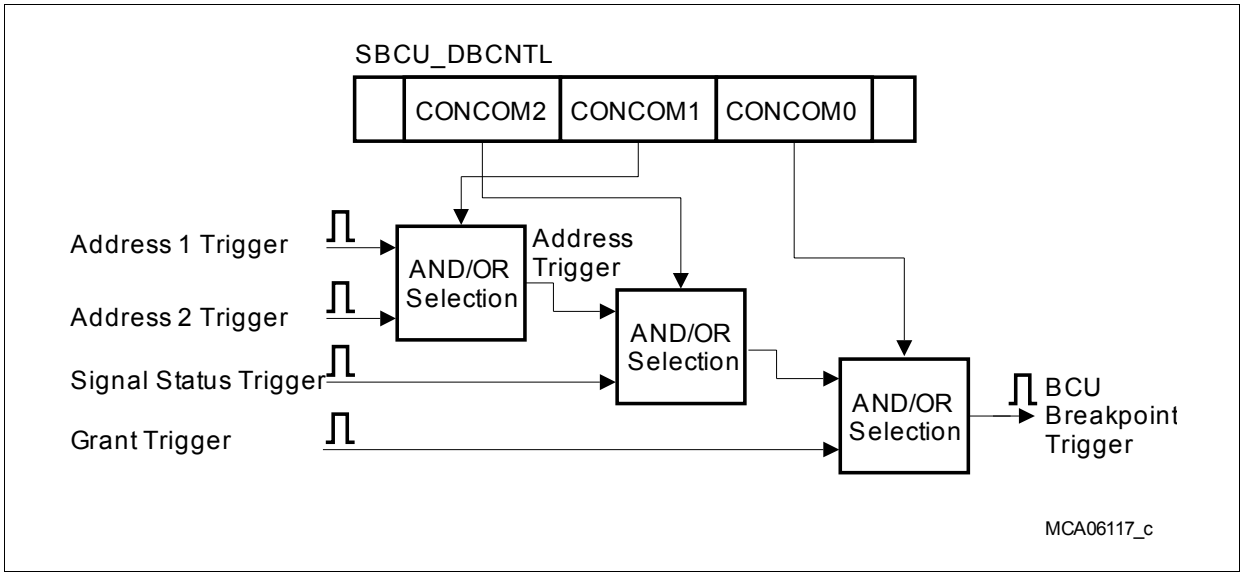

Figure 6-12 Basic FPI Bus Transactions

Page 7-16

Table 7-7 must be exchanged by the following table (see corrections in red):

Table 7-7 Load Page Buffer Command

Cycle No.	PFLASH		DFLASH		
	Address	**Data**	**Bank**	**Address**	**Data**
32-Bit Load Page Buffer Command					
Cycle 1	A000 **55F0**$_H$	32-bit data	DB0	AFE0 **55F0**$_H$	32-bit data
			DB1	AFE1 **55F0**$_H$	
Cycle 2	A000 **55F4**$_H$	32-bit data	DB0	AFE0 **55F4**$_H$	32-bit data
			DB1	AFE1 **55F4**$_H$	
64-Bit Load Page Buffer Command					
Cycle 1	A000 **55F0**$_H$	64-bit data	DB0	AFE0 **55F0**$_H$	64-bit data
			DB1	AFE1 **55F0**$_H$	

Page 7-41

The first paragraph of column "Description" for bit FABUSY should be changed as follows:
"This status flag is a flag for test purposes that should not be used by software drivers. It indicates whether any of the Flash arrays is in busy state. FABUSY is cleared by any reset operation."

Page 7-49 to 7-51

The following footnote [1] must be added to the following FCON bits and bit fields: WSPFLASH, WSECPF, WSWLHIT, WSDFLASH, and WSECDF:

[1] These bits and bit fields can be changed at any time, also with code fetched from Program Flash. A modified wait state parameter will be taken into account with the next corresponding access.

Page 8-3

The word "PCP" in the second paragraph "Note that ..." must be deleted.

Page 9-5

In the description of section "Segment 14" the word "CSRAM" at the end of the first parapraph must be corrected into "**SP**RAM".

Page 9-7

Column "Description" of Table 9-2, last but one row: the content should be corrected into "**D**MU stand-by data memory (SBRAM)".+

Page 9-9

Column "Description"of Table 9-2: the word "CSRAM" must be corrected into "SPRAM".

Page 10-9

Port 4 has the same behavior as all other GPIO ports concerning input pull devices. Therefore, the sentence "Port 4 has a different PCx coding ...." in the first paragraph on the top of the page must be deleted. Also Table 10-4 must be completely deleted.

Page 10-16

The following sentence must be added at the end of paragraph "Port 0 is a general-purpose 16-bit ... software afterwards.":

"Note that some of the P0.[7:0] lines are used for configuration purposes, too (see **Page 10-23**)."

Page 10-23

Section 10.3.3.3 must be changed as described below:

10.3.3.3 Reserved Port 0 Pins

Depending on the TC1796 device version used in an application, several Port 0 lines (meaning several SWOPT bits) are reserved and cannot be used for user system

purposes during a HDRST reset operation. **Table 10-9** defines the reserved Port 0 lines (indicated by 0 or 1) as well as the Port 0 lines that can be used by a user program (indicated by "user") for software configuration selection (or as GPIO pins) depending on the specific TC1796 device version.

Table 10-9 Reserved Port 0 Lines of TC1796 Devices

TC1796 Device Versions	SWOPTx Bits (x = 0-15)					
	P0. [15:8]	**P0. [7:6]**	**P0.5**	**P0.4**	**P0.3**	**P0. [2:0]**
TC1796	user	user	user	1	user	1)
TC1796ED (Emulation device)		user	0 or 1 2)	1		
TC1796-L (Flash-Not-Available version)		user	11B 3)	0		
TC1796ED in TC1796-L socket		11_B 3)	0 or 1 2)	0		

1) The P0.[2:0] bits are only used in alternate boot modes (see **Page 4-28**). If alternate boot modes are not required or used in an application, P0.[2:0] can also be used for user program software configuration selection purposes during a hardware reset operation or as GPIO pins.

2) 0: Emulation device functionality is not available.
1: Emulation device functionality is fully supported.

3) In Flash-Not-Available devices/sockets with P0.4 = 0, P0.[7:6] are used for test purposes and must always be set to 11_B during a hardware reset operation.

Page 10-49

The table footnote 1) must be completely deleted. See also the corrections on page 10-9 and page 24-228.

Page 11-58

Bit 5 in the register image of register PCP_ES must be changed into 0,r (instead of ME,rh).

Page 11-59

Column "Description " for bit 5 must be corrected into: "Reserved; read as 0."

Page 11-73

The second row (RC0) of **Table 11-12** must be replaced by the following row:

CNT0		**Counter Reload Value (COPY)** The COPY instruction uses an implicit counter to generate multiple data transfers. The CNT0 value given in the instruction specifies how many data transfers are to be performed by the instruction. See also **Figure 11-13** on **Page 11-76**.
	CNT0 = $001_B..111_B$	Perform 1..7 data transfers
	CNT0 = 000_B	Perform 8 data transfers
		Block Size (BCOPY) Selects the FPI block size used for a BCOPY instruction.
	CNT0 = 000_B	Use block size of 8 words.
	CNT0 = 010_B	Use block size of 2 words.
	CNT0 = 011_B	Use block size of 4 words.
	Others	Reserved

Page 11-77

Figure 11-14 must be replaced by the following figure (block "DATA Transfer" has been changed):

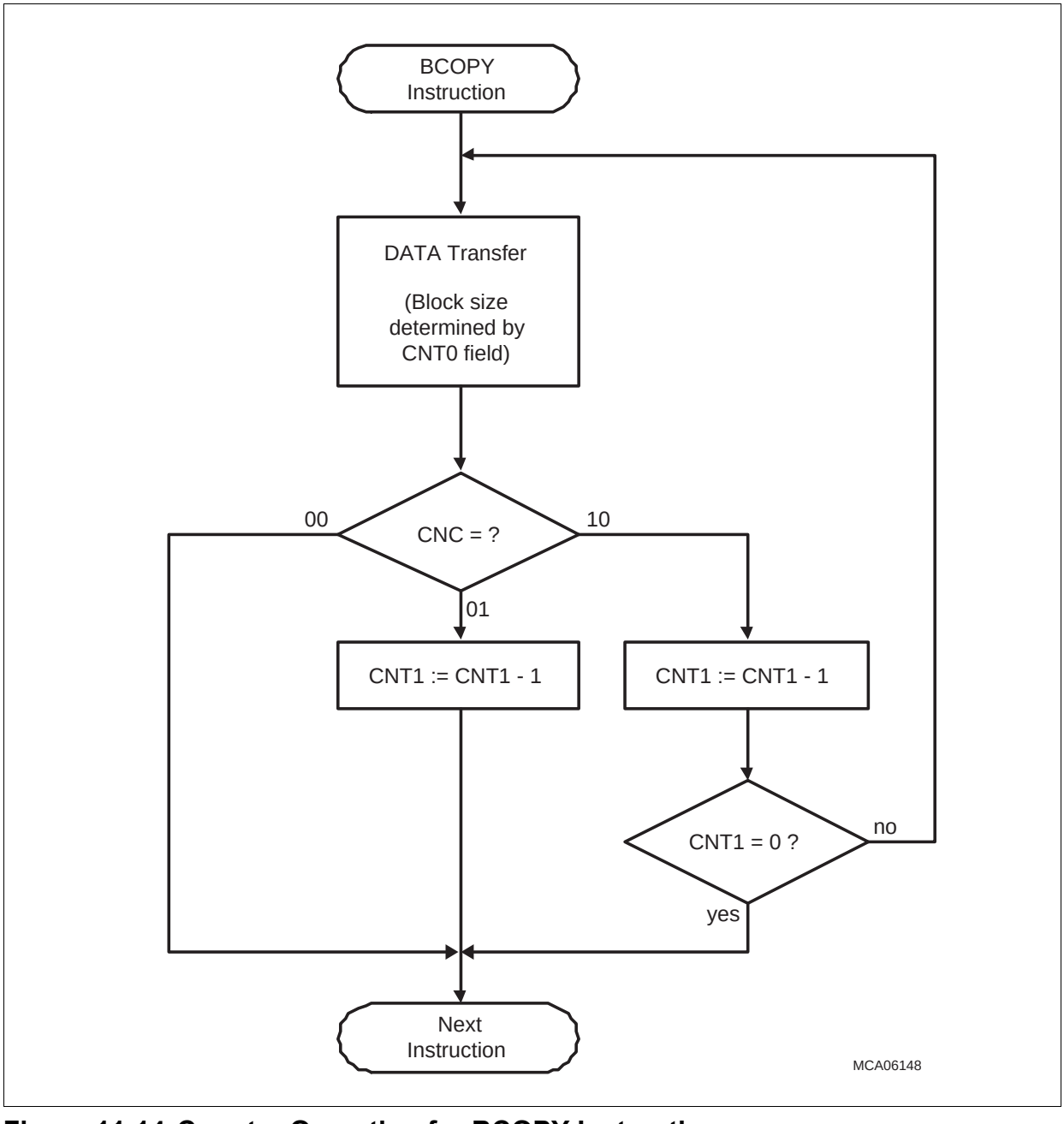

Figure 11-14 Counter Operation for BCOPY Instruction

Page 11-98

In the syntax description of the ST.PI instruction of the PCP, the register name "Ra" must be replaced by "**Rb**".

Page 12-9

The wordings "SHADR0n with CHCR0n.SHCT = 01_B" on the left of the first waveform from the bottom of Figure 12-5 must be replaced with "SHADR0n with ADRCR0n.SHCT = 01_B".

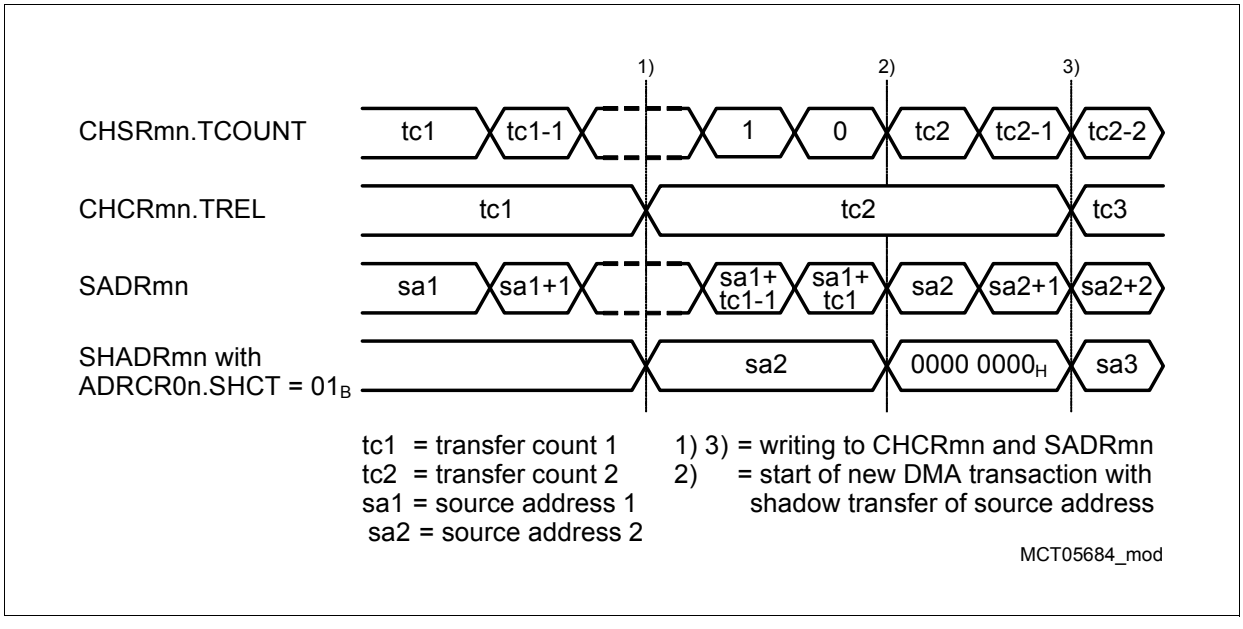

Figure 12-5 Channel Request Control

Page 12-10

Figure 12-6 must be updated caused by the changes on pages 12-34 and 12-49.

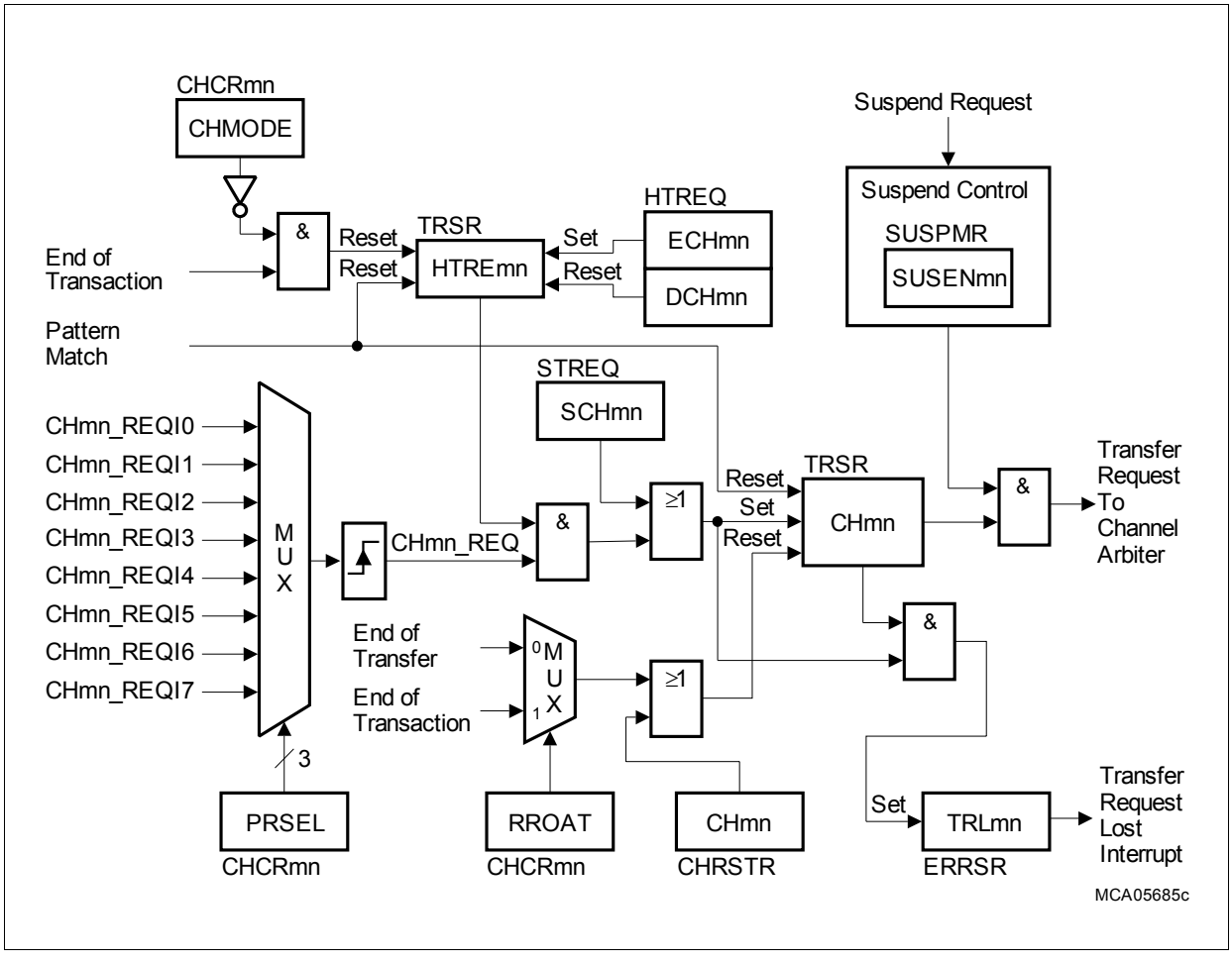

Figure 12-6 Channel Request Control

The last sentence of the second last paragraph should be replaced with: "A software request can be generated by setting bit STREQ.**S**CH0n."

Page 12-16

The paragraphs below "When CHRST.CH0n is set to 1:" must be replaced by the following paragraphs:

- Bits TRSR.HTREmn, TRSR.CHmn, ERRSR.TRLmn, INTSR.ICHmn, INTSR.IPMmn, WRPSR.WRPDmn, WRPSR.WRPSmn, CHSRmn.LXO, and bit field CHSRmn.TCOUNT are reset.
- Source and destination address register will be set to the wrap boundary. SHADRmn will be cleared.
- All automatic functions are stopped for channel mn.

A user program must execute the following steps for resetting a DMA channel:

1. If hardware requests are enabled for the DMA channel mn, disable the DMA channel mn hardware requests by setting HTREQ.ECHmn = 0.

2. Writing a 1 to CHRST.CHmn.
3. Waiting (polling) until CHRST.CHmn = 0.

A user program should execute the following steps for restarting a DMA channel after it was reset:

1. Optionally (re-)configuring the address and other channel registers.
2. Restarting the DMA channel mn by setting HTREQ.ECHmn = 1 for hardware requests or STREQ.SCHmn = 1 for software requests.

The value of CHCRmn.TREL is copied to CHSRmn.TCOUNT when a new DMA transaction is requested and shadow address register contents is not equal 00000000_H.

Page 12-29

In Section 12.1.8.2, the register name EERSR must be replaced by ERRSR in the third sentence of the first paragraph, first sentence of the second paragraph and within Figure 11-18. The corresponding text must be replaced by :
"If such a transaction request lost condition occurs, bit E**R**RSR.TRLmn is set." and "A transaction request lost condition of DMA channel mn is indicated by status flag E**R**RSR.TRLmn, which can be reset by setting bit CLRE.CTLmn or CHRSTR.CHmn."

Figure 12-18 must be replaced by:

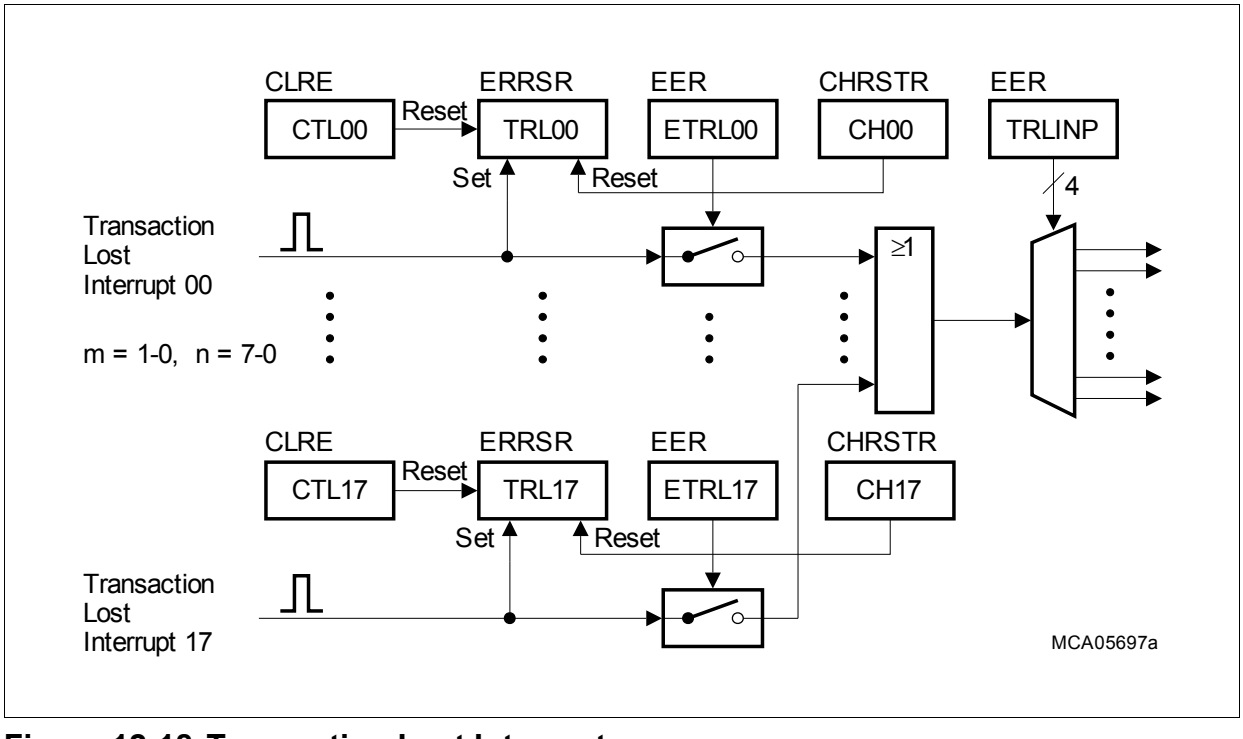

Figure 12-18 Transaction Lost Interrupt

Page 12-30

In Section 12.1.8.3, the register name EERSR must be replaced by ERRSR in the first sentence of the third paragraph and within Figure 11-19. The corresponding text must be replaced by :
"A source error of Move Engine m is indicated by the status flag E**R**RSR.MEmSER."

Figure 12-19 must be replaced by:

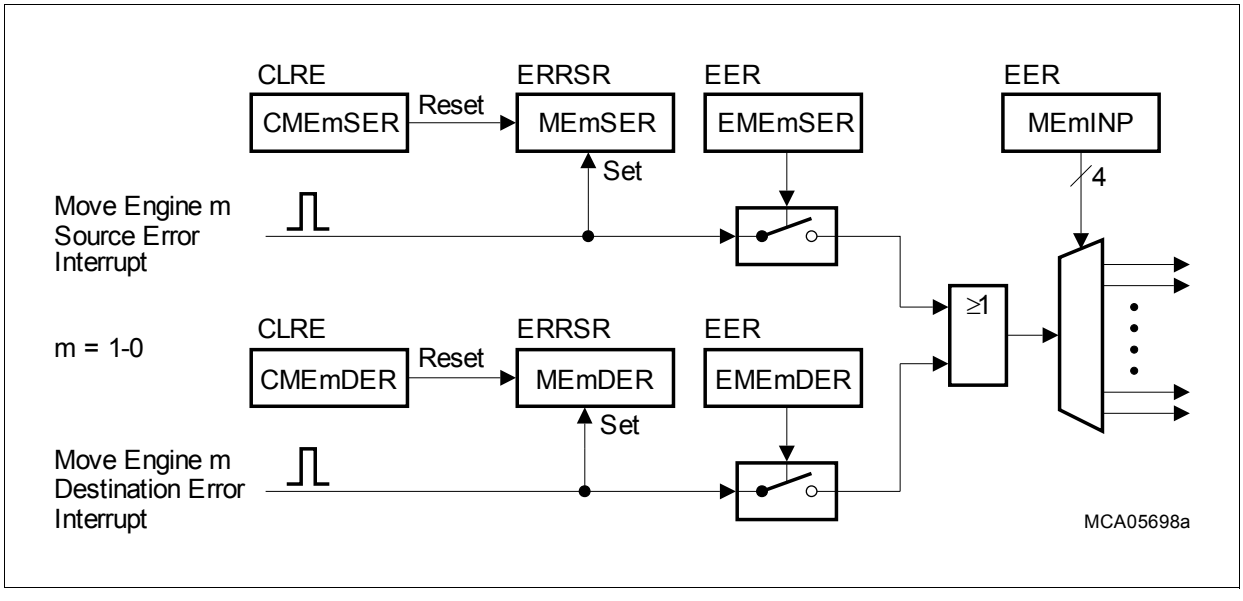

Figure 12-19 Move Engine Interrupts

Page 12-34

The following paragraphs should be added after the last (third) paragraph under Section 12.1.9 Pattern Detection:

Depending on CHCRmn.PATSEL and on the positive result of the comparison, two actions follow (if CHCRmn.PATSEL=00, no action will be taken when a pattern match is detected, so the wrap interrupt can be used):

- The activation of the interrupt corresponding to the current active channel mn using the Interrupt Pointer defined in CHICRmn.WRPP.
- Reset TRSR.HTREmn and TRSR.CHmn in order to stop the current transaction (Hardware and Software request enable). The value of CHSRmn.TCOUNT can be read out by the interrupt SW.

The software will have to service the interrupt and to activate again the channel.

Page 12-49

The description of bit field CHmn must be extended by the following sentence:
"CHmn is reset when a pattern match is detected".

The description of bit field HTREmn must be extended by the following sentence: "HTREmn is reset when a pattern match is detected".

Page 12-80

The second sentence of the last paragraph should be replaced with: "If DMA channel mn is active when writing to SADRmn, the source address will not be written into SADRmn directly but will be buffered in the shadow register **SHADRmn** until the start of the next DMA transaction."

Page 12-81

The second sentence of the last paragraph should be replaced with: "If DMA channel mn is active when writing to DADRmn, the source address will not be written into DADRmn directly but will be buffered in the shadow register **SHADRmn** until the start of the next DMA transaction."

Page 13-3

Section 13.2.1: The third sentence "External devices with 8, 16 or 32 bits of data..." must be corrected into "External devices with 16 or 32 bits of data...".

Additionally, the following note should be added at the end of this section:

Note: The TC1796 does not directly support for 8-bit data bus width. When 8-bit wide devices are used they must be arranged in pairs to implement either a 16-bit or a 32-bit wide memory region.

Page 13-24

The note paragraph at the bottom of the CONF32BIT bit field description should be replaced by the following note paragraph:

Note: In the TC1796, the EBU does not actually use bits 31 to 16 of the configuration word when CONF32BIT is 1. However, to allow future expansion this bit should be programmed to 0.

Page 14-26

Figure 14-5 must be updated with the following corrected drawing.

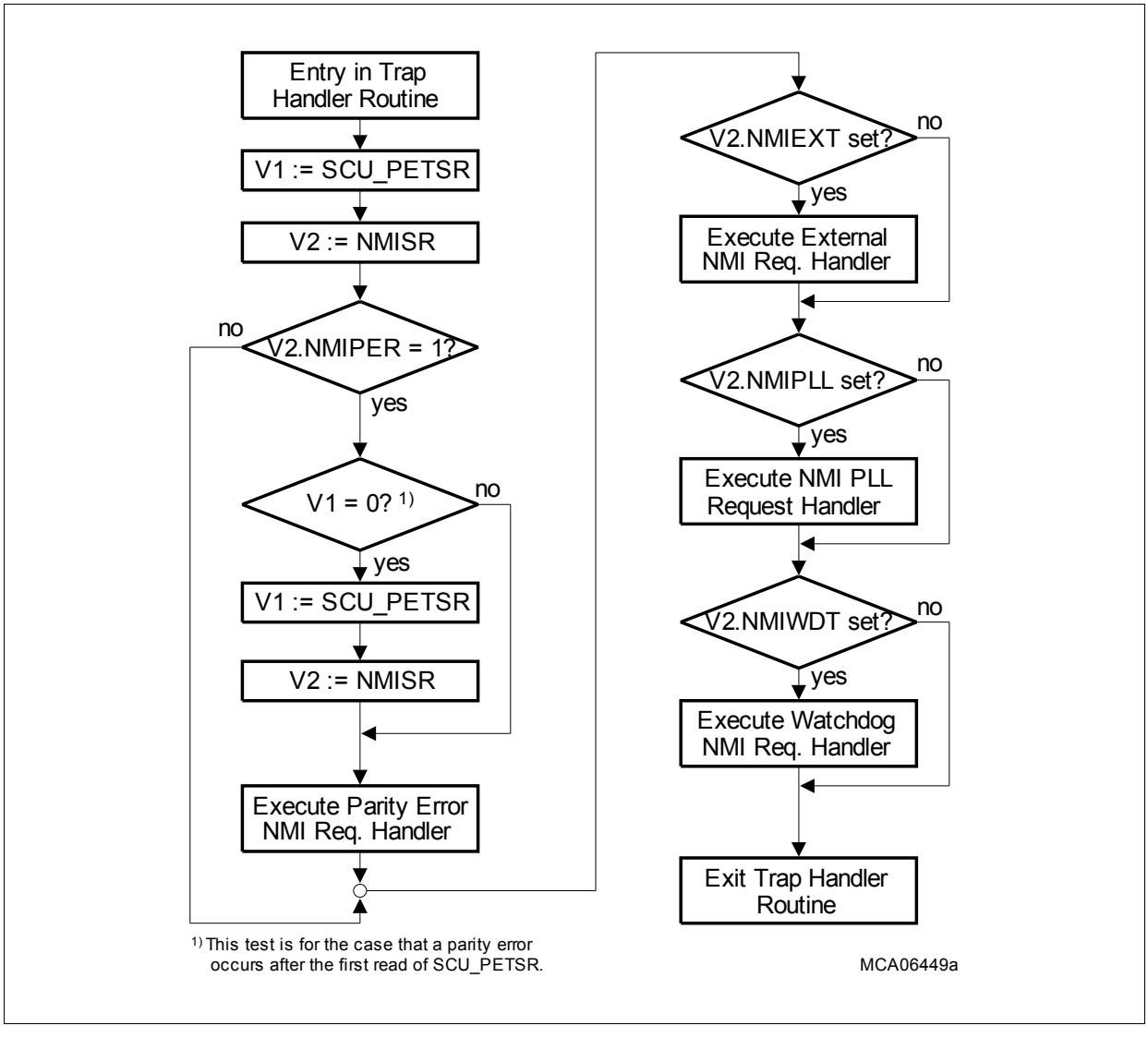

Figure 14-5 NMI Trap Handler Routine for Parity Error Handling

Page 18-16

The long name in column "Description" of Table 18-7 of register MSC0_UD2 must be changed into "MSC0 Upstream **Data** Register **2**".

The read and write access modes for address location F000 0804_H of Table 18-7 must be both changed from "nBE" into "BE".

Page 18-17

The long name in column "Description" of Table 18-7 of register MSC0_UD3 must be changed into "MSC0 Upstream Data Register 3".

The read and write access modes for address location F000 0904_H of Table 18-7 must be both changed from "nBE" into "BE".

The write access mode for register MSC1_ID in column "Access Mode - Write" of Table 18-7 must be changed from "BE" into "nBE".

Page 18-98

The long name in column "Description" of Table 18-30 of register MLI0_TPxBAR for x = 0-3 must be changed into "MLI0 **Transmitter Pipe x** Base Address Register".

Page 18-102

The write access mode for register MLI1_TIER in column "Access Mode - Write" of Table 18-30 must be changed from "SV" into "U, SV".

Page 18-105

The short name of register MMUCON in Table 18-33 must be changed into "MMU_CON".

Page 18-122

The address values of all entries (except the first row) of Table 18-38 must be corrected from F87FF**E**..$_H$ into F87FF**A**..$_H$.

3 User's Manual - Peripheral Units Part (Volume 2)

This section describes corrections for the Peripheral Units part of the User's Manual.

Page 20-21

In Figure 20-11 the wording "CON.PH = CON.PO = 1" must be replaced by ""CON.PH = **0;** CON.PO = 1".

Page 20-22

After the first sentence on the top of this page, the following sentence must be added: "With a TB write operation, all timing parameters stored in register SSOTC as well as the SSOC register are latched and remain valid for the consecutive transmission."

In the paragraph above Figure 20-12 the wording "SSOC.OEN = 0" must be replaced by "SSOC.OEN = **1**".

Page 20-23

In the first line below heading "Slave Select Register Update" , the text in brackets "with the activation of SLSOn" must be replaced by the text "with the TB register write operation".

Page 20-25

In the note paragraph on the upper part of this page the wording "CON.REN = 1" must be replaced by "CON.**A**REN = 1".

The following note paragraph must be added below the first note paragraph on this page:

Note: This error can occur after any transfer if the communication is stopped. This is the case due to the fact that SSC module supports back-to-back transfers for multiple transfers. In order to handle this the baud rate detection logic expects after a finished transfer immediately a next clock cycle for a new transfer.

Page 20-28

In the description for bit STIP the sentence "This bit determines..." must be replaced by the following sentence:
"This bit determines the logic level of the Slave Mode transmit signal when the SSC **slave select input signals are inactive** (PISEL.SLSIS $\neq$ $\mathbf{000_B}$)".

Page 20-30

The bit description of bit EN must be extended by the following sentence:
"Note that EN should only be reset by software while no transfer is in progress (STAT.BSY = 0)"

Page 20-34

The note paragraph at the bottom of the page must be replaced by the following note paragraph:

Note: The SSOC register content is latched by each TB register write operation and remains latched during the consecutive serial transmission.

Page 20-35

In the bit description of register SSOTC a footnote [1)] must be added to the bit combinations 00_B of bit fields LEAD, TRAIL, and INACT:

"[1)] For getting a best case timing with no timing delays (see Figure 20-11), this bit field value should be set when the SLSOn outputs are disabled (SSOC.OENn bits set to 0)."

Page 20-36

The note paragraph after the SSOTC register description table must be replaced by the following note paragraph:

Note: The SSOTC register timing parameters are latched by each TB register write operation and remain latched during a consecutive serial transmission.

Page 21-4

The first "Dash" paragraph under the third bullet paragraph under "Features" must be changed into:

Baud rate: f_{MSC} divided by **4**, 8, 16, 32, 64, 128, or 256

Page 21-20

At the bottom of this page the following sentence should be added:
"Note that in this case no time frame finished interrupt is generated any more."

Page 21-21

In the last paragraph the text "... of f_{MSC}/8 up to f_{MSC}/512." must be replaced by the text "... of f_{MSC}/4 up to f_{MSC}/256".

Page 21-25

Correction in Figure 21-17: the clock on the left side of block "Programmable Clock Divider" should be f_{MSC} instead of f_{MSC}/2.

In the paragraph below Figure 21-17 the wording "...derived from f_{MSC}/2" must be replaced by "...derived from f_{MSC}".

The factor "divide by 2" must be deleted in Equation (21.2).

Table 21-6 (column "Baud Rate") must be corrected in the following way (bold characters indicate changes):

Table 21-6 Upstream Channel Divide Factor DF Selection & Baud Rate

USR.URR	Divide Factor DF	Baud Rate
000_B	reception disabled	–
001_B	4	f_{MSC}/**4**
010_B	8	f_{MSC}/**8**
010_B	16	f_{MSC}/**16**
100_B	32	f_{MSC}/**32**
101_B	64	f_{MSC}/**64**
110_B	128	f_{MSC}/**128**
111_B	256	f_{MSC}/**256**

Note that the register description for bit field USR.URR on page 21-38 is correct.

Page 21-26

In the second line from the top the wording "...clocked with f_{MSC}/2" must be replaced by "...clocked with f_{MSC}".

Correction in Figure 21-18: the naming for the clock signal "f_{MSC}/2" must be changed into "f_{MSC}".

Page 21-41

Description of bit field NDBH: for bit combination NDBH = 00000_B, the text "No SRH bit shifted" must be replaced by "No SRH bit shifted; no selection bit is generated, the SRH active phase is completely skipped.".

Page 21-63

The factor "divide by 2" must be deleted in Equations (21.7) and (21.8).

Page 22-53

The following paragraph should be added after the last paragraph:

"In order to avoid direct reception of a message by a slave message object, as if it was an independent message object and not a part of a FIFO, the bit RXEN of each slave object must be cleared. The setting of the bit RXEN is "don't care" only if the slave object is located in a list not assigned to a CAN node."

Page 22-54

The first paragraph should be extended by a second sentence:

"A transmit FIFO consists of one base message object and one or more slave message objects."

Page 22-58

Table 22-4: The offset addresses of four register must be corrected as follows:

MSIMASK = $01C0_H$
PANCTR = $01C4_H$
MCR = $01C8_H$
MITR = $01CC_H$

Page 22-77

In Table 22-6, the two sentences in column "Signification" for LEC value 111_B at the bottom of the page must be replaced by the following two sentences:

"Whenever the CPU writes the value 111_B to LEC, it takes the value 111_B. Whenever the CPU writes another value to LEC, the written LEC value is ignored."

Page 22-87

In the first row of Table 22-8, column "CAN Bus State", the wording "reserved bits, " must be deleted. In the second row of Table 22-8, column "CAN Bus State", the wording "reserved bits, " must be added/inserted at: " .....RTR, reserved bits, IDE, ...".

Page 22-97, 22-101

In the description of the Message Object n Function Control Register MOFCRn the "0,r" bit and bit fields must be changed into "0,rw". This correction must be done at the register image diagram on page 22-97 and at the register description table. At page 22-101 the last row must be changed into:

0	[7:4], [15:12], 19	rw	**Reserved;** Read as 0 after reset; value last written is read back.

Page 22-103, 22-104

In the description of the Message Object n Acceptance Mask Register MOAMRn the "0,r" bit field must be changed into "0,rw". This correction must be done at the register image diagram on page 22-103 and at the register description table. At page 22-104 the row must be changed into:

0	[31:30]	rw	**Reserved;** Read as 0 after reset; value last written is read back.

Page 22-152

The link in column "Description see" of Table 22-13 for register STSRH must be corrected to point to register STSRH (instead pointing to STSRL).

Page 22-198

The paragraph after Equation (22-2) must be replaced by the following:

Equation (22-1) applies to normal divider mode (CAN_FDR.DM = $\mathbf{01}_B$) of the fractional divider. Equation (22-2) applies to fractional divider mode (CAN_FDR.DM = $\mathbf{10}_B$).

Page 22-203

The word "eight" in the second line of the first paragraph under "22.9.4.2 Node Receive Input Selection" must be deleted.

Page 23-2

The bullet paragraph "Programmable baud rate: ....." under "Features" must be changed as follows:

- Programmable baud rates
  - MLI transmitter baud rate: max. $f_{MLI/2}$ (= 37.5 Mbit/s @ 75 MHz module clock)
  - MLI receiver baud rate: max. f_{MLI}

Page 23-30

The following sentence must be added under the paragraph below "23.1.5 MLI Receiver Operation":

"The MLI receiver is able to operate with a maximum receive clock (RCLK) frequency up to the frequency of the module clock f_{MLI}.

Page 23-79

In the register table of register RPxBAR the row for bits [3:0] should be deleted. The range of the ADDR bit field must be extended to [31:0].

Page 23-109

The following paragraph with the formula must be added after the last paragraph:

The receiver baud rate is defined by the following formula.

$$\text{Baud rate}_{RCLKmax} = f_{MLI} \quad (23.4)$$

Page 23-112

The title of 23-7 should be corrected into “MLI0 and MLI1 I/O Line Selection and Setup“.

Page 24-61

The first three sentences of the second paragraph on the top must be replaced by three extended sentences:

Old:

“Normally, a GTC is enabled by writing GTCCTRk.EOA (Enable-Of-Action) with 0. Note that bit EOA is hardware protected. Therefore, any bit operation on EOA will result in a read-modify-write access.“

New:

“A GTC is enabled by writing (ST byte, word, half-word operation) GTCCTRk.EOA (Enable-Of-Action) with 0. Because bit EOA is hardware protected, read-modify-write operations (LDMST, ST.X, SWAP) only enable the GTC if bit EOA is modified from 1 to 0.“

Page 24-69

In the first sentence, the wording "adjacent GTCs" must be replaced by "adjacent LTCs".

Page 24-71

Fourth bullet paragraph in section "Free-Running Timer Mode": "GTCkOUT" must be replaced by "LTCkOUT".

Page 24-72

Second bullet from the top: "GTCkOUT" must be replaced by "LTCkOUT".

Third bullet paragraph in section "Compare Mode": "GTCkOUT" must be replaced by "LTCkOUT"

Last note paragraph must be completely deleted.

Page 24-75

Paragraph above the figure: "GTCs" must be replaced twice by "LTCs".

Paragraph below the figure title paragraph: "GTCCTRk.OCM0" must be replaced by "LTCCTRk.OCM0".

Page 24-76

The header text “Local Capture or Compare Event” of the second column in Table 24-4 must be replaced by “Local Capture, Compare, or TImer Overflow Event”.

Page 24-77

The first three sentences of the first paragraph on the top must be replaced by three extended sentences:

Old:

“Normally an LTC is enabled by writing LTCCTRk.EOA (Enable-Of-Action) with 0. Note that bit EOA is hardware protected. Therefore, any bit operation on EOA will result in a read-modify-write access.“

New:

“An LTC is enabled by writing (ST byte, word, half-word operation) LTCCTRk.EOA (Enable-Of-Action) with 0 in Capture Mode or Compare Mode. Because bit EOA is hardware protected, read-modify-write operations (LDMST, ST.X, SWAP) only enable the LTC if bit EOA is modified from 1 to 0 in Capture Mode or Compare Mode. If switching to Timer Mode, the LTC cell is enabled. If in Timer Mode every write operation into bit 0..7 will enable the LTC.“

Page 24-92

End of the second paragraph from the top: "GTC0 to GTC3" must be replaced by "GTCG0 to GTCG3".

Page 24-97

Third bullet paragraph: "I/O groups OG0 to OG6" must be replaced by "I/O groups IOG0 to IOG6".

Page 24-126

The text "else DCMk.Timer ++" must be included between the last two "endif" lines on the bottom.

Page 24-133

Below the second last line of the page : "GTCk.Cell_Enable = 1", the following line must be added: "GTCk.Enable_Of_Action = 0"

Page 24-174

The long name of register LTCCTRk must be corrected twice into “Local Timer Cell Control Register k .....”.

Page 24-179

The long name of register LTCCTR63 must be corrected twice into “Local Timer Cell Control Register 63”.

Page 24-228

The last sentence ““Note that Port 4 pins ...” in the first paragraph from the top must be completely deleted. See also the corrections on page 10-9 and page 10-49.

Therefore, Table 24-24 must be corrected, too (no special input selection for Port 4).

Page 24-237

Figure 24-91 must be replaced by the following figure: The red marked parts indicate the changes.

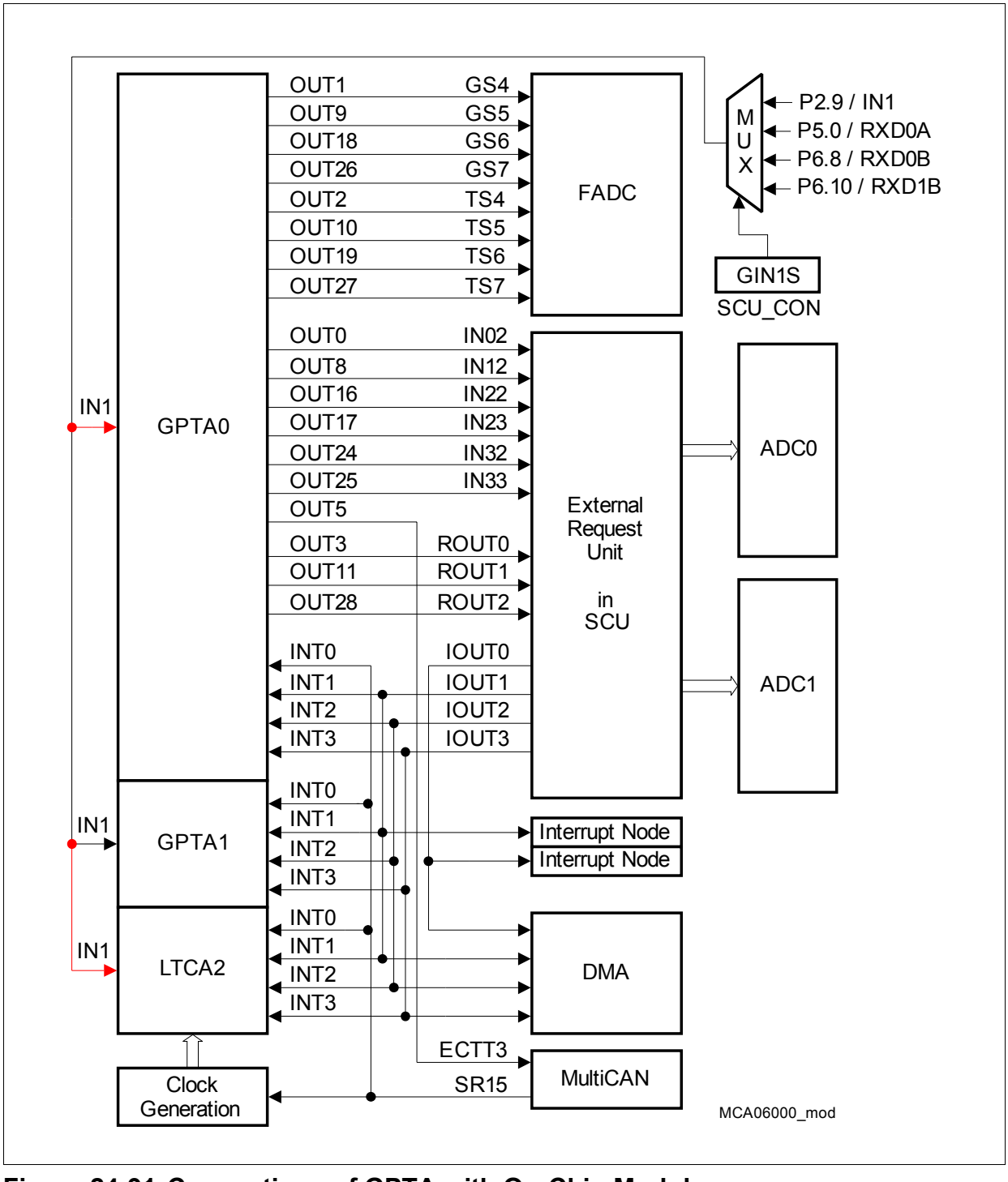

Figure 24-91 Connections of GPTA with On-Chip Modules

Page 24-238

The paragraph above Table 24-29 must changed:

"The input line**s** IN1 of the GPTA**0/GPTA1/LTCA2** module**s are** connected to the output of a 4-to-1 multiplexer. This multiplexer is controlled by bit field SCU_CON.GIN1S and allows the GPTA input **lines** IN1 to be connected to one out of four port input lines. This feature especially allows the baud rates of an ASC0 of ASC1 receiver input signal to be measured by timers of the GPTA.

Additionally, the title of Table 24-29 must be changed into "GPTA Input Line IN1 Connections".

Page 24-240

The following attention paragraph must be added at the bottom of this page:

Attention: If the frequencies of the module timer clocks f_{GPTA0}, f_{GPTA1}, or f_{LTCA2} are configured to be smaller than the control clock f_{CLC} (as programmed in register GPTA0_FDR) or even disabled (as programmed in register GPTA0_EDCTR), an action initiated by a write access to a module register could be significantly delayed, because the register write access is clocked by f_{CLC} and the register content is evaluated by hardware using the slower or disabled module timer clocks f_{GPTA0}, f_{GPTA1}, or f_{LTCA2}.

Page 25-9

The formula on the bottom of the page must be corrected into:

$$t_{TPERIOD} = TRLD \times \frac{20}{f_{ADC}} \qquad (25.1)$$

Page 25-120

The ADC0/ADC1 address ranges are wrong. The correct values are:

- ADC0 module:
  - Module Base Address = F0**1**0 0400H
  - Module End Address = F0**1**0 05FFH
- ADC1 module:
  - Module Base Address = F0**1**0 0600H
  - Module End Address = F0**1**0 07FFH

Page 26-6

The two heading paragraphs must be corrected in the following way:
Replace "**Configuration 3**" with "**Configuration 2**"
Replace "**Configuration 4**" with "**Configuration 3**"

Page 26-7

The text in the leftmost column of Table 26-1must be corrected in the following way:
Replace "(Configuration 2)" with "(Configuration 1)"
Replace "(Configuration 3)" with "(Configuration 2)"
Replace "(Configuration 4)" with "(Configuration 3)"

The last row of Table 26-1 (FAINxN | FAINxP | XX_B | 512) must be deleted.

Page 26-8

The second formula of equation (26.1) must be corrected in the following way:

$V_{FAREFM} = V_{FAGND} + (V_{FAREF} - V_{FAGND})/2$

Page 26-48

In the description for bit field MAVL value 11_B, the text "43 values" must be corrected into "4 values".

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Published by Infineon Technologies AG