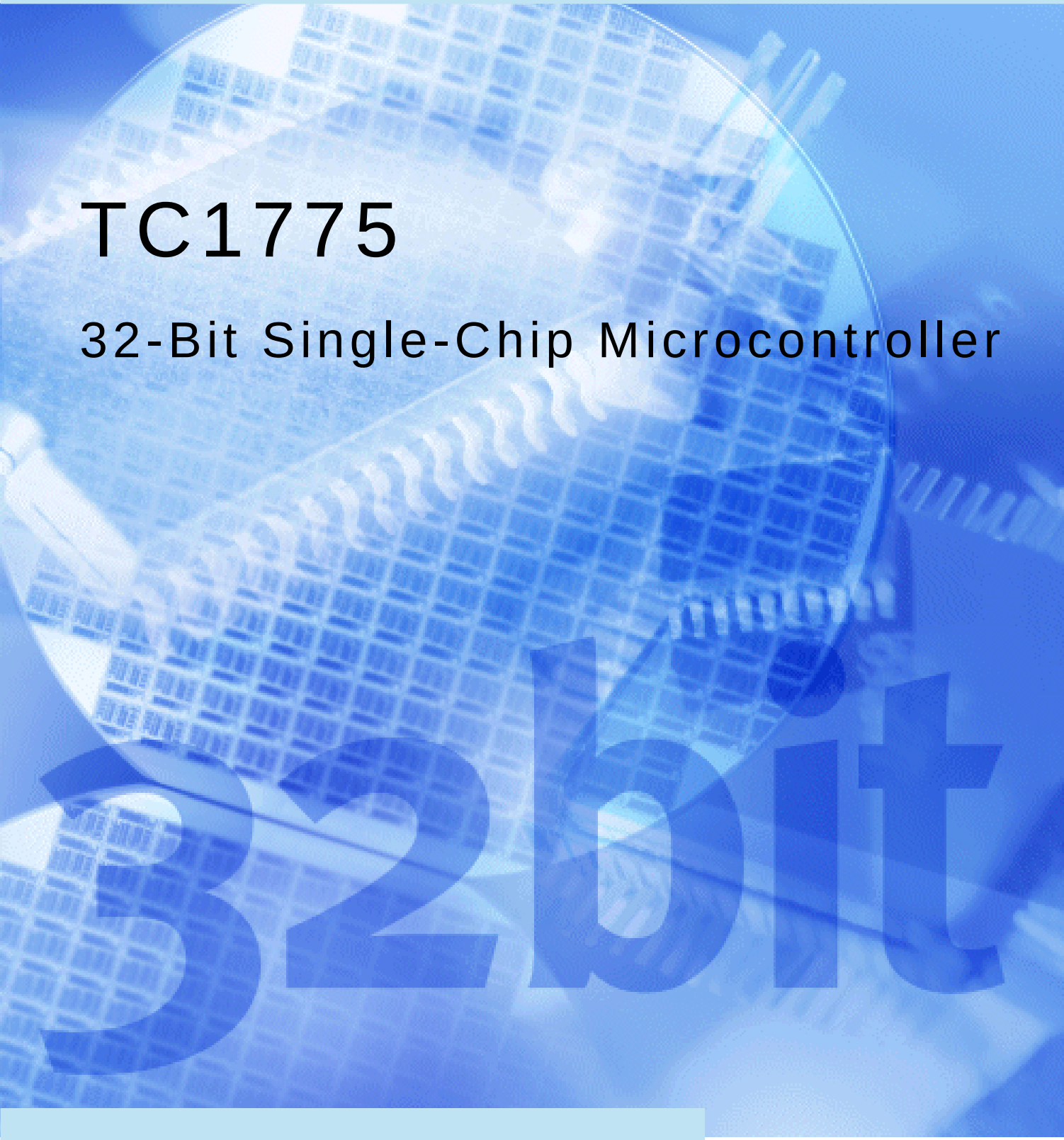
Documentation Addendum, V 1.4, Nov. 2004

TC1775

32-Bit Single-Chip Microcontroller



Microcontrollers

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Revision History:	**2004-11**	V 1.4
Previous Version:	V1.3 2003-02, V1.2 2002-07, V1.1 2001-10, V 1.0 2001-07	

Page	Subjects (major changes since last revision)
Changes for V1.3 to V1.4	
Page 6	Correction of special cache instructions;
Page 17	Descriptions of WDT corrected;
Page 20	Descriptions of SSC error flags corrected;
Page 21	Description of Node Control Register bit SIE corrected;
Page 22	GTC and LTC cascading information added;
Page 24	Correction of Figure 7-40
Page 25	PLLDTR.DTR width corrected; description of bit GTCTRm.SCO bit field corrected;
Page 26	Bit description of GTCCTRm.OCM corrected;
Page 28	Coding of bit field LCC of all ADC0/ADC1 CHCONn registers corrected;

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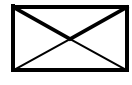

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1 Introduction

This document describes corrections, changes, and improvements for the two parts of the TC1775 User's Manual V2.0 2001-02, the System Units book and the Peripheral Units book. These corrections will be considered with the next update of these User's Manual documents.

The referenced documents to this addendum are:

- TC1775 System Units User's Manual, V2.0, Feb. 2001 (**Link to the PDF**)
  Ordering No.: B158-H7780-X-X-7600
- TC1775 Peripheral Units User's Manual, V2.0, Feb. 2001 (**Link to the PDF**)
  Ordering No.: B158-H7781-X-X-7600
- TC1775 Data Sheet, V1.2, May 2002 (**Link to the PDF**)

2 User's Manual - System Units Part

Page 1-3, Table 1-2

The definition of "U" must be changed into:

"Access permitted in User Mode 1 only.

Note: User Mode definitions see bit PSW_IO at Page 2-20"

Page 3-4

2nd paragraph, additional sentence after "(unconnected).":

"If the external clock signal at XTAL1 is stopped e.g. for test purposes (not a normal operating condition), XTAL1 should be held at high level."

Page 3-18

The following paragraph will be added on the bottom of this page and before the "Note" paragraph on the next page:

"When a disabled module is switched on by writing an appropriate value to its MOD_CLC register, status bit DISS changes from 1 to 0. During the phase, where the module becomes active any write access to corresponding module registers (when DISS is still set) will generate a bus error. Therefore, when enabling a disabled module, application software should check after activation of the module once whether DISS is already reset, before a module register will be written to."

Page 3-22, Table 3-5

The row for register STM_CLC must be corrected into:

STM_CLC	STM	enabled	■	–	–	–	–	–

Page 5-7, Section 5.3.1

The first sentence of the paragraph "When both of these conditions ...." is replaced by the following three sentences:

"When both of these conditions are met the $\overline{\text{HDRST}}$ output is released and tri-stated by the TC1775. If within this tri-state phase $\overline{\text{HDRST}}$ is still driven by an external device, the TC1775 remains in the reset condition as long as $\overline{\text{HDRST}}$ is at low level. When $\overline{\text{HDRST}}$ is again pulled to high level externally, the power-on reset sequence is terminated."

Page 5-7, Section 5.3.2

The last two paragraphs from the bottom must be replaced by the following new paragraph (see CR106566):

"The external hardware reset pin $\overline{\text{HDRST}}$ serves as an external reset input as well as a reset output. It is an active-low, bidirectional open-drain pin with an internal weak pull-up. An active-low signal at this pin causes the chip to enter its internal hardware reset sequence at the next system clock (f_{SYS}) transition. For synchronization purposes, $\overline{\text{HDRST}}$ must be at low level at least for two system clock cycles. $\overline{\text{HDRST}}$ is not actively driven by the TC1775 during a hardware reset sequence. If other hardware is reset by the signal line connected to $\overline{\text{HDRST}}$, the $\overline{\text{HDRST}}$ driving device must meet timing requirements for this hardware. After the TC1775 has terminated its hardware reset sequence internally, flag RST_SR.HDRST is set.

When $\overline{\text{HDRST}}$ is driven low by the TC1775 in software reset or in Watchdog Timer reset, the duration of $\overline{\text{HDRST}}$ low pulse is $16 \times t_{SYS}$ (t_{SYS} is the period of the system clock with frequency f_{SYS}), this means 400 ns at f_{SYS} = 40 MHz."

Page 5-8 Section 5.3.3

At the end of this section the following paragraph should be added:

"During a software reset operation the $\overline{\text{HDRST}}$ output signal is generated when RSTREQ.RREXT = 1. Note, that if after the end of such a software reset operation ($\overline{\text{HDRST}}$ output released and tri-stated by the TC1775) $\overline{\text{HDRST}}$ is still driven low by an external device, the TC1775 detects an external hardware reset condition and starts executing it as described in **Section 5.3.2**."

Page 5-11, Table 5-2

The two rows with Module/Function = "System Timer" and "Reset output pin $\overline{\text{HDRST}}$" must be corrected into:

System Timer	■	■	Optional	Not affected	■
Reset output pin $\overline{\text{HDRST}}$	■	■	Optional	Tri-stated	■

Page 5-9, Last paragraph of 5.3.4

In the last but one sentence "RSDBG, " should be deleted. This flag is not available.

Page 5-9

The text in the last paragraph beginning with "If a Watchdog Timer error occurs ...." until the end of this section on the next page 5-10 should be replaced by the following new paragraph:

"However, the reset circuitry of the TC1775 is designed to detect a double reset condition of the Watchdog Timer. If a Watchdog induced reset occurs twice, a severe system malfunction is assumed and the TC1775 is held in reset until a power-on reset or hardware reset occurs (see also **Chapter 18**)."

Page 6-9, Second paragraph of 6.3.3.5

The following sentence is added at the end of this paragraph: "Note also that the external NMI status flag NMISR.NMIEXT is not set after this Deep Sleep Mode exit case because the reset sequence clears NMISR.NMIEXT again after it has been set shortly through the falling edge on the $\overline{\text{NMI}}$ pin."

Page 7-5

In the last three paragraphs of the description below "Segment 11", the "and" between the address region values should be replaced by "to".

Page 8-5

In Table 8-2 the second column should ne named "CBP" instead of "CPB".

Page 8-9

Description of bit TERF: for TERF = 0 and TERF = 1 the words "... on a cache miss ..." must be replaced twice by "... on a RFB miss ...".

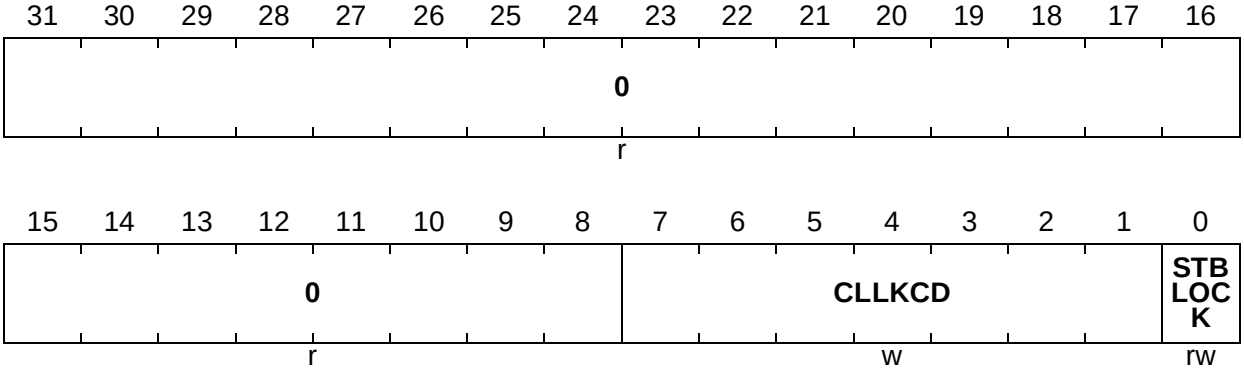
Page 9-4

The three special cache instructions in section 9.1.4 are wrong. "DFLASH, DINV and DFLINV" must be replaced by "CACHEA.W, CACHEA.I and CACHEA.WI".

Page 9-11

The description of register DMU_CON must be corrected in the following way:

DMU_CON
DMU Control Register **Reset Value: 0000 0000$_H$**



Field	Bits	Type	Description
STBLOCK[1)]	0	rw	**Lock Standby Data Memory** Bit can be set by writing a 1 to it (in supervisor mode only). Bit can only be reset (in supervisor mode only) by writing a 0 to it together with the appropriate clear lock code. 0 Normal operation of standby data memory 1 Standby data memory is locked. No read or write access of/to standby SRAM is possible. The state of STBLOCK after power-on reset is undefined. A hardware or software reset does not effect this bit.
CLLKCD	[7:1]	w	**Clear Lock Code** This bit field has to be written with 65$_H$ together with STBLOCK = 0 to reset the lock of the standby RAM.
0	[31:8]	r	**Reserved**; read as 0; should be written with 0.

1) This bit field is not available in the TC1775 BA11 step.

Page 10-17

The Data Range numbering in **Figure 10-2** is not correct. The figure must be updated in the following way:

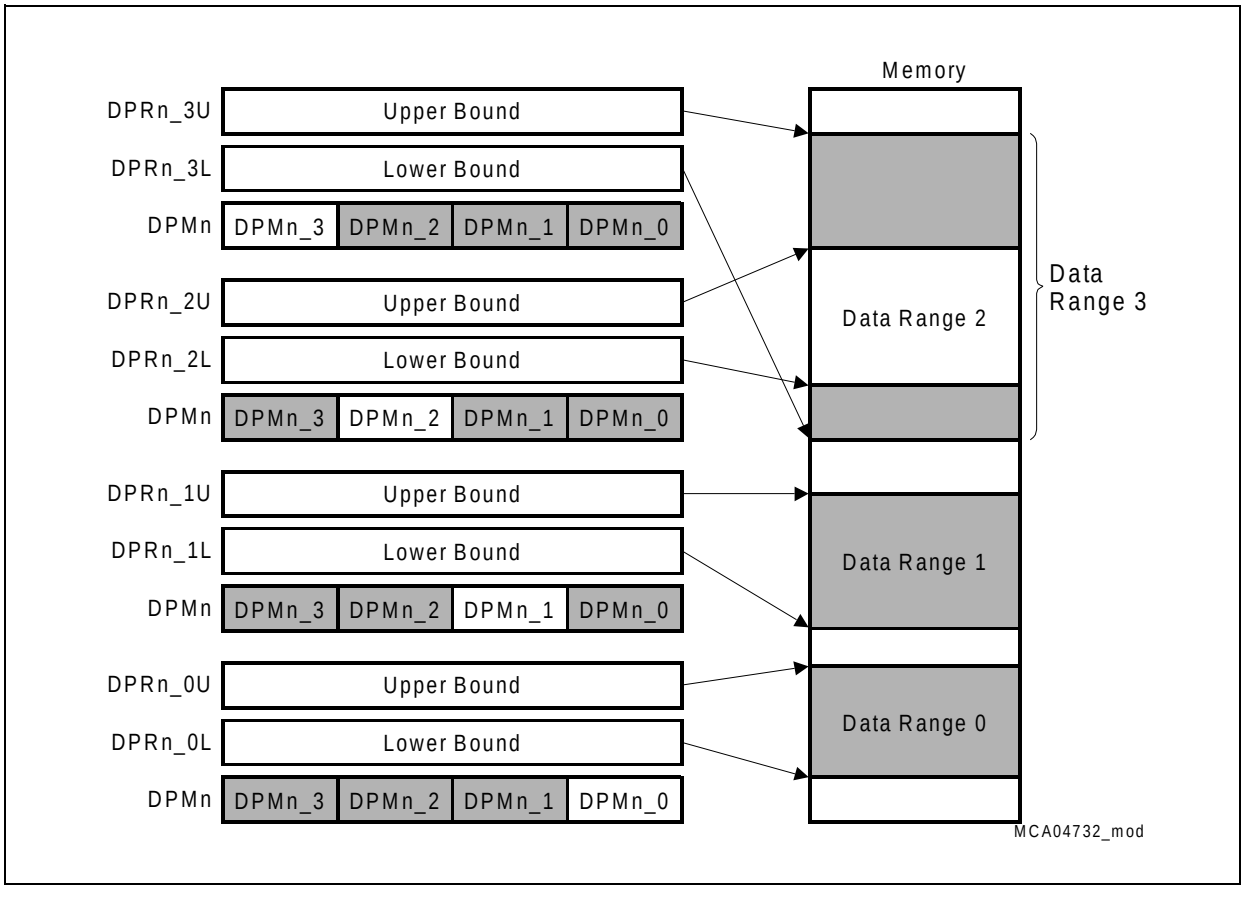


Figure 10-2 Example Configuration of a Data Protection Register Set

Page 11-54, Figure 11-18

In Figure 11-18 the block for registers P13_ALTSEL0 and P13_ALTSEL1 must be exchanged.

Page 11-36, Table 11-14

Column "Alternate Function": "EBU inactive" must be replaced by "Trace disabled". Also the note below Table 11-14 is changed into "Alternate functions of Port 5 (trace outputs) are controlled by hardware (bit SCU_CON.ETEN, see also **Chapter 4**)".

Page 12-15, Second paragraph

"A[26:0]" should be replaced by "A[25:0]".

Page 12-19, 12-20

In **Table 12-8** several parts are not correct. The following table shows only the corrected rows of **Table 12-8**.

Table 12-8 Data Assembly/Disassembly

FPI Bus Access Width	Data Width of External Device	FBU operation for demultiplexed access	$\overline{BC3}$	$\overline{BC2}$	$\overline{BC1}$	$\overline{BC0}$
16-bit	8-bit	first Byte access with A[0] = 0	high	high	high	low
		second Byte access with A[0] = 1 [1)]				
32-bit	8-bit	first Byte access with A[1:0] = 00_B	high	high	high	low
		second Byte access with [1)] A[1:0] = 01_B				
		third Byte access with [1)] A[1:0] = 10_B				
		fourth Byte access with [1)] A[1:0] = 11_B				
	16-bit	first Halfword access on byte lanes 0 and 1 with A[1:0] = 00_B	high	high	low	low
		second Halfword access on byte lanes 2 and 3 with A[1:0] = 10_B [2)]				

1) This byte access is performed automatically in consecutive to the previous byte access.

2) This half-word access is performed automatically in consecutive to the pervious halfword access.

Page 12-21, 12-22 (Figure 12-6), 12-24 (Figure 12-7), and 12-62

The TC1775 provides an additional demultiplexed read timing feature called "Early Sample". This feature is shown in the corrected **Figure 12-6** and controlled via bit 26 (called ES for "Early Read Sample Select") in register EBU_BUSCONx. EBU_BUSCONx.ES must be added as described on **Page 12**).

Due to this new feature, the paragraph starting with "Phase 2: ..." on page 12-21 must be replaced by the following description:

- "Phase 2: This cycle is always part of a read access. Please note that the read signal is deactivated (high) on the falling edge of CLKOUT. The data input is sampled and latched with this clock edge (EBU_BUSCONx.ES = 0) or with the rising edge of CLKIN when early sample is enabled with EBU_BUSCONx.ES = 1."

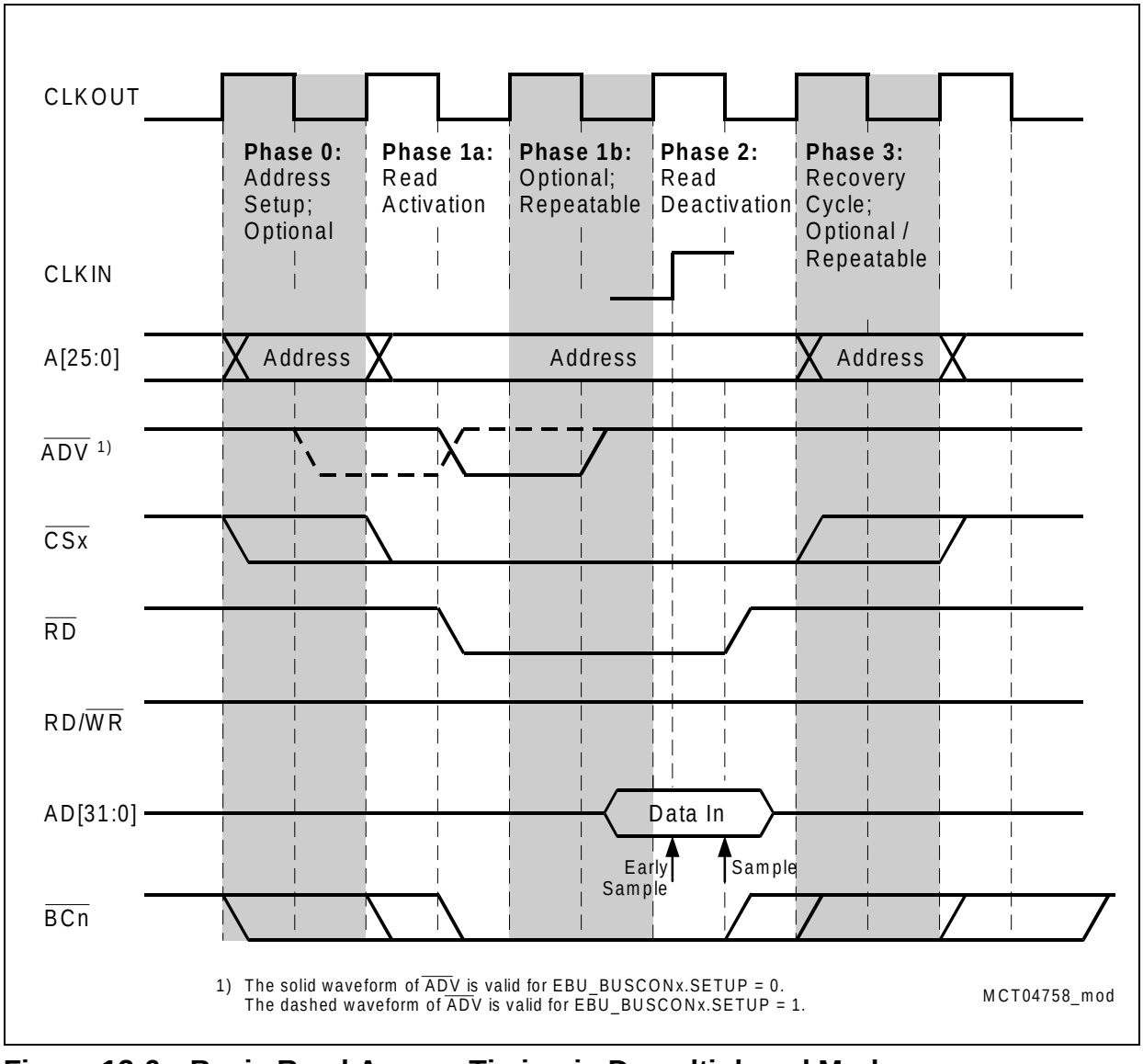


Figure 12-6 Basic Read Access Timing in Demultiplexed Mode

Figure 12-6 and **Figure 12-7** are also corrected concerning signal $\overline{ADV}$. As shown in these two figures, the $\overline{ADV}$ timing depends on the setting of bit EBU_BUSCONx.SETUP.

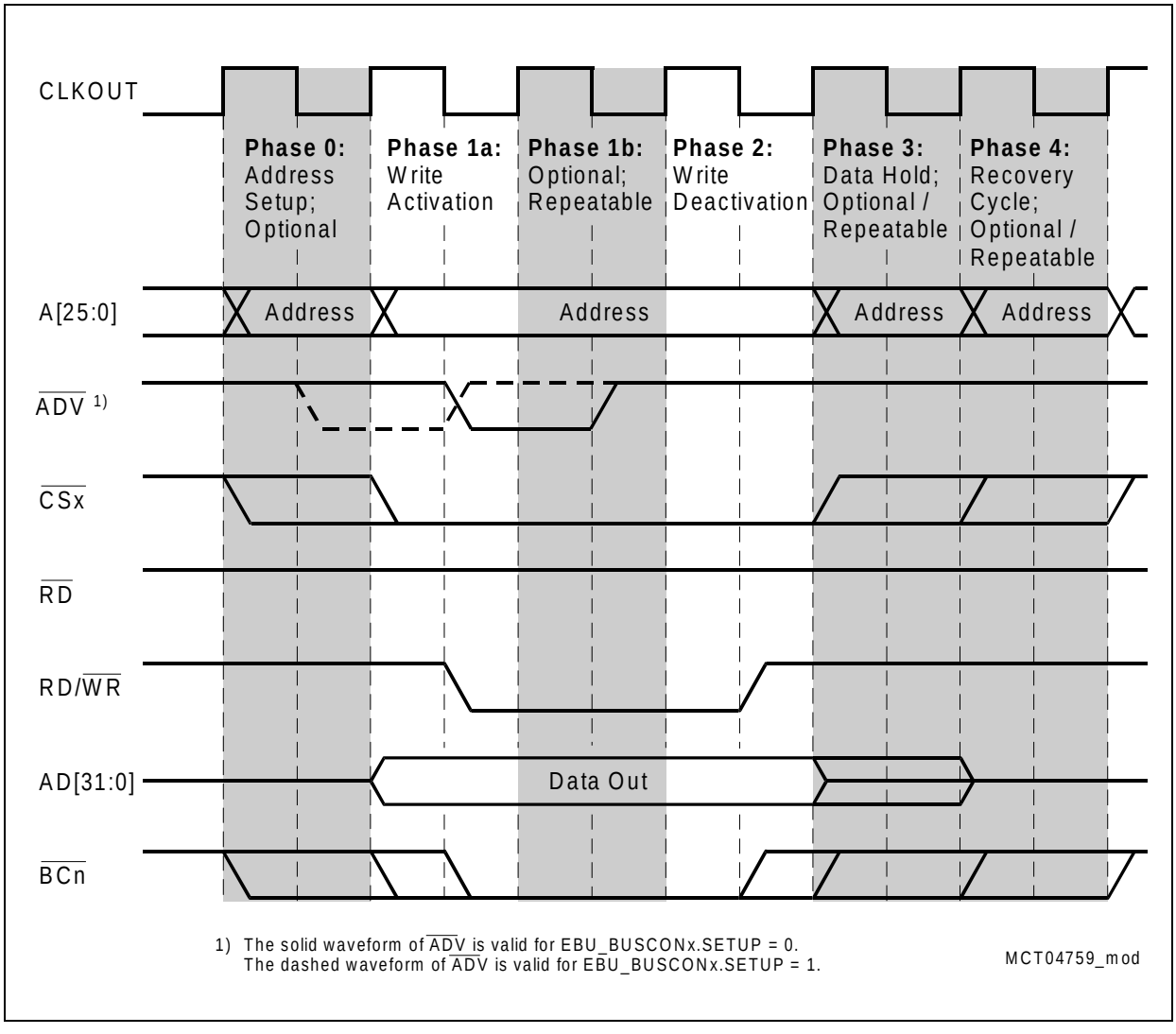


Figure 12-7 Basic Write Access Timing in Demultiplexed Mode

EBU_BUSCONx (x = 3-0)

EBU Bus Configuration Register x **Reset Value: E802 61FF$_H$**

31	30 29	28 27	26	25 24	23 22	21 20	19	18	17 16
WR DIS	ALEC	BCGEN	ES	AGEN	CMULTR	WAIT	WAI TINV	SET UP	PORTW
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

15 14 13 12 11 10 9	8 7 6	5 4	3 2	1 0
WAITRDC	WAITWRC	HOLDC	RECOVC	CMULT
rw	rw	rw	rw	rw

ES	26	rw	**Early Read Sample Select** 0 Reads are performed with regular timing. Data is sampled with the falling edge of CLKOUT. (default after reset) 1 Early read sampling of data is enabled. Data is sampled with the rising edge of CLKIN.

Page 12-42, Bullet list

Bit WAITRDC in the last but one entry of the bullet list belongs to register EBU_BUSCON0 instead of EBU_BUSCON.

Page 12-44, Update of Figure 12-16

Figure 12-16 should be update with the following drawing:

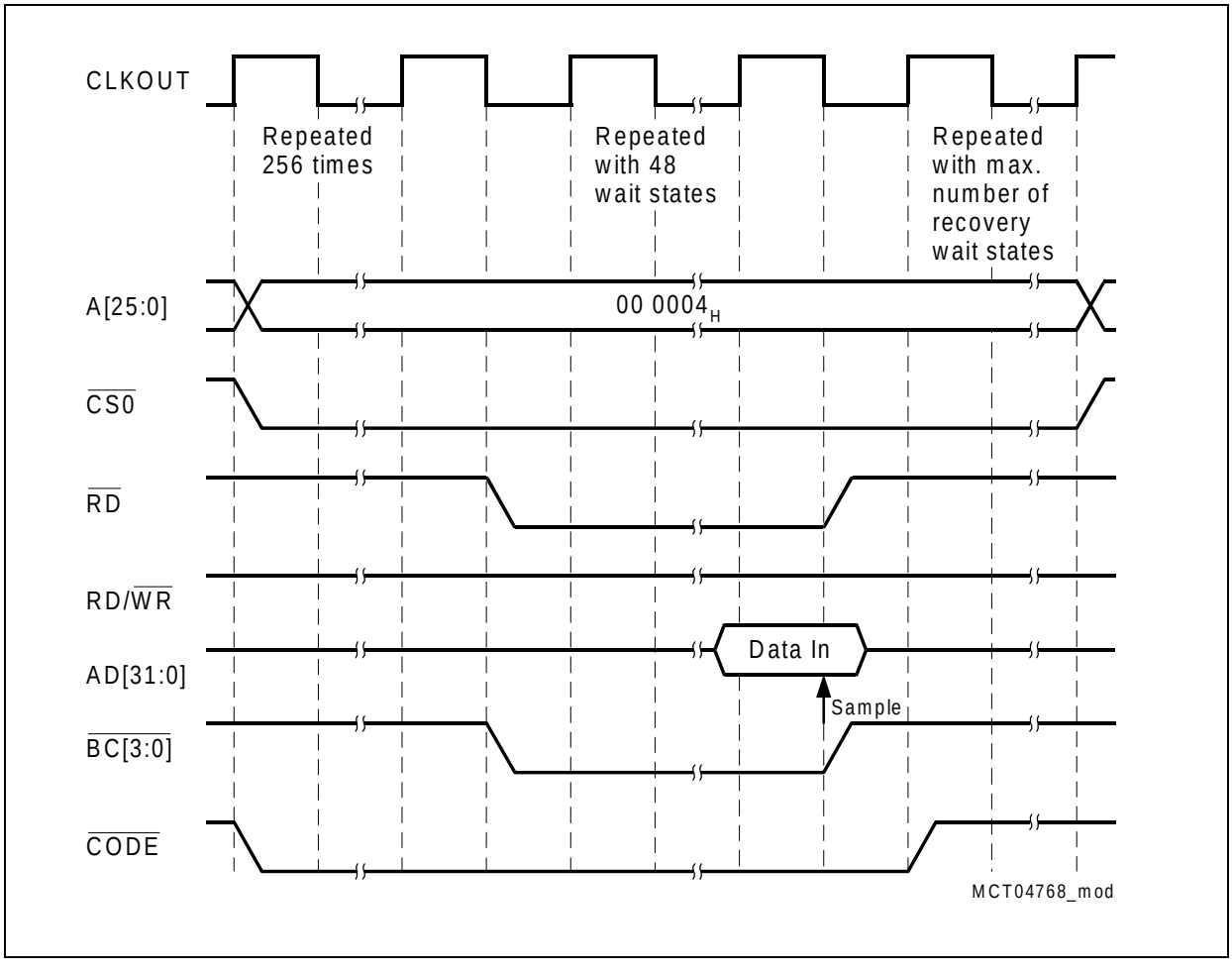


Figure 12-16 EBU Boot Process after Reset

Page 12-61

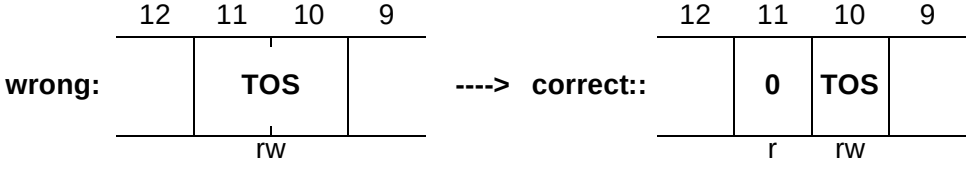
Bit EBU_ADDSELx.REGEN is of type "rw" instead of "r". It can be written, of course.

Page 12-70

The correct reset value of EBU_EXTCON should be 3C08 0240_H.

Page 13-5

Bit field TOS in the service request control registers is implemented as a single bit and not as a 2-bit bit field. This affects all SRC registers of the TC1775 (except PCP)!



TOS	10	rw	**Type of Service Control** 0 CPU service is initiated. 1 PCP service is initiated.
0	11	r	**Reserved**; read as 0; should be written with 0.

Section 13.3.1.5 must be corrected in the following way:

13.3.1.5 Type-of-Service Control (TOS)

There are two Service Providers for service requests in the TC1775, the CPU and the PCP. The TOS bit is used to select whether a service request generates an interrupt to the CPU (TOS = 0) or to the PCP (TOS = 1).

Page 13-23

CPU_SRC.TOS must be corrected according the description above.

Page 14-4

"Note" paragraph should be deleted and its text (sentence) should be added to the table footnote [1)] (at its end).

Page 14-6

In the last line of the paragraph below "MPW Trap" the words ".. with read permissions .." must be replaced by ".. with write permissions .." .

Page 14-12, Section 14.4.1, second paragraph

In the first sentence "The CPU detects a zero-to-one transition of the NMI input signal..." should be corrected into "The CPU detects a one-to-zero transition of the $\overline{\text{NMI}}$ input signal"

Page 14-13

The following "Note" paragraph should be added to the description of bit NMIEXT:

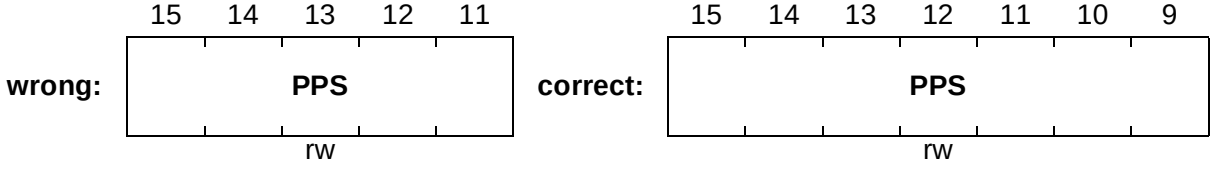
Note: This bit is reset after an exit from Deep Sleep Mode through pin $\overline{NMI}$ when bit PMG_CON.DSRW has been set before (full reset sequence executed).

Page 15-7, Section 15.3.1.3

In this paragraph "R5 and R6" should be replaced by "R4 and R5".

Page 15-44, 15-46

Bit field PPS in register PCP_CS is not defined correctly. The diagram below shows the correction and the revised bit field description.



Field	Bits	Type	Description
PPS	[15:9]	rw	**PRAM Partition Size** 0 Default, only allowed with PPE = 0 1 CSA contains 3 context save regions .. .. n CSA contains 1 + 2 × n context save regions *Note: The actual size of the CSA (in words) is given by the formula (2 × n + 1) × m, where m is the number of registers in the selected context model.* *If PPE = 1 and the PCP attempts to perform a data write to PRAM addresses below the CSA an error condition has occurred.* *This setting also controls the maximum channel number (MCN) used in system. If n = 1 the maximum channel number is MCN = 2 × n. If the SRPN is greater than MCN, an error condition has occurred.* *E.g. setting PPS to n = 3 will give a CSA containing 7 context save regions. As channel 0 cannot be used and MCN = 6, channels 1 to 6 are allowed.*

Page 15-80

Description of SUB.F instruction should be corrected form "Subtract the sign-extended contents ...." into "Subtract the zero-extended contents ....". Further, the "Operation" code should be "R[b] = R[b] - zero_ext(FPI[R[a]])".

Page 16-7, Table 16-2

The definition for the acknowledge code ACK must be corrected into:

ACK = 01_B: SPT
ACK = 10_B: RTY
ACK = 11_B: ERR

Page 16-8, Table 16-4

In the TC1775, block transfers are not used by the FPI Bus master units. Therefore, Table 16-4 with the last sentence of the paragraph above will be modified into:

"Note that block transfers (OPC = 0100_B to 0110_B) and split transactions (OPC = 1000_B to 1110_B) are not used in the TC1775.

Table 16-4 FPI Bus Operation Codes (OPC)

OPC	Description	OPC	Description
0000_B	Single Byte Transfer (8-bit)	**1000_B**	Split Block Transfer Request (1 transfer)
0001_B	Single Half-Word Transfer (16-bit)	**1001_B**	Split Block Transfer Request (2 transfers)
0010_B	Single Word Transfer (32-bit)	**1010_B**	Split Block Transfer Request (4 transfers)
0011_B	Single Double-Word Transfer (64-bit)	**1011_B**	Split Block Transfer Request (8 transfers)
0100_B	2-Word Block Transfer	**1100_B**	Split Block Response
0101_B	4-Word Block Transfer	**1101_B**	Split Block Failure
0110_B	8-Word Block Transfer	**1110_B**	Split Block End
0111_B	Reserved	**1111**	No operation

Note: Shaded FPI Bus transactions are not used in the TC1775."

Page 16-15

BCU_SRC.TOS must be corrected according the description on **Page 14**.

Page 17-1, Bullet list

The two points in the bullet list:

- Counting begins at power-on reset
- Continuous operation is not affected by any reset condition except power-on reset

should be replaced by the following three bullet points:

- Counting starts automatically after a reset operation
- STM is reset under following reset causes (see also Chapter 5.3):
  - Wake-up reset (PMG_CON.DSRW must be set)
  - Watchdog reset
  - Software reset (RST_REQ.RRSTM must be set)
  - Power-on reset
- STM is not reset at a hardware reset ($\overline{\text{HDRST}}$ = 0)

Page 18-2

The first sentence of the last but one paragraph "Double Reset Detection" must be replaced by the following sentence:

"If a Watchdog induced reset occurs twice, a severe system malfunction is assumed and the TC1775 is held in reset until a power-on reset or hardware reset occurs."

Page 18-16

Table 18-7: the last sentence "A write attempt..." in the "Description" cell of row "Operation" must be deleted. There's no bus error generated in this mode.

Page 18-17

If a power saving mode is awakened by the WDT, no NMI trap occurs. Therefore, the section 18.4.6.5 must be replaced by the following description:

18.4.6.5 WDT Operation During Power-Saving Modes

If the CPU is in Idle Mode or Sleep Mode it cannot service the Watchdog Timer because no software is running. Excluding the case where the system is running normally, a strategy for managing the WDT is needed while the CPU is in Idle Mode or Sleep Mode. There are two ways to manage the WDT in these cases. First, the Watchdog can be disabled before idling the CPU. This has the disadvantage that the system will no longer be monitored during the idle period.

A better approach to this problem relies upon a wake-up features of the WDT. Whenever the CPU is put in Idle or Sleep Mode and the WDT is not disabled, it causes the CPU to be awakened at regular intervals. When the Watchdog Timer changes its count value (WDT_SR.WDTTIM) from $7FFF_H$ to 8000_H (when the most significant bit of the WDT counter changes its state from 0 to 1), the CPU becomes awakened and continues to

execute the instruction that follows the instruction which has been executed as the last instruction before entering the Idle or Sleep Mode.

Note: Before switching into a non-running power-management mode, software should perform a Watchdog service sequence. With the Modify Access, the Watchdog reload value, WDT_CON0.WDTREL, should be programmed such that the wake-up occurs after a period which best meets application requirements. The maximum period between two CPU wake-ups is one-half of the maximum Watchdog Timer period.

Page 18-18

The second paragraph "Double Watchdog Errors are detected ....." must be replaced by the following paragraphs:

"The purpose of the Double Watchdog Error feature is to avoid loops such as: Reset - software does not start correctly - prewarning - watchdog reset - software does not start correctly - .....

The WDT has an internal counter that generates internally a constant reset after a second watchdog error. This counter can be cleared only by external reset sources (power-on reset or hardware reset)."

Page 18-29

In table cell "Field", bit name for bit 0 should be "ENDINIT".

Page 19-15

RTC_SRC.TOS must be corrected according the description on **Page 14**.

Page 20-6

Section 20.1.4.3, bottom of the page: the first two actions that are performed on a breakpoint trap are incorrect. The correct order of actions is:

- Write PCXI to BE80 0000_H
- Write PSW to BE80 0004_H
- .....

Page 20-15

SBSRC0.TOS must be corrected according the description on **Page 14**.

Page 20-27

The functionality described in section 20.4.5 "Trace with External Bus Address" is not available. Therefore, this section must be deleted.

Page 21-1, Table 21-1

The definition of "U" must be changed into:

"Access permitted in User Mode 1 only.

Page 21-10

In Table 21-4, a "32" should be added to the "Access Mode" "Read" and "Write" cells for PCP Data Memory and PCP Code Memory (as in Table 15-14 on page 15-93).

Pages 21-21 and 21-21

The long name (description) of registers TB and RB in Table 21-5 must be corrected:

– SSC0_TB = "SSC0 Transmit**ter** Buffer Register"
– SSC0_RB = "SSC0 Receive**r** Buffer Register"
– SSC1_TB = "SSC1 Transmit**ter** Buffer Register"
– SSC1_RB = "SSC1 Receive**r** Buffer Register"

Page 21-46 and 21-51

The long name (description) of registers MSS0 and MSS1 in Table 21-5 must be corrected:

– ADC0_MSS0 = "ADC0 **Module** Service Request Status Register 0"
– ADC0_MSS1 = "ADC0 **Module** Service Request Status Register 1"
– ADC1_MSS0 = "ADC1 **Module** Service Request Status Register 0"
– ADC1_MSS1 = "ADC1 **Module** Service Request Status Register 1"

3 User's Manual - Peripheral Units Part

Page 2-12, Second paragraph

"± 16" and in asynchronous modes and "± 4" should be replaced by "÷ 16" and "÷ 4".

Page 2-24

"FDV contains the .." should be corrected into "FD_VALUE contains the ...".

Pages 2-25 and 2-26

The long name (description) of registers TBUF and RBUF in must be corrected:

– TBUF = "Transmit Buffer Register"
– RBUF = "Receive Buffer Register"

This correction also requests a change on the bottom of pages 1-7 and 2-3: correct is "... On a transmit buffer .." and " ... On a receive buffer ..".

Page 2-35

Bit field TOS of all ASC0 and ASC1 SRC registers must be corrected according the description on **Page 14**.

Pages 3-13, 3-14

In case of an error, the corresponding error flag is always set independently of the error enable bit. The error interrupt line EIR becomes only activated if the corresponding error enable bit is set (as shown Figure 3-7). The description does not describe this behavior correctly.Therefore, the following sentences must be corrected:

Page 3-13, 1. paragraph: "When an error is detected, the respective error flag is always set and the error interrupt request will be generated by activating the EIR line if the corresponding error enable bit is set (see Figure 3-7)."

Page 3-13, last paragraph below Figure 3-7: "This condition sets the error flag STAT.RE and, if enabled via CON.REN, sets the error interrupt request line EIR."

Page 3-14, 1. paragraph: "This condition sets the error status flag STAT.PE and, if enabled via CON.PEN, the error interrupt request line EIR."

Page 3-14, 2. paragraph: "This condition sets the error status flag STAT.BE and, if enabled via CON.BEN, the error interrupt request line EIR."

Page 3-14, paragraph below 1. "Note": "This condition sets the error status flag STAT.TE and, if enabled via CON.TEN, the error interrupt request line EIR."

Pages 3-21

The long name (description) of registers TB and RB in must be corrected:

– TB = "Transmit Buffer Register"
– RB = "Receive Buffer Register"

Page 3-18

After the last paragraph (and therefore before the note on the next page), the following paragraph should be added for clarification:

"When a disabled module is switched on by writing an appropriate value to its MOD_CLC register, status bit DISS changes from 1 to 0. During the phase, where the module becomes active any write access to corresponding module registers (when DISS is still set) will generate a bus error. Therefore, when enabling a disabled module, application software should check after activation of the module once whether DISS is already reset, before a module register will be written to."

Page 3-27

Bit field TOS of all SSC0 and SSC1 SRC registers must be corrected according the description on **Page 14**.

Page 4-49

The description of Node Control Register bit SIE must be improved:
replace ".. when a message transfer ..." by ".. when any valid message transfer ..."

Page 4-86

CAN_SRC[7:0].TOS must be corrected according the description on **Page 14**.

Page 5-8

Typo: second paragraph "The SDLM ..." under 5.1.4.3: "... Bus-side receive buffer ..."

Page 5-60

SDLM_SRC[1:0].TOS must be corrected according the description on **Page 14**.

Page 6-39 and 6-40

Bits T2ADIR and T2BDIR should be marked as "rh" instead of "rw".

Page 6-59

GPTU_SRC[7:0].TOS must be corrected according the description on **Page 14**.

Page 7-47

Table 7-2 must be exchanged with the following table (shaded cells are different):

Table 7-2 Selection of GTC Output Operations and Action Transfer Modes

Bit Field OCM[2:0]	Local GTC Capture or Compare Event	M1O, M0O	State of Local Data Output Line
0 0 0	not occurred occurred	0 0 0 0	not modified not modified
0 0 1	not occurred occurred	0 0 0 1	not modified inverted
0 1 0	not occurred occurred	0 0 1 0	not modified 0
0 1 1	not occurred occurred	0 0 1 1	not modified 1
1 0 0	not occurred occurred	M1I M0I M1I M0I	modified according M1I, M0I modified according M1I, M0I
1 0 1	not occurred occurred	M1I M0I 0 1	modified according M1I, M0I inverted
1 1 0	not occurred occurred	M1I M0I 1 0	modified according M1I, M0I 0
1 1 1	not occurred occurred	M1I M0I 1 1	modified according M1I, M0I 1

Page 7-47, 7-54

This issue (limitation of GTC and LTC cascading) is an extension for the GPTA which must be added to the GPTA chapter.

Page 7-47: adding a note paragraph on the bottom of this page:

Note: Cascading of GTCs to logical operating units is limited. TC1775 specific details are given on Page 6-131.

Page 7-54: adding a note paragraph after the first paragraph:

Note: Cascading of LTCs to logical operating units is limited. TC1775 specific details are given on Page 7-131.

Section "7.3 GPTA Module Implementation" on the bottom of Page 7-131: adding the following subsection:

"7.3.2.3 Limits of Cascading GTCs and LTCs"

As noted on Page 6-47 and Page 7-54, at maximum 32 GTCs and at maximum 64 LTCs can be cascaded to logical operating units. In the TC1775, however cascading of GTCs and LTCs is limited under certain conditions. The limitations directly depend on the f_{GPTA} module clock frequency.

Table 1 Limits of Cascading GTCs and LTCs

f_{SYS}	Selected Clock Divider Ratio[1)]	f_{GPTA}	Max. Number of Cascaded GTCs/LTCs
40 MHz	1	40 MHz	16
	2	20 MHz	32
	3	13.3 MHz	no limits for GTCs, 48 LTCs
	4 and greater	10 MHz	no limits
20 MHz	1	20 MHz	32
	2 and greater	10 MHz	no limits

1) Selected by bit field GPTA_CLC.RMC.

Page 7-49

Text in brackets will be added at the end of the first bullet paragraph under "Architecture": "(YI of LTC00 is always 0000_H)"

Page 7-51

Text in brackets will be added at the end of the first bullet paragraph under "Capture Mode": "(LTC00 always copies 0000_H)"

Page 7-52

3. paragraph from the top "Note: ...": in this Note paragraph, "GTC" and "GTCXR" must be replaced by "LTC" and "LTCXR".

Page 7-53

Table 7-3 must be exchanged with the following table:

Table 7-3 Selection of LTC Output Operations and Action Transfer Modes

Bit Field OCM[2:0]	Local LTC Capture or Compare Event	M1O, M0O	State of Local Data Output Line
0 0 0	not occurred occurred	0 0 0 0	not modified not modified
0 0 1	not occurred occurred	0 0 0 1	not modified inverted
0 1 0	not occurred occurred	0 0 1 0	not modified 0
0 1 1	not occurred occurred	0 0 1 1	not modified 1
1 0 0	not occurred occurred	M1I M0I M1I M0I	modified according M1I, M0I modified according M1I, M0I
1 0 1	not occurred occurred	M1I M0I 0 1	modified according M1I, M0I inverted
1 1 0	not occurred occurred	M1I M0I 1 0	modified according M1I, M0I 0
1 1 1	not occurred occurred	M1I M0I 1 1	modified according M1I, M0I 1

Page 7-57

In Figure 7-40, the "0" at the cutting point of the two axes should be replaced by "$FFFF_H$" or "-1".

Page 7-84

The code

```
if (GTCk.Capture_opposite_timer) then
   GTCk.X = GTm.Timer
else ......
```

must be corrected into

```
if (GTCk.Capture_opposite_timer) then
   GTCk.X = GT!m.Timer
else ......
```

Page 7-90

Table row "LTCk.X_write_access": comment "Internal value set to indicate the LTCk.X was modified ...." is extended into "Internal value set to indicate the LTCk.X was modified (written, incremented, or reset) ...."

Page 7-96

Bit 0 to 5 of FPCCTR1 are "rwh" bits (not "rw" bits). The paragraph ""Bit protection is ..." in the bit description will be completed by: "(see also Note on **Page 7-124**)." The Note on page 7-124 is described at section **"Page 7-124 to 7-126" on Page 26**of this document.

Pages 7-99 and 7-100

Bits PDLCTR.ERR0 and PDLCTR.ERR1 are "rh" instead of "rw".

Page 7-104

The bit description for bit PLLCTR.PEN must be completed with the following sentence: "Bit protection is implemented for PEN to allow read-modify-write instructions. (see also Note on **Page 7-124**).". The Note on page 7-124 is described at section **"Page 7-124 to 7-126" on Page 26**of this document.

Page 7-107

The width of bit field PLLDTR.DTR must be corrected into [24:0]. Bits [31:25] are 0,r.

Page 7-109

The description of bit GTCTRm.SCO bit field must be corrected/improved in the following way:

This bit field defines the bit of the operation result "GTm timer value - data bus value" which is used as TGE flag.

0000_B **10th** bit is used as TGE flag.
0001_B 11th bit is used as TGE flag.
... ...
1110_B 24th bit is used as TGE flag.
1111_B **25th** bit is used as TGE flag.

The description of bit field GTCTRm.MUX should be extended as follows:

000_B = Clock bus line CLK0 selected
001_B = Clock bus line CLK1 selected
010_B = Clock bus line CLK2 selected
011_B = Clock bus line CLK3 selected
100_B = Clock bus line CLK4 selected

101_B = Clock bus line CLK5 selected
110_B = Clock bus line CLK6 selected
111_B = Clock bus line CLK7 selected

Page 7-113

The bit description for OCM = $1XX_B$ should be corrected into:

"GTCkOUT output line state is affected by an internal GTCk event and/or by an operation occurred in an adjacent GTCn (n = less or equal k) and reported by the M1I, M0I interface lines."

Page 7-117

The description of bit CUD must be corrected in the following way:

CUD	9	rwh	**Timer Reset Mode: Coherent Update Enable** 0 Select line output SO is not toggled on timer reset overflow. 1 Select line output SO is toggled on next timer reset overflow. When CUD is set by software it remains set until the next timer reset overflow (LTCk reset event) occurs and is cleared by hardware afterwards. When CUD is set, it cannot be reset by software by writing a 0 to it.

Page 7-118

Description of bit field LTCTRk.OCM must be corrected as follows:

OCM = $X11_B$: LTCk data output line is forced with 1.

Page 7-120

Description of bit fields OMXk for k = 32 to 63 is wrong (in the table the two rows from the bottom. According Figure 7-43 on page 7-60, the following bit combinations must be corrected:

OMXk (k = 32-47) = 01_B: Port line k is driven by GTCk - 32 output
OMXk (k = 32-47) = 11_B: Port line k is driven by LTCk - 32 output

OMXk (k = 48-63) = 01_B: Port line k is driven by GTCk - 32 output
OMXk (k = 48-63) = 11_B: Port line k is driven by LTCk - 32 output

Page 7-124 to 7-126

The type of all "rw" bits of registers SRS0, SRS1, SRS2, and SRS3 must be changed into "rwh". Further the following footnote must be added to "rwh" bits in the register bit

description tables: "Bit protection is implemented to allow "read-modify-write" instructions."

Page 7-124 on top, below paragraph "7.2.11 ...": the following note paragraph will be added:

Note: The write protected bits in the Service Request State Registers are not changed during a read-modify-write instruction, i.e. when hardware sets e.g. an request state bit between the read and the write of the read-modify- write sequence. It is guaranteed that only the intended bit(s) is/are effected by the write-back operation.

Page 7-132

GPTA_SRC[53:00].TOS must be corrected according the description on **Page 14**.

Page 8-7

The paragraph below Figure 8-9 becomes replaced by the following one:

The channel injection request control register CHIN contains a conversion request bit CINREQ, a control bit CIREN for selecting the cancel inject repeat feature, a control bit field (EMUX) for external multiplexer settings, a control bit RES for selecting the resolution of the ADC, and the channel number CHNRIN to be converted.

Page 8-18

The beginning "On a timer overflow" of the last sentence in the paragraph below Figure 8-3 must be replaced by "If the timer = 0".

Page 8-31

The formula for f_{ANA} in the middle of the page is wrong. The correct formula is:

$$f_{ANA} = \frac{f_{BC}}{CPS + 3} = \frac{1}{CPS + 3} \times \frac{f_{DIV}}{CTC + 1}$$

Page 8-34

The first formula on this page	"$V_{AREF}[0] \leq V_{DDA} + 0.1V$; $V_{DDA} \leq 5V$"
should be replaced by	"$V_{AREF}[0] \leq V_{DDM} + 0.05V$; $V_{DDM} \leq 5V$"
Further on the bottom the relation	"$0\ V \leq V_{AREF} \leq V_{DDM} + 0.1\ V$"
should be corrected into	"$0\ V \leq V_{AREF} \leq V_{DDM} + 0.05\ V$"

At the bottom of this page, the following two additional notes should be added:

Note: Is is not recommended in general to set V_{AREF} below 50% of V_{DDM}.

Note: The analog input voltages V_{AIN} must be in the range between V_{AGND} and the selected V_{AREF}.

Page 8-41

The 2nd sentence in section "8.1.8.3 Timing of external Multiplexer" is extended:

"Therefore, the information to drive an external multiplexer is available one f_{ADC} clock cycle before the sample time begins".

Page 8-56 and 8-57

The register long name of MSS0, MSS1, and SRNP in Table 8-13 must be corrected:

– MSS0 = "Module Service Request Status Register 0"
– MSS0 = "Module Service Request Status Register 1"
– SRNP = "Service Request Node Pointer Register"

Page 8-58

Bit field LCC of all ADC0/ADC1 CHCONn registers must be corrected in the following way:

LCC	[22:20]	rw	**Limit Check Control** 000_B Neither limit check is performed nor a service request is generated on write of the conversion result to bit field STAT.RESULT. 001_B Generate service request if conversion result is **not** in area I. 010_B Generate service request if conversion result is **not** in area II. 011_B Generate service request if conversion result is **not** in area III. 100_B Generate s service request on write of conversion result to bit field STAT.RESULT. 101_B Generate a service request result if conversion result is in area I. 110_B Generate a service request result if conversion result is in area II. 111_B Generate a service request result if conversion result is in area III.

Page 8-92

Bit field TOS of all ADC0 and ADC1 SRC registers must be corrected according the description on **Page 14**.

4 Data Sheet

Page 66

The operating condition parameter “Digital supply voltage” must be extended by two notes describing the V_{DD} overshoot conditions for class A and class B/C power supplies.

Note to be added for V_{DDP813}:

– Voltage overshoot to 6.5 V is permissible, provided that the pulse duration is less than 100 µs and the cumulated summary of the pulses does not exceed 1 hour.

Note to be added for V_{DD} and V_{DDOSC}:

– Voltage overshoot to 4 V is permissible, provided that the pulse duration is less than 100 µs and the cumulated summary of the pulses does not exceed 1 hour.

Page 68

The V_{IL}/V_{IH} TTL test condition is not applicable for $\overline{\text{HDRST}}$ and BYPASS. These pins are only tested with CMOS levels. An additional note is added in the corresponding row.

Pins CFG[3:0] are only tested with TTL input voltage test conditions (valid during reset).

The two rows of the table below shows the additional two notes in the red marked table cells (note 1) and 2)).

Class A Pins (V_{DDP813} = 3.0 to 5.25 V)

Input low voltage5)	V_{IL}	SR	-0.5	0.8	V	V_{DDP813} = 4.5 to 5.25 V (TTL)1)
				0.43 × V_{DDP813}	V	V_{DDP813} = 4.5 to 5.25 V (CMOS)2)
				0.2 × V_{DDP813}	V	V_{DDP813} = 3.0 to 4.49 V (CMOS)2)
Input high voltage5)	V_{IL}	SR	2.0	V_{DDP813} + 0.5	V	V_{DDP813} = 4.5 to 5.25 V (TTL)1)
			0.73 × V_{DDP813}		V	V_{DDP813} = 3.0 to 5.25 V (CMOS)2)

1) This test condition is not applicable for pins $\overline{\text{HDRST}}$ and BYPASS.

2) This test condition is not applicable for pins CFG[3:0]. The functionality of these pins can only be tested with TTL input voltage levels.

Page 68, 69

The pull-up/pull-down current spec must be corrected and completed for Class A and Class B pins. Note that also an additional footnote must be added.

Correction for Class A pins (at the bottom of Page 68):

Pull-up current[1)]	$\lvert I_{PUH}\rvert$ CC	–	10	µA	$V_{OUT} = V_{DDP813}$ - 0.02 V
	$\lvert I_{PUL}\rvert$ CC	120	600	µA	$V_{OUT} = 0.5 \times V_{DDP813}$
Pull-down current[1)]	$\lvert I_{PDL}\rvert$ CC	–	10	µA	V_{OUT} = 0.02 V
	$\lvert I_{PDH}\rvert$ CC	120	700	µA	$V_{OUT} = 0.5 \times V_{DDP813}$

1) The two pull-up/pull-down current test conditions for V_{OUT} cover the curves as shown in **Figure 22** and **Figure 23**. All pull-up/pull-down currents are given as absolute values.

Correction for Class B pins (in the middle of Page 69):

Pull-up current[1)]	$\lvert I_{PUH}\rvert$ CC	–	10	µA	$V_{OUT} = V_{DDP05}$ - 0.02 V
	$\lvert I_{PUL}\rvert$ CC	50	250	µA	$V_{OUT} = 0.5 \times V_{DDP05}$
Pull-down current[1)]	$\lvert I_{PDL}\rvert$ CC	–	10	µA	V_{OUT} = 0.02 V
	$\lvert I_{PDH}\rvert$ CC	40	300	µA	$V_{OUT} = 0.5 \times V_{DDP05}$

1) The two pull-up/pull-down current test conditions for V_{OUT} cover the curves as shown in **Figure 22** and **Figure 23**. All pull-up/pull-down currents are given as absolute values.

Page 77

Note [3)] is also valid for test condition “Sum of I_{DDS}“.

Page 82

Caused by the correction of Figure 31 on page 83, the last paragraph must be updated as follows: “Figure 31 gives an example for typical jitter curves with K = 4 @40 MHz, K = 6 @33 MHz, and K = 8@20/25 MHz.“

Page 83

Figure 31 must be corrected as shown below.

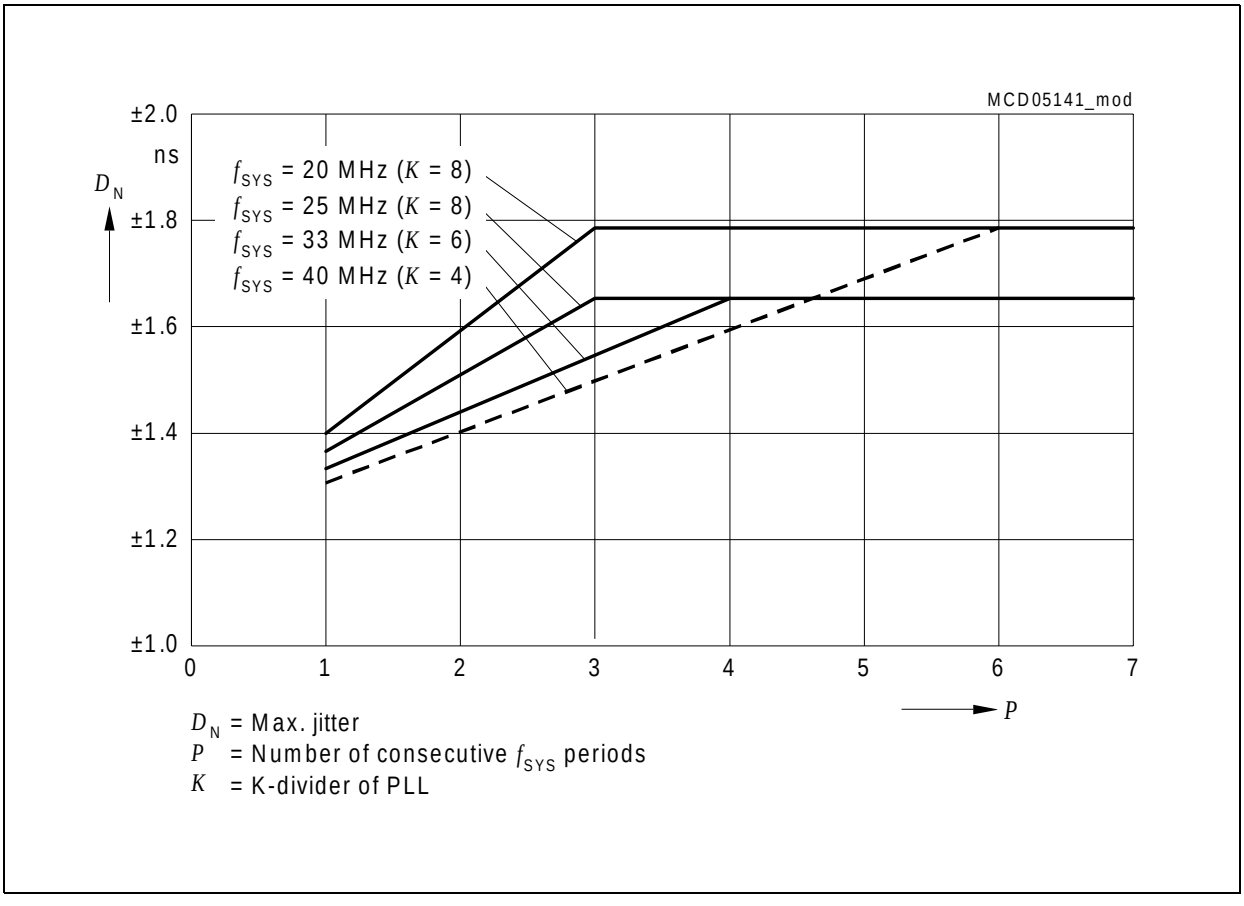


Figure 31 Approximated Maximum Accumulated PLL Jitter for Typical System Clock Frequencies f_{SYS}

Page 90

AC parameter t_{30} min (output delay from CLKIN rising edge) is **2 ns** instead of 0 ns.

AC parameter t_{32} min (data hold from CLKIN rising edge) is **2 ns** instead of 3 ns.

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