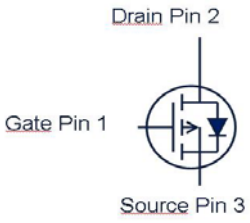
SIPMOS® Power-Transistor

Features

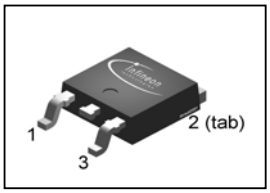
- P-Channel
- Enhancement mode
- Logic level
- Avalanche rated
- Pb-free lead plating; RoHS compliant
- ° Qualified according to AEC Q101

Product Summary

V_{DS}	-100	V
$R_{DS(on),max}$	850	mΩ
I_D	-4.2	A



PG-TO-252-3



Type	Package	Marking	Lead free	Packing	Tape and reel information
SPD04P10PL G	PG-TO252-3	04P10PL	Yes	Non dry	1000 pcs / reel

Maximum ratings, at T_j=25 °C, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
			steady state	
Continuous drain current	I_D	T_C=25 °C	-4.2	A
		T_C=100 °C	3.0	
Pulsed drain current	$I_{D,pulse}$	T_C=25 °C	-16.8	
Avalanche energy, single pulse	E_{AS}	I_D=-4.2 A, R_{GS}=25 Ω	57	mJ
Gate source voltage	V_{GS}		±20	V
Power dissipation	P_{tot}	T_C=25 °C	38	W
Operating and storage temperature	T_j, T_{stg}		-55 ... 175	°C
ESD class		JESD22-A114-HBM	1A (250 V to 500 V)	
Soldering temperature			260 °C	
IEC climatic category; DIN IEC 68-1			55/175/56	

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Thermal characteristics						
Thermal resistance, junction - soldering point	R_{thJC}		-	-	3.9	K/W
Thermal resistance, junction - ambient	R_{thJA}	minimal footprint, steady state	-	-	75	
		6 cm^2 cooling area[1)], steady state	-	-	50	
Electrical characteristics, at T_j=25 °C, unless otherwise specified						
Static characteristics						
Drain-source breakdown voltage	$V_{(BR)DSS}$	V_{GS}=0 V, I_D=-250 mA	-100	-	-	V
Gate threshold voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=-380 µA	-1	-1.5	-2	
Zero gate voltage drain current	I_{DSS}	V_{DS}=-100 V, V_{GS}=0 V, T_j=25 °C	-	-0.1	-1	µA
		V_{DS}=-100 V, V_{GS}=0 V, T_j=150 °C	-	-10	-100	
Gate-source leakage current	I_{GSS}	V_{GS}=-20 V, V_{DS}=0 V	-	-10	-100	nA
Drain-source on-state resistance	$R_{DS(on)}$	V_{GS}=-4.5 V, I_D=-2.75 A	-	787	1050	mΩ
		V_{GS}=-10 V, I_D=-3.0 A	-	550	850	
Transconductance	g_{fs}	$\|V_{DS}\|>2\|I_D\|R_{DS(on)max}$, I_D=-3.0 A	1.5	3.0	-	S

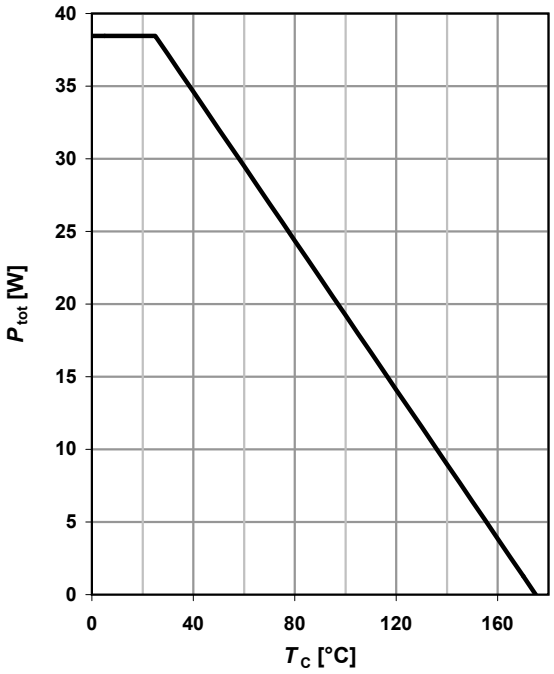
[1)] Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm^2 (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Dynamic characteristics						
Input capacitance	C_{iss}	V_{GS}=0 V, V_{DS}=-25 V, f=1 MHz	-	280	372	pF
Output capacitance	C_{oss}		-	70	94	
Reverse transfer capacitance	C_{rss}		-	34	51	
Turn-on delay time	$t_{d(on)}$	V_{DD}=-50 V, V_{GS}=-10 V, I_D=-4.2 A, R_G=6 Ω	-	4.6	6.9	ns
Rise time	t_r		-	5.7	8.6	
Turn-off delay time	$t_{d(off)}$		-	18	27	
Fall time	t_f		-	5.0	7.5	
Gate Charge Characteristics[2)]						
Gate to source charge	Q_{gs}	V_{DD}=-80 V, I_D=-4.2 A, V_{GS}=0 to -10 V	-	1.1	1.5	nC
Gate to drain charge	Q_{gd}		-	4.6	6.9	
Gate charge total	Q_g		-	12	16	
Gate plateau voltage	$V_{plateau}$		-	4.1	-	V
Reverse Diode						
Diode continuous forward current	I_S	T_C=25 °C	-	-	-4.2	A
Diode pulse current	$I_{S,pulse}$		-	-	16.8	
Diode forward voltage	V_{SD}	V_{GS}=0 V, I_F=-4.2 A, T_j=25 °C	-	0.94	1.2	V
Reverse recovery time	t_{rr}	V_R=50 V, I_F=$\|I_S\|$, di_F/dt=100 A/µs	-	68	85	ns
Reverse recovery charge	Q_{rr}		-	178	223	nC

[2)] See figure 16 for gate charge parameter definition

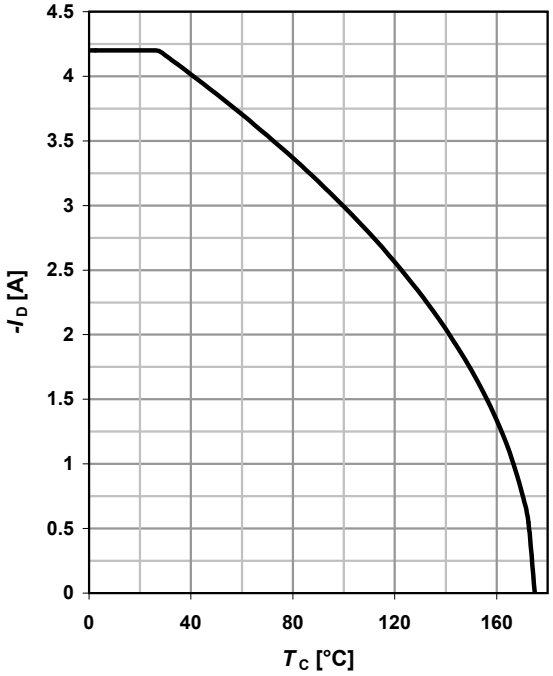
1 Power dissipation

$P_{tot}=f(T_C)$



2 Drain current

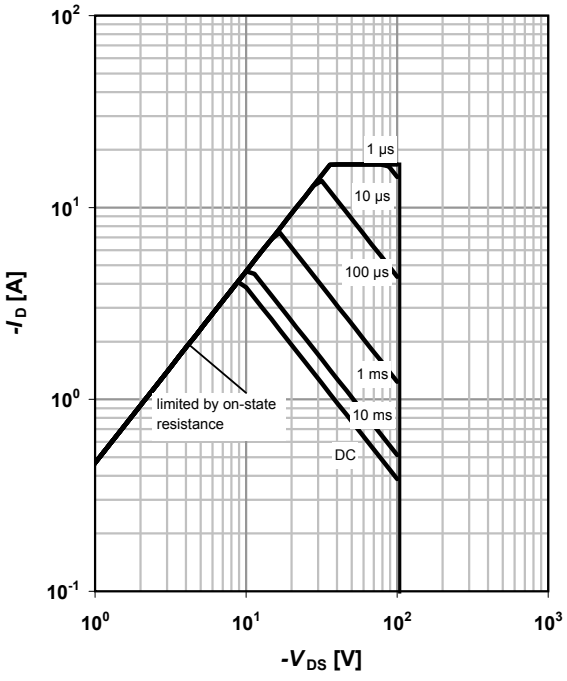
$I_D=f(T_C)$; $|V_{GS}|\geq 10$ V



3 Safe operating area

$I_D=f(V_{DS})$; $T_C=25$ °C; $D=0$

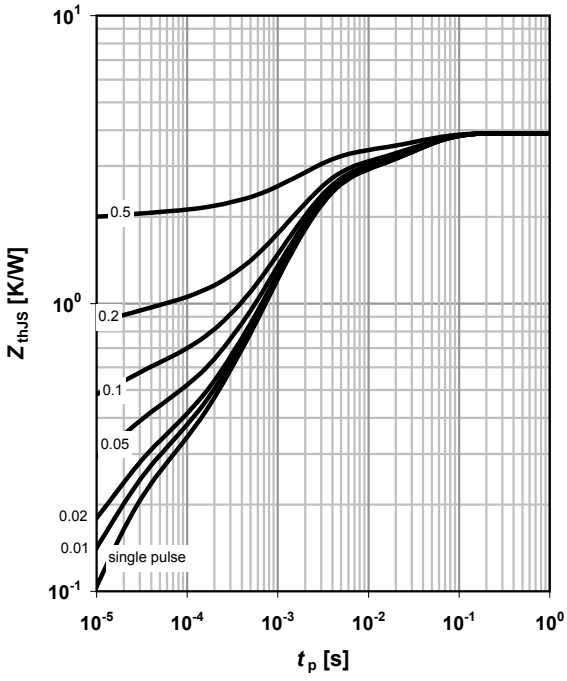
parameter: t_p



4 Max. transient thermal impedance

$Z_{thJC}=f(t_p)$

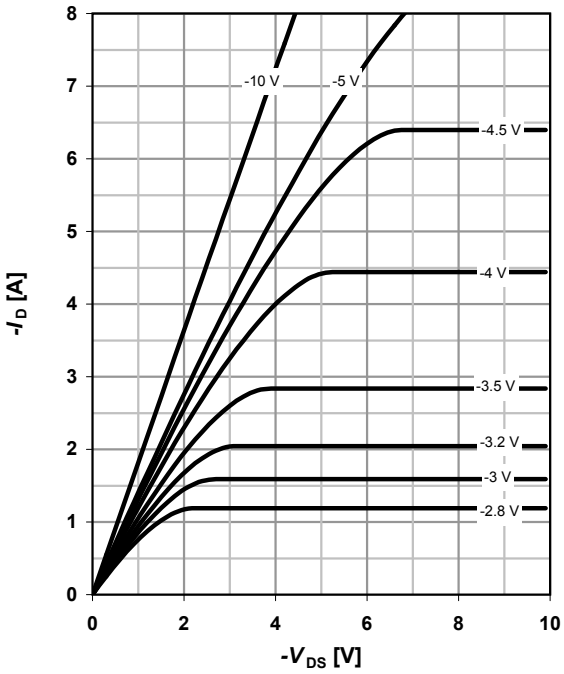
parameter: $D=t_p/T$



5 Typ. output characteristics

I_D=f(V_{DS}); T_j=25 °C

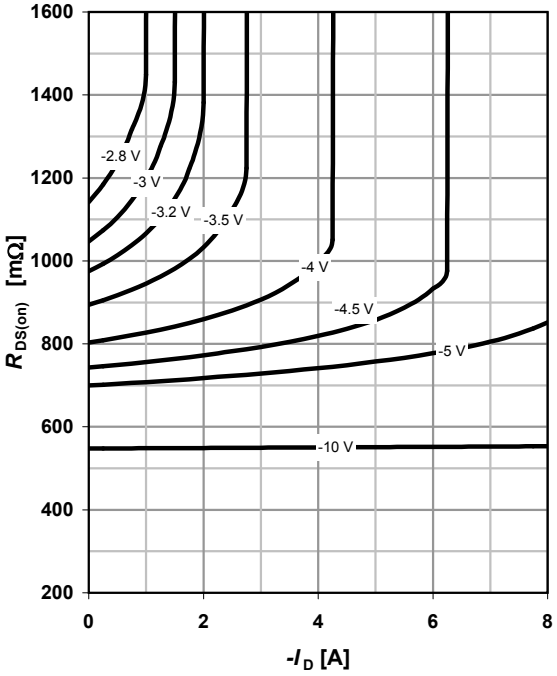
parameter: V_{GS}



6 Typ. drain-source on resistance

$R_{DS(on)}$=f(I_D); T_j=25 °C

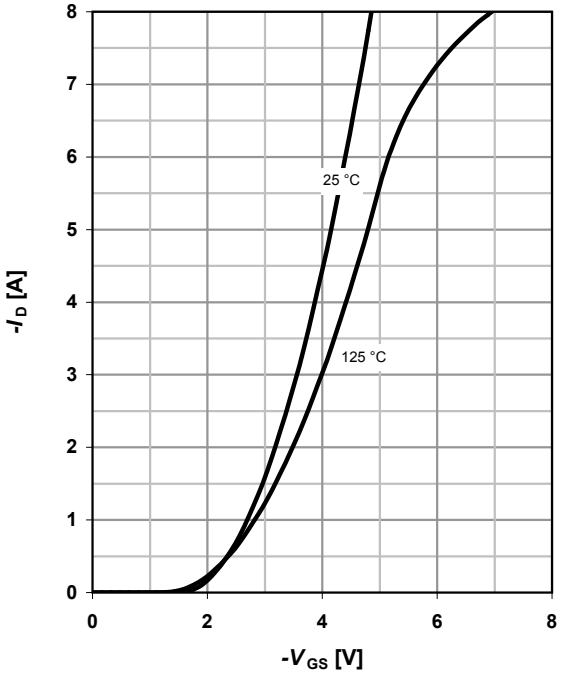
parameter: V_{GS}



7 Typ. transfer characteristics

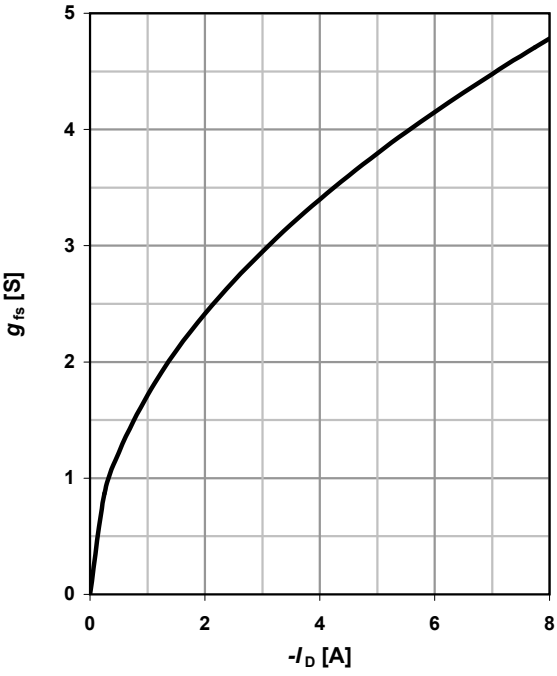
I_D=f(V_{GS}); $|V_{DS}|>2|I_D|R_{DS(on)max}$

parameter: T_j



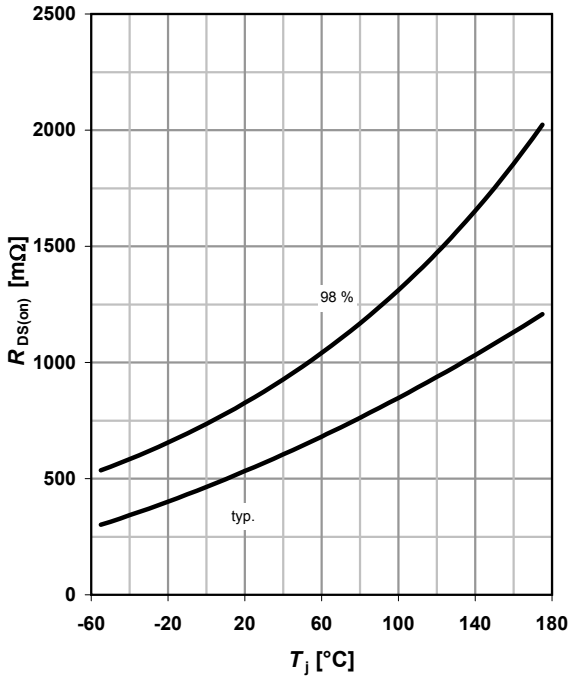
8 Typ. forward transconductance

g_{fs}=f(I_D); T_j=25 °C



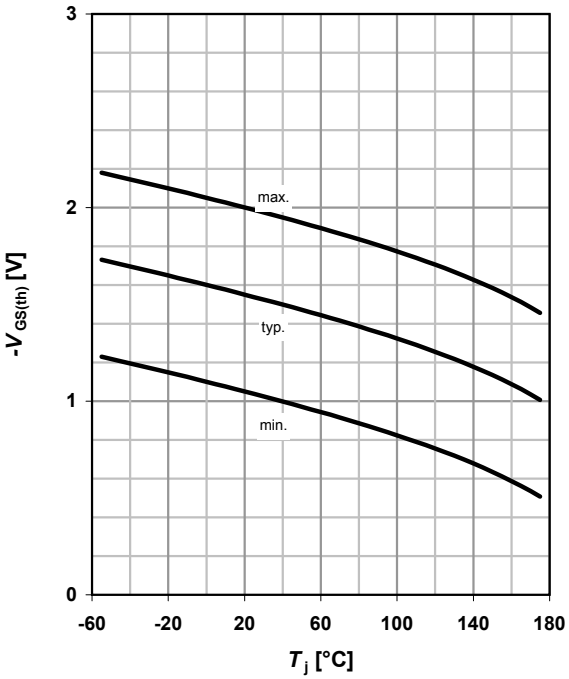
9 Drain-source on-state resistance

$R_{DS(on)}$=f(T_j); I_D=-3 A; V_{GS}=-10 V



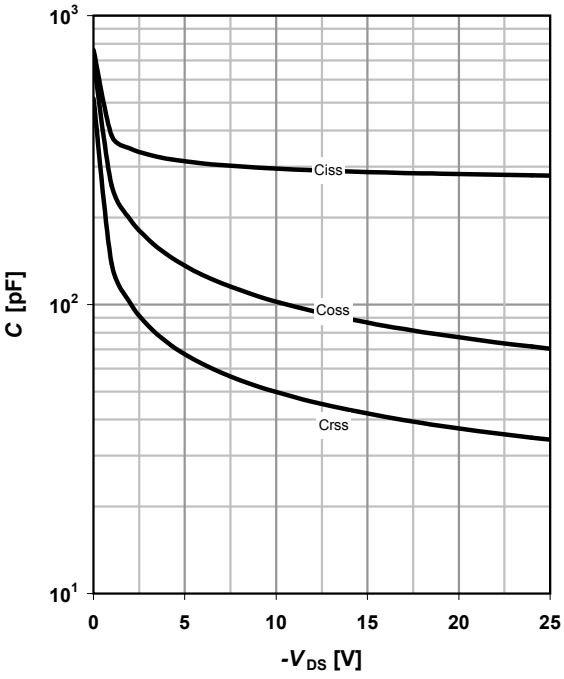
10 Typ. gate threshold voltage

$V_{GS(th)}$=f(T_j); V_{GS}=V_{DS}; I_D=-380 µA



11 Typ. capacitances

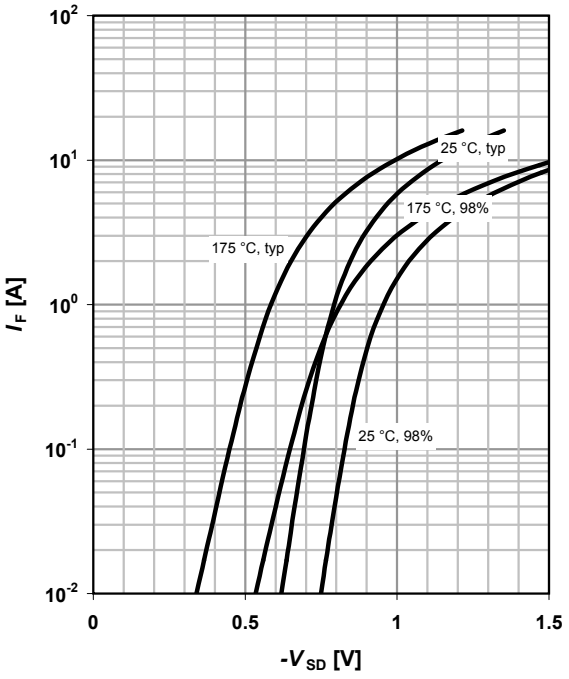
C=f(V_{DS}); V_{GS}=0 V; f=1 MHz



12 Forward characteristics of reverse diode

I_F=f(V_{SD})

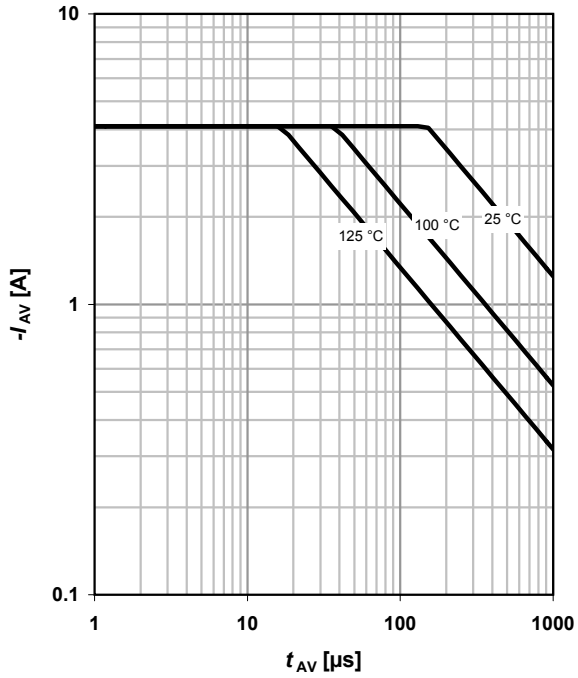
parameter: T_j



13 Avalanche characteristics

I_{AS}=f(t_{AV}); R_{GS}=25 Ω

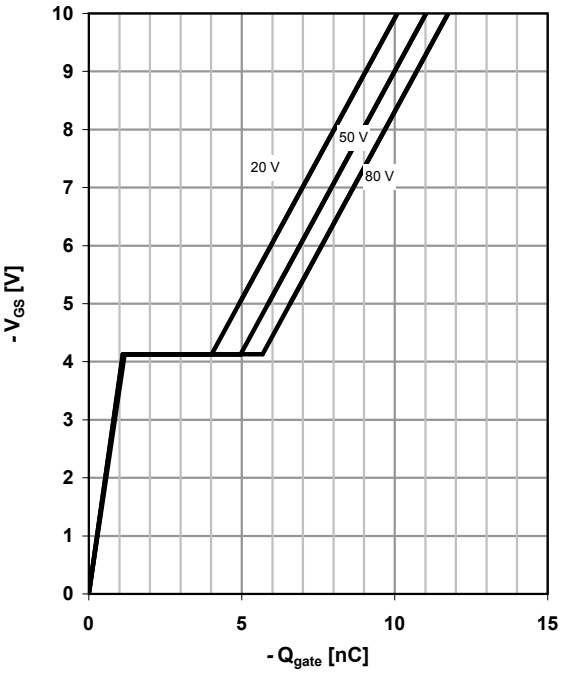
parameter: $T_{j(start)}$



14 Typ. gate charge

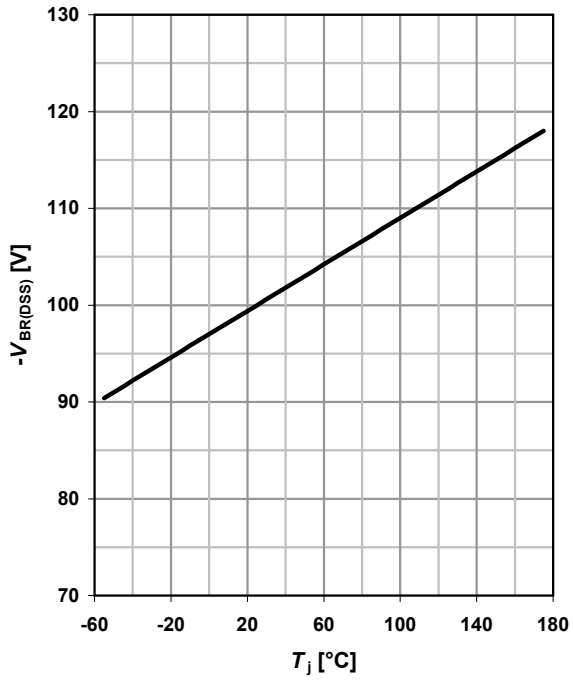
V_{GS}=f(Q_{gate}); I_D=-4.2 A pulsed

parameter: V_{DD}

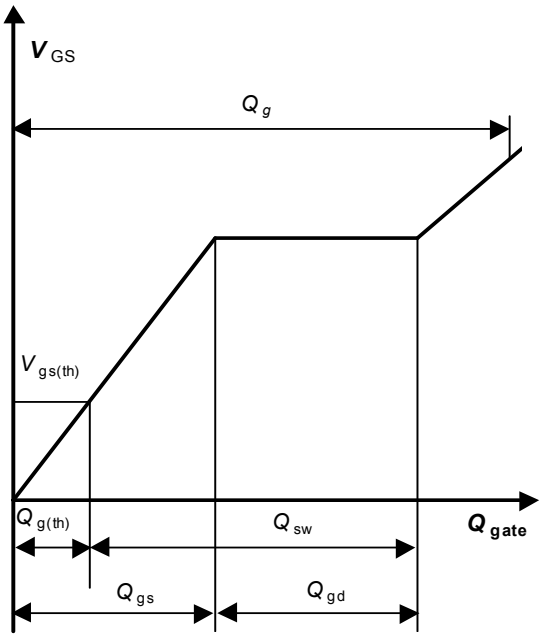


15 Drain-source breakdown voltage

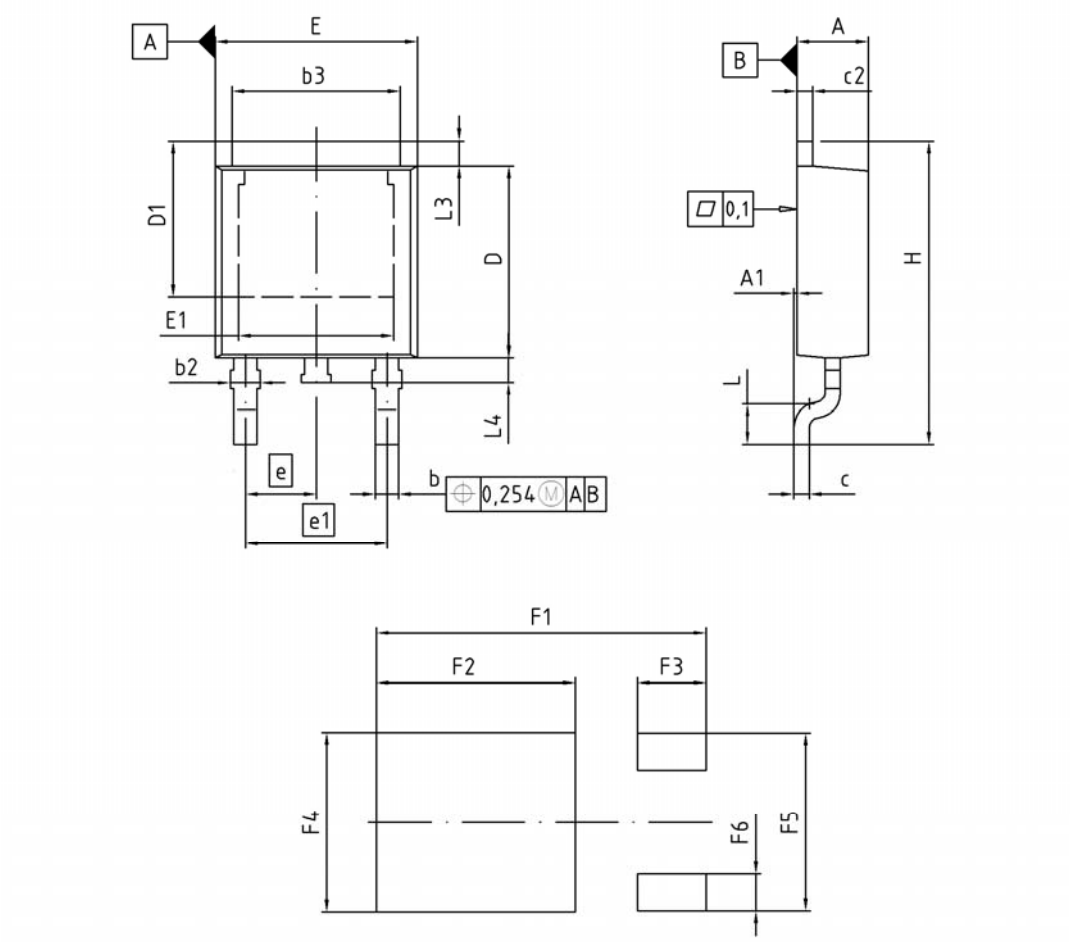
$V_{BR(DSS)}$=f(T_j); I_D=-250 µA



16 Gate charge waveforms



Package Outline: PG-TO-252-3



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.16	2.41	0.085	0.095
A1	0.00	0.15	0.000	0.006
b	0.64	0.89	0.025	0.035
b2	0.65	1.15	0.026	0.045
b3	5.00	5.50	0.197	0.217
c	0.46	0.60	0.018	0.024
c2	0.46	0.98	0.018	0.039
D	5.97	6.22	0.235	0.245
D1	5.02	5.84	0.198	0.230
E	6.40	6.73	0.252	0.265
E1	4.70	5.21	0.185	0.205
e	2.29		0.090	
e1	4.57		0.180	
N	3		3	
H	9.40	10.48	0.370	0.413
L	1.18	1.70	0.046	0.067
L3	0.90	1.25	0.035	0.049
L4	0.51	1.00	0.020	0.039
F1	10.50	10.70	0.413	0.421
F2	6.30	6.50	0.248	0.256
F3	2.10	2.30	0.083	0.091
F4	5.70	5.90	0.224	0.232
F5	5.66	5.86	0.223	0.231
F6	1.10	1.30	0.043	0.051

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