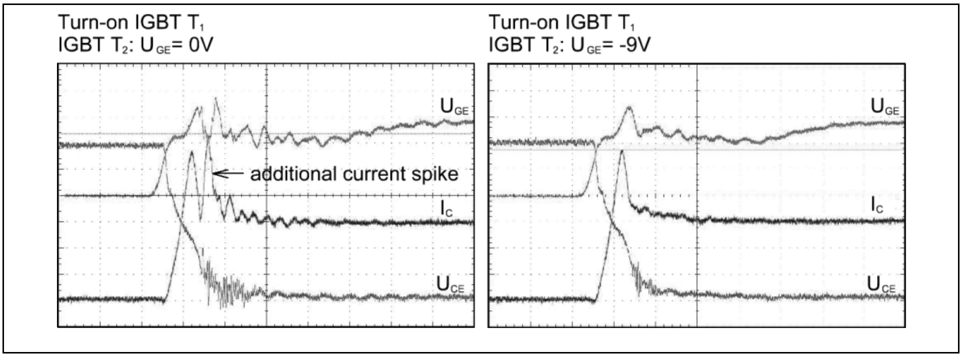

Fig. 7.1 Parasitic turn-on for U_{GE} = 0V compared with U_{GE} = -9V

Fig. 7.1 exemplifies the process of parasitic turn-on in a measurement of the half-bridge test configuration according to Fig. 3.9 The left picture shows clearly two collector current peaks for IGBT T_1. The first current peak is caused by the reverse recovery current of diode D_2, whilst the brief turn-on of IGBT T_2 causes the second current peak with a duration of approximately 50ns[4]. This additional current pulse does not pose a risk directly for the power semiconductor. However, the extra losses in the IGBT may lead to a critical temperature rise and a reduction of the lifetime. Further, oscillations are generated which may cause disruptions in the control electronics of the driver stage or the controller. Different countermeasures such as the operation with a negative voltage at the gate of IGBT T_2 will stop the parasitic turn-on under these conditions[5].

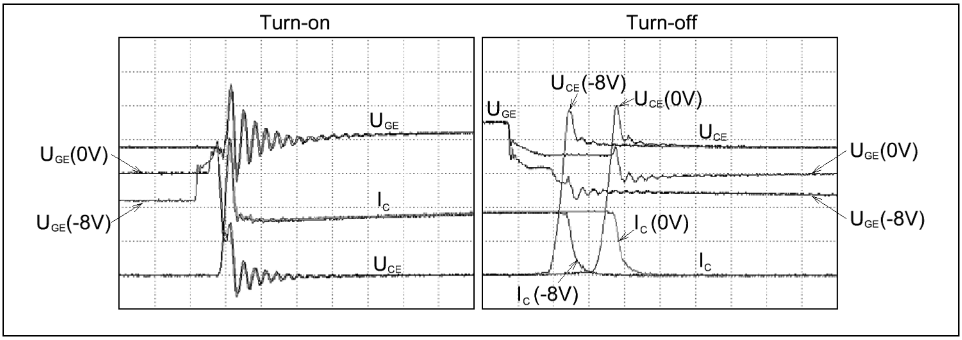

Fig. 7.2 Dependency of the IGBT switching behaviour on the control voltage U_{GE}[6]

Another effect which occurs when turning off with voltages in the range of 0V to -15V is the change of the switching times. Exemplified is this in Fig. 7.2 when turning on and off a 1.2kV IGBT with a gate voltage of 0V/15V and -9V/15V. The turn-on process with 0V/15V compared to a gate voltage of -9V/15V shows a delay of approx. 200ns in this

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[4] Timebase here is 100ns per division.

[5] IGBT T_1 is still turned on with a gate voltage of 0/15V. In a real application, of course, both IGBTs are to be operated with the same gate voltages – in this example -9V/15V.

[6] During the turn-on process the trigger point of the oscilloscope was set to the collector current I_C, while during the turn-off it depended on the gate voltage U_{GE}. The timebase is 500ns per division.