# Recommendations for Printed Circuit Board Assembly of Infineon QFP Packages

## Additional Information

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# 1 Package Description

**P**lastic **G**reen – **M**etric/ **T**hin/ **L**ow-profile **Q**uad **F**lat **P**ackages (PG-M/T/LQFPs) are plastic encapsulated leadframe packages (Figure 1). Some of them have an exposed pad on the bottom of the package, which is created by an appropriate down-set. These are called exposed die pad QFPs. The die pad is typically also soldered to the Printed Circuit Board (PCB) to provide the primary heat removal path as well as excellent electrical grounding to the PCB. There are several modifications with various pitches from 0.4 mm to 0.8 mm, numbers of leads ranging from 44 to 256, and various outline dimensions. **"G"** denotes "green" QFP packages, which have Pb-free package materials and are RoHS compliant**.**

**Features**

- Optimized electrical performance
- Enhanced thermal performance through exposed die pad structure (package-specific; details can be found in Infineon's package data base at www.infineon.com/packages)
- Gullwing leads and exposed die pad are plated with Sn or NiPd (AuAg-alloy)
- Thin packages (low profile)
- Package outline meets JEDEC MS-026 standard

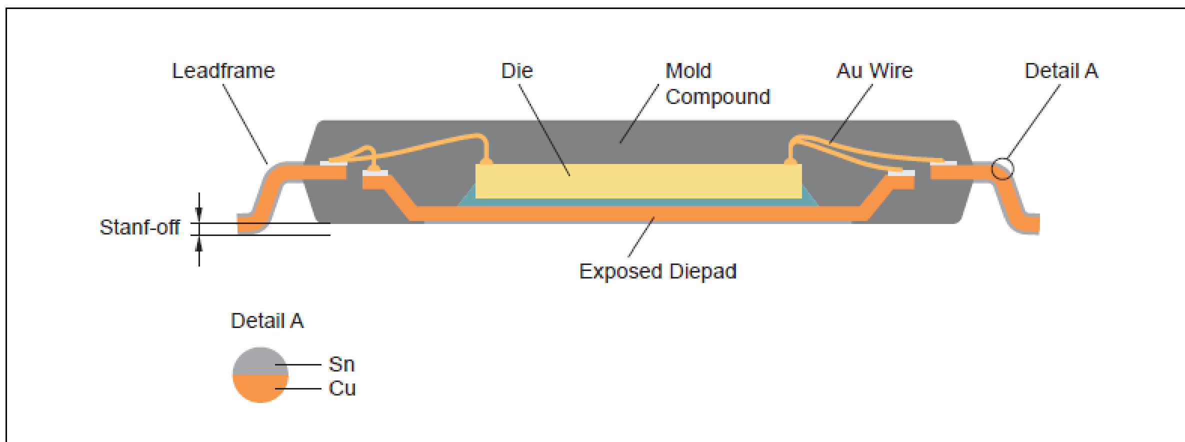


**Figure 1 PG-LQFP with exposed die pad and external Sn-plating**

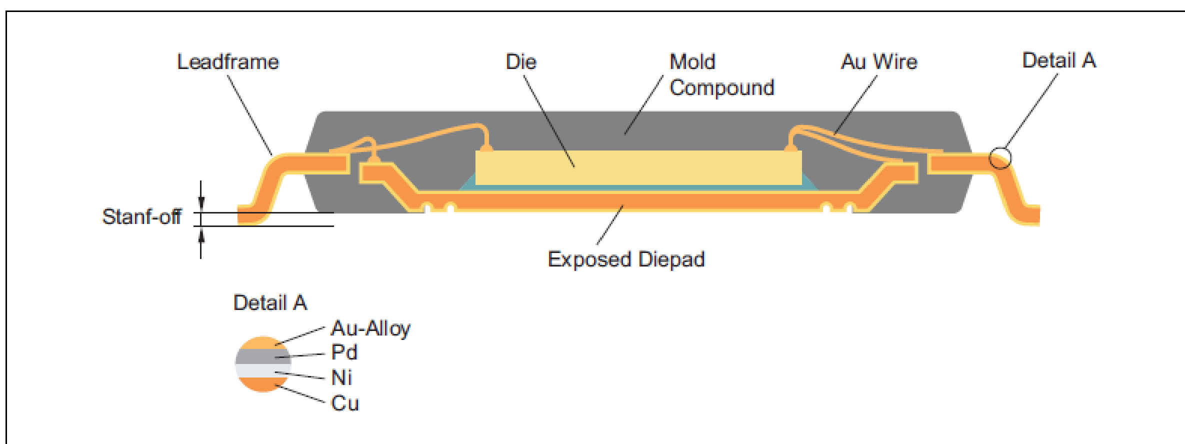


**Figure 2 PG-LQFP with exposed die pad and overall NiPd(Au-Ag-alloy)-plating**

Semiconductor devices are sensitive to excessive electrostatic discharges, moisture, mechanical handling, and contamination. Therefore, they require specific precautionary measures during transport, storage, handling, and processing. For details, please refer to the Package Handling section in General Recommendations for Assembly of Infineon Packages (available at www.infineon.com/packages).

# 2 Printed Circuit Board (PCB)

## 2.1 General remarks

PCB design and construction are key factors for achieving a high board-assembly yield and sufficient reliability. Examples are PCB pad designs for the leads and for the large central exposed pad, which is generally recommended to be soldered to the PCB for optimum thermal, electrical, and board-level reliability and performance. In addition, via design and board finish must be considered.

We want to emphasize that this document is just a guideline to support our customers in board design. Further studies at the customer's facilities may be necessary for optimization in order to take into account the actual PCB manufacturer's capability, the customer's SMT process, and product specific requirements.

## 2.2 PCB Pad Design

The interconnect solder joint-to-board is influenced by:

- General pad technology (Solder Mask Defined and Non-Solder Mask Defined short SMD and NSMD)
- Specific pad dimensions
- Pad finish (also called metallisation or final plating)
- Via layout and technology

Further information can be found in the Printed Circuit Board section in General Recommendations for Assembly of Infineon Packages (available at www.infineon.com\packages).

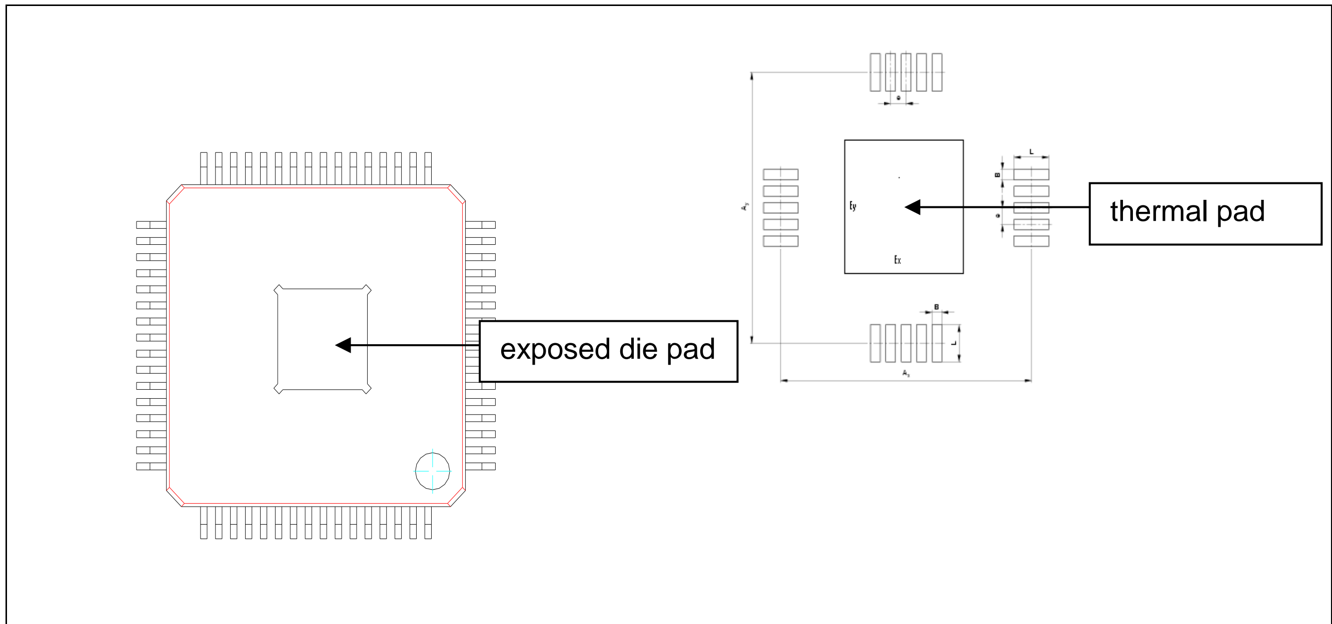


**Figure 3. Bottom view of PG-LQFP-64 (incl. die pad)**

**Figure 4. Schematic drawing of PCB pad design recommendation**

When designing the PCB pad for the lead lands, you will need to consider the footprint of the respective package. Footprint information can be found for each package at www.infineon.com\packages.

## 2.3 Vias in thermal pad

Some products and applications require that the thermal pad is connected to inner copper layers of the PCB by vias. One reason may be to maximize the electrical performance especially for products operating at high frequencies. Another reason may be the optimization of the thermal performance for products having high thermal power dissipation. In these cases, plated through-hole vias that are (if possible fully) connected to inner and/or bottom copper planes of the board will help to distribute the heat into the board area. This heat penetrates from the chip over the package die pad and the solder joint to the thermal pad on the board.

The number of vias is application-specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed.

A typical diameter for such thermal vias is 0.2-0.4 mm. The number of vias in the thermal pad depends on the thermal requirements of the end product, the power consumption of the product, the application, and the construction of the PCB. However, an array of thermal vias with pitch 1.2-1.5 mm is a reasonable starting point for most products and applications. This pitch may be modified for further optimization.

If the vias remain open during board manufacturing, solder may flow into the vias during LQFP board assembly (“solder wicking”). This could create large voids in the thermal solder joint under the die pad, and/or cause solder to protrude from the other side of the board, which may disturb a second solder paste printing process on this other board side. If necessary, solder wicking can be avoided in 2 ways.

The recommended solution is to plug the vias (filling them with epoxy) with additional plating, that means no stand-off, and therefore no limitations regarding solder paste.

Another option is tenting the vias with solder mask (e.g. with dry-film solder mask). Via tenting should be done from top, because with via tenting from the bottom side, the voiding rate is significantly higher. In this case, sufficient area must be available for good wettability of the exposed die pad. The solder mask diameter should be at least 0.1 mm larger than the via diameter.

Note: These recommendations are to be used as a guideline only.

# 3 Board Assembly

## 3.1 General remarks

Many factors in the board assembly process can affect assembly yield and board-level reliability. Examples are design and material of the stencil, the solder paste material, solder paste printing process, component placement, and reflow process. Further studies at the customer's facilities may be necessary for optimization in order to take into account the actual PCB, the customer's SMT equipment, and product-specific requirements.

## 3.2 Solder Stencil

The solder paste is applied onto the PCB metal pads by screen printing. The volume of the printed solder paste is determined by the stencil aperture and the stencil thickness. In most cases the thickness of a stencil has to be matched to the needs of all components on the PCB.

For a standard non-exposed die pad leadframe package, the stencil thickness depends only on lead pitch and coplanarity. However, the package standoff must also be considered for the exposed die pad packages. Thus for exposed die pad LQFPs of pitch 0.5 mm, 125-150 µm thick stencils are recommended. To ensure a uniform and high solder-paste transfer to the PCB, laser-cut (mostly made from stainless steel) and electroformed stencils (nickel) are preferred. Rounding the corners of the apertures (radius ~50 µm) can support good paste release.

The apertures for the lead solder joints should be the same size as the metal pads on the PCB (for recommendations, see package-specific recommendations at www.infineon.com\packages). The stencil in the thermal pad area should be segmented into smaller, multiple openings (see schematic example of Figure 5). One large opening would result in excessive solder volume under the LQFP die pad compared to the lead pads as well as significantly higher voiding rate and higher risk of solder balling.

In our tests we printed a total area of about 70-80% of the thermal pad with solder paste. With this procedure we achieved good results in board assembly yield and reliability. The resulting solder joint stand-off at the exposed die pad was typically in the range of 100 µm. The most appropriate way of segmenting depends on the number and location of vias (if present) and the solder resist layout on this thermal pad. In case of a regular thermal via matrix, the stencil openings should be arranged in areas between the vias. In our evaluations we typically have used opening sizes in the range of 0.6-1 mm$^2$, depending on via density and thermal pad size.

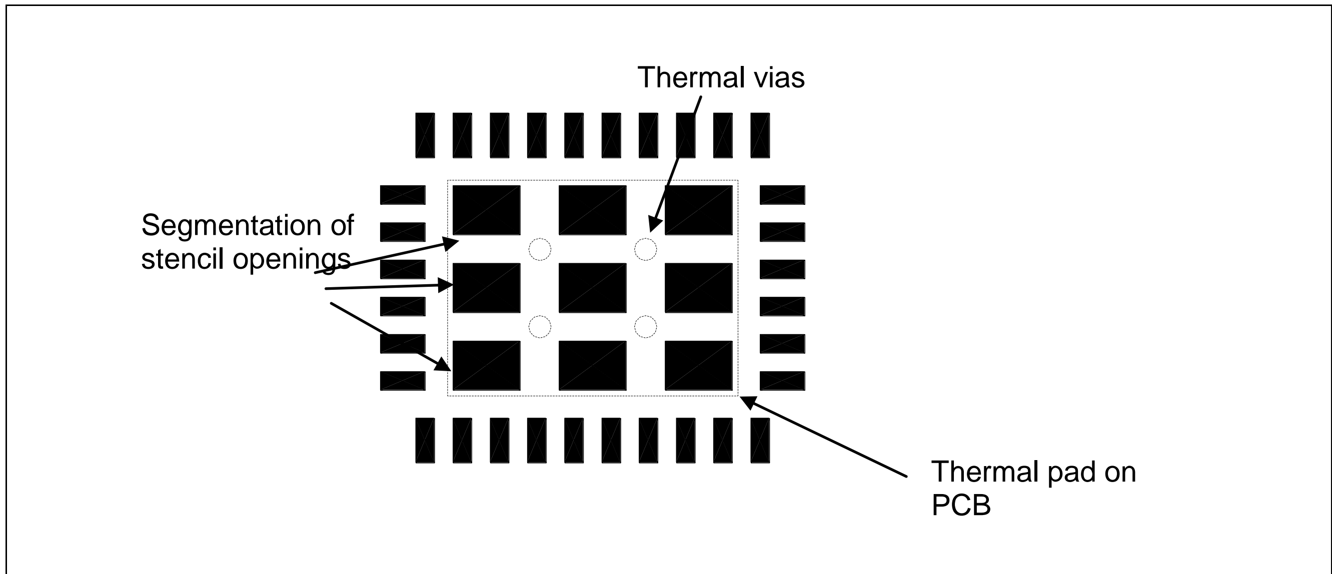


**Figure 5: Example of segmentation of stencil openings on thermal pad area of PCB.**

## 3.3 Solder Paste

Solder paste consists of solder alloy and a flux system. Normally the volume is about 50% alloy and 50% flux. In term of mass this means approx. 90 wt% alloy and 10 wt% flux system. One of the functions of the flux system is to remove the contamination from the contact partners (PCB finish/component lead finish) during the soldering process. The capability of removing contamination is given by the respective activation level.

Pb-free solder pastes contain so-called SAC alloys (typically 1-4% Ag and <1% Cu). A “no-clean” solder paste is preferred, because cleaning under soldered QFPs and exposed pad QFPs in particular is difficult. The paste must be suitable for printing the solder stencil aperture dimensions. A solder paste with powder size 3 (J-STD-006) or higher is recommended. Solder paste is sensitive to storage time, temperature, and humidity. Please follow the handling recommendations of the paste manufacturer.

## 3.4 Component Placement

Although the self-alignment effect due to the surface tension of the liquid solder will support the formation of reliable solder joints, exposed die pad QFPs in particular have to be placed accurately depending on their geometry. Manually positioning of the packages is not recommended.

Component placement accuracies of ±50 µm are obtained with modern automatic component placement machines using vision systems. With these systems both the PCB and the components are optically measured and the components are placed on the PCB at their programmed positions. The fiducials on the PCB are located either on the edge of the PCB for the entire PCB, or on individual mounting positions (local fiducials). They are detected by a vision system immediately before the mounting process. Recognition of the packages is performed by a special vision system, enabling the complete package to be centered correctly.

The maximum tolerable displacement of the components is 20% of the metal pad width on the PCB (for NSMD pads). Consequently, for QFPs with 0.5 mm lead pitch, the misalignment between the

device pad and the PCB pad has to be less than 50 µm to assure a robust mounting process. Generally this is achievable with a wide range of placement systems.

For details about factors influencing the component placement, please refer to the Mounting of SMDs section in the General Recommendations for Assembly of Infineon Packages (available at www.infineon.com\packages).

## 3.5 Soldering

Soldering determines the yield and quality of assembly fabrication to a very large extent. Generally standard soldering processes such as:

- Forced convection
- Vapor phase
- Infrared (with restrictions)

and typical temperature profiles are suitable for board assembly of QFPs.

Wave soldering an exposed-pad QFP is not possible because the package has to be attached to the PCB by SMD glue. In QFPs with exposed pad, this is not possible if the exposed pad is intended to be soldered to the PCB. Furthermore, wave soldering is only possible if the products in QFPs are qualified for wave soldering (passing the solder heat test). Generally wave soldering of QFPs is difficult because the leads have to be soldered at all four sides of the component. Using a 45° rotated layout is recommended to allow the solder to wet the leads more easily. Wave soldering of QFPs with lead pitches of 0.65 mm or smaller may lead to excessive bridging and therefore is not recommended.

During the reflow process, each solder joint has to be exposed to temperatures above the solder melting point (liquidus) for a sufficient time to get the optimum solder joint quality, whereas overheating the PCB with its components has to be avoided. Please refer to the bar code label on the packing for the maximum package body temperature. When using infrared ovens without convection, special care may be necessary to assure a sufficiently homogeneous temperature profile for all solder joints on the PCB, especially on large, complex boards with different thermal masses of the components. The recommended type of process is forced convection reflow. Nitrogen atmosphere can generally improve solder joint quality, but is normally not necessary for soldering SnPb metal alloys. Performing the Pb-free process with higher reflow temperatures in a nitrogen atmosphere may reduce oxidation and improve the solder joint quality.

Figure 6 shows a general forced-convection reflow profile suitable for soldering QFPs. Table 1**Error! Reference source not found.** shows an example of the key parameter of a reflow profile that can be used for the Pb-free alloys listed above.

For further details about the reflow profile (especially for Pb-containing solder pastes), please refer to the Mounting of SMDs section in General Recommendations for Assembly of Infineon Packages (available at www.infineon.com\packages).

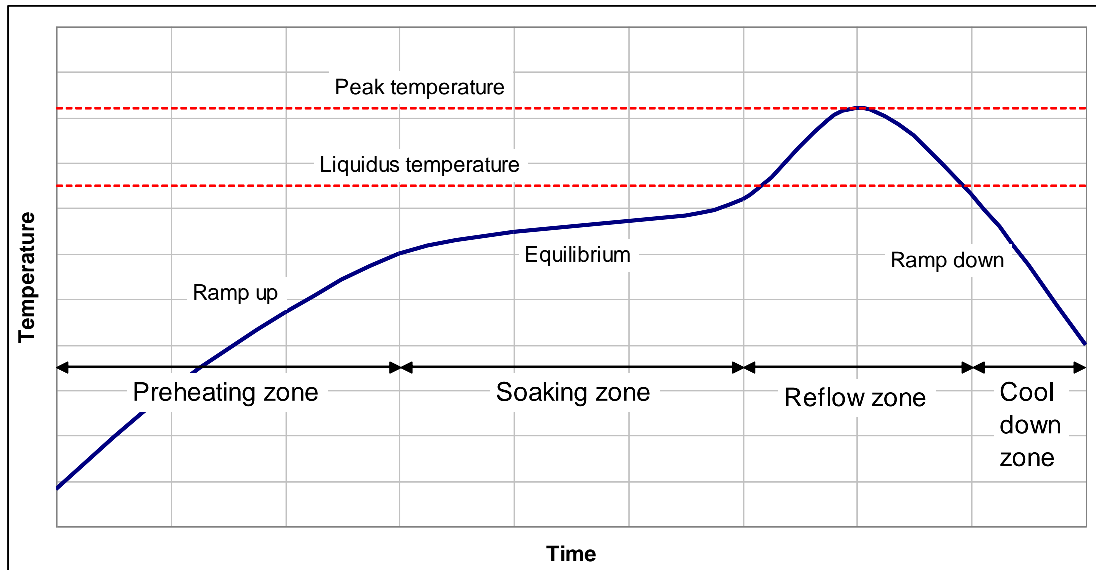


**Figure 6. General forced-convection reflow solder profile**

**Table 1: Example of the key data of a forced-convection reflow solder profile**

| Parameter | Minimum values | Typical values | Maximum values (acc. IPC/JEDEC J-STD-020) | Main influences |
|---|---|---|---|---|
| Preheating rate | 1.0 K/s | 2.5 K/s | 3.0 K/S | Flux system (solder paste) |
| Soaking temperature | 140-170°C | 140-170°C | 150-200°C | Flux system (solder paste) |
| Soaking time | 50 s | 80 s | 120 s | Flux system (solder paste) |
| Peak temperature | 230°C | 245°C | 260°C | Alloy*) (solder paste) |
| Reflow time above melting point (liquidus) | 40 s | 60 s | 150 s | Alloy*) (solder paste) |
| Cool-down rate | 1.0 K/s | 2.5 K/s | 8.0 K/s | |

*) e.g. SAC305 or comparable alloys have liquidus temperatures of 217 to 220°C

**Double-Sided Assembly**

LQFPs are generally suitable for mounting on double-sided PCBs. That means that in a first step, board assembly is done on one side of the PCB (including soldering). Afterwards the second side of the PCB is assembled.

If the solder-joint thickness is a critical dimension, please be aware that solder joints of components on the first side will be reflowed again in the second reflow step. In the reflow zone of the oven (i.e. where the solder is liquid), the components are only held by wetting forces from the molten solder. Gravity acting in the opposite direction will elongate the solder joints, unlike joints on the top side, where gravity forces the components nearer to the PCB surface. This shape will be frozen at temperatures below the melting point of solder and therefore result in a higher stand-off on the bottom side after the reflow process. Heavy vibrations in a reflow oven may cause devices to drop off the PCB.

# 4 Cleaning

After the reflow soldering process, some flux residues can be found around the solder joints. If a “no-clean” solder paste has been used for solder paste printing, the flux residues usually do not have to be removed after the soldering process. However, if the solder joints have to be cleaned, the cleaning method (e.g. ultrasonic, spray or vapor cleaning) and solution have to be selected while taking into account the kinds of packages to be cleaned, the flux used in the solder paste (rosin-based, water-soluble, etc.), and environmental and safety aspects. Even small residues of the cleaning solution must be removed/dried very thoroughly. Contact the solder paste or flux manufacturer for recommended cleaning solutions. Note: Exposed die pad LQFPs are capable of being cleaned at the leads, while cleaning of the die pad area is limited under the package body.

# 5 Inspection

**After component placement:**

A visual inspection after component placement can be done by microscope or Automatic Optical Inspection (AOI) in order to check if the mounting was done completely or if severe misplacements occurred. The orientation of the component can also be checked.

**After soldering:**

A simple visual inspection of the solder joints can be done by optical microscope.

The only visible areas are leads and leadframe areas that extend beyond the package body.

Figure 7 shows a QFP-like SMD lead with ideal wetting. For QFPs, the joint quality under leads should be assessed, especially under the exposed pad with x-ray and/or cross sections.

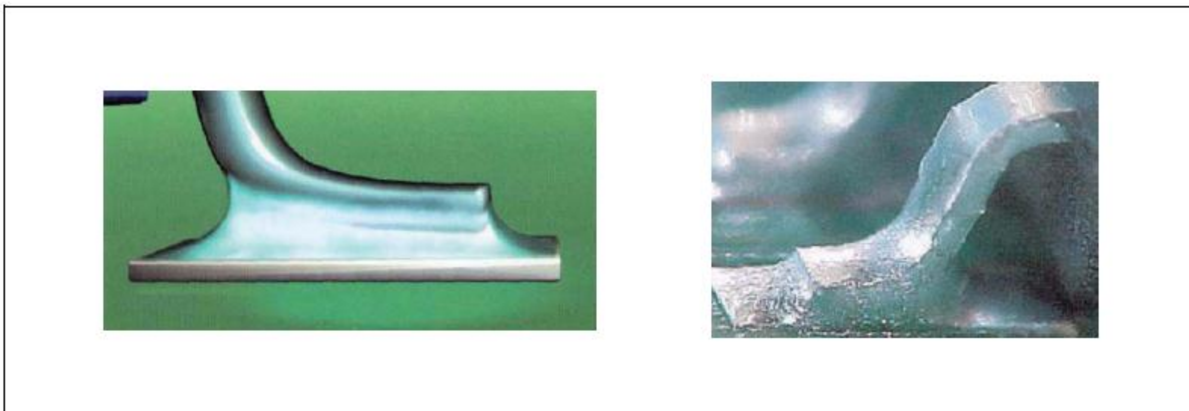

**Figure 7: Example of an ideally wetted SMD lead (source: IPC A-610)**

If exposed die pads are soldered, the only reliable inspection method for the whole solder joint is by X-ray.

An automated visual inspection of the solder joints with conventional AOI systems is limited to the outer solder joints. Please keep in mind that the non-wetting of the punched or sawn lead tip is not a criterion for rejection. For packages with exposed pads, the only reasonable method for efficient inline control is to use Automatic X-ray Inspection (AXI) systems. AXI systems are available as 2D and 3D solutions. They usually consist of an X-ray camera and the hardware and software needed for inspection, controlling, analyzing, and data transfer routines. These systems enable the user to reliably detect soldering defects such as poor soldering, bridging, voiding, and missing parts. For the acceptability of electronic assemblies, please refer also to the IPC-A-610 standard.

Cross-sectioning of a soldered package as well as dye penetrant analysis can serve as tools for sample monitoring only, because of their destructive character. Nonetheless, these analysis methods must be used during engineering of new products to get detailed information about the solder joint quality.

Pb-free solder joints look different from Pb-containing (e.g. SnPb) solder joints. Tin-lead solder joints typically have a bright and shiny surface. Pb-free (SnAgCu) solder joints typically do not have a bright surface. Pb-free solder joints are often dull and grainy. These surface properties are caused by the irregular solidification of the solder, as the solder alloys used are not exactly eutectic, unlike 63Sn37Pb solder alloy. This means that SnAgCu-solders do not have a melting point but a melting range of several degrees. Although lead-free solder joints have this dull surface, this does not mean that lead-free joints are of lower quality or weaker than the Pb-containing joints.

Also NiPd(Au-Ag-alloy)-plated leads and corresponding solder joints look different compared to wide spread Sn-plated.

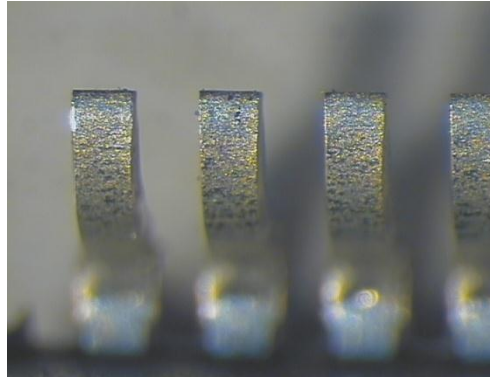

**Figure 8: NiPd(AuAg alloy) plated Gullwing lead**

Compared to Sn-plated pins, NiPd (AuAg alloy)-plated leads appear with a slight gold or yellow color on their surface. This appearance sometimes is confused with that of contaminated Sn-plated pins. This optical appearance pictured in Figure 8 is typical for NiPd (AuAg alloy)-plated leadframes and does not imply poor wettability.

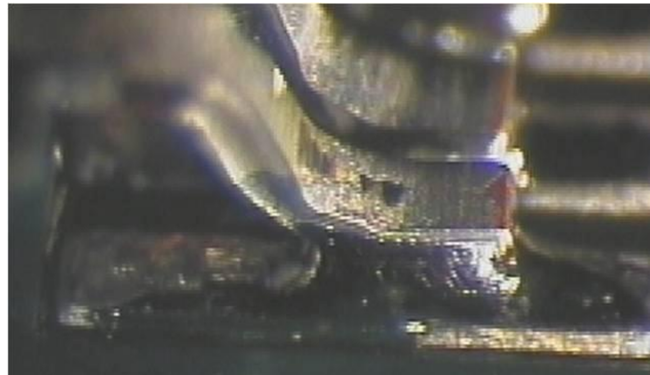

**Figure 9: Typical view of solder joints containing a NiPd(AuAg alloy) plated Gullwing lead**

Looking at a solder joint between a NiPd (AuAg alloy)-plated lead and a PCB (Figure 9), the wetted area at the pin is different compared to a solder joint containing an Sn-plated pin (Figure 7). This behavior is caused by the characteristics of the NiPd (AuAg alloy) which do not allow solder to flow into the pins' grooves. Investigations concerning soldering and durability of this kind of plating and corresponding solder joints have proven that the appearance shown in Figure 9 guarantees an equal reliability of the solder joints compared to Sn plating.

It is therefore necessary to teach the inspection staff what these Pb-free joints or NiPd (Au-Ag-alloy)-plated packages look like, and/or to adjust optical inspection systems to handle Pb-free solder joints or NiPd (Au-Ag-alloy)-plated packages.

# 6 Rework

If a defective component is detected after board assembly, the device can usually be removed and replaced by a new one. Due to possible damage while removing the component, a desoldered component should not be reused.

Desoldering the old component (if analysis afterwards is planned) and resoldering of the new component have to be done very thoroughly.

Single solder-joint repair of Power-SON packages is very difficult, if not impossible, and therefore not recommended at all.

The following restrictions have to be taken into account prior to and during rework process:

- Dry the PCB and components prior to rework. A proper drying procedure for SMD packages is described in the international standard IPC/JEDEC J-STD-033. Please also refer to the recommendations of your PCB manufacturer and take all specific needs of components, PCB, and other materials into account.
- Use tools that do not damage the component mechanically. Please note that mechanical forces need not lead necessarily to external damage, which could be detected more easily, but may cause internal damage and reduce the component reliability. The most gentle process is probably to use a handling system with a vacuum nozzle, and is therefore recommended. However, the impact of rework tools has to be assessed properly.
- Whatever heating system is used (hot air, infrared, hot plate, etc.), the applied temperature profile at the component must never exceed the maximum profile specified in the international standard IPC/JEDEC J-STD-020. Internal investigations have shown that in any case a recording of the temperature profile is needed.
- In general, more manual handling increases the effort for documentation, training, and monitoring of the rework process(es). Investigations have shown that if distance, time, and airflow are properly controlled, a hot-air temperature of 300°C can be used, for example, without violating the maximum allowed reflow profile. On the other hand, the same hot-air temperature setting was able to heat up the component to above 280°C, which exceeds the component's specification by far, if other process parameter were changed.
- If a desoldered component is supposed to be reused, please consider that components are qualified to withstand a maximum of three reflow cycles. In this specific case, two cycles are already applied during rework and only one is left for the board assembly.

For further information about tooling and process steps for rework, please refer to the Rework section in the General Recommendations for Assembly of Infineon Packages (available at www.infineon.com/packages).

# 7 List of references

IPC/EIA/JEDEC-J-STD-006 (Requirements for Electronic Grade Solder Alloys and Fluxed and Non-fluxed Solid Solders for Electronic Soldering Applications)

IPC/EIA/JEDEC-J-STD-001 (Requirements for Soldered Electrical and Electronic assemblies)

IPC A-610 (Acceptability of Electronic Assemblies)

IPC/EIA/JEDEC J-STD-002 (Solderability tests for Component Leads, Terminations, Lugs, Terminals and Wires)

IPC/JEDEC J-STD-033/-020 (Handling, Packing, Shipping and Use of Moisture/Reflow Sensitive Surface Mount devices)/(Moisture/reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices)

JESD22-B102 (Test Method for Solderability)

IEC 60068-2-58 (Test methods for solderability, resistance to dissolution of metallization and to soldering heat of surface mounting devices)

IPC 7351/7355 (Generic Requirements for Surface Mount Design and Land Pattern Standard)

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