A large, light blue, stylized graphic element consisting of a thick, curved line that forms a partial circle, with a small circle at its top end, resembling a stylized 'C' or a circuit path.

Recommendations for Printed Circuit Board Assembly of Infineon DSO and SSOP Packages

Additional Information

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1 Package Description

P(G)-DSOs (Plastic (Green) Dual Small Outline Packages) and P(G)-SSOP (Plastic (Green) Shrink Small Outline Packages) are leaded surface mount packages with gull wing lead form, where the leads are bent outwards at the tip. This bent lead tip area is the seating plane and the area bonded to the PCB.

P(G)-DSO and P(G)-SSOP packages are available in narrow, standard and wide package body width sizes.

P(G)-DSO and P(G)-SSOP packages are available in non-exposed pad (**Figure 1**) and exposed pad versions (**Figure 2**). P(G)-DSO packages additionally in heatslug versions (**Figure 3**). Exposed pad and heatslug packages for thermal performance improvement has the center leadframe area exposed to the bottom side of the package or with reverse lead bending to the top side of the package. Exposed pads or heatslugs at the bottom can be soldered to the PCB and the majority of the heat is dissipated through this region. Exposed pads at the top can be equipped with a heatsink or a clamp to get improved heat dissipation on the topside. The non-exposed pad version has the mold compound covering the entire top and bottom side of the package.

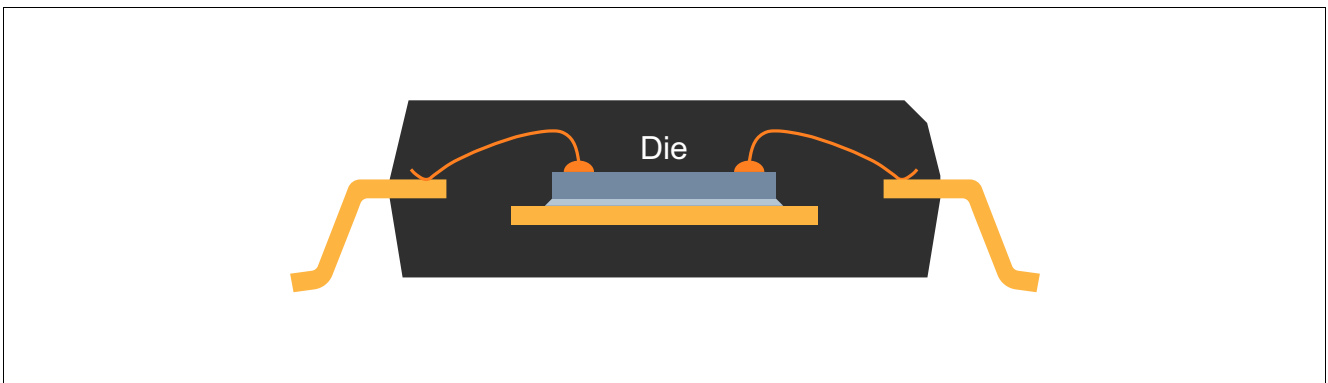


Figure 1 P(G)-DSO or P(G)-SSOP without Exposed Die Pad

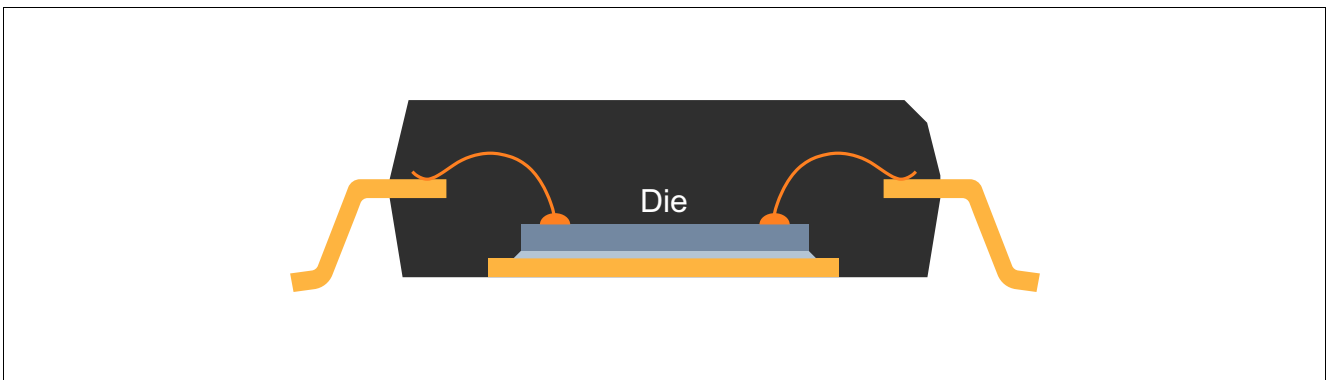


Figure 2 P(G)-DSO or P(G)-SSOP with Exposed Die Pad

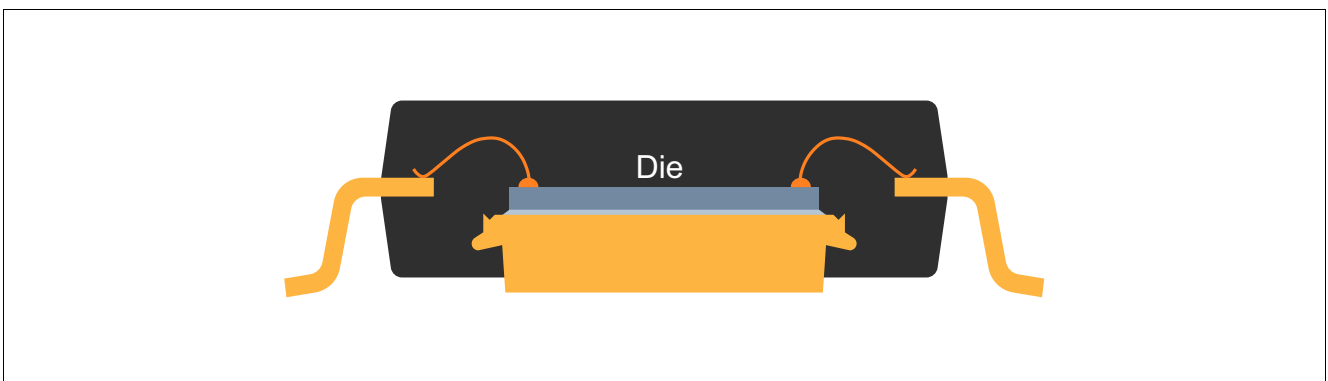


Figure 3 P(G)-DSO or P(G)-SSOP with Heatslug

2 Package Handling

2.1 ESD Protective Measures

Semiconductor devices are normally electrostatic discharge sensitive devices (ESDS) requiring specific precautionary measures in respect of handling and processing. Only in this way it is possible to ensure that the components can be inserted into assemblies without becoming damaged. Discharging of electrostatic charged objects over an IC, caused by human touch or by processing tools may cause high current respectively high voltage pulses, which may damage or even destroy sensitive semiconductor structures. On the other hand ICs may also be charged during processing. If discharging takes place too quickly ("hard" discharge), it may cause load pulses and damages, either. ESD protective measures must therefore prevent a contact with charged parts as well as a charging of the ICs. Protective measures against ESD include both the handling and processing and the packing of ESDS. A few hints are provided below on handling and processing.

2.1.1 Workplace-ESD Protective Measures

- Standard marking of ESD protected areas
- Access controls, with wrist strap and footwear testers
- Air conditioning
- Dissipative and grounded floor
- Dissipative and grounded working and storage areas
- Dissipative chairs
- Earth bonding point for wrist strap
- Trolleys with dissipative surfaces and wheels
- Suitable shipping and storage containers
- No sources of electrostatic fields

2.1.2 Equipment for Personal

- Dissipative/conductive footwear or heel straps
- Suitable smocks
- Wrist strap with safety resistor
- Volume conductive gloves or finger cots
- Regular training of staff

2.1.3 Production Installations and Processing Tools

- Machine and tool parts made of dissipative or metallic materials
- No materials having thin insulating layers for sliding tracks
- All parts reliably connected to ground potential
- No potential difference between individual machine and tool parts
- No sources of electrostatic fields

Detailed information on ESD protective measures may be obtained from the ESD Specialist through Area Sales Offices. Our recommendations are based on the internationally applicable standards IEC 61340-5-1 and ANSI/ESD S2020.

2.2 Packing of Components

List of relevant standards which should be considered if applicable for the given package or product.

IFX packs according to the IEC 60286-* series (The IEC 60286-3 is similar to the EIA 481-*)

- IEC 60286-1 Packaging of components for automatic handling - Part 1:
Tape packaging of components with axial leads on continuous tapes
- IEC 60286-2 Packaging of components for automatic handling - Part 2:
Tape packaging of components with unidirectional leads on continuous tapes
- IEC 60286-3 Packaging of components for automatic handling - Part 3:
Packaging of surface mount components on continuous tapes
- IEC 60286-4 Packaging of components for automatic handling - Part 4:
Stick magazines for dual-in-line packages
- IEC 60286-5 Packaging of components for automatic handling - Part 5:
Matrix trays
- IEC 60286-6 Packaging of components for automatic handling - Part 6:
Bulk case packaging for surface mounting components

Moisture Sensitive Surface Mount Devices are packed according to IPC/JEDEC J-STD-033A July 2002: Handling, Packing, Shipping and Use of Moisture/Reflow Sensitive Surface Mount Devices

Detailed packing drawings: [Packing Information \(Internet\)](#)

Other references

- ANSI/EIA-481-* Standards Proposal No. 5048, Proposed Revision of ANSI/EIA-481-B 8 mm through 200 mm Embossed Carrier Taping and 8 mm & 12 mm Punched Carrier Taping of Surface Mount Components for Automatic Handling (if approved, to be published as ANSI/EIA-481-C)
- EIA-726 8 mm Punched & Embossed Carrier Taping of Surface Mount Components for Automatic Handling of Devices Generally Smaller than 2.0 mm x 1.2 mm
- EIA-747 Adhesive Backed Punched Plastic Carrier Taping of Singulated Bare Die and Other Surface Mount Components for Automatic Handling of Devices Generally Less than 1.0 mm Thick
- EIA/IS-763 Bare Die and Chip Scale Packages Taped in 8 mm & 12 mm Carrier Tape for Automatic Handling
- EIA-783 Guideline Orientation Standard for Multi-Connection Package (Design Rules for Tape and Reel Orientation)

2.3 Storage and Transportation Conditions

Improper transportation and unsuitable storage of components can lead to a number of problems during subsequent processing, such as poor solderability, delamination and popcorn effects.

List of relevant standards which should be considered

- IEC 60721-3-0 Classification of environmental conditions: Part 3:
Classification of groups of environmental parameters and their severities; introduction
- IEC 60721-3-1 Classification of environmental conditions: Part 3:
Classification of groups of environmental parameters and their severities; Section 1: Storage
- IEC 60721-3-2 Classification of environmental conditions: Part 3:
Classification of groups of environmental parameters and their severities; Section 2: Transportation
- IEC 61760-2 Surface mounting technology - Part 2:
Transportation and storage conditions of surface mounting devices (SMD) - Application guide
- IEC 62258-3 Semiconductor Die Products - Part 3:
Recommendations for good practice in handling, packing and storage
- ISO 14644-1 Clean rooms and associated controlled environments Part 1:
Classification of airborne particulates

Table 1 General Storing Conditions - Overview

Product	Condition for Storing
Wafer/Die	N2 or MBB (IEC 62258-3)
Component - moisture sensitive	MBB ¹⁾ (JEDEC J-STD-033*)
Component - not moisture sensitive	1K2 (IEC 60721-3-1)

1) MBB = Moisture Barrier Bag

Maximum storage time

The conditions to be complied with in order to ensure problem-free processing of active and passive components are described in standard IEC 61760-2.

Internet links to standards institutes

[American National Standards Institute \(ANSI\)](#)

[Electronics Industries Alliance \(EIA\)](#)

[Association Connecting Electronics Industries \(IPC\)](#)

3 Printed Circuit Board, PCB

3.1 Routing

Generally the printed circuit board design and construction is a key factor for achieving a high reliability of the solder joints. For example, it is recommended not to place P(G)-DSO packages with soldered exposed die pad or heatslug at the same opposite locations on the PCB (if double sided mounting is used), because this results in a stiffening of the assembly with earlier solder joint fatigue compared to a design where the component locations are shifted against each other. Furthermore it is known, that the board stiffness itself has a significant influence to the reliability (temperature cycling) of the solder joint interconnect, if the system works in critical temperature cycling conditions.

We want to emphasize, that this document is just a guideline to support our customers in board design. Additionally studies at the customers may be necessary for optimization, which take into account the actual PCB, manufacturer’s capability, the customer’s SMT process, and product specific requirements.

3.2 PCB Pad Design

The solder pads have to be designed to assure optimum manufacturability and reliability. Generally two basic types of solder pads are commonly used:

- “Solder mask defined” (SMD) pad ([Figure 4](#)): The copper metal pad is larger than the solder mask opening above this pad. Thus the land area is defined by the opening in the solder mask.

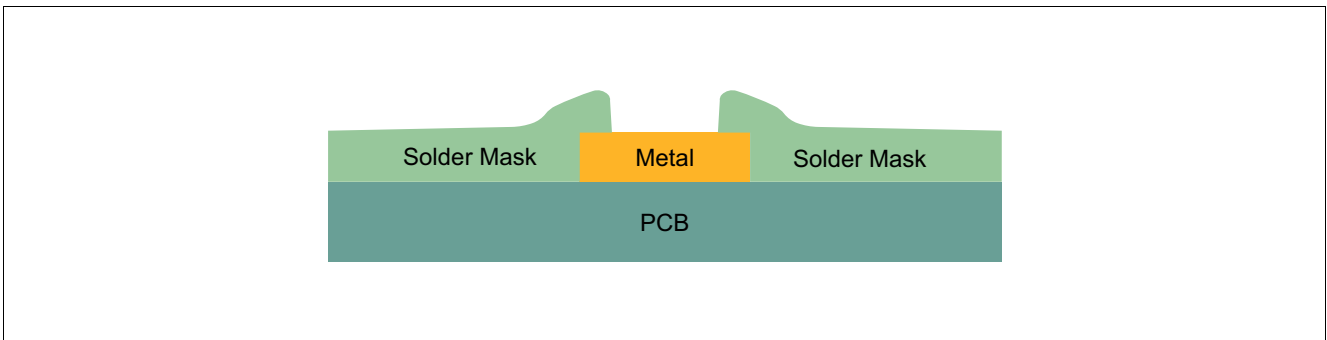


Figure 4 SMD Pad

- “Non solder mask defined” (NSMD) pad ([Figure 5](#)): Around each copper pad there is solder mask clearance. It is necessary to specify the dimensions and tolerances of the solder mask clearance in this way, that no overlapping of the solder pad by solder mask occurs (depending on PCB manufacturers tolerances, 75 µm is a widely used value).

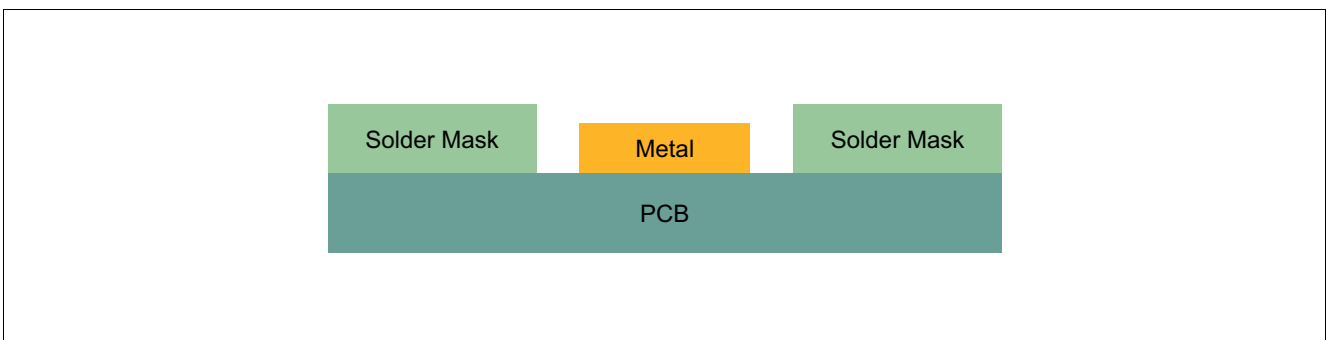


Figure 5 NSMD Pad

Because NSMD pads provide more space for routing and result in a higher solder joint reliability (also the side walls of the lands are wetted by the solder, which results in less stress concentration), NSMD type is recommended for the solder pads on the PCB.

Some P(G)-DSO packages have got a central metallic “die pad”, so-called exposed die pad or heatslug. The surface plating is the same as for the outer package pads. The exposed die pad or heatslug serves to conduct a large amount of heat into the PCB to achieve higher thermal performance and therefore should be soldered to the board. Furthermore soldering of the center pad contributes to solderjoint reliability of the outer leads.

For P(G)-DSO packages with exposed diepad or heatslug the solder pad in the center can be either NSMD or soldermask defined.

Figure 6 shows the recommended PCB Pad design. Refer to **Table 2** for the appropriate dimensions, which are package specific. Please note, that there is no exact congruency of PCB pads and package pads.

The exposed die pad or heatslug can be soldered completely to the board (for dimensions of the exposed die pad or heatslug please refer to **Table 2**) or it can be devided in so-called “Pockets”; these are defined rectangular openings in the solder resist mask (= SMD). In both cases an adjusted amount of solder paste has to be used to meet optimal thermal connection and to avoid tilting, beading or increased voiding.

Also because of thermal performance reasons the PCB design should include thermal vias. The vias serve to conduct the heat into deeper layers of the board and can be located close to the package or under the package. The latter gives the most direct thermal connection, but result in higher efforts to take care about filling or covering the vias. The best way in terms of reliability is to plug and overplate the vias. Generally it is less reliable to use a solder resist lid to protect the vias. Also a filling with solder during reflow is possible.

If microvias or other overplated vias are placed inside the solder pads, it is recommended to specify a good flatness of the vias. Deep dips inside the pads may cause solder joint voiding.

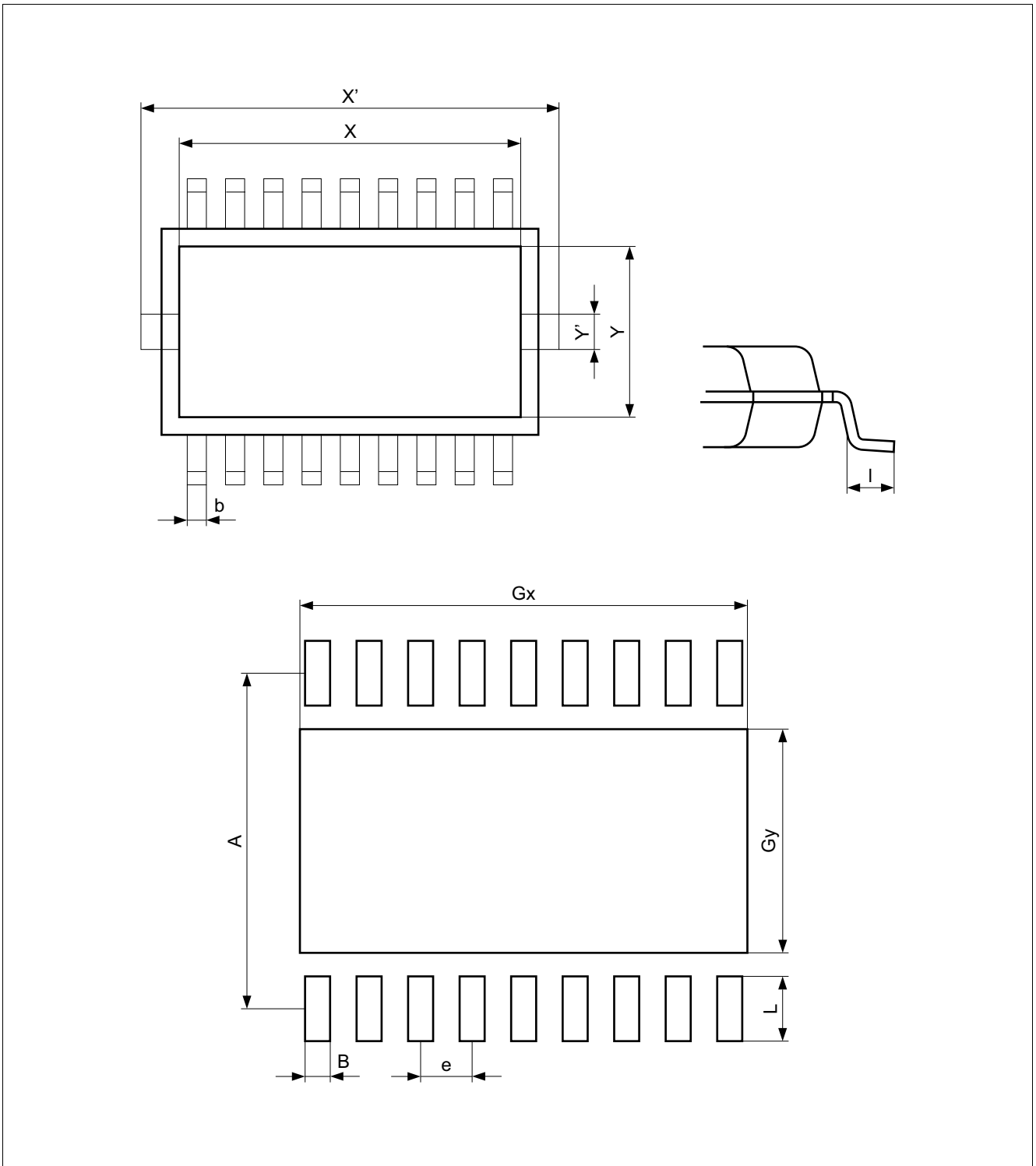


Figure 6 PCB Pad Design Recommendation

Table 2 Recommended PCB Pad Dimensions for P(G)-DSO and P(G)-SSOP Packages

Package Name	Perimeter Lead Size on Package		Exposed Die Pad / Heatslug Size on Package		Perimeter Lead Size on PCB		Pad Mean Distance	Pad Pitch	Exposed Die Pad / Heatslug Size on PCB		Exposed die pad/ Heatslug down/up
	l	b	X / X'	Y / Y'	L	B	A	e	Gx	Gy	
P/PG-DSO-6-1, -2	0.4	0.35			1.31	0.65	5.69	1.27			
P/PG-DSO-8-1, -4, -5	0.4	0.35			1.31	0.65	5.69	1.27			
P/PG-DSO-8-2	0.64	0.41			1.31	0.65	5.69	1.27			
P/PG-DSO-8-3, -6, -7, -8, -10, -13, -15, -18, -19, -20, -23	0.64	0.41			1.31	0.65	5.69	1.27			
P/PG-DSO-8-27	0.64	0.41	3	2.65	1.31	0.65	5.69	1.27	3	2.65	Down
P/PG-DSO-12-2, -3, -6	0.7	0.4	5.1/7.8	4.2/1.6	1.67	0.65	9.4	1	8.1	4.5	Down
P/PG-DSO-12-4, -5	0.7	0.25	5.1/7.8	4.2/1.6	1.67	0.65	9.4	1	8.1	4.5	Down
P/PG-DSO-14-1, -22, -30, -31, -32, -35	0.64	0.41			1.31	0.65	5.69	1.27			
P/PG-DSO-14-2	0.64	0.41			1.31	0.65	5.69	1.27			
P/PG-DSO-14-3, -8, -9, -11, -14	0.64	0.41			1.31	0.65	5.69	1.27			
P/PG-DSO-14-13, -19	0.64	0.41			1.31	0.65	5.69	1.27			
P/PG-DSO-14-33, -40, -43	0.64	0.41	6.4	2.65	1.31	0.65	5.69	1.27	6.4	2.65	Down
P/PG-DSO-16-1	0.4	0.35			1.31	0.65	5.69	1.27			
P/PG-DSO-16-3, -5	0.4	0.35			1.67	0.65	9.73	1.27			
P/PG-DSO-16-4	0.81	0.41			1.67	0.65	9.73	1.27			
P/PG-DSO-16-6, -10	0.64	0.41			1.31	0.65	5.69	1.27			
P/PG-DSO-16-9, -11, -12	0.64	0.41			1.31	0.65	5.69	1.27			
P/PG-DSO-20-1, -6, -7, -9, -14, -15, -17, -18, -21, -31, -32, -35, -36, -42, -45	0.4	0.35			1.67	0.65	9.73	1.27			
P/PG-DSO-20-2	0.8	0.41			1.81	0.63	9.41	1.27			
P/PG-DSO-20-5	0.95	0.4	13.7/16.1	5.9/3.2	1.83	0.68	13.48	1.27	N.A.	N.A.	Up
P/PG-DSO-20-10, -12, -13, -16, -33, -34, -37, -48, -50	0.95	0.4	13.7/15.74	5.9/3.2	1.83	0.68	13.48	1.27	13.5	5.8	Down
P/PG-DSO-20-24	0.95	0.4	13.7/16.1	5.9/3.2	1.83	0.68	13.48	1.27	N.A.	N.A.	Up
P/PG-DSO-20-27	0.7	0.4	5.2	4.6	1.67	0.65	9.73	1.27	5.2	4.6	Down
P/PG-DSO-20-30	0.7	0.4	7	4.8	1.67	0.65	9.73	1.27	7	4.8	Down
P/PG-DSO-20-38	0.7	0.4	7	4.8	1.67	0.65	9.73	1.27	7	4.8	Down

Table 2 Recommended PCB Pad Dimensions for P(G)-DSO and P(G)-SSOP Packages (cont'd)

Package Name	Perimeter Lead Size on Package		Exposed Die Pad / Heatslug Size on Package		Perimeter Lead Size on PCB		Pad Mean Distance	Pad Pitch	Exposed Die Pad / Heatslug Size on PCB		Exposed die pad/ Heatslug down/up
	l	b	X / X'	Y / Y'	L	B	A	e	Gx	Gy	
P/PG-DSO-24-1, -3, -8, -9	0.4	0.35			1.67	0.65	9.73	1.27			
P/PG-DSO-24-10	0.76	0.41			1.67	0.65	9.73	1.27			
P/PG-DSO-28-1, -6,-9, -11, -13, -14, -16, -17, -18, -19	0.4	0.35			1.67	0.65	9.73	1.27			
P/PG-DSO-28-3	0.8	0.41			1.81	0.63	11.11	1.27			
P/PG-DSO-28-20	0.76	0.41			1.67	0.65	9.73	1.27			
P/PG-DSO-32-1	0.8	0.41			1.81	0.63	11.11	1.27			
P/PG-DSO-32-2	0.79	0.41			1.79	0.66	11.21	1.27			
P/PG-DSO-36-5	0.95	0.25	13.7/ 15.74	5.9/3.2	1.83	0.45	13.48	0.65	N.A.	N.A.	Up
P/PG-DSO-36-10, -12, -13, -14, -15, -16	0.95	0.25	13.7/ 15.74	5.9/3.2	1.83	0.45	13.48	0.65	13.5	5.8	Down
P/PG-DSO-36-20	0.4	0.33			1.67	0.45	9.73	0.65			
P/PG-DSO-36-24	0.7	0.33	7	5.1	1.67	0.45	9.73	0.65	7	5.1	Down
P/PG-DSO-36-25	0.7	0.33	6.4	4.5	1.67	0.45	9.73	0.65	6.4	4.5	Down
P/PG-DSO-36-28	0.7	0.33	9	4.2	1.67	0.45	9.73	0.65	9	4.2	Down
P/PG-DSO-36-36	0.7	0.33	6.8	4.2	1.67	0.45	9.73	0.65	6.8	4.2	Down
P/PG-SSOP-14-1, -2, -3	0.64	0.25	3.0	2.65	1.31	0.45	5.69	0.65	3.0	2.65	Down
P/PG-SSOP-20-1	0.75	0.3			1.51	0.45	7.19	0.65			
P/PG-SSOP-24-1	0.9	0.3			1.51	0.45	7.19	0.65			
P/PG-SSOP-24-4	0.64	0.25	6.4	2.65	1.31	0.45	5.69	0.65	6.4	2.65	Down
P/PG-SSOP-24-5	0.64	0.25			1.31	0.45	5.69	0.65			
P/PG-SSOP-28-1	0.75	0.3			1.51	0.45	7.19	0.65			

3.3 Pad Surfaces

The solder pads must have good wettability to the soldering material (solder paste). All finishes listed here are well proven for SMT assembly, but especially for fine pitch applications the quality of the plating gets more important. Therefore Hot Air Solder Leveling finish can be used, but the flatness of the single pads has to be specified for high quality, not to bring on soldering problems. The properties of some preservatives are listed in [Table 3](#).

Table 3 Properties of Some Solderability Preservative Layers on PCBs

Finish	Typ. Layer Thickness [µm]	Properties	Concerns
HASL (SnAg) (Hot Air Solder Leveling)	> 5	Cheap, widely usage, know how in fabrication	Uneven surface, formation of humps, flatness of single pads has to be good for fine pitch applications
Electroless Tin	0.3 - 1.2	Solder joint consists only of copper and solder, no further metal is added to the solder joint	Long-term stability of protection may be a concern, baking of PCB may be critical
Electroless Silver	0.2 - 0.5	Solder joint consists only of copper and solder, no further metal is added to the solder joint	Long-term stability of protection may be a concern, baking of PCB may be critical
Electroless Ni / Immersion Au (ENIG)	3 - 7 / 0.05 - 0.15	Good solderability protection, high shear force values	Expensive, concerns about brittle solder joints
Galvanic Ni/Au	> 3 / 0.1 - 2	Only for thicker layers, typically used for connectors	Expensive, not recommended for solder pads
OSP (Organic Solderability Preservatives)	Typical 1	Cheap, simple, fast and automated fabrication	Must be handled carefully to avoid damaging the OSP; not as good long-term stability as other coatings; at double-sided reflow only suitable with inert gas reflow

The question about the best preservative surface can not be answered generally. It depends strongly on board design, pad geometry, components on board or process conditions. In literature the test results of solderability, wetting force and wetting time for several preservative layers are not always coincident.

Special notes for green (“G”) packages:

The PCB must be able to resist the higher temperatures which are occurring at the lead-free process.

This question should be discussed with the PCB-supplier. Generally, the wettability of tin-lead solder paste on the described surface platings is better compared to lead-free solder paste.

4 PCB Assembly

4.1 Solder Stencil

The solder paste is applied onto the PCB metal pads by stencil printing. The volume of the printed solder paste is determined by the stencil aperture and the stencil thickness. In most cases the thickness of a stencil has to be matched to the needs of all components on the PCB. For P(G)-DSO and P(G)-SSOP packages it is recommended to use 100 - 150 μm thick stencils.

The apertures of the perimeter pads on the PCB should be of the same size and shape as the metal pads (for recommendations please see PCB section). For P(G)-DSO packages with exposed die pad or heatslug solder thickness, tilting, building of voids and filling of vias (if needed) can be severely influenced by the chosen stencil apertures. In case of using “pockets” a stencil layout with the same geometry like the solder mask opening is in many applications sufficient. In case of soldering the exposed die pad to one big area the stencil in the thermal pad area shall be segmented in smaller, multiple openings (see schematic example of [Figure 7](#)). One large opening would result in excessive solder volume under the P(G)-DSO die pad or heatslug compared to the perimeter pads as well as significantly higher voiding rate and higher risk of solder balling.

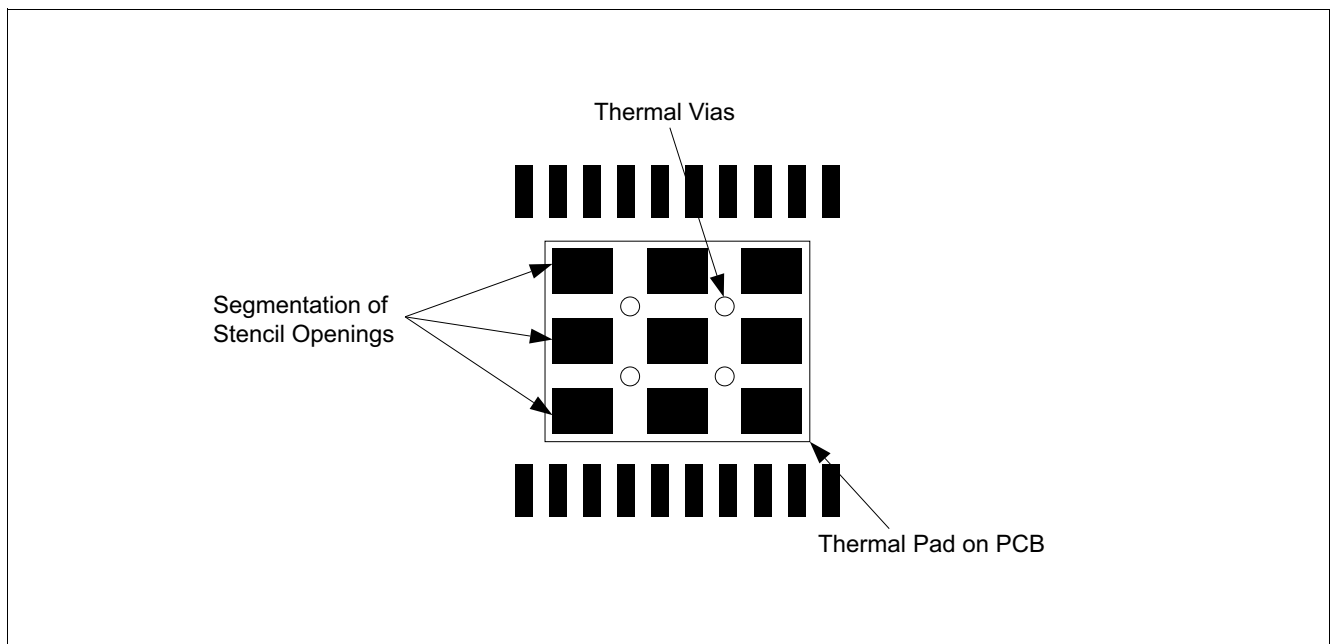


Figure 7 Example for Segmentation of Stencil Openings on Thermal Die Pad Area

To ensure a uniform and high solder paste transfer to the PCB, lasercut (mostly made from stainless steel) or electroformed stencils (Nickel) are preferred. Rounding the corners of the apertures (radius $\sim 50 \mu\text{m}$) can be supportive for the paste release.

4.2 Solder Paste

Solder paste consists of solder alloy and a flux system. Normally the volume is split into about 50% alloy and 50% flux. In term of mass this means approx. 90 wt% alloy and 10 wt% flux system. The flux system has the function to remove the contaminations from the surfaces to be soldered during reflow. The capability of removing contaminations is given by the respective activation level. The metal alloy in case of Pb-containing solder pastes is typically eutectic SnPb or near eutectic SnPbAg. In case of leadfree solder pastes so-called SAC-alloys can be found (typically 1 - 4% Ag and $< 1\%$ Cu). A “no-clean” solder paste is preferred, because cleaning under the soldered P(G)-DSO or P(G)-SSOP may be difficult. The paste must be suitable for printing the solder stencil aperture dimensions, Type 3 paste is recommended. Solder paste is sensitive to age, temperature and humidity. Please notice the handling recommendations of the paste manufacturer.

4.3 Component Placement

P(G)-DSO and P(G)-SSOP packages have to be placed accurately according to their geometry. Positioning the packages manually is not recommended.

Component placement accuracies of $\pm 50 \mu\text{m}$ are obtained with modern automatic component placement machines using vision systems. With these systems both the PCB and the components are optically measured and the components are placed on the PCB at their programmed positions. The fiducials on the PCB are located either on the edge of the PCB for the entire PCB or additionally on individual mounting positions (local fiducials). They are detected by a vision system immediately before the mounting process. Recognition of the packages is performed by a special vision system, enabling a correct centering of the complete package.

The maximum tolerable displacement of the components is 20% of the metal pad width on the PCB (for non solder mask defined pads). In consequence, for P(G)-DSO and P(G)-SSOP packages with the smallest package pads of 0.25 mm, the device pad to PCB pad misalignment has to be better than $50 \mu\text{m}$ to assure a robust mounting process. Generally this is achievable with a wide range of placement systems.

The following remarks are important:

- Especially on large boards local fiducials close to the device can compensate a large amount of PCB tolerances.
- It is recommended to use the lead recognition capabilities of the placement system, rather than the outline centering.
- To ensure the identification of the packages by the vision system, an adequate lighting as well as the correct choice of the measuring modes are necessary. The accurate settings can be taken from the equipment manuals.
- Too high placement force can lead to squeezed out solder paste and cause solder joint shorts. On the other hand too low placement force can lead to insufficient contact between package and solder paste and may result in insufficient sticking of the component on the solderpaste which furthermore may lead to shifted or dropped devices.

4.4 Soldering

Soldering determines the yield and quality of assembly fabrication to a very large extent. Generally all standard reflow soldering processes

- forced convection
- vapour phase
- infrared (with restrictions)

and typical temperature profiles are suitable for board assembly of P(G)-DSO and P(G)-SSOP packages.

Wave soldering is possible for P(G)-SSOP and P(G)-DSO without exposed die pad or heatslug. Please be aware: The smaller the pitch, the more difficult is the adjustment of the wave soldering process to avoid bridging. Fine pitch components ($\leq 0.65 \text{ mm}$) are not recommended for wave soldering due to increasing jeopardy for bridging adjacent leads.

In any case wave soldering of SMT components requires special attention with respect to the heat shock resistivity of the components and PCB-design, which may differ in the suitable landing pad design for wave compared to reflow soldering (e.g. enlarged board pads, orientation towards transport direction, additional board pads, so-called solder fenders)

At the reflow process each solder joint has to be exposed to temperatures above solder liquidus for a sufficient time to get the optimum solder joint quality, whereas overheating the PCB with its components has to be avoided. Please refer to the bar code label on the packing for the maximum peak package body temperature. When using infrared ovens without convection special care may be necessary to assure a sufficiently homogeneous temperature profile for all solder joints on the PCB, especially on large, complex boards with different thermal masses of the components, including those under the P(G)-DSO or P(G)-SSOP. The most recommended type is forced convection reflow. Nitrogen atmosphere can generally improve solder joint quality, but is normally not necessary for soldering with typically used solder pastes, components and board finishes.

The temperature profile of a reflow process is one of the most important factors of the soldering process. The temporal progression of the temperature profile is divided into several phases, each with a special function. **Figure 8** shows a general forced convection reflow profile for soldering P(G)-DSO or P(G)-SSOP packages, **Table 4** shows an example of the key data of such a solder profile for Tin-lead and for lead-free alloys. The single parameters are influenced by various facts, not only by the package. It is essential to follow the solder paste manufactures application notes, too. Additionally, most PCBs contain more than one package type and therefore the reflow profile has to be matched to all components' and materials' demands. We recommend to measure the solder joints' temperatures by thermocouples beneath the respective packages. It has to be considered, that components with large thermal masses don't heat up in the same speed as lightweight components, and also the position and the surrounding of the package on the PCB, as well as the PCB thickness can influence the solder joint temperature significantly. Therefore no concrete temperature profile can be given.

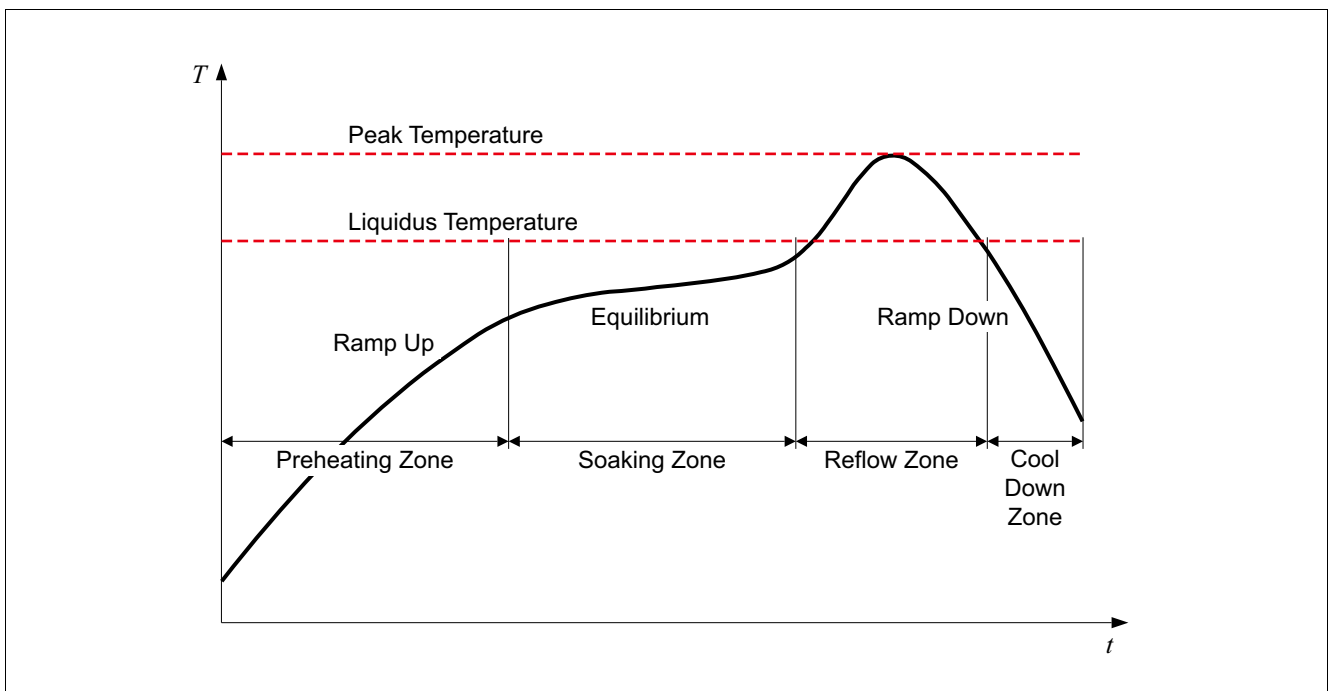


Figure 8 General Forced Convection Reflow Solder Profile

The following table is an example, not a recommendation (for reference only).

Table 4 EXAMPLE for the Key Data of a Forced Convection Reflow Solder Profile

Parameter	Tin-lead Alloy (SnPb or SnPbAg)	Lead-free Alloy (SnAgCu)	Main Requirements From
Preheating rate	2.5 K/s	2.5 K/s	Flux system (Solder paste)
Soaking temperature	140 - 170°C	140 - 170°C	Flux system (Solder paste)
Soaking time	80 s	80 s	Flux system (Solder paste)
Peak temperature	225°C	245°C	Alloy (Solder paste)
Reflow time over Liquidus	60 s	60 s	Alloy (Solder paste)
Cool down rate	2.5 K/s	2.5 K/s	

4.4.1 Double-Sided Assembly

P(G)-DSO and P(G)-SSOP packages are generally suitable for mounting on double-sided PCBs. That means that in a first step one side of the PCB is populated with components and soldered. Afterwards the second side of the PCB is populated with components and soldered again.

4.4.2 Processing of Moisture-Sensitive Components

For moisture-sensitive packages like some P(G)-DSO or P(G)-SSOP it is necessary to control the moisture content of the components. The penetration of moisture into the package molding compound is generally caused through exposure to the ambient air. Moisture absorption leads in many cases to moisture concentrations in the component which are high enough to destroy the package during the solder cycle (“popcorn effect” due to the evaporation of the humidity). Hence the necessity to dry moisture-sensitive components, to seal them in a moisture-resistant bag and only to remove them immediately prior to processing (soldering onto the PCB). The permissible time (from opening the moisture barrier bag until the final soldering process) that a component can remain unprotected in an environment with a level of humidity approximating to real-world conditions (e.g. 30°C/60% RH) is a measure of the sensitivity of the component to ambient humidity (Moisture Sensitivity Level, MSL). The most commonly applied standard IPC/JEDEC J-STD-033* thus defines eight different MSLs (see [Table 5](#)). Please refer to the “Moisture Sensitivity Caution Label” on the packing material, which contains informations about the moisture sensitivity level of the product.

Table 5 Moisture Sensitivity Levels (acc. to IPC/JEDEC J-STD-033*)

Level	Floor Life (out of bag)	
	Time	Conditions
1	Unlimited	≤ 30°C / 85% RH
2	1 year	≤ 30°C / 60% RH
2a	4 weeks	≤ 30°C / 60% RH
3	168 hours	≤ 30°C / 60% RH
4	72 hours	≤ 30°C / 60% RH
5	48 hours	≤ 30°C / 60% RH
5a	24 hours	≤ 30°C / 60% RH
6	Mandatory bake before use. After bake, must be reflowed within the time limit specified on the label.	≤ 30°C / 60% RH

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If moisture-sensitive components have been exposed to ambient air longer than the specified time according to their MSL, or the humidity indicator card dot 10% is wet (read 1 minute after bag opening), the packages have to be baked prior to the assembly process. Please refer to IPC/JEDEC J-STD-033* for bake procedure. Baking a package too often can cause solderability problems due to oxidation and/or intermetallic growth. Notice that packing material possibly can not withstand the baking temperature. See imprints/labels on the respective packing for maximum temperature.

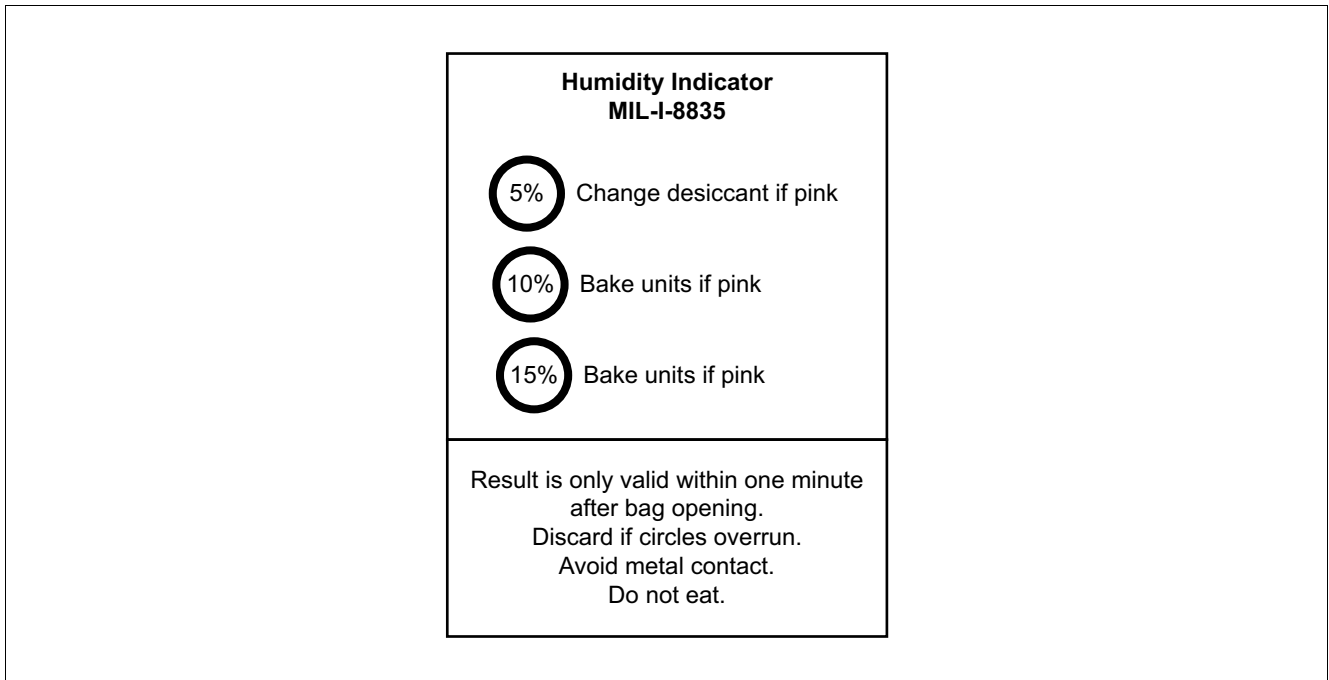


Figure 9 Humidity Indicator

4.4.3 Special Notes for Green (“G”) Packages

Like in Tin-lead-process, generally all commonly used reflow soldering processes (vapour phase, forced convection, infrared) are suitable for board assembly. But due to a higher peak temperatures at the lead-free process, some equipment can reach the limits of their technical capability. Normally reflow with forced convection is chosen. Due to the aggravated conditions at the lead-free process, nitrogen atmosphere may reduce oxidation and improve the solder joint quality. Be aware, that the increasing temperature stress may worsen the MSL. Therefore the data for lead-free packages may name 2 MSLs: One for a lower reflow peak temperature (tin-lead) and one for a higher reflow peak temperature (lead-free). Each one is valid for the respective application.

4.5 Cleaning

After the reflow soldering process some flux residues can be found around the solder joints. If a “no-clean” solder paste has been used for solder paste printing, the flux residues usually don’t have to be removed after the soldering process. Be aware, that cleaning beneath a P(G)-DSO or P(G)-SSOP package is difficult because of the small gap between package substrate and PCB and is therefore not recommended. Whether the solder joints have to be cleaned, however, the cleaning method (e.g. ultrasonic, spray or vapor cleaning) and solution has to be selected with consideration of the packages to be cleaned, the used flux in the solder paste (rosin-based, water-soluble, etc.), environmental and safety aspects. Removing/Drying even of small residues of the cleaning solution should also be done very thoroughly. Contact the solder paste manufacturer for recommended cleaning solutions.

4.6 Inspection

A visual inspection of the solder joints of the outer, gullwing-shaped terminals with conventional AOI (automatic optical inspection) systems is a standard procedure. Please keep in mind the non-wetting of the punched lead tip is not a reject criterion. For the acceptability of electronic assemblies please refer also to the IPC-A-610 standard.

The inspection of solder joints of exposed pad or heatslug with AOI is not possible. The only reasonable method is the usage of x-ray, e.g. AXI (automatic X-ray inspection) systems. AXI systems are available as 2D and 3D solutions. They usually consist of an X-ray camera and the hard- and software needed for inspection, controlling, analyzing and data transfer routines. These systems enable the user to detect soldering defects like poor soldering, bridging, voiding and missing parts quite reliable. But other defects like broken solder joints are not easily detectable by X-ray.

Cross sectioning of a soldered package as well as dye penetrant analysis can serve as tools for sample monitoring only, because of their destructive character. In case of soldering exposed die pads or heatslugs it is highly recommended to check the quality of the solderjoint under the component also via cross sections especially during engineering stadium and as a monitoring.

Special notes for green (“G”) packages:

Lead-free solder joints look different than tin-lead (SnPb) solder joints. Tin-lead joints have a bright and shiny surface, a dull surface is an indicator for a insufficient solder joint. Lead-free solder joints don’t have this bright surface. Lead-free solder joints are dull and grainy. This surface properties are caused by the irregular solidification of the solder, as the used solder alloys are not exactly eutectic (like the 63Sn37Pb solder alloy). This means this SnAgCu-solders don’t have a melting point but a melting range of some degrees. Although lead-free solder joints have this dull surface, this does not mean that lead-free joints are of lower quality or weaker than the SnPb joints. This characteristic makes it necessary to instruct the inspection personnel how these new lead-free joints look like, and/or to adjust optical inspection systems to lead-free solder joints.

5 Rework

If a defect component is observed after board assembly the device can be removed and replaced by a new one. Repair of components' single perimeter solder joints is not recommended, but possible by using soldering iron or hot air nozzle. An overheating of the component or damage due to too high moisture uptake has to be avoided in any case.

5.1 Tooling

The rework process is commonly done on special rework equipment. There are a lot of systems available on the market, and for processing these packages the equipment should fulfill the following requirements:

- *Heating:* Hot air heat transfer to the package and PCB is strongly recommended. Temperature and air flow for heating the device should be controlled. With free-programmable temperature profiles (e.g. by PC controller) it is possible to adapt the profiles to different package sizes and thermal masses. PCB preheating from underside is recommended. Infrared heating can be applied, especially for preheating the PCB from underside, but it should be only supporting the hot air flow from the upside. Instead of air also nitrogen can be used.
- *Vision system:* The bottom side of the package as well as the site on the PCB should be observable. For precise alignment of package to PCB a split optic should be implemented. Microscope magnification and resolution should be appropriate for the pitch of the device.
- *Moving and additional tools:* The device should be relocatable on the whole PCB area. Placement accuracy is recommended to be better than $\pm 50 \mu\text{m}$. The system should have the capability of removing solder residues from PCB pads (special vacuum tools).

5.2 Device Removal

If it is intended to send a defect component back to the supplier, please note that during the removal of this component no further defects must be introduced to the device, because this may hinder the failure analysis at the supplier. This includes the following recommendations:

- *Moisture:* According to his moisture sensitivity level, possibly the package has to be dried before removal. If the maximum storage time out of the dry pack (see label on packing material) is exceeded after board assembly, the PCB has to be dried according to the recommendations (see [Chapter 4.4](#)), otherwise too much moisture may have been accumulated and damage may occur (popcorn effect).
- *Temperature profile:* During soldering process it should be assured that the package peak temperature is not higher and temperature ramps are not steeper than for the standard assembly reflow process (see [Chapter 4.4](#)).
- *Mechanics:* Be aware not to apply high mechanical forces for removal. Otherwise failure analysis of the package can be impossible or PCB can be damaged. To pick-up the component by pipettes is the most gentle way. Such pipettes are implemented on most rework systems.

5.3 Site Redressing

After removing the defect component the pads on the PCB have to be cleaned from solder residues. Don't use steel brushes because steel residues can lead to bad solder joints. Before placing a new component it is recommended to apply solder paste on each PCB pad by printing (special micro stencil) or dispensing. It is recommended to use no-clean solder paste.

5.4 Reassembly and Reflow

After preparing the site, the new package can be placed onto the PCB. Regarding placement accuracy and placement force the process should be comparable to the automatic pick & place process (please refer to [Chapter 4.3](#)). During soldering process it should be assured that the package peak temperature is not higher and temperature ramps are not steeper than for the standard assembly reflow process (see [Chapter 4.4](#)).

Special notes for green (“G”) packages:

Packages with lead-free pads can be reworked like leaded packages, but peak temperatures have to be adjusted due to another liquidus of the lead-free solder alloy (see also [Chapter 4.4](#)).

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