New XC2200 Microcontroller Family

March 2007
Agenda
XC2200 Microcontroller Family for BODY Applications

- Family Concept
- XC2200 Highlights
- Block Diagrams, Benefits
- Technical Details
  - C166SV2 – Core
  - System Control Unit (SCU): Power saving modes
  - Powerful Peripherals: CAPCOM, ADC, USIC, MultiCAN
Agenda
XC2200 Microcontroller Family for BODY Applications

- Family Concept
- XC2200 Highlights
- Block Diagrams, Benefits
- Technical Details
  - C166SV2 – Core
  - System Control Unit (SCU): Power saving modes
  - Powerful Peripherals: CAPCOM, ADC, USIC, MultiCAN
Infineon Microcontroller
Our strength are Cores ...

High Performance 32-bit CPU
3 level super-scalar,
4 stage pipeline,
running up to 150 MHz

Peripheral Control Processor
32 bit core single cycle
Specialized for transfer function

C166S-V2
Core Single-Cycle
MAC Instructions
DMA-like Peripheral
Event Controller

XC166

XC2xx

XC800

C800

C500

8 bit core op-code
of the 8051

New 8 bit high core two cycles per
instruction, op-code of the 8051

Well established Core
in powertrain 50%
of EU Market and 30% WW
Market production
25 million pieces a year
Dedicated Features for Body and Gateway applications

Real family concept reflected in Hardware and Software scalability

Low Power Consumption

Intelligent features and feature connections to unload CPU performance and lower logistics costs at customer

First to offer a 6th CAN-node for Gateway
# Microcontroller Naming Conventions

**XC2200-Family**

### Industrial/Automotive families:
- 2: Body
- 3: Safety, Vehicle dynamics
- 7: Powertrain

**C166S CPU:**
- V2: XC-2 (any version)

**Pin Count:**
- 4 = 64 Pin
- 6 = 100 Pin
- 8 = 144 Pin
- 9 = 176 Pin

**Prefix**
- SA

**Temp. Range Code**
- F = -40/ 85 °C
- H = -40/ 105°C
- K = -40/ 125°C

**Type**
- A

**Variant**
- Z

**Memory Size (Code+Data)**
- L

**Code Mem. Type**
- F

**Freq. (in Mhz)**
- 20

**Package Code**
- L

**SRAM Size**
- #

**Size of on-chip memory:**
- Total number of memory to be used for Code and Data
- Memory size = shown number x 8
- e.g.: shown number = 40
  - 320KB total memory

**Size of on-chip SRAM**
- L = Flashless
- F = Flash
- R = ROM

**Example:**
- SAK-XC2287B-96F80L24

---

#### Table:

<table>
<thead>
<tr>
<th>Prefix</th>
<th>Temp. Range Code</th>
<th>Type</th>
<th>Variation</th>
<th>Memory Size (Code+Data)</th>
<th>Code Mem. Type</th>
<th>Freq. (in Mhz)</th>
<th>Package Code</th>
<th>SRAM Size</th>
</tr>
</thead>
<tbody>
<tr>
<td>SA</td>
<td>F H K</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>L</td>
<td>#</td>
</tr>
</tbody>
</table>

---

**Opt. (in case of variants):**
- to further specify feature set

---

**1 digits: component specific**
XC2200 - Performance Drives BODY

Cost
- True 32-bit performance for 16-bit price
- Less external components needed
- Light Bulb Supervision without CPU calculation
- Gateway functionality without using CPU performance
  ⇒ lower frequency and lower EMI

Quality
- “No Compromise” quality strategy and policy
- All Flash Modules with HW ECC
- Less external components needed

Flexibility
- Reduced development time with existing LLD
- Scalability with a rich choice of different devices
- Pin and “Routing” compatibility between all packages

Excellent Support through strong sales and FAE force
XC2200 16/32bit µC – Benefits

Benefits
- Flexible power management
- 16bit µC with 32bit performance
- Quality and reliability
- Family Concept HW / SW Scalability

Benefits
- Flexible usage of serial interfaces
- Triggering of ADC by PWM
- Automatic Gateway without CPU performance
- Reputation and customer access

XC2200
- Best-in-class feature set to be one step ahead of competition!
# XC2200 Microcontroller Family

## Family Details

<table>
<thead>
<tr>
<th>Package</th>
<th>64 Pin</th>
<th>100 Pin</th>
<th>144 Pin</th>
<th>176 Pin</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Memory Incl. Data-Flash</strong></td>
<td>32K - 320K eFlash 6K-34K SRAM</td>
<td>64K-768K eFlash 10K-82K SRAM</td>
<td>320K - 1088K eFlash 26K - 82K SRAM</td>
<td>512K - 1280K eFlash 54K - 82K SRAM</td>
</tr>
<tr>
<td><strong>CAN</strong></td>
<td>0 - 2 Nodes</td>
<td>0 - 6 Nodes</td>
<td>2 - 6 Nodes</td>
<td>2 - 6 Nodes</td>
</tr>
<tr>
<td><strong>Flexray</strong></td>
<td>External CIC310</td>
<td>External CIC310</td>
<td>External CIC310</td>
<td>2 Channels</td>
</tr>
<tr>
<td><strong>I/O</strong></td>
<td>Up to 40 (two I/O domains opt.)</td>
<td>Up to 76 (two I/O domains opt.)</td>
<td>Up to 118 (two I/O domains opt.)</td>
<td>Up to 140 (two I/O domains opt.)</td>
</tr>
<tr>
<td><strong>Timer</strong></td>
<td>Up to 9</td>
<td>Up to 15</td>
<td>Up to 15</td>
<td>Up to 17</td>
</tr>
<tr>
<td><strong>Serial interfaces</strong></td>
<td>2 – 4 ch (Multi protocol opt.)</td>
<td>2 – 6 ch (Multi protocol opt.)</td>
<td>4 – 6 ch (Multi protocol opt.)</td>
<td>4 – 10 ch (Multi protocol opt.)</td>
</tr>
<tr>
<td><strong>PWM Channels CC2/CC6</strong></td>
<td>12</td>
<td>24</td>
<td>32</td>
<td>Up to 48 incl. CC1</td>
</tr>
<tr>
<td><strong>ADC</strong></td>
<td>2 Modules 9ch / 10Bit</td>
<td>2 x 8ch / 10Bit</td>
<td>2 x 12ch / 10Bit</td>
<td>2 x 15ch / 10Bit</td>
</tr>
<tr>
<td><strong>Performance</strong></td>
<td>40MHz</td>
<td>40/66/80MHz</td>
<td>40/66/80MHz</td>
<td>66/80MHz</td>
</tr>
</tbody>
</table>

**XC2200 Family offers Scalability**
XC2200 Microcontroller Family
Pin compatibility between LQFP144/LQFP-100/LQFP-64
Availability

- EES of XC22xx
  - available!
- ES delivery of XC22xx:
  - August 2007
- Qualification finished:
  - December 07

Evaluationboard available!
AUTOSAR aims to improve complexity management of integrated E/E architectures through increased reuse and exchangeability of SW modules.

**MC-ISAR** MicroController – Infineon Software ARchitecture

**MC-ISAR**: MCU, WDG, GPT, SPI, PORT, DIO, ICU, PWM, ADC  
**MC-ISAR COM**: CAN, CANRxTx, LIN  
**MC-ISAR MEM**: FLASH, FEE
Agenda
XC2200 Microcontroller Family for BODY Applications

- Family Concept
- XC2200 Highlights
- Block Diagrams, Benefits
- Technical Details
  - C166SV2 – Core
  - System Control Unit (SCU): Power saving modes
  - Powerful Peripherals: CAPCOM, ADC, USIC, MultiCAN
# History of Infineon’s 16-Bit Family

Infineon has experience in 16/32-Bit Microcontroller for more than 15 years !!!

<table>
<thead>
<tr>
<th>Generation</th>
<th>Release</th>
<th>(\mu)C</th>
<th>Features</th>
</tr>
</thead>
<tbody>
<tr>
<td>1st</td>
<td>1990</td>
<td>80C166</td>
<td>20 MHz, 2 clock cycle/instruction, 32 kB ROM, 100 ns instruction execution from ROM (@ 20 MHz)</td>
</tr>
<tr>
<td>2nd</td>
<td>1992</td>
<td>C167</td>
<td>16 MB address range, integrated CS# signals, ATOMIC/EXTEND instructions, CAN</td>
</tr>
<tr>
<td></td>
<td>1994</td>
<td>C167CR</td>
<td>PLL, XRAM, up to 33 MHz, 128 kB ROM</td>
</tr>
<tr>
<td>3rd</td>
<td>1997</td>
<td>C161xx</td>
<td>Enhanced low power modes, up to 40 MHz (50 ns instruction execution from ROM @ 40 MHz), OTP (12V), 3V versions</td>
</tr>
<tr>
<td></td>
<td></td>
<td>C164xx</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>C167CS</td>
<td></td>
</tr>
<tr>
<td>4th</td>
<td>2001</td>
<td>XC16x</td>
<td>Single cycle machine, MAC unit, up to 256 kB eFlash, 40 MHz (25 ns instruction execution from flash @ 40 MHz) 32bit enhancements, TwinCAN, OCDS</td>
</tr>
<tr>
<td>5th</td>
<td>2006</td>
<td>XC2200</td>
<td>Up to 80 MHz, 32bit enhancements, Enhanced system control unit, up to 1.2 MB eFlash, MultiCAN, USIC, ...</td>
</tr>
</tbody>
</table>
Features

- Increase maximum performance from 40MHz to **80MHz**
- **130 nm technology** (Automotive Excellence)
- **Single power supply** – Core voltage generated on chip
- Enhanced **power saving** and **power down** concept
- Clock generation optional with **on chip oscillator** or XTAL
- Two **FLASH** modules with parallel access for **code** and **data**
- Enhanced **Interrupt** and PEC Response Time
- **Flexible Power Supply** 3.0V...5.5V (two independent domains)
- New and enhanced **Peripherals** *(USIC, ADC, MultiCAN, CAPCOM6, ...)*
- **Scalable** and **pin compatible** microcontroller concept

Binary Op-Code **compatible to (X)C166 Architecture**
Agenda
XC2200 Microcontroller Family for BODY Applications

- Family Concept
- XC2200 Highlights
- Block Diagrams, Benefits
- Technical Details
  - C166SV2 – Core
  - System Control Unit (SCU): Power saving modes
  - Powerful Peripherals: CAPCOM, ADC, USIC, MultiCAN
**Key Features:**
- Up to 768 kB code/data Flash
- Up to 82 kB SRAM
- High-speed MultiCAN 2 nodes, 32 message objects, full CAN 2.0B
- On Chip Debug System
- 8-channel 10-bit Dual ADC parallel conversion, 1.2 µs cycle time
- 2x LIN, 2x SPI
- Five 16-bit timers (GPT1/2)
- 2 x 6-channel PWM unit (CAPCOM6) good fit for motor control: AC, DC, BLDC
- 12-channel CAPCOM2
- Up to 74 I/O-lines
- Single supply 3.0 V to 5.5 V
- On chip regulators for core voltages
- Advanced power saving features
- Up to 80 MHz @ -40/125 °C
- PG-LQFP-100 Package w/ exposed die pad

**Key Benefits:**
- Single-cycle instruction set with MAC-unit
- Automotive peripheral set (MultiCAN, PWM, CAPCOM)
- On-chip power supply, power control debug support
- Opcode compatibility to C16x, XC16x
**XC2267**
16/32 Bit Microcontroller

**Key Features:**
- Up to 768 KB code/data Flash
- Up to 82 KB SRAM
- High-speed MultiCAN w/ TTCAN
  - 5 nodes, 128 message objects, full CAN 2.0B
- On Chip Debug System
- 16-channel 10-bit Dual ADC
  - parallel conversion, 1.2 µs cycle time
- 6 x serial IO channels
  - Opt.: multiple protocols: LIN, RS232, SPI, I²C, I²S
- Five 16-bit timers (GPT1/2)
- 4 x 6-channel PWM unit (CAPCOM6)
  - good fit for motor control: AC, DC, BLDC
- 12-channel CAPCOM2
- Up to 74 I/O-lines
- Single supply 3.0 V to 5.5 V
- On chip regulators for core voltages
- Advanced power saving features
- Up to 80 MHz @ -40/125 °C
- PG-LQFP-100 Package w/ exposed die pad

**Key Benefits:**
- Single-cycle instruction set with MAC-unit
- Automotive peripheral set
  - (MultiCAN, PWM, CAPCOM)
- On-chip power supply, power control debug support
- Opcode compatibility to C16x, XC16x
**Key Benefits:**
- Single-cycle instruction set with MAC-unit
- Automotive peripheral set (MultiCAN, PWM, CAPCOM)
- On-chip power supply, power control debug support
- Opcode compatibility to C16x, XC16x

**Key Features:**
- Up to 768 kB code/data Flash
- Up to 82 kB SRAM
- High-speed MultiCAN 2 nodes, 128 message objects, full CAN 2.0B
- On Chip Debug System
- 12-channel 10-bit Dual ADC parallel conversion, 1.2 µs cycle time
- 2x LIN, 2x SPI
- Five 16-bit timers (GPT1/2)
- 2 x 6-channel PWM unit (CAPCOM6)
  - good fit for motor control: AC, DC, BLDC
- 16-channel CAPCOM2
- Up to 116 I/O-lines
- Single supply 3.0 V to 5.5 V
- On chip regulators for core voltages
- Advanced power saving features
- Up to 80 MHz @ -40/125 °C
- PG-LQFP-144 Package w/ exposed die pad
Block Diagram
XC2285
**Key Benefits:**
- Single-cycle instruction set with MAC-unit
- Automotive peripheral set (MultiCAN, PWM, CAPCOM)
- On-chip power supply, power control debug support
- Opcode compatibility to C16x, XC16x

**Key Features:**
- Up to 768 kB code/data Flash
- Up to 82 kB SRAM
- High-speed MultiCAN 3 nodes, 128 message objects, full CAN 2.0B
- On Chip Debug System
- 24-channel 10-bit Dual ADC parallel conversion, 1.2 µs cycle time
- 3x LIN, 3x SPI
- Five 16-bit timers (GPT1/2)
- 2 x 6-channel PWM unit (CAPCOM6) good fit for motor control: AC, DC, BLDC
- 16-channel CAPCOM2
- Up to 116 I/O-lines
- Single supply 3.0 V to 5.5 V
- On chip regulators for core voltages
- Advanced power saving features
- Up to 80 MHz @ -40/125 °C
- PG-LQFP-144 Package w/ exposed die pad
**Key Features:**
- Up to 768 KB code/data Flash
- Up to 82 KB SRAM
- High-speed MultiCAN w/ TTCAN
  5 nodes, 128 message objects, full CAN 2.0B
- On Chip Debug System
- 24-channel 10-bit DualADC
  parallel conversion, 1.2 µs cycle time
- 6 x serial IO channels
  Opt.: multiple protocols: LIN, RS232, SPI, I²C, I²S
- Five 16-bit timers (GPT1/2)
- 4 x 6-channel PWM unit (CAPCOM6)
  good fit for motor control: AC, DC, BLDC
- 16-channel CAPCOM2
- Up to 116 I/O-lines
- Single supply 3.0 V to 5.5 V
- On chip regulators for core voltages
- Advanced power saving features
- Up to 80 MHz @ -40/125 °C
- PG-LQFP-144 Package w/ exposed die pad

**Key Benefits:**
- Single-cycle instruction set with MAC-unit
- Automotive peripheral set
  (MultiCAN, PWM, CAPCOM)
- On-chip power supply, power control debug support
- Opcode compatibility to C16x, XC16x
Block Diagram
XC2287
Why to Buy XC2200 Microcontroller
10 Excellent Reasons

- True scalability from high-performance (80 MIPs) to lowest cost (64-Pin)
- Unique HW and SW compatibility to ensure PCB scalability
- Best in class re-use factor for your SW and HW

- AUTOSAR compliant

- User’s choice: 32bit or 16bit
- Best in class CPU/Peripheral performance share

- Automotive proven technology
- Most robust design for highest quality expectations

- Fastest wake up out of application required sleep modes
- Best in class on chip integration: supply, clock, drive, control
Agenda
XC2200 Microcontroller Family for BODY Applications

- Family Concept
- XC2200 Highlights
- Block Diagrams, Benefits
- Technical Details
  - C166SV2 – Core
  - System Control Unit (SCU): Power saving modes
  - Powerful Peripherals: CAPCOM, ADC, USIC, MultiCAN
32bit features of the C166S-V2 Core

- Instruction size: **mixed 16/32bit**
- **RISC architecture**: almost all instructions executed in 1 cycle
- **Scalar architecture**
- **5 stage pipeline**
- **32bit arithmetic**

Software and C-Compiler: With ISO C99 compliant C-code and compilers any transition between architectures is transparently supported:

⇒ Decide yourself how to treat C166-V2 CPU, as 16bit or 32bit machine
A standard module in C166S V2 core used in XC166 and XC2000 MCU families

- Single instruction-cycle
- Single cycle 32-bit additions and subtractions
- Single cycle 16-bit by 16-bit multiplication with 40 bit register and 32 bit results
- Second ALU (Arithmetic and Logic Unit) or an extension of the ALU in the 16 bit C166S V2 core, dedicated for 32 bit and 64 bit operations
- Very useful for the 32 bit and 64 bit mathematical calculation with long (32 bit) and long long (64 bit) data format, and DSP operation
Since May 2006 a new Tasking C compiler is available using Viper technology

Viper perfectly uses MAC instructions and shows same performance on 32bit operations like low end 32bit CPUs

Viper supports all ISO C99 defined data types including long long integer (64 bit)!

In the new Viper compiler the customer can select to treat the XC2000 DSC as 16 or 32 bit machine

Viper compiler is a completely new compiler and provides much better performance in comparison with Tasking V8.6 in speed and code size
Agenda
XC2200 Microcontroller Family for BODY Applications

- Family Concept
- XC2200 Highlights
- Block Diagrams, Benefits
- Technical Details
  - C166SV2 – Core
  - System Control Unit (SCU): Power saving modes
  - Powerful Peripherals: CAPCOM, ADC, USIC, MultiCAN
System control unit (SCU)

Power supply and control
System Control Unit
Power supply and control

- **3.0 - 5.5 V voltage domains**
  - two independent IO supply domains 'A'..'B' and
  - two independent core domains, power generated by independent EVRs which can be set to different voltage levels or switched off
  - internal voltage regulators guarantee equal core performance level over total operating range (3.0-5.5V)

- **Supply Watchdog (IO supply)**
  - Internal Power On Detection, no external PORST circuits necessary
  - Two independent configurable comparators to validate user defined under/over voltage levels (Interrupt or Reset or Status)

- **Power Validation Circuit (Core supply)**
  - Two independent configurable comparators to validate user defined under/over voltage levels (Interrupt or Reset or Status)

- **Short circuit protection**
  - short protection on VDDI Pins, smooth voltage startup
## System Control Unit
### External Power Supply Pins

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Pin</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{DDPA}$</td>
<td>20</td>
<td>Digital <strong>Pad Supply</strong> Voltage for Domain A</td>
</tr>
<tr>
<td>$V_{DDPB}$</td>
<td>2, 36, 38, 72, 74, 108, 110, 144</td>
<td>Digital <strong>Pad Supply</strong> Voltage for Domain B *Note: The on-chip voltage regulators are fed from supply voltage $VDDPB$.</td>
</tr>
<tr>
<td>$V_{SS}$</td>
<td>1, 37, 73, 109</td>
<td>Digital <strong>Ground</strong></td>
</tr>
<tr>
<td>$V_{DDIM}$</td>
<td>15</td>
<td>Digital <strong>Core Supply</strong> Voltage for Domain M</td>
</tr>
<tr>
<td>$V_{DDI1}$</td>
<td>54, 91, 127</td>
<td>Digital <strong>Core Supply</strong> Voltage for Domain 1</td>
</tr>
<tr>
<td>$V_{AREF0}$</td>
<td></td>
<td><strong>Reference</strong> Voltage for A/D Converter ADC0</td>
</tr>
<tr>
<td>$V_{AREF1}$</td>
<td>29</td>
<td><strong>Reference</strong> Voltage for A/D Converter ADC1</td>
</tr>
<tr>
<td>$V_{AGND}$</td>
<td>31</td>
<td><strong>Reference Ground</strong> for A/D Converters ADC0/1</td>
</tr>
</tbody>
</table>

*Note: The on-chip voltage regulators are fed from supply voltage $VDDPB$. 

** ADC0/1**

![Power Domain Table]

---

Page 37
Supervision of external supply voltage (port pins)

- **Detection of the ramp-up voltage**: device can be started without requiring an external power-on reset signal (PORST)
- Monitoring of the external voltage allows the usage of a **low-cost regulator** without additional status signals
- **Two completely independent thresholds**, comparators and respective output signals
- **16 selectable threshold** levels between 2.9 V and 5.5 V
- **Internal reference voltage** generation
- Start-up **reset request**, if supply is below 2.0 V
- **Power Saving** Mode
- **Spike filter** for VDD noise suppression
A PVC monitors the **internal core supply voltage** of a core supply domain. It can be configured to monitor **two programmable independent voltage** levels.

**Feature list**

- Two completely independent comparators and respective output signals
- Voltage levels programmable
- Shut-off, which disables the complete module. OK output signals are set to active or held active (glitch-less).
- Configurable level action selection
# System Control Unit

## Power saving modes

<table>
<thead>
<tr>
<th>Power State</th>
<th>$V_{D,M}$</th>
<th>$V_{D,1}$</th>
<th>$f_{OP}$</th>
<th>Description</th>
<th>Grid State</th>
</tr>
</thead>
<tbody>
<tr>
<td>Active Mode</td>
<td>=1.5 V</td>
<td>=1.5 V</td>
<td>&gt;0 Hz</td>
<td>Peripherals active, CPU active</td>
<td>DD</td>
</tr>
<tr>
<td>Stopover Mode</td>
<td>=1.5 V</td>
<td>&lt;1.0 V</td>
<td>=0 Hz</td>
<td>Status of 1.0 V, modules preserved, wake-up self-timed or external</td>
<td>DA/DB</td>
</tr>
<tr>
<td>Standby Mode</td>
<td>=1.0 V</td>
<td>&lt;1.0 V</td>
<td>=0 Hz</td>
<td>Status of 1.0 V, modules preserved, wake-up external</td>
<td>BA/BB</td>
</tr>
</tbody>
</table>

1. The operating clock can be stopped completely in active mode, without changing the supply voltage.

### Standby

#### DMP_M not clocked

- **State**: BA
  - $V_{D,M}$: 1.0 V
  - $V_{D,1}$: 0.0 V
  - $f_{OP}$: 0 Hz
  - DMP_M: 0 Hz
  - DMP_1: -----
  - Description: Standby with Operational Power Down; DMP_M holds the stored values but is not active. DMP_1 is no longer powered.

- **State**: BB
  - $V_{D,M}$: 1.0 V
  - $V_{D,1}$: 1.0 V
  - $f_{OP}$: 0 Hz
  - DMP_M: 0 Hz
  - DMP_1: 0 Hz
  - Description: Device Standby; DMP_M and DMP_1 holds the stored values but are no longer active.

### Stopover

#### DMP_M clocked

- **State**: DA
  - $V_{D,M}$: 1.5 V
  - $V_{D,1}$: 0.0 V
  - $f_{OP}$: $f_{WU}$
  - DMP_M: $f_{WU}$
  - DMP_1: ----- 
  - Description: Wake-up active with Operational Power Down; DMP_M is active. DMP_1 is not powered.

- **State**: DB
  - $V_{D,M}$: 1.5 V
  - $V_{D,1}$: 1.0 V
  - $f_{OP}$: $f_{WU}$
  - DMP_M: $f_{WU}$
  - DMP_1: 0 Hz
  - Description: Wake-up active with Operational Standby; DMP_M is active. DMP_1 holds the stored values but is not active.

### Active

- **State**: DD
  - $V_{D,M}$: 1.5 V
  - $V_{D,1}$: 1.5 V
  - $f_{OP}$: $f_{PLL}$
  - DMP_M: $f_{PLL}$
  - DMP_1: $f_{PLL}$
  - Description: Maximum Performance; DMP_M and DMP_1 are both active.
System control unit (SCU)

Clock generation
Several Clock sources
1. VCO of PLL
   - Includes OSC-WD feature
2. Low power on chip oscillator, OSC-LP 5MHz
   - Fast start
   - Low power, low accuracy
   - Accuracy can get improved by trimming through SW (3%)
1. Ultra low power oscillator, OSC-ULP 400kHz
   - Ultra low power, accuracy 20%, ~1µA
2. Crystal Oscillator, OSC-HP 4-16MHz
   - High accuracy, 0.5mA max.
5. External Pin
Switch between clock supply modes by SW
System Control Unit
Wake-up timer
The oscillator watchdog monitors the incoming clock from OSC_HP and checks if it fits for an operation in Normal Mode.

Only incoming frequencies that are too low (below 300 kHz) to enable a stable operation of the VCO circuit are detected.

As reference clock the internal oscillator (OSC_PLL) frequency $f_{\text{INT}}$ is used and therefore the internal oscillator has to be put into operation.
The following sources can trigger a reset:

- **1 External power-on hardware reset**: PORST, (cold reset)
- **3 External System Request** reset triggers; ESR0, ESR1, and ESR2, (cold/warm reset)
- **Supply Watchdog** reset request trigger; (SWD), (cold reset)
- **Power Validation** reset request triggers; (cold reset)
- **Watchdog Timer** (WDT) reset request trigger, (cold/warm reset)
- **Software reset** (SW), (warm reset)
- **CPU reset** (CPU), (warm reset)
- **Debug** (OCDS) reset request trigger, (warm reset)
- **Memory parity and ECC** (MP), (warm reset)
- **JTAG** reset (special reset)
Agenda
XC2200 Microcontroller Family for BODY Applications

- Family Concept
- XC2200 Highlights
- Block Diagrams, Benefits
- Technical Details
  - C166SV2 – Core
  - System Control Unit (SCU): Power saving modes
  - Powerful Peripherals: CAPCOM, ADC, USIC, MultiCAN
Capture
Compare Units

Best in class
- High-resolution capture and compare
- **Synchronized** PWM channels
- 3 + 3 + 1 PWM outputs
- Powerful capture modes
- Optimized modes for **electric drive control** from low- to high-end
- Complete **shadow buffer**
- Start-stop control
- **Counting inputs** (XC2000)
- Capability to **trigger ADC**
- **Emergency stop** input
- **Digital dead-time control** for power inverters
- Up to 4 CCU6 modules with available **synchronous** start for all timers (XC2000)
Analog Digital Converter (ADC)

Best in class
Analog – Digital – Converter

**Analog Features**

- Operating voltage range from **3 V to 5.5 V**
- Input multiplexer **width of 16 possible analog input** channels
- Conversion time about **1µs to 1.5µs, TUE of 2 LSB @ operating voltage 5V**
- Possibility to select the **reference voltage** among different sources (VAREF and 1 alternative reference input at channel 0)
- Programmable sample time (in periods of fADCI)
- **Cancel feature** for running conversions
- Wide range of accepted analog clock frequencies fADCI and clock duty cycles (minimum high and low times)
Digital Features

- 8 independent result registers
- Different conversion trigger (e.g. external events, auto scan, programmable sequence, timer for equidistant sampling, etc.)
- Possibility to synchronize two ADC modules for concurrent conversion starts
- External analog multiplexer is supported
- Different sampling times for different channels can be configured
- Possibility to cancel running conversions on demand and to restart them automatically
- Flexible interrupt generation (PEC support) with a scalable number of interrupt service nodes
- Synchronous data exchange between the digital part and the analog part
- Support of power saving modes
Analog – Digital – Converter

■ Arbiter
  - Scans regularly the request sources to find the channel with the highest priority. The priority of each source can be programmed individually.

■ Channel Control registers
  - Defines how the conversion has to be done: (Limit checking, parallel conversion, etc.)

■ Request sources
  - Several events can trigger the analog conversion

■ Input class registers
  - Defines the behavior (sample time, etc.) of the analog input

■ Result registers
  - Up to 8 registers are able to store the conversion result
Power Saving Modes
- Analog part off / on
- Power reduction mode (10µs / 3 µs weak up)

Wait for start mode
- Current conversion is completed normally, next pending conversion takes place as soon as possible

Wait for read mode
- If 2 requested sources target the same result register the lower priority cannot be interrupted by the higher one

Cancel Inject repeat
- Current conversion is aborted immediately if a conversion with a higher priority has been found

Auto scan mode is supported

Equidistant sampling can be delivered by connecting external timers
Data Reduction
- The incoming result is added to the value already stored in the result register and the data reduction counter is decremented until it becomes zero, then a interrupt is generated.

Limit Checking
- Comparing the conversion result to two selected boundary values.
- The boundary values can be programmed.
- An interrupt can be generated according to the limit check result.

Result FIFO Functionality

Synchronization of both ADC modules
- One Master Kernel / one slave kernel

External Trigger Events
- GPT12, CAPCOM6 (Timer T13PM), CAPCOM2 (Channel 31)

Pseudo Parallel sampling mode
- By converting the channels A-B-B-A in a sequence quickly one after the other
Universal Serial Interface (USIC*)

*Multiple protocol handling available as optional feature
Each USIC* channel

- is capable of handling **UART, SSC, LIN, IIC** and **IIS**
- can be **individually configured** (incl. baud rate generation)
- can handle **full duplex data** transfers
- can be **reprogrammed without chip reset***
- a USIC* module is a cluster of 2 **independent**, identical USICs

*Multiple protocol handling available as optional feature
Universal Serial Interface (USIC*)

- **UART (ASC, asynchronous serial channel)**
  - module capability: **receiver/transmitter** with max. baud rate $\frac{f_{sys}}{4}$
  - application target baud rate range: **1.2 kBaud to 3.5 MBaud**
  - number of **data bits** per data frame **1 to 63**
  - **MSB or LSB** first

- **LIN** Support by HW (low-cost network, baud rate up to 20 kBaud)
  - data transfers based on ASC protocol
  - **baud rate detection** possible by built-in capture event of baud rate generator
  - **checksum** generation under SW control for higher flexibility

- **SSC/SPI** (synchronous serial channel with or without slave select lines)
  - module capability: **slave** mode with max. **baud rate** $f_{sys}$
  - module capability: **master** mode with max. **baud rate** $\frac{f_{sys}}{2}$
  - application target baud rate range: **2 kBaud to 10 MBaud**
  - number of **data bits** per data frame **1 to 63**, more with explicit stop condition
  - **MSB or LSB** first

- **IIC** (Inter-IC Bus)
  - application baud rate **100 kBaud to 400 kBaud**

- **IIS** (infotainment audio bus)
  - module capability: receiver with max. **baud rate** $f_{SYS}$
  - module capability: transmitter with max. **baud rate** $\frac{f_{SYS}}{2}$
  - application target baud rate range: up to **26 MBaud**

*Multiple protocol handling available as optional feature*
**Universal Serial Interface (USIC*)**

**Input signals:** DX0, DX1, DX2

<table>
<thead>
<tr>
<th>Selected Protocol</th>
<th>Shift Data Input (handled by DX0)</th>
<th>Shift Clock Input (handled by DX1)</th>
<th>Shift Control Input (handled by DX2)</th>
</tr>
</thead>
<tbody>
<tr>
<td>ASC, LIN</td>
<td>RxD</td>
<td>optional: external frequency input or TxD collision detection</td>
<td>optional: transmit data validation</td>
</tr>
<tr>
<td>SSC, SPI (master)</td>
<td>DIN (MRST, MISO)</td>
<td>optional: external frequency input or delay compensation</td>
<td>optional: transmit data validation or delay compensation</td>
</tr>
<tr>
<td>SSC, SPI (slave)</td>
<td>DIN (MTSR, MOSI)</td>
<td>SCLKIN</td>
<td>SELIN</td>
</tr>
<tr>
<td>IIC</td>
<td>SDA</td>
<td>SCL</td>
<td>optional: transmit data validation</td>
</tr>
<tr>
<td>IIS (master)</td>
<td>DIN</td>
<td>optional: external frequency input or delay compensation</td>
<td>optional: transmit data validation or delay compensation</td>
</tr>
<tr>
<td>IIS (slave)</td>
<td>DIN</td>
<td>SCLKIN</td>
<td>WAIN</td>
</tr>
</tbody>
</table>

*Multiple protocol handling available as optional feature*
### Universal Serial Interface (USIC*)

**Output signals:** DOUT, SCLKOUT, MCLKOUT, SELO[7:0]

<table>
<thead>
<tr>
<th>Selected Protocol</th>
<th>Shift Data Output</th>
<th>Shift Clock Output</th>
<th>Shift Control Outputs</th>
<th>Master Clock Output</th>
</tr>
</thead>
<tbody>
<tr>
<td>ASC, LIN</td>
<td>TxD</td>
<td>not used</td>
<td>not used</td>
<td>optional: master time base</td>
</tr>
<tr>
<td>SSC, SPI (master)</td>
<td>DOUT (MTSR, MOSI)</td>
<td>master shift clock</td>
<td>slave select, chip select</td>
<td>optional: master time base</td>
</tr>
<tr>
<td>SSC, SPI (slave)</td>
<td>DOUT (MRST, MISO)</td>
<td>optional: independent clock output</td>
<td>not used</td>
<td>optional: independent clock output</td>
</tr>
<tr>
<td>IIC</td>
<td>SDA</td>
<td>SCL</td>
<td>not used</td>
<td>optional: master time base</td>
</tr>
<tr>
<td>IIS (master)</td>
<td>DOUT</td>
<td>master shift clock</td>
<td>WA</td>
<td>optional: master time base</td>
</tr>
<tr>
<td>IIS (slave)</td>
<td>DOUT</td>
<td>optional: independent clock output</td>
<td>not used</td>
<td>optional: independent clock output</td>
</tr>
</tbody>
</table>

*Multiple protocol handling available as optional feature*
Universal Serial Interface (USIC*)

Basic Data Buffer
General

*Multiple protocol handling available as optional feature
Universal Serial Interface (USIC*)

FIFO Buffer Structure
General

64 FIFO buffer entries!

*Multiple protocol handling available as optional feature
Transmit Buffering
Transmit Control Information

Additional control parameters for data transfer. Dynamically change the:

- Data word length (WLEMD)
- Frame length (FLEMD)
- Select output control (SELMD)
- Word address control (WAMD)

*Multiple protocol handling available as optional feature*
MultiCAN module

Best in class
MultiCAN

Feature set

- Conform to specification **V2.0 B active**
- **2-6 independent CAN nodes** available
- Dedicated control registers for each CAN node
- **32-256 message objects**, separately highly flexible assigned to CAN nodes
- **Multiple FIFOs** with free configurable length
- **Data transfer rate up to 1MBaud**, separately programmable for each node.
- **Gateway** functionality
MultiCAN
CAN module - module block structure
Message objects
up to 6 CAN nodes share message buffer of 256 objects
Message objects

- 256 independent message buffers (objects) are available

<table>
<thead>
<tr>
<th></th>
<th>identifier</th>
<th>data</th>
<th>status</th>
<th>control</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>254</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>255</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

shared message buffer area

- Each message object consists of the following sub-registers:
  - MO Control
  - MO Data
  - MO Arbitration ID
  - MO Acceptance Mask
  - MO Interrupt Pointer
  - MO FIFO/Gateway Pointer
  - MO Function Control

\[ \text{MO\_BASE} = 1000_{16} + n \times 20_{16} \]

\[ \text{MO\_BASE}^+ \]
The received identifier from the bus is compared to the programmed identifiers in the message objects:

- Each identifier bit can be individually tagged “don’t care” by an acceptance mask, groups of identifiers can be received by the same message object.
- Each message object has its own identifier and acceptance mask.
MultiCAN

CAN module - interrupt nodes

- interrupt selection to 16 interrupt nodes via SFR Message Object n Interrupt Pointer Register MOIPRn

- flexible structure of interrupt generation
  - separation of different tasks supported
  - different request priorities programmable

selection via node pointer

interrupt x

interrupt y
Enhanced FIFO Feature

Advanced Message Object Functionality

- Message Objects can be combined to build FIFO message buffers of arbitrary size, which is only limited by the total number of message objects.
- Message objects can be linked to form a gateway to automatically transfer frames between 2 different CAN busses. A single gateway can link any two CAN nodes. An arbitrary number of gateways may be defined.
Messages can be organized as FIFO buffers for transmission and reception.
Gateway Mode

- Gateway mode allows transfer of messages between two nodes without CPU intervention.
- Two nodes may operate at different Baudrates.
- Gateway FIFOs can be built.
http://www.infineon.com

„Never stop thinking“