Microcontrollers

AppNote AP1670

IBIS Models for Infineon 16 bit Microcontrollers

Infineon Technologies provides a series of IBIS (I/O Buffer Information Specification) models for its 16 bit microcontrollers. IBIS represents an industry standard used to model the output driver characteristics of a device to help users decide what kind of termination, filter components and even layout technique they may need in their system.

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Page of actual Rel.	Page of prev. Rel.	Subjects changes since last release
5	5	Updated list of available IBIS models

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1 Introduction

Infineon Technologies provides a series of IBIS (I/O Buffer Information Specification) models for its 16 bit microcontrollers. IBIS represents an industry standard used to model the output driver characteristics of a device to help users decide what kind of termination, filter components and even layout technique they may need in their system. A commercially available tool suite was used to generate IBIS models based on version 2.1 as a common platform for all concerned products. A list of tabulated current versus voltage (I/V) characteristics, rise and fall characteristics as well as package information are part of each modeled output driver.

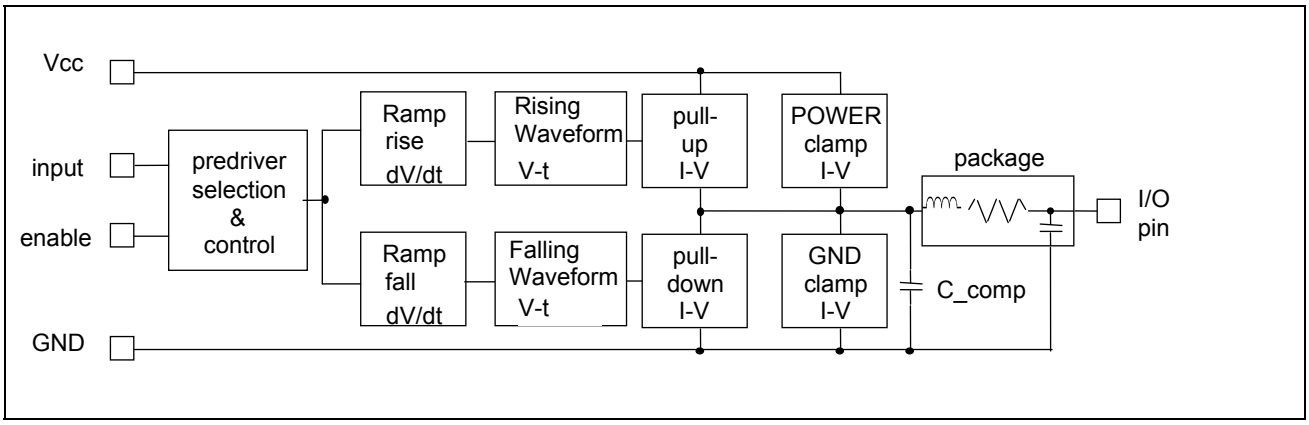

Figure 1: Characterization of output drivers with IBIS

2 General aspects on the available IBIS models

- The currently available IBIS models are of Version 2.1, which is widely implemented in the common tools of signal integrity simulators.

- All the data are generated through HSPICE simulations. To generate the HSPICE models, already available model formats were used and converted. The models of the clamping diodes could not be modeled yet in neither simulation platform, consequence, the models do not have included the whole effects of the clamping diodes (**Power/Ground clamp**).

- Each **I/O pin** comes along with a single model, as it is sufficient for the very most applications. If the pin can be switched by software or hardware to another driver type, then the model has to be changed manually, because of the missing keyword “model selector” only available in IBIS version 3.0 upwards.

- The silicon die capacitance **C_comp** is derived by simulation with HSPICE.

- The temperature range over which all the V-I and V-t curves are derived is from 0° C to 70° C, having 25° Celsius as typical temperature.

- The voltage range tolerance of the supply voltage varies from the typical value of 5V to a +10% and –10% values of the typical value. Also the process variation from nominal to strong and weak is considered.

- The static V-I curves (**Pullup, Pulldown**) are simulated in the voltage range from about –3.0 V up to 6.5 V, because of serious convergence problems in HSPICE outside this region.

- The ramp data define the rise and fall time the signal goes from 20% to 80% of its final value. The ramp data are derived from simulation of the output buffer without package parasitics.

- Also the “waveform” simulations were done without package parasitics. The testfixture consists, as required in the IBIS cookbook, only of a resistive load of 50Ω, if not otherwise required by the buffer specification.

- The dynamic V-t curves (**Ramp up/Ramp down**) are simulated in general with a 50Ω load connected to the Vdd and consecutively to GND, so that four waveforms will be available for each model.

- The RLC-values of the **package** model were delivered from the package manufacturer and represent an average over all the package pins. The minimum/maximum values of the package parasitics stands for the center/corner data of the packages. The typical value is in general the average between minimum and maximum.

3 Products covered by IBIS models

Infineon Technologies provides free models of the products listed below.

Note that the shrinked versions of these products (fabricated in 0.45µm CMOS) show a deviation less than 10% in switching characteristics from those listed. Therefore no dedicated IBIS are provided.

Table 1: 16 bit microcontroller products and IBIS models

Product	Process	VDD	Package	File Reference
C161JI/JC/CS-32FF-CB	0.5µm CMOS	5V	TQFP-128	C161JI.ibs
C161O-HA	0.5µm CMOS	3.3V	MQFP-80	C161O_HA_3V3.ibs
C161PI-LM-AA	0.5µm CMOS	5V	MQFP-100	C161PI_LM_AA.ibs
C161PI-LM-AA	0.5µm CMOS	3.3V	MQFP-100	C161PI_AA_M_3V3.ibs
C161PI-LF-AA	0.5µm CMOS	5V	TQFP-100	C161PI_LF_AA.ibs
C161PI-LF-AA	0.5µm CMOS	3.3V	TQFP-100	C161PI_AA_T_3V3.ibs
C164CI-8RM-AB	0,5µm CMOS	5V	MQFP-80	C164CI_8RM_AB.ibs
C165-L25F	0.5µm CMOS	5V	TQFP-100	C165_L25F.ibs
C165-HA	0.5µm CMOS	3.3V	MQFP-100	C165_HA_M_3V3.ibs
C165-HA	0.5µm CMOS	3.3V	TQFP-100	C165_HA_T_3V3.ibs
C167CR-LM	0,5µm CMOS	5V	MQFP-144	C167CR_LM.ibs
C167CR-4RM	0,5µm CMOS	5V	MQFP-144	C167CR_4RM.ibs
C167CR-16RM	0,5µm CMOS	5V	MQFP-144	C167CR_16RM.ibs
C167S-4RM	0,5µm CMOS	5V	MQFP-144	C167S_4RM.ibs
C167SR-LM	0,5µm CMOS	5V	MQFP-144	C167SR_LM.ibs
C167CS-32FM-CB	0,5µm CMOS	5V	MQFP-144	C167CS_32FM_CB.ibs
C167CS-4RM/LM-AA	0,5µm CMOS	5V	MQFP-144	C167CS_4RM.ibs
C167CS-LM-BA	0,5µm CMOS	3.3V	MQFP-144	C167CS_LM_BA_3V3.ibs