L90

90 nm CMOS Platform Technology

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Never stop thinking

Infineon L90 –
Technology for Logic and Analog/Mixed Signal Applications

Infineon Stands for Customer Orientation
Target Markets & Applications / Core Competencies

Automotive, Industrial & Multimarket

Car Electronics: power train, safety management, body & convenience, infotainment,
Power control: distributed power generation, automation / motor control, transportation, power supplies, medical, building control,
Chipcard & Security: communications, payment, identification, entertainment

Communication Solutions

Wireless communications: mobile phones, cellular base stations, cordless telephones, RF technology for short, medium and long-range distances, TV receivers, navigation,
Wireline communications: Voice and broadband data communications, integrated voice and data communications, wireless infrastructure, home networks

Customers

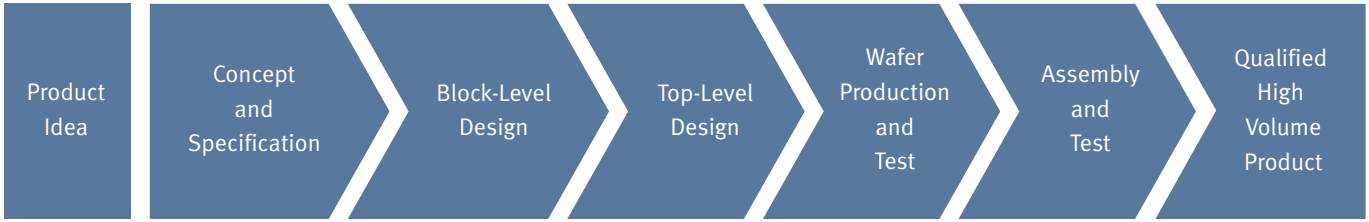
Analog/Mixed Signal

RF

Power

Embedded Control

Complete Offering over the Value Chain



Support & Services from Infineon Technologies

- Process design kit (PDK)
- Concept reviews
- Design and layout reviews
- Concept and specification
- Design and layout services
- IP blocks
- Test development
- Manufacturing services
- Logistics
- Quality
- Assembly and test

Design System, Tools, Methods, Environment

Fully integrated design system

- "Exportable" + flexible design infrastructure
- Leading RF design and highly optimized low power methodology
- Fast cycle time from RTL to chip
- Re-usable IP macros leveraging IFX' ASSP roadmaps
- Netlist and RTL sign-off procedures with tight parameter bands and small margins for most efficient designs
- DFM - Design for Manufacturability

Intimate technology know-how for full exploitation of internal and 3rd party manufacturing for first-time right designs

- Methodology to assess cost, performance, leakage/power of target manufacturing platform and site
  - Simulation environment for frontend (device) and backend technology
  - Testchip architectures for accurate model-hardware correlation
- Area optimized standard cell libraries and high performance I/O
- Highly configurable memories, optimized for lowest standby power, small area and high yield
- Digital and analog circuit and system know-how for custom solutions

L90 is a high performance technology optimized for high frequency, low power, and mixed-signal applications with excellent signal-to-noise ratio

- 90 nm CMOS Platform Technology for Logic and Analog/Mixed Signal applications
- High density, high performance, low power technology
- Metallization: 4 – 5 fine pitch layers (Cu)
  1 – 2 double pitch layers (Cu)
  1 redistribution/pad metal layer (Al)
- Supply voltage of 1.0 V (1.2 V) ±10% for standard digital operation
- I/O voltage of 2.5 V (3.3 V capable with area restriction)
- Supply voltage down to 0.9 V for low power (active well concepts)
- SRAM cell size 1.26 μm^2
- Packing density: > 350 kGates/mm^2 (SP device)

Standard Features and Options

Standard Features

- Non-epi substrate
- 193 nm & 248 nm lithography with OPC & Att. PSM for critical layers
- Shallow-Trench Isolation (STI)
- Triple gate-oxide
  - 1.6 nm for standard and high performance applications (SP family)
  - 2.2 nm for low leakage applications (LL family)
  - 5.2 nm for I/O and analog circuits
- MOS Devices (N & P)
  - Regular V_T/High V_T/Low V_T
  - Thick oxide for 2.5 V analog and 2.5 V I/Os (3.3 V capable)
- Salicide technology ($CoSi_2$)

Options

- Mixed V_T design
- Triple well
- Triple gate oxide
  - Combines low leakage and standard devices for low power & mixed-signal applications
- Salicide-blocked devices
- Embedded memory
  - eSRAM, via prog. ROM
- Cu metallization: 5 to 7 metal layers in FSG IMD
- Last metal aluminum also used for redistribution
- FUSES: salicided-poly eFuse
- Additional devices: low & high ohmic resistors, metal & thick oxide capacitors, parasitic bipolar, diodes, inductors

Device Specifications

		SP-HVT		SP		LL-HVT	I/O & Analog
V_{DD}	[V]	1.0/1.2				1.2	2.5
T_{OX}	[nm]	1.55				2.2	5.2
L_{Gate}	[nm]	70				80	230
V_T N V_T P	[mV]	370 300	360 280	250 200	230 180	535 450	440 420
$I_{d\text{-}sat}$ N $I_{d\text{-}sat}$ P	[µA/µm]	480 195	710 300	655 250	900 370	385 155	600 270
$I_{d\text{-}leak@27^{\circ}C}$ N $I_{d\text{-}leak@27^{\circ}C}$ P	[nA/µm]	0.25 0.40	0.35 0.55	7 8	10 11	0.005 0.012	0.01 0.009
$I_{d\text{-}leak@85^{\circ}C}$ N $I_{d\text{-}leak@85^{\circ}C}$ P	[nA/µm]	2.0 3.7	tbd	29 51	tbd	0.11 0.225	2.8 1.6

Standard Cell Libraries

Features and Benefits

- Targeted for IFX standard high V_T (SP-HVT), low leakage high V_T (LL-HVT), standard high performance (SP) and extended high performance (SP-LVT) process options
- Available for typ. V_{DD} voltage range 1.0 V ... 1.2 V, slow mode down to 0.9 V
- Optimized for performance and low leakage current
- Offers Multi V_T to reduce leakage (SP-HVT and LL-HVT can be mixed)
- Customer tailored layout, optimized for performance and place & route fully exploiting the process capabilities
- Offers a big variety of special cells, e.g. level-shifters, power switches, gated clock, scan version for all flip-flops, etc.

Key Parameters		
Power Supply Voltage	**1.2 V**	**1.0 V**
Number of cells	524	524
Number of tracks	10	10
Number of drive strengths	3 ... 17	3 ... 17
High Performance	**SP – StarLib**	
Gate density [k/mm²]	385	385
ND2, typ. delay, FO = 2 [ps]	17	21
ND2, typ. power, C_L = 0 [nW/MHz]	6.2	4.4
Leakage (ND2 equiv., typ.) [nA]	11.5	8.5
Standard	**SPHVT – StarLib**	
Gate density [k/mm²]	385	385
ND2, typ. delay, FO = 2 [ps]	23	28
ND2, typ. power, C_L = 0 [nW/MHz]	5.3	3.8
Leakage (ND2 equiv., typ.) [nA]	0.74	0.53
Low Leakage	**LLHVT – StarLib**	
Gate density [k/mm²]	355	355
ND2, typ. delay, FO = 2 [ps]	37	56
ND2, typ. power, C_L = 0 [nW/MHz]	4.5	3.3
Leakage (ND2 equiv., typ.) [pA]	16	12

SRAMs and ROMs

Functions

- Single Port RAMs (low leakage and high speed versions)
- Dual Port RAMs
- ROMs (via programmable)

Features

- Typical voltage range 1.0 V ... 1.2 V ±10% (slow mode down to 0.9 V)
- Special features (e.g. single-bit write, BIST)
- Power efficient, leakage-only static power
- Edge-sensitive synchronous interfaces
- Scalable word redundancy enabled by electrical fuses
- Highly configurable, flexible aspect ratio
- Optimized for area and yield
- Routing over macro possible

Key Parameters					
MemLib	Low Power/Leak. Single Port SRAM	High Speed Single Port SRAM	Low Power/Leak. Dual Port SRAM	High Speed Dual Port SRAM	Sync. High Speed Via2 ROM
Core cell size	1.26 µm²	1.26 µm²	2.38 µm²	2.38 µm²	0.256 µm²
Max. size	256 kbit	256 kbit	576 kbit	576 kbit	1 Mbit
max. bits/word	128 bit	128 bit	144 bit	144 bit	64 bit
4 k × 16, P/T = typ/27°C	SPHVT-LLHVT	SP-SPHVT	SPHVT-LLHVT	SP-SPHVT	SPHVT
Area [mm²]	0.146 (CM16)	0.138 (CM16)	0.24 (CM32)	0.24 (CM32)	0.039 (CM32)
T_{cc} @ 1.2/1.0 V	– /2.41 ns	1.02/1.41 ns	– /4.14 ns	1.15/1.61 ns	– /2.73 ns
T_{acc} @ 1.2/1.0 V	– /2.10 ns	0.78/1.13 ns	– /4.02 ns	0.98/1.38 ns	– /1.97 ns
Dyn. Power	– /22	66/47	– /31	92/66	9.7/5.2
av. r/w @ 1.2/1.0 V	µW/MHz	µW/MHz	µW/MHz	µW/MHz	µW/MHz

I/O Libraries

Features and Benefits

- Offers a big set of standard I/O cell libraries, e.g. based on 2.5 V I/O-devices (3.3 V with restrictions):
  - CMOS
  - HS I^2C
  - HSTL
  - LVDS (622 MHz)
  - DDR-1
  - DDR-2
  - MVI Interface
  - I/Os for Mobile RAM
- Has an extended range of standard I/O macros, e.g. based on I/O-2.5 V devices:
  - Universal low swing MHz-oscillator
  - Ultra low power, low voltage kHz-oscillator
  - PCI-Express
  - USB-Macro (LS, FS, HS, OTG)

Key Parameters	
I/O signal range (nom.) Core signal voltage	... 2.5 V 1.32/1.2/1 V
Number of metal layers Standard bond pad pitch Packaging features – Area saving probe & bond pad separation, flexible pitch – Bond over active area concept – Efficient Flip-Chip support	6 60 µm (inline)
ESD hardness (HBM) Latchup immunity (EIA/JESD78)	≥ 2 KV 100 mA
Example: CMOS 1.5 V ... 2.5 V – Standard driver strengths – Cell height without bondpad	4 ... 16 mA 186 µm

Key Design Rules

	Min. Width [nm]	Min. Space [nm]
N-Well	520	520
Diffusion	120	140
Polysilicon	80	160
n+/p+ Isolation	420	
Salicide Blocking	500	500
Contact	120 (fixed)	140
Metal 1	120	120
Via 1	140 (fixed)	160
Metal 2 – 6	140	140
Via 2 – 6	140 (fixed)	140
Metal 7 – 8	280	280

Design Kit

General	Design Package Release	V 2.0.0
	Cadence Release	5.1
	Platform	Solaris, Linux
	Methodology	Full Custom (Analog Mixed Signal Flow)

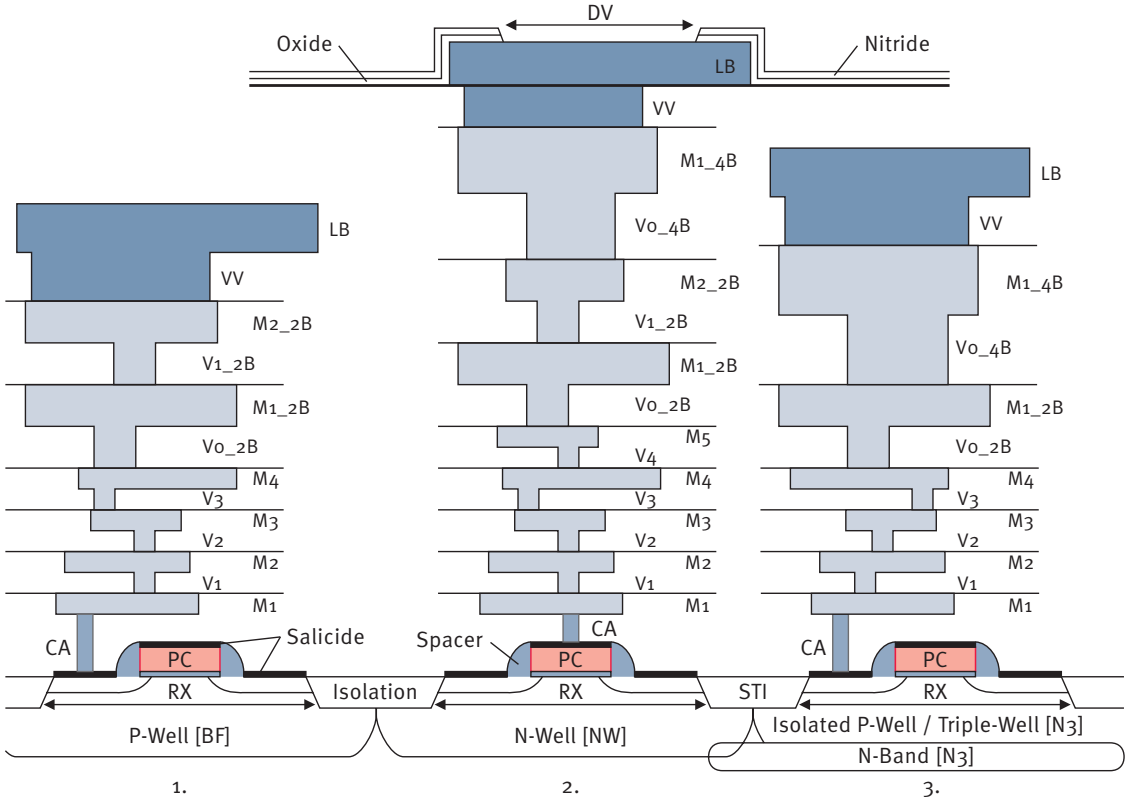
Libraries	IFX Standard Device Libraries	IFXc12n, IFXdevsymbol, IFXdevlayout
	L90: RF Technology Dependent Device Library	Special L90/RF-CMOS Library (varactors, inductors, ...)
	L90 Technology Dependent Cell Library	- L90 LP leakage optimized Starlibs (10-track); logic switches - L90 HS performance optimized Starlibs (10-track) - L90 LP-SP SRAM/LP-DPS RAM/ROM/LP-efuse/p-switches/HDFR - L90 HS-SPSRAM/HS-DP SRAM/ROM/HS-efuse/HDFR CMOS-I/Os; HS I^2C I/Os, kHz Oscillator

Modeling	General	BSIM 4.3
	Active Models	Fixed cell models for RF optimized geometries Sub-circuit models with substrate parasitic and RF noise
	Passive Models	Pre-characterized coils, fixed varactor models, VppCap valid over large frequency range, R-String-Resistor, Sandwich-Caps
	Statistical Simulation	Monte Carlo modeling supported

Design Kit

Supported Tools	Schematic Entry	Composer
	Analog & RF Simulation	Spectre (RF), Titan, Eldo, Nanosim
	Monte Carlo Simulation	Spectre Direct, Titan
	Mixed Signal Simulation	Spectre (S)-Verilog, ADMS, Titan, Eldo, Nanosim
	Layout Creation	Virtuoso-XL
	Digital Simulation	Verilog-XL, Affirma NC
	Place & Route	Magma Blastfusion, VCAR
	Layout Verification	Calibre DRC, ERC, LVS, ESDNetchecks
	RCX Parasitic Extaction	Assura, StarRCXT

Schematic Cross Section of L90 CMOS



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