JEDEC Registration of SMD Top Side Cooling Packages

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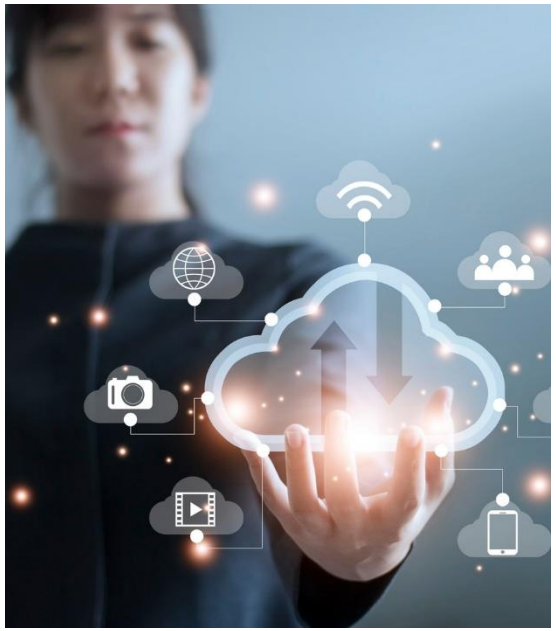
9 February 2023

Decarbonization and digitalization are driving massively power management towards new trends



Efficiency

Weight

Cost

Density

Range

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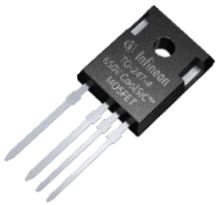
Technology innovation has to be linked with package innovation to enable key trends in eMobility

- Higher power needs
- Higher power density
- Higher efficiency
- Weight reduction

Technology Innovation

- Si
- SiC
- GaN

Package Innovation



Technology alone is only the basis, coupled with package it's the perfect solution for future power needs

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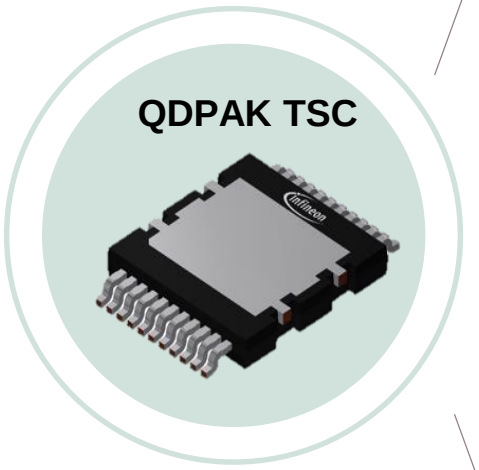
Top side cooling innovation with QDPAK enables key technical trends and contributes to cost savings



Addresses higher power needs : Optimized structure for scallable dies, low ohmic dies and multiple dies are possible

Increased power density: Top side cooling enables highest PCB utilization

Higher efficiency: Optimized costruction with low ohmic properties and ultra low parasitic inductance enables higher efficiency

Weight reduction: overall cooling and thermal optimization enables to build smaller housing and safes material and weight

Higher power, more dense designs coupled by higher efficiency will be enabled by new package technology

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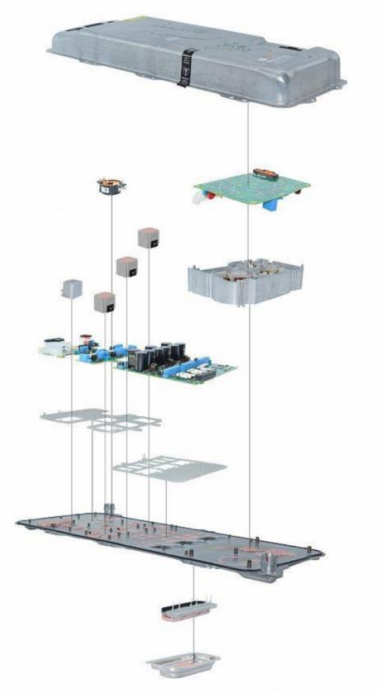
Top side cooling innovation with QDPAK high optimization in manufacturing, enabling faster assembly at lower system cost

Simplified assembly



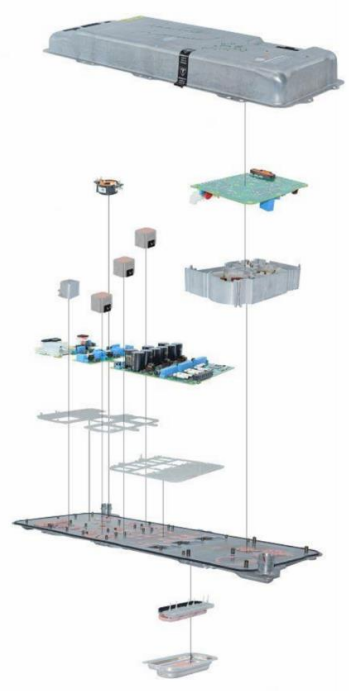
41 -76%
Nr. of connectors

PCB: FR4

No stacking of different boards needed

One big FR4 PCB:
all power components
and IC/driver/magnetics

System cost optimization



16$ -33%
Assembly costs

41$ -18%
FR4 PCB cost

41 -76%
Nr. of connectors

* Assembly analysis based on A2MAC comparison of traditional vs top side cooling design

Faster and highly automated manufacturing paired with lower assembly cost are key benefits

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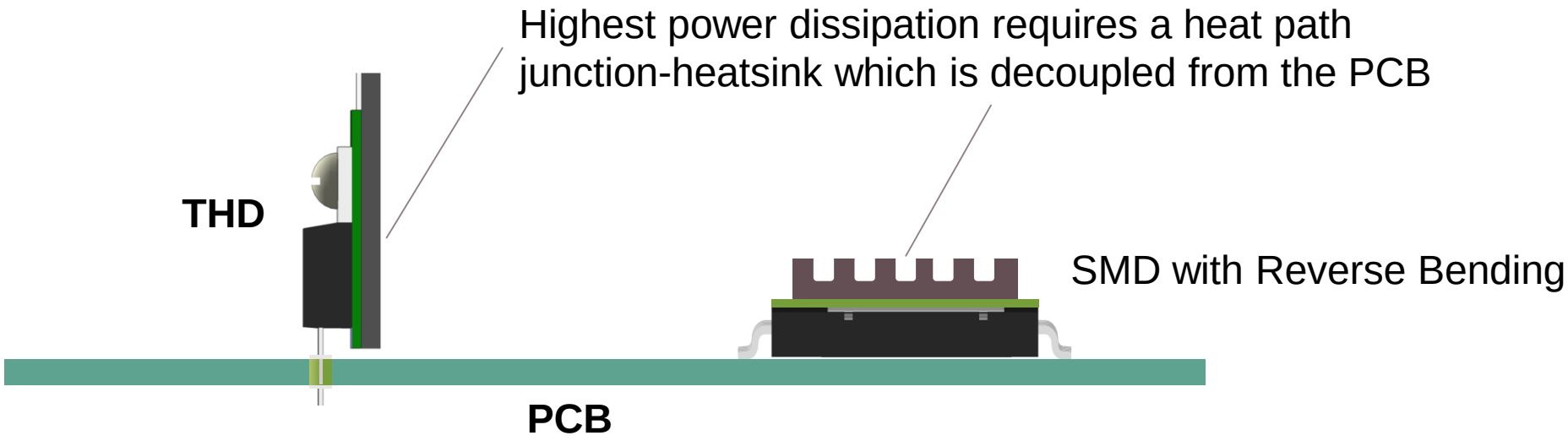
Thermal management drives power application

Thermal design of a power application board

Optimizing MOSFET application require the lowest possible thermal resistance of the system (R_{thja}) in combination with a highest possible junction temperature (T_j)

- Maximizing the heat flow into the heatsink
- Minimizing the heat flow into the Printed-Circuit-Board (PCB)

This **requires a Through-Hole-Device (THD) or a TSC-Extension of Surface-Mounted-Device (SMD)**



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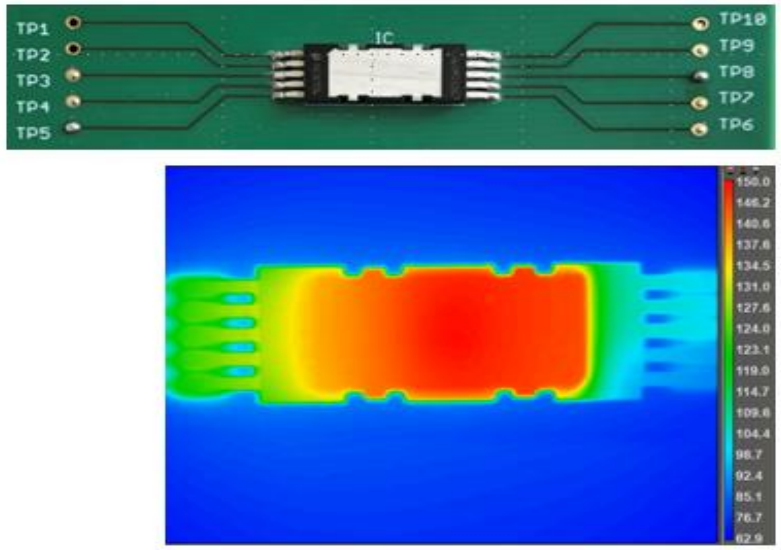
Thermal decoupling gives higher performance & robustness

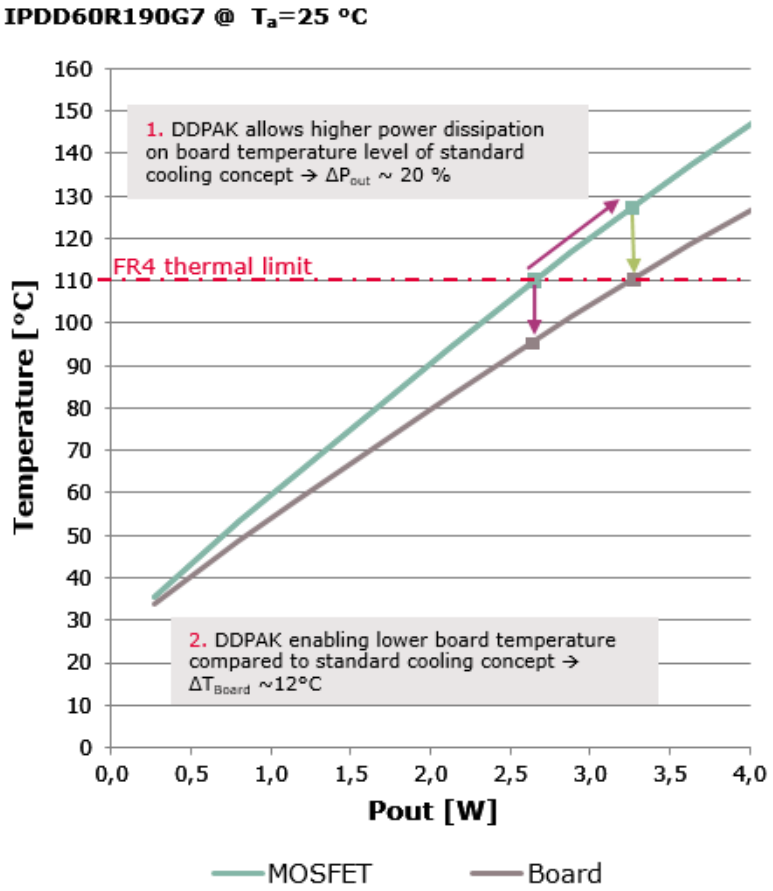
Set up and benefit of top-side cooling concept



In today's common bottom-side cooling concepts the temperature of the PCB equals the temperature the MOSFET.
The top-side cooling concept of DDPAK allows thermal decoupling of PCB to chip junction and enables

- **~ 20% higher power dissipation at same board temperature or**
- **Improved system lifetime based on reduced board temperature**

Temperature Measurement @ T_a = 25°C



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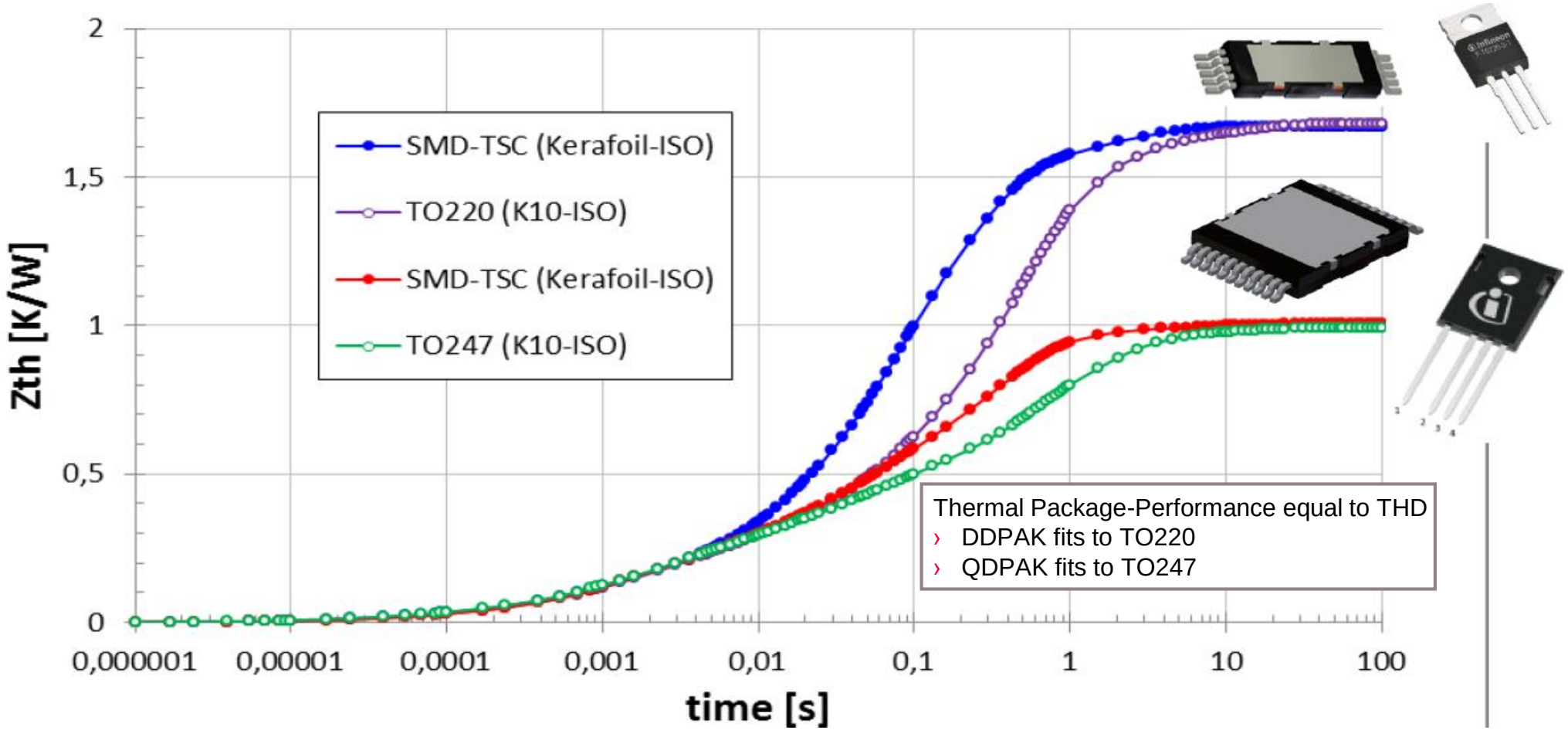
Thermal adaption with standard THD (TO220 & TO247)

Set SMD/THD Package-Comparison



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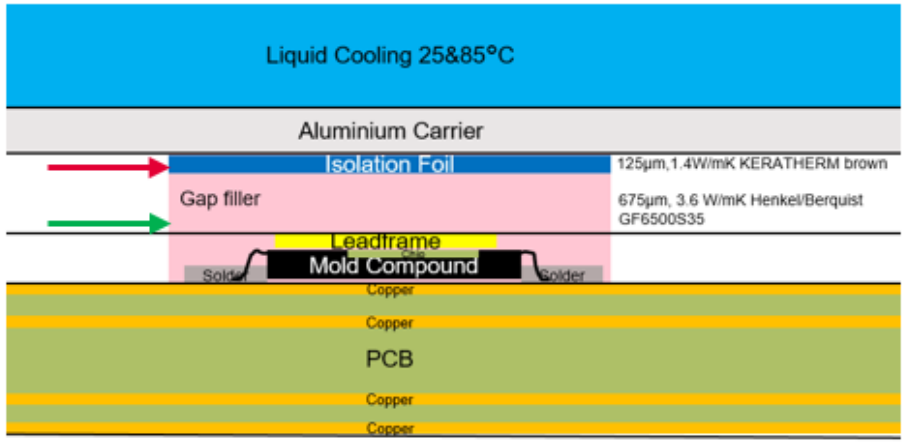
Thermal performance within power application (e.g. OBC)

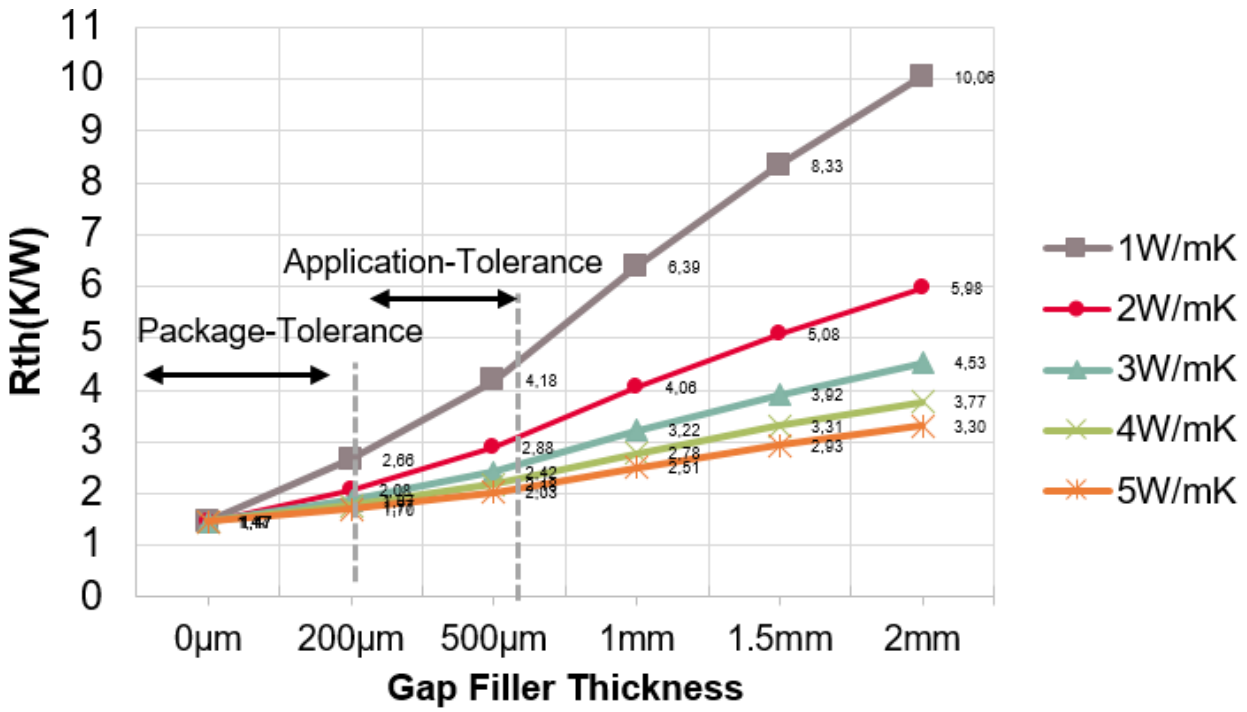


Isolation Foil	125 um, 1.4 W/(mK)	fixed
Gap Filler	200 … 2000 um	
	1… 5 W/(mK)	would be varied

Isolation Management by Isolation Foil → Dedicated Foil-Performance covers Appl.-Requirements

Thermal Management by Gap Filler → Compensation of Package- & Appl.-Tolerances

Gap Filler Influence with Isolation Foil: 1.4 W/mK (5 kV Iso-Strength)



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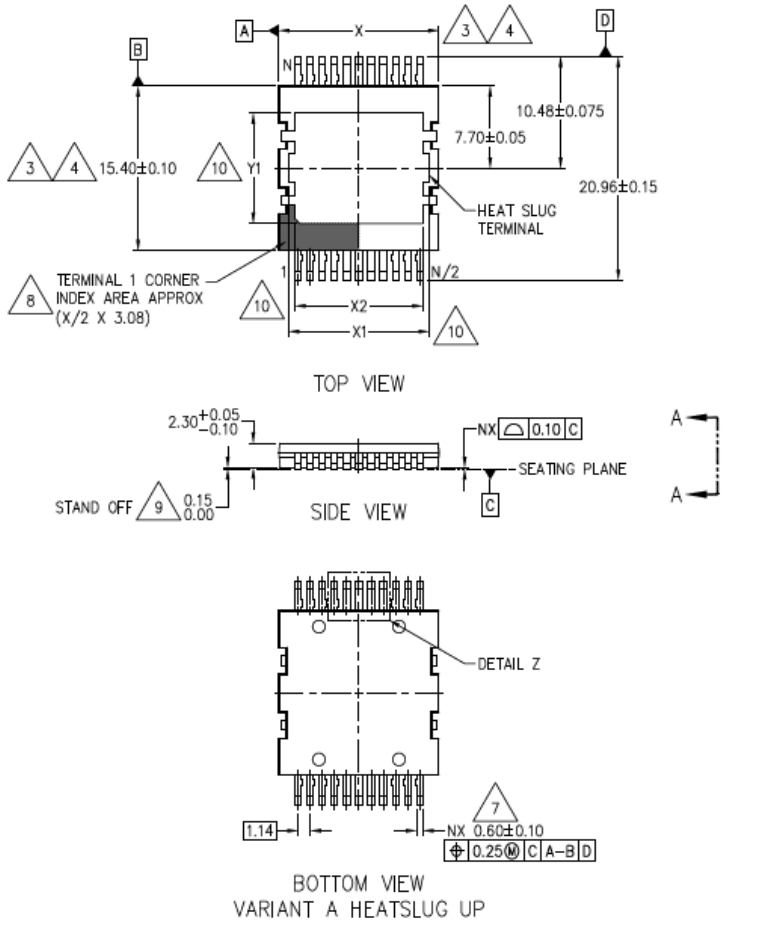
Thermal implementation requires standardization (MO-354)



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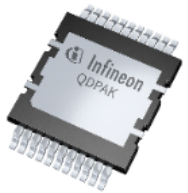

QDPAK TSC

JEDEC registrated

DDPAK TSC

JEDEC is an independent semiconductor organization and standardization body headquartered in the U.S., with over 300 members including computer companies – source to popular package drawings for semiconductors such as TO220 & TO247.

Why is JEDEC release of our TSC* Packages important?

- To drive standardization in the semiconductor industry for TSC* Packages , enabling unified solutions for power trends in the future.
- To enable second source solutions in the market with same footprint and helping customer to widely adopt this technology faster.

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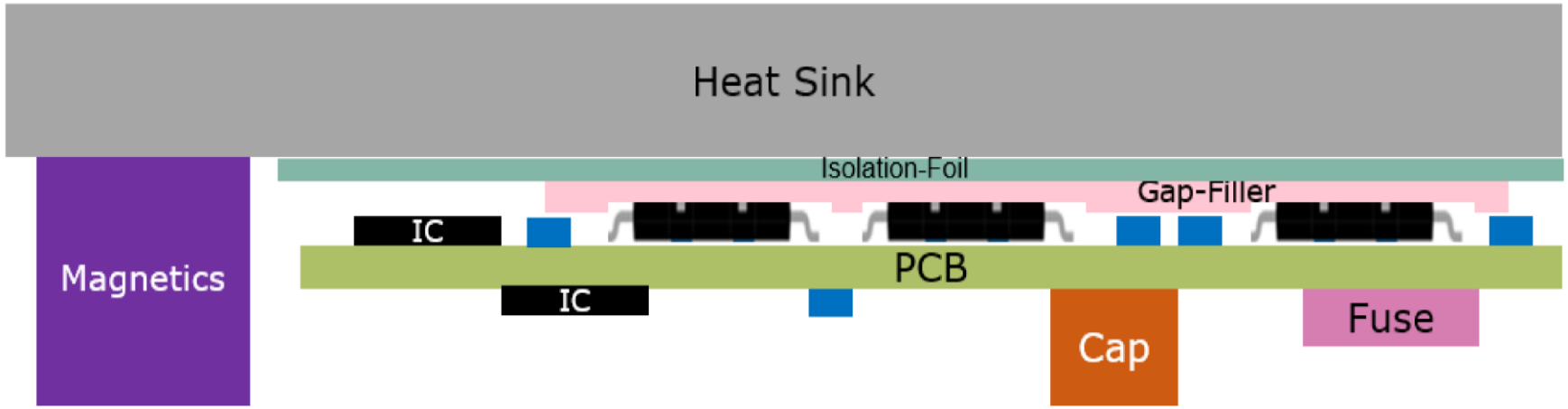
Thermal redistribution requires a common height (2.3 mm)



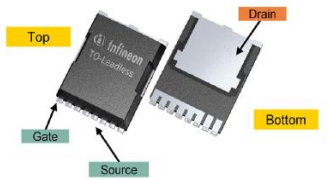
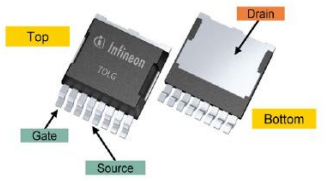
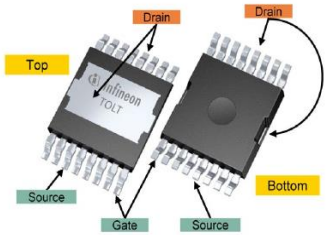
Common package height supports easy appl.-cooling

› Flat Heatsink-Design ⇔ LowCost-Design

2.3 mm package height fits to SMD TSC & BSC

› Many running SMD already with 2.3 mm

Table 1 TOLL / TOLG / TOLT Package Comparison

TOLL	TOLG	TOLT
		
JEDEC registration #: MO-299B	JEDEC registration #: MO-327A	JEDEC registration #: MO-332A
Dimensions: 10x11x2.3 mm	Dimensions: 10x11x2.3 mm	Dimensions: 9.9x15x2.3 mm
Optimized for high current applications	Optimized for Thermal Cycling on Board (TCoB) performance	Optimized for superior thermal performance

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