Sl. No.	Section	Subsection	Change Description	Current Spec *G content	New Spec *H content	Reason for change	Customer Impact
1	All	All	Traveo™ II naming	Traveo™ II	TRAVEO™ T2G	Infineon standard naming alignment	None
2	All	All	Trigger MUX signal name	Generic signal	Signal name aligned with Datasheet	Update	None
3	1.2.1 CPU Subsystem	1.2.2.4IMO Clock Source	IMO Tolerence removed	The IMO operates at a frequency of 8 MHz ±1%. The internal trim settings for the IMO can be dynamically updated to provide a tolerance of less than 1%.	The IMO operates at a frequency around 8 MHz.	To be referred to from device specific datasheet	None
4	2 Getting Started	All	NA	Cypress programmer (CYP)	Cypress Auto-Flash Utility (AFU)	Naming correction	None
5	2.3 Development Kits	2.3.2 Evaluation Board	Figure caption	Figure 2-1. Evaluation Board Hook Up	Figure 2-1. Example Evaluation Board Hookup with 176-LQFP CPU Board	Correction	None
6	7.1.8 P-DMA Descriptor Structure	Description	Added description	DESCR_X_CTL - Descriptor X loop control	DESCR_X_CTL - Descriptor X loop control This register is not present for a single transfer descriptor type.	Add information	None
7	7.1.8 P-DMA Descriptor Structure	Description	Added description	DESCR_NEXT_PTR - Descriptor next pointer Note: For a single transfer descriptor type, this register is at offset 0x0c. For a 1D transfer descriptor type, this register is at offset 0x.	DESCR_NEXT_PTR - Descriptor next pointer Note: For a single transfer descriptor type, this register is at offset 0x0c. For 1D and CRC transfer descriptor types, this register is at offset 0x10. For a 2D transfer descriptor type, this register is at offset 0x14.	Add information	None
8	7.3.2 Channels	Description	Added description	none	Trigger multiplexer may not offer for connecting the output triggers of the M-DMA controller and the P-DMA controller to the input triggers of the AXI DMA controller. These triggers can be performed in software, by chaining a descriptor that writes the AXI_DMAC_CHx_TR_CMD register of the AXI DMA controller channel.	Add information	None
9	11.3.2 Multicore Boot	Description	Add content	None	In addition, the CPUSS_CM4_PWR_CTL register is used to check current power mode. Note: The CPUSS_IDENTITY and the CPUSS_CM4_PWR_CTL registers are read from the CM4 master in boot process. Therefore, these registers must allow read access from the CM4 master in boot process.	Clarify operation of CM4 during BootROM	None
10	11.3.4.5 Security Enhancement PPU Configuration in Sflash	Description	Add content	None	11.3.4.5 Security Enhancement PPU Configuration in SFlash	Allignning with Device Enhancement	None
11	18 Clocking System	PLL with SSCG and Fractional Operation (400-MHz PLL)	Add a sentence	-	Note that you cannot operate SSCG and fractional operation together.	Adding information	Minor impact
12	19.1 Reset Sources		Table 19-1 updated in terms of SRAM retention. Note e added.	a. AIRCR.SYSRESETREQ is software reset. b. Yes if there is an orderly shutdown of the RAM. c. Reset occurs if the source triggers during DeepSleep. d. Yes if there is an orderly shutdown of the RAM and the CSV resets is not from CSV_HF0. Note for WDT/SRAM Retention changed	a. AIRCR.SYSRESETREQ is software reset. b. Yes, if there is an orderly shutdown of the RAM. c. Reset occurs if the source triggers during DeepSleep. d. Yes, if there is an orderly shutdown of the RAM only during a warning interrupt. e. Yes if there is an orderly shutdown of the RAM and the CSV reset is not from CSV_HF0.	Enhancement	yes
13	19.1 Reset Sources		Table 19-1: Note changed for WDT/SRAM Retention	b	d	Enhancement	yes
14	19.1 Reset Sources		Table 19-1: Note changed for MCWDT/Debug	a	c	Enhancement	yes
15	19.1 Reset Sources		Table 19-1: Note changed for CSV HF/SRAM Retention	d	e	Enhancement	yes
16	19.1 Reset Sources		Additional note which describes the used areas in retention RAM during boot process. Add reference to SRAM interface chapter.		Note: The SRAM region from (SRAM size minus 6 KB) to (SRAM size minus 2 KB) is used by Cypress firmware during boot operation. Therefore, this region is available to the user; however, data retention across resets is not guaranteed in this area, because it can be overwritten by Cypress boot firmware. See RAM Retention Configuration on page 130 for details.	Enhancement	yes
17	19.1 Reset Sources		Add PXRES	XRES	XRES_L/PXRES	Enhancement	yes
18	19.1 Reset Sources	19.1.6 Programmable Reset	Add description for PXRES		PXRES is a programmable XRES_L trigger. This is a software-accessible register that triggers a full-scope reset equivalent to XRES_L, except it records in a different RES_CAUSE flag, RESET_PXRES. Hardware clears this bit during POR.	Enhancement	yes
19	19.1 Reset Sources		Remove PXRES	XRES_L/PXRES	XRES	Correction	yes
20	19.1 Reset Sources	19.1.6 Programmable Reset	Remove description for PXRES	PXRES is a programmable XRES_L trigger. This is a software-accessible register that triggers a full-scope reset equivalent to XRES_L, except it records in a different RES_CAUSE flag, RESET_PXRES. Hardware clears this bit during POR.	Remove description	Correction	yes
21	19.1 Reset Sources	19.1.11 PMIC Reset	Add new sub chapter		Add PMIC Reset description	Improvement	yes
22	19.1 Reset Sources	19.1.4 Over Current Reset	REGHC support		Add REGHC description	Improvement	yes
23	19.2 Identifying Reset Sources	Table 19-2	Add Reset Sources		Add Reset Sources: RESET_OCD_REGHC RESET_PMIC	Improvement	yes
24	19.2 Identifying Reset Sources	Table 19-2	Remove RESET_PXRES reset source		Remove Reset Source RESET_PXRES	Correction	yes
25	19.1 Reset Sources		SRAM region update		Note: The SRAM region of the last 6 KB is used by the Cypress boot firmware during boot operation. Therefore, this region is available to the user; however, data retention across resets is not guaranteed in this area because it can be overwritten by the Cypress boot firmware. See RAM Retention Configuration on page 130 for details.	Correction	yes
26	19.3 Register List		Add note		Add a note: Check the device datasheet to see if the feature is supported	Correction	yes

27	Section	Subsection	Change Description	Current Spec *G content	New Spec *H content	Reason for change	Customer Impact
28	24.3.5 TX Handling	24.3.5.2Dedicated TX Buffers	NA	If multiple Tx Buffers are configured with the same Message ID, the Tx Buffer with the lowest buffer number is transmitted first.	These Tx buffers shall be requested in ascending order with lowest buffer number first. Alternatively all Tx buffers configured with the same Message ID can be requested simultaneously by a single write access to CANFDx_CHy_TXBAR.	Correction	Minor impact
29	24.3.5 TX Handling	24.3.5.4TX Queue	NA	If multiple queue buffers are configured with the same Message ID, the queue buffer with the lowest buffer number is transmitted first.	In case that multiple Tx Queue buffers are configured with the same Message ID, the transmission order depends on numbers of the buffers where the messages were stored for transmission. As these buffer numbers depend on the then current states of the PUT index, a prediction of the transmission order is not possible.	Correction	Minor impact
30	24.3.5 TX Handling	24.3.5.4TX Queue	NA	An Add Request cyclically increments the Put Index to the next free TX buffer.	The Put Index always points to the free buffer of the Tx Queue with the lowest buffer number.	Correction	Minor impact
31	24.5 TTCAN Operation	24.5.3 TTCAN Gap Control	NA	In time-triggered operation, bit Next_is_Gap = '1' in the reference message will be ignored, and the bits CANFDx_CHy_TTOCN.NIG, CANFDx_CHy_TTOCN.FGP, and CANFDx_CHy_TTOCN.TMG will be considered.	In time-triggered operation, bit Next_is_Gap = '1' in the reference message will be ignored, as well as the bits CANFDx_CHy_TTOCN.NIG, CANFDx_CHy_TTOCN.FGP, and CANFDx_CHy_TTOCN.TMG.	Correction	Minor impact
32	26. LIN	Block Diagram	figure replaced			signal name alignment with DS	No
33	28. Event Generator (EVTGEN)	DeepSleep Interrupt Accuracy Analysis	new			signal name alignment with DS	No
34	28. Event Generator (EVTGEN	all	trigger signal name changed			signal name alignment with DS	No
35	29.3 Trigger Multiplexing	NA	Trigger MUX signal name	The debug mode is indicated by the level trigger input tr_debug_freeze, which is connected to a CPUSS CTI trigger output, sys.tr_cti_out.	The debug mode is indicated by the level trigger input x_DEBUG_FREEZE_TR_IN1 , which is connected to a CPUSS CTI trigger output, CTI_TR_OUTx.	Alignment as per the datasheet	None
36	29.4 Trigger Functionality	NA	Figure 29-8. Example of 1-to-1 Trigger update	1 routing example	2 different routing example	Update	None
37	30. Clock Extension Peripheral Interface (CXPI)	Block Diagram	figure replaced			signal name alignment with DS	No
38	30. Clock Extension Peripheral Interface (CXPI)	P-DMA Transfer Trigger	figure replaced			signal name alignment with DS	No
39	31.3 Operation	Note before figure 31-2 ADC Core Block Diagram	The peripheral clock divider for ADC (CLK_PERI) must be at least 2. The ePass SAR requires a 50/50 duty cycle clock; this is generated only when CLK_PERI is at least 2. ■ Do not divide CLK_GR9; this makes CLK_GR9 = CLK_PERI, keeping all clocks coming to SAR ADC at the same frequency. If these clocks are not equal, it can cause the GRP_CANCELLED bit to be set	Was missing in the *E spec and was added in *F spec, but was not added in the change log	The description has been added	Was required for clarity and avoid mistakes from Users	Yes
40	31.2 Block Diagram	Figure 31-1	Added signal names in the naming format for the trigger input and output in the block diagram	Names were missing	The description has been added	Was required for better understanding	None
41	31.5 SAR Sequencer	Figure 31-5	Added signal names in the naming format for the trigger input and output in the block diagram	Names were missing	The description has been added	Was required for better understanding	None
42	31.5.4 Averaging		**Added more description as below:** For true averaging, the averaging count needs to be a power of 2 and the right shift needs to be set to the corresponding value. For non-power of 2 averaging counts the right shift can only approximate the required divide. If a true averaging result is required, the software will need to do a divide. Note that the acquisitions for averaging are considered to be atomic, i.e. when the channel is aborted due to a preemption then the results are discarded and on return the averaging starts from scratch. On the flip side when the FINISH_RESUME preemption type is used, or in case of a debug freeze trigger, all averaging acquisitions are completed before the preemption or freeze happens.	Not available in *F spec	The description has been added	Was required for better understanding	Yes
43	31.5.5 Right Shifting	NA	Added a new section for Right Shifting	Not available in *F spec	The description has been added	It is required for averaging	Yes

44	Section	Subsection	Change Description	Current Spec *G content	New Spec *H content	Reason for change	Customer Impact
45	31.5.5 Right Shifting	Before 31.5.6	**Sentence rephrased:** The right shift post processing step takes the 20-bit output from the averaging step, then right shift by 4, resulting in an output of a 16-bit result by eliminating the 4 least significant bits.	**Earlier sentence:** The Right shift post processing step takes the 20-bit output from the averaging step and after the Right shift outputs a 16-bit result by dropping the top 4.	The description has been added	Was required for better understanding	None
46	31.6.2 Triggers	Before table 31-10	**Signal naming convention description added:** The input trigger signal naming convention is given below. TCPWM: PASS[x]:PASSx_CH_TR_IN[y] where x is instance and y is the channel y varies between 0-19 for TCPWM0 group 0 and y varies between 20-31 for TCPWM0 group 1 GENERIC: PASS:PASS_GEN_TR_IN[y] where y varies between 0 to 3. Freeze Pass0 during Debug: PASS:PASS_DEBUG_FREEZE_TR_IN	Not available in *F spec	The description has been added	Was required for better understanding	None
47	31.7.1 Trigger Outputs	Before 31.7.1.1 Channel Done Trigger	**Signal naming convention description added:** The trigger output signal naming convention is given below: x : instance, y : channel Range Violation : PASS[x]:PASSx_CH_RANGEVIO_TR_OUT[y] Channel Done : PASS[x]:PASSx_CH_DONE_TR_OUT[y] Generic : PASS[x]:PASSx_GEN_TR_OUT[y]	Not available in *F spec	The description has been added	Was required for better understanding	None
48	32.2.4	Note	update the Trace events naming		naming update	harmonize Trigger Label namaing with the datatsheets	None
49	33.4 System Calls	Functional Description	Mentioned a note that the software must ensure that the default hardfault vector entry is replaced with the specific user handler.	No note about the hardfault vector handler	added a note about the hardfault vector handler	enhancement	No
50	33.4 System Calls	WriteRow	"Access Restrictions Encoding" table updated mentioning ARs are applied only to SRAM0	Mentions SRAM instead of SRAM0	Changed SRAM -> SRAM0 Added a note for "SYS_AP_MPU_ENABLE" on impact to SRAM when enabled	enhancement	No
51	34.3.4.3 TOC2 Structure	None	Add description about security update marker TOC2_SECURITY_UPDATES_MARKER	No description	The description has been added	Add description of the recently added field	Yes
52	34.3.2.3 Initialization	None	Add description of configuration for PERI_MS_PPU_FX_PERI_GR2_BOOT	No description	The description has been added	Add description of the recently added change	Yes
53	34.3.4.3 TOC2 Structure	None	Fix the default adress of signature verification key	SFlash row 59	Zero	To fix the mistake in the description	Yes