

| KINTEX ULTRASCALE DEVELOPMENT BOARD      |              |
|--|--------------|
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# KINTEX ULTRASCALE DEVELOPMENT BOARD


10/2/2015

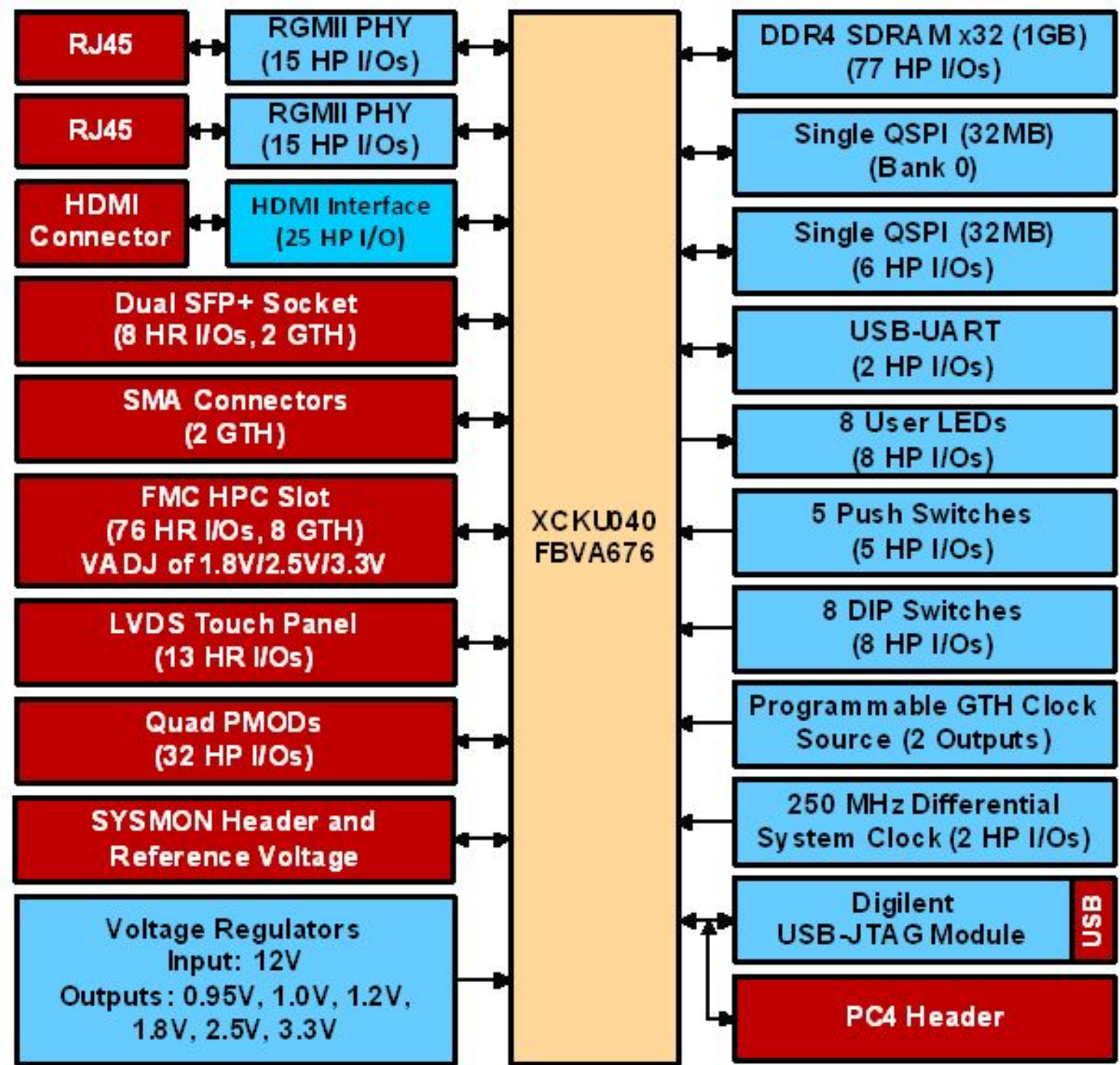
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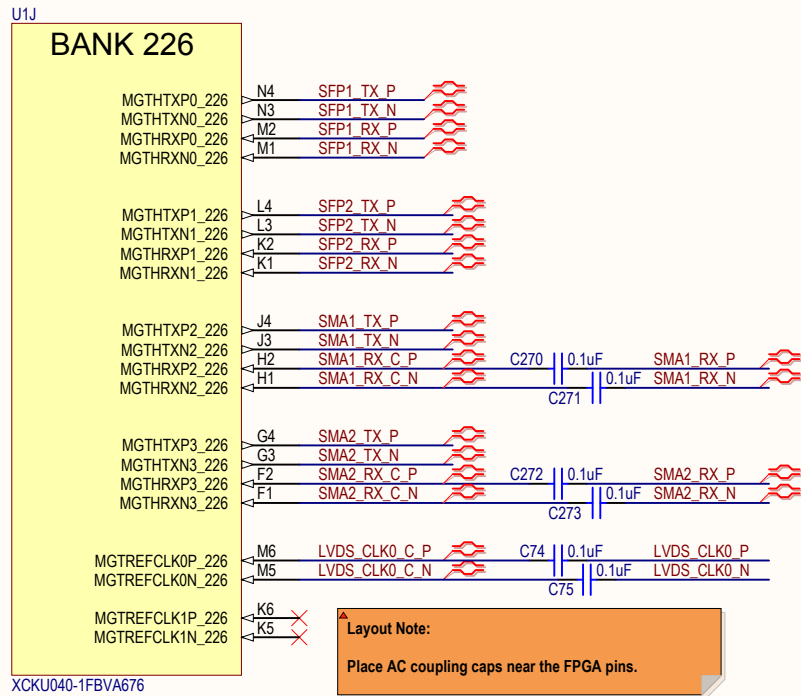
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|  <b>AVNET®</b> |   | <b>Avnet Engineering Services</b>                |               |
| Sheet Title: <b>Cover Sheet</b>   |   |  |               |
| Size: <b>B</b>  | Document Name: <b>Kintex UltraScale Development Board</b> | Variant Description: <b>KU040-DB-PRJ-B-01-00</b> | Rev: <b>B</b> |
| Date: <b>10/2/2015</b>  | Doc Num: <b>KU040-DB-SCH-B</b>                            | Sheet: <b>1</b> of <b>14</b>                     |               |



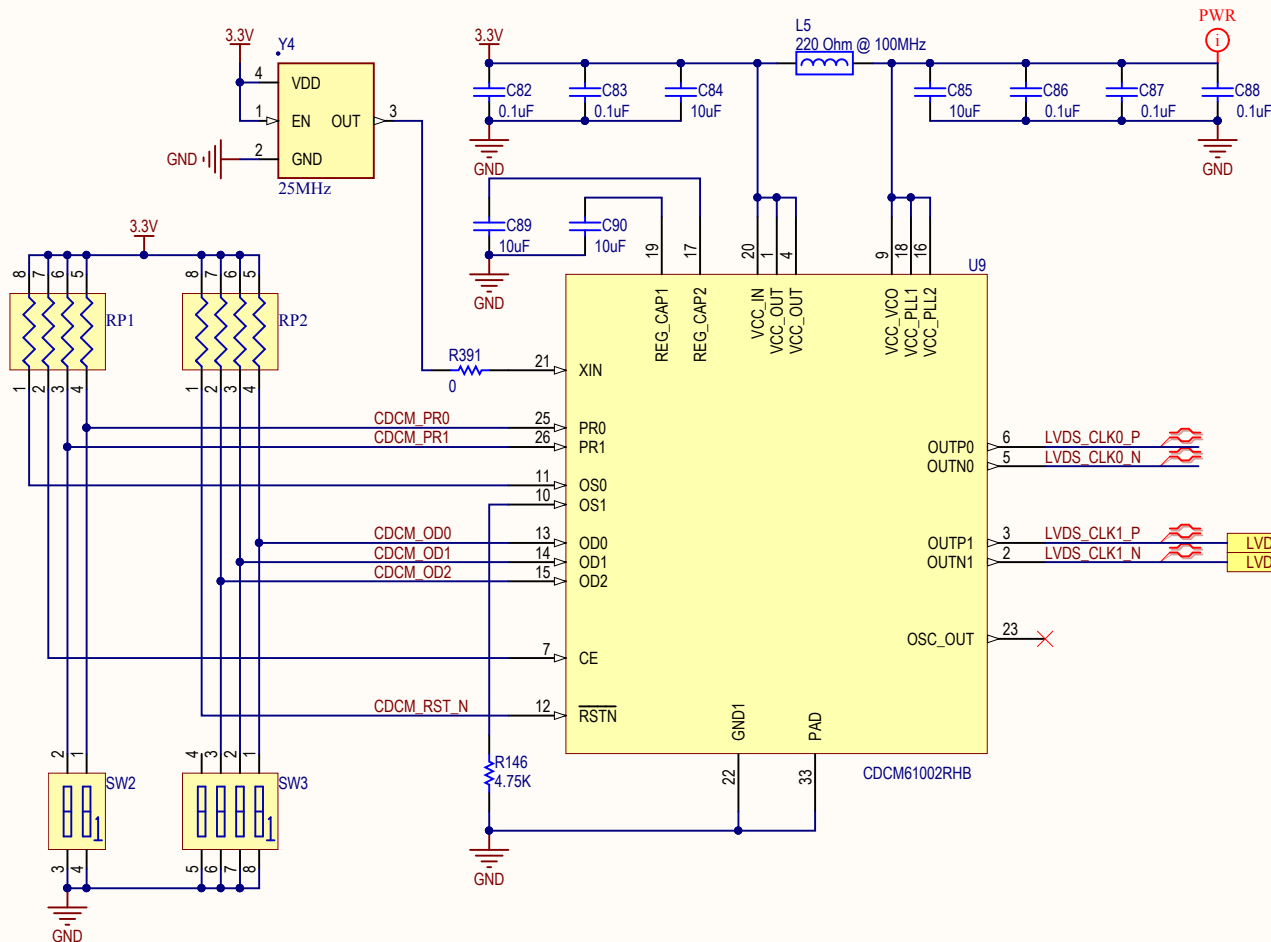
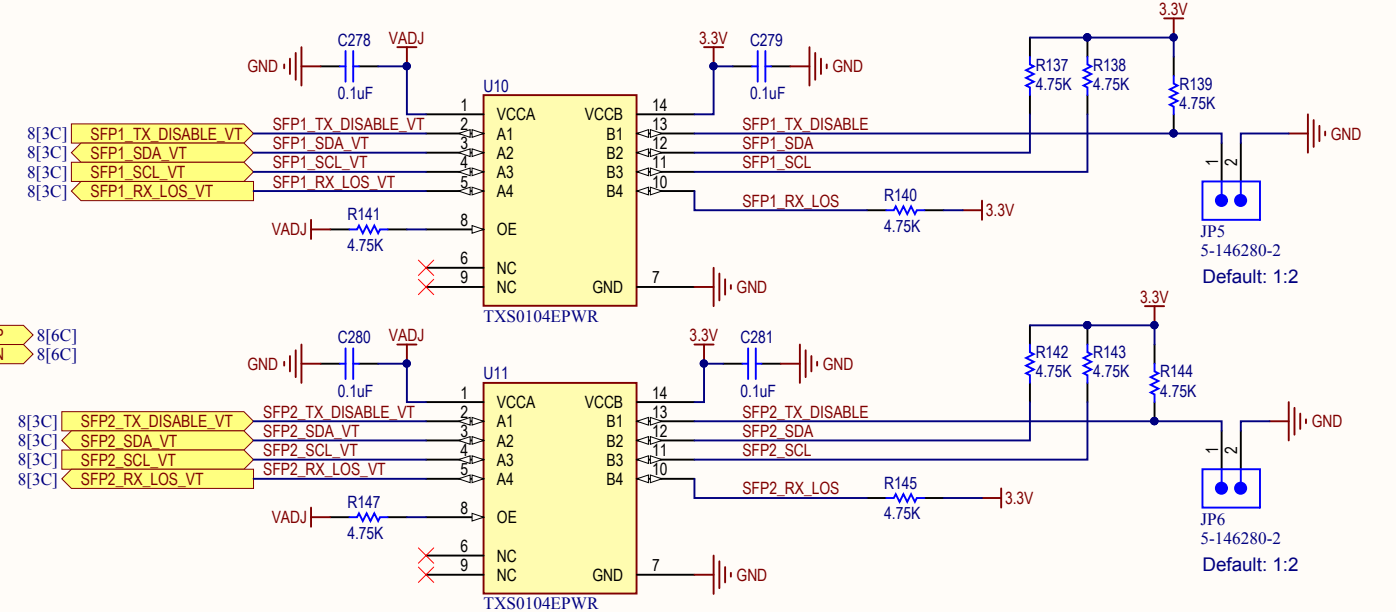
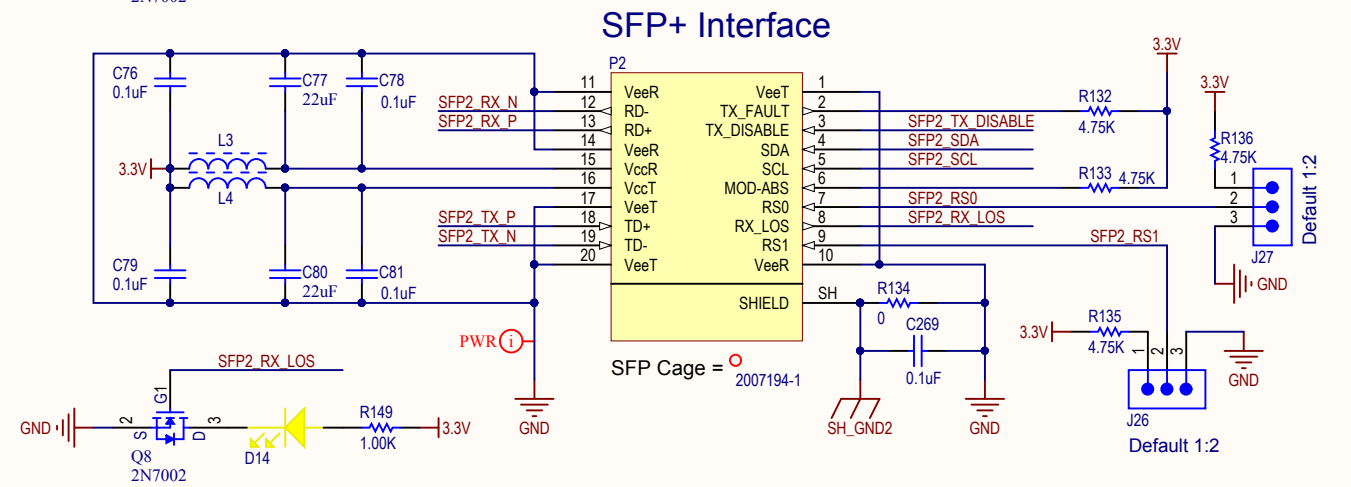
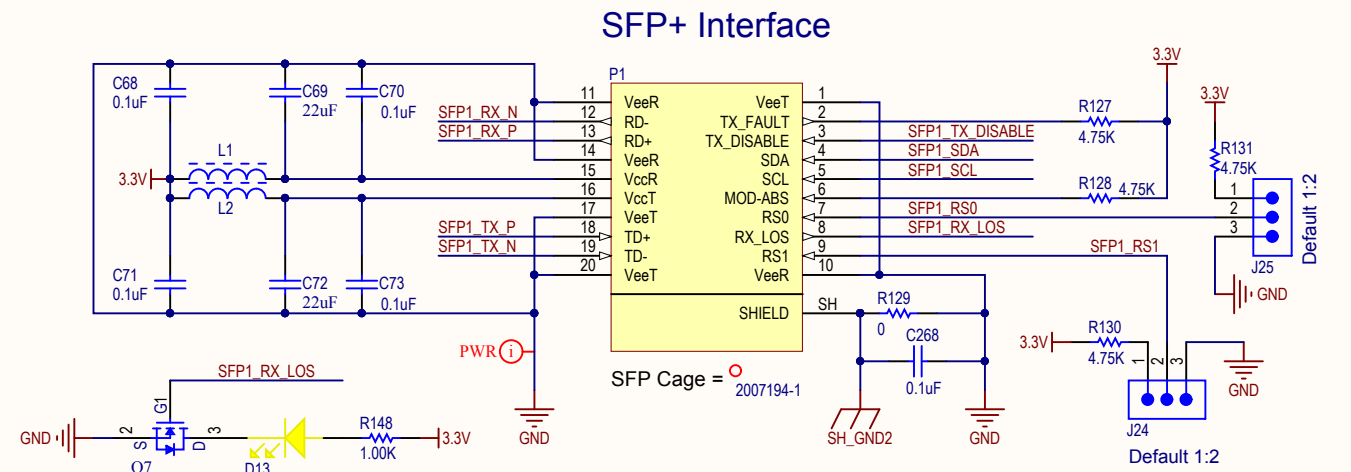
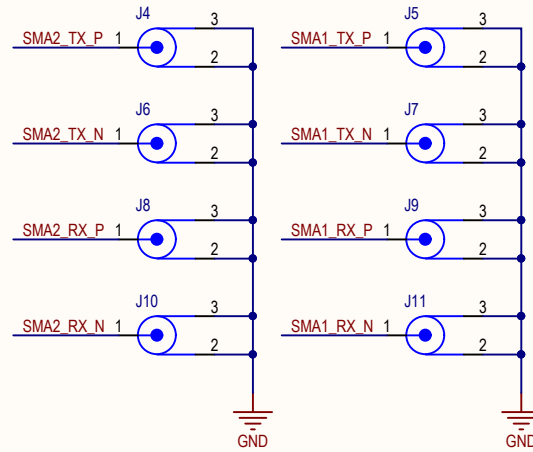


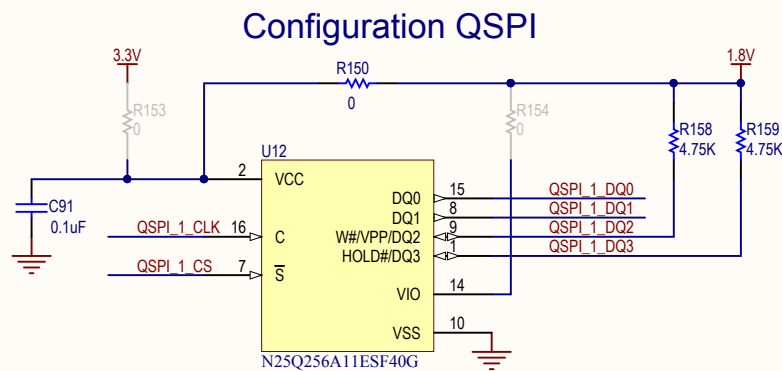
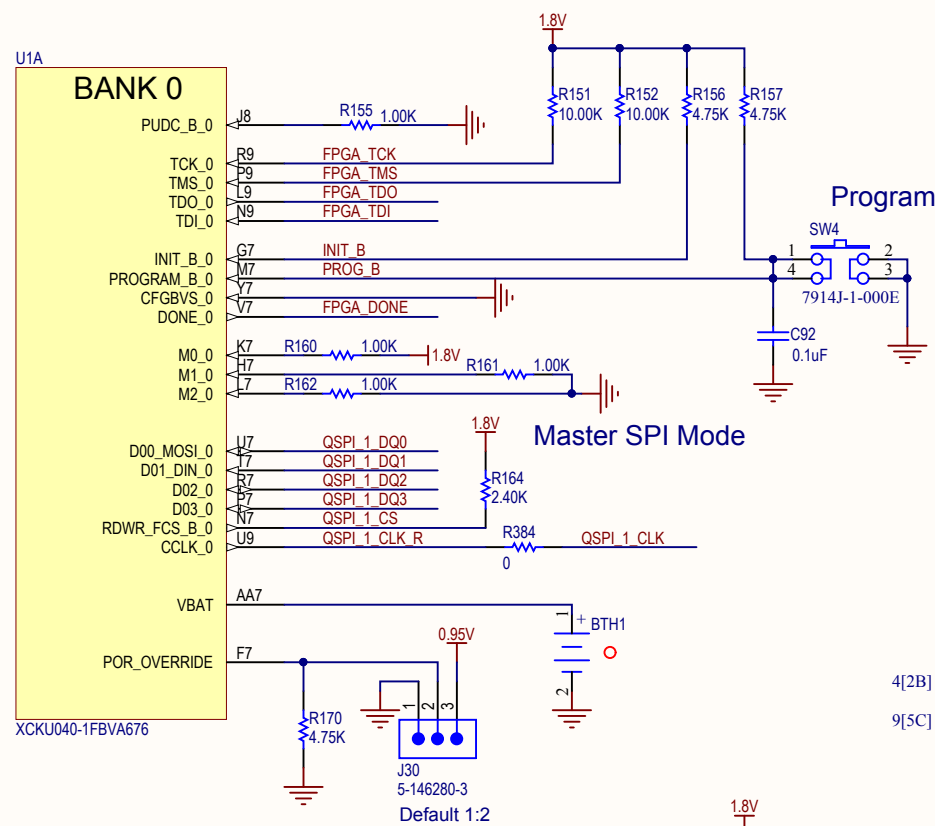






## GTH SMA CONNECTORS





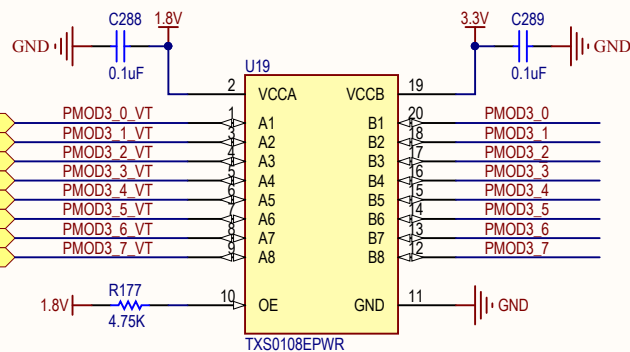
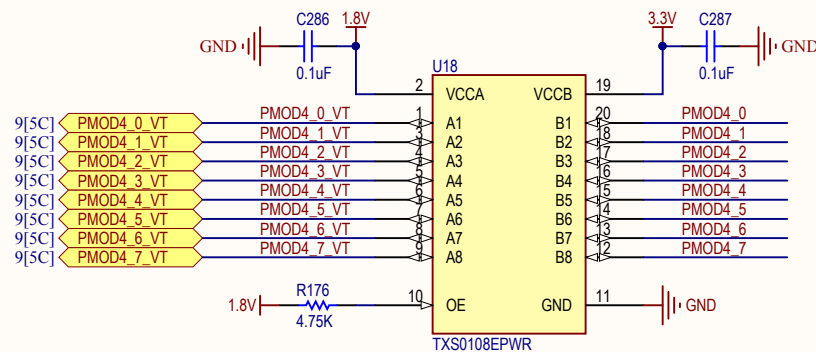
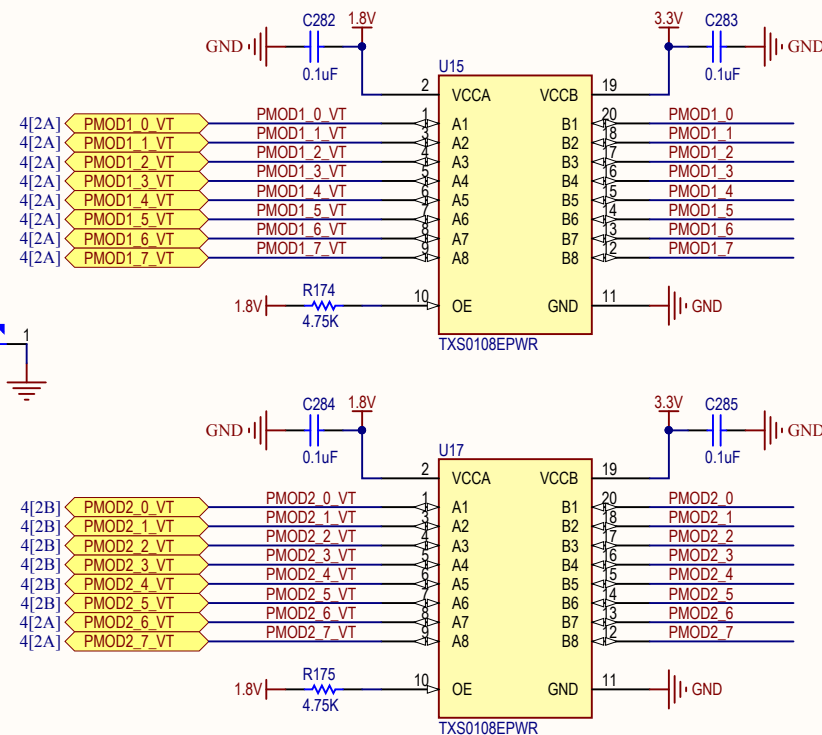
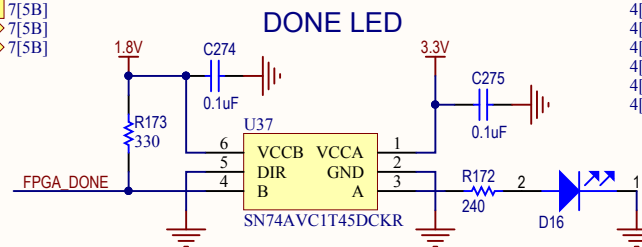
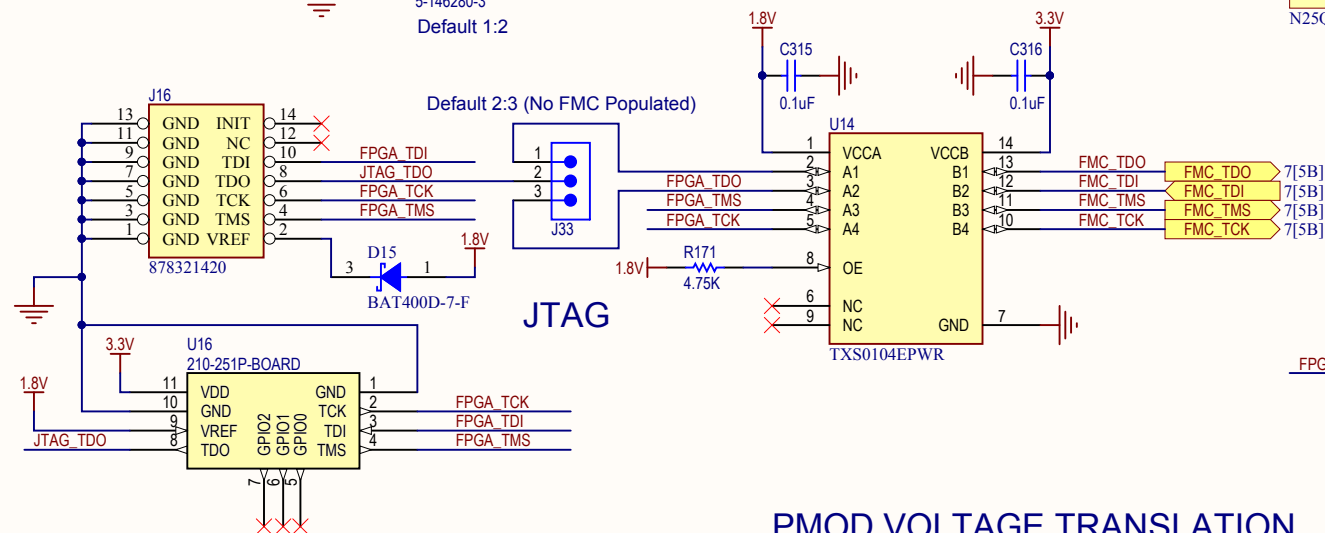
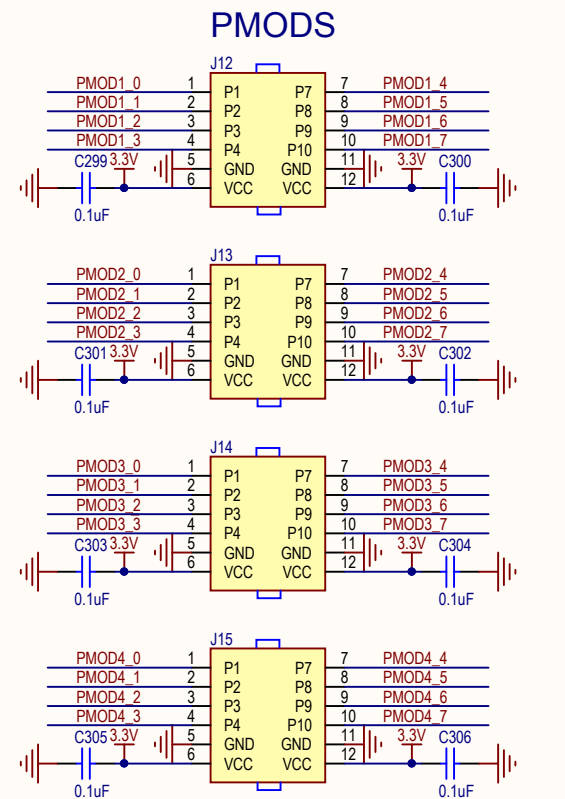
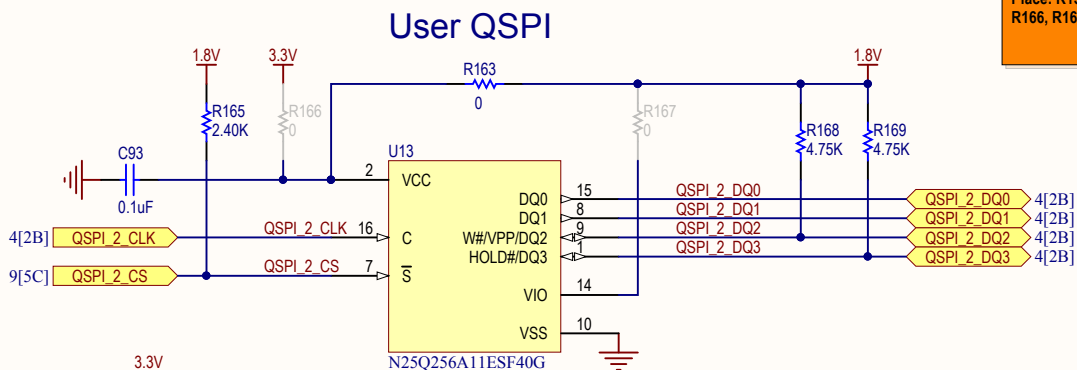
**Assembly Note:**

QSPI IC land patterns designed to accommodate Micron (shown) or Spansion QSPI device S25FL128SAGMFIRO.

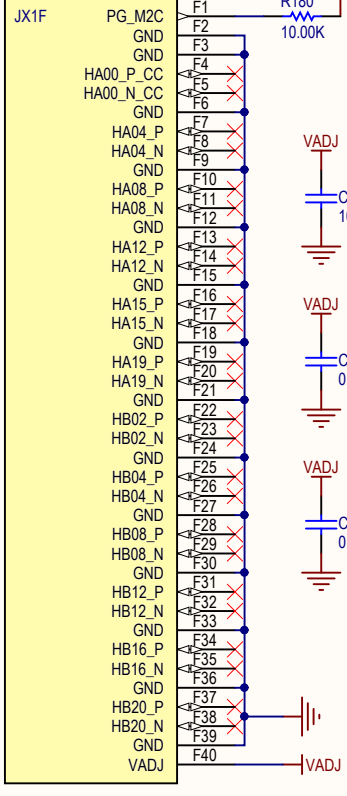
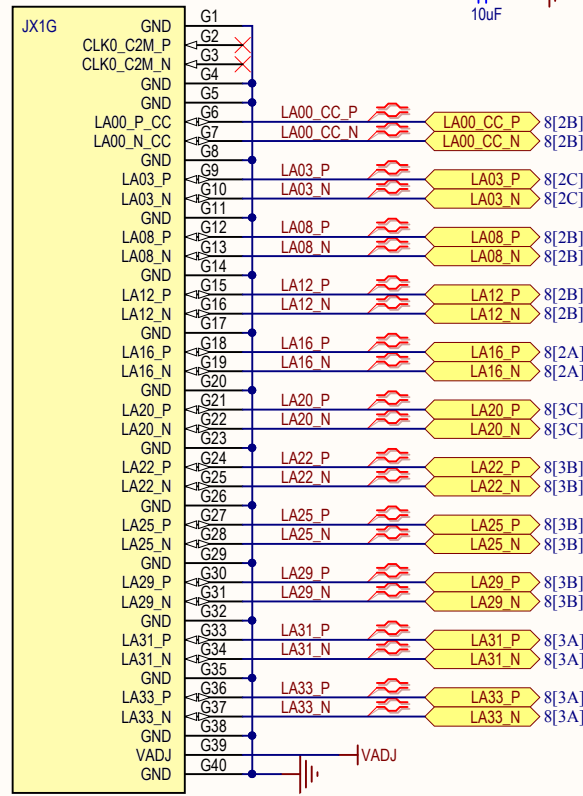
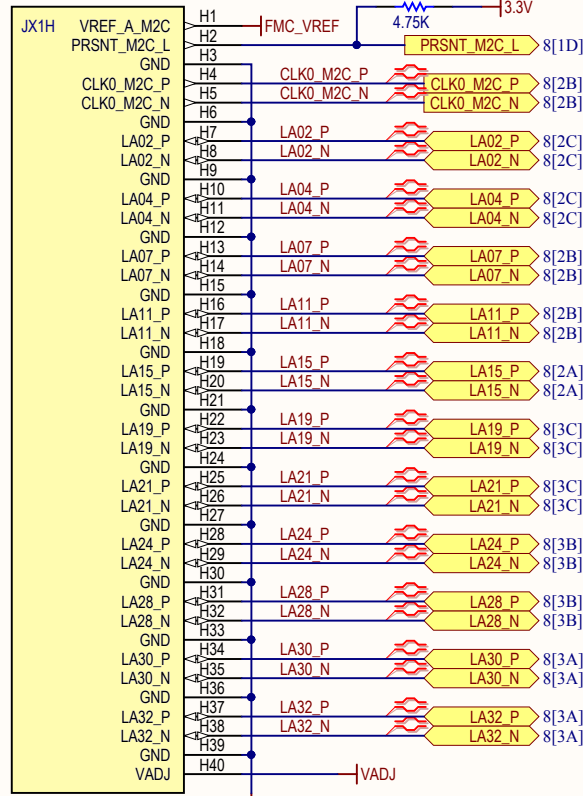
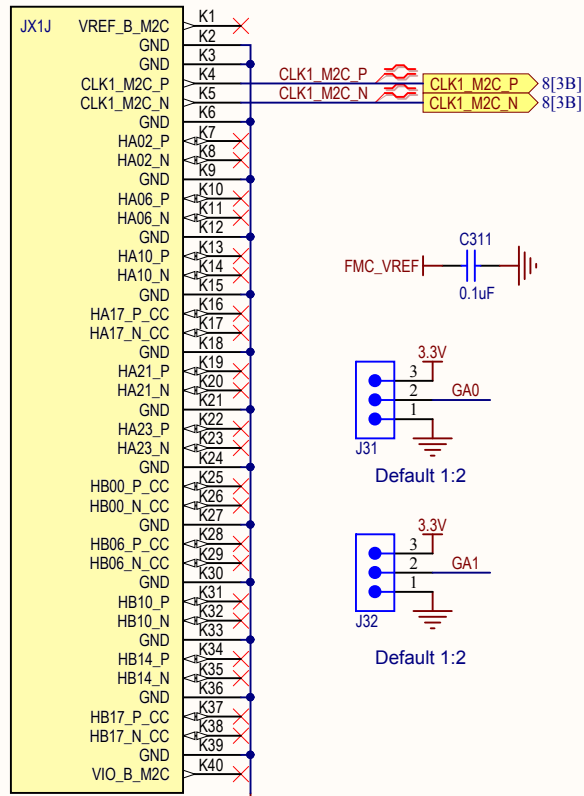
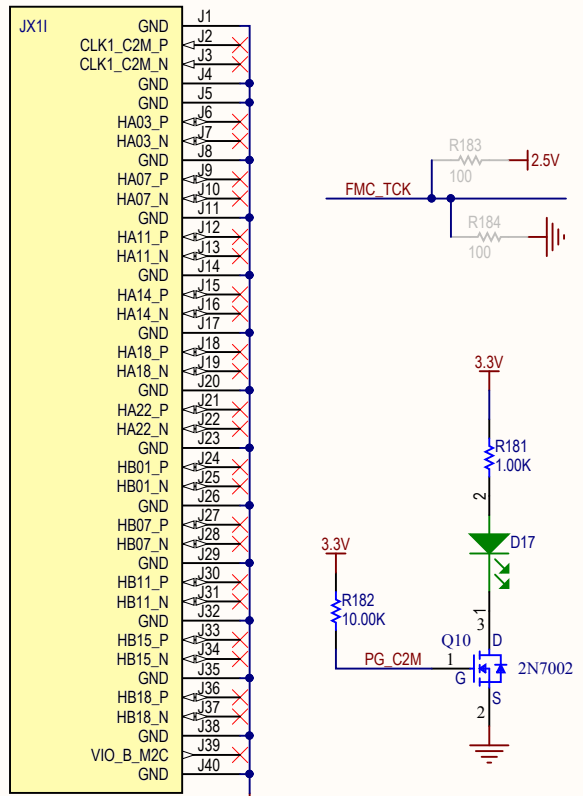
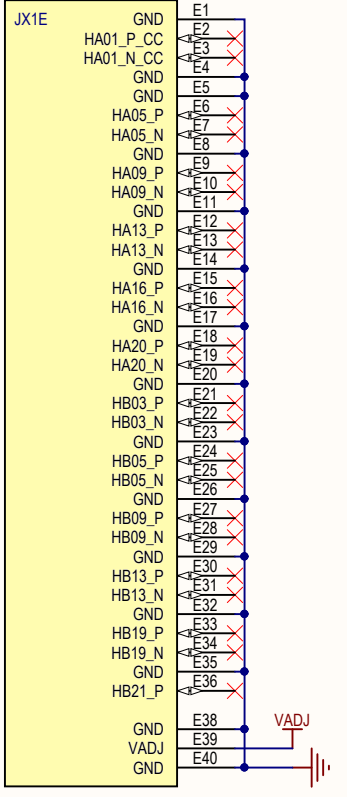
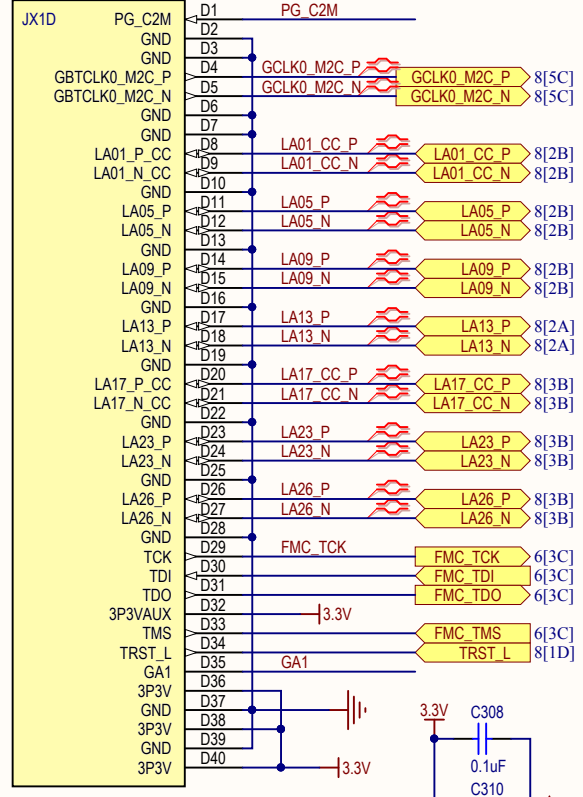
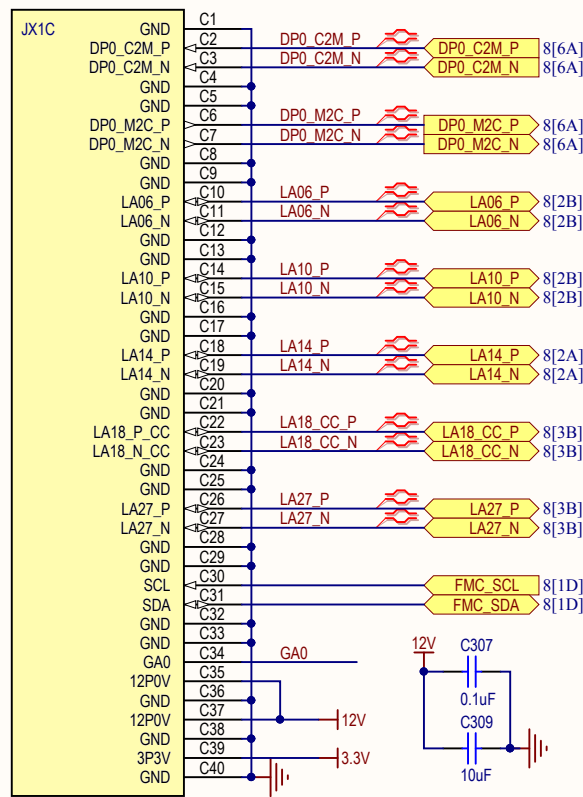
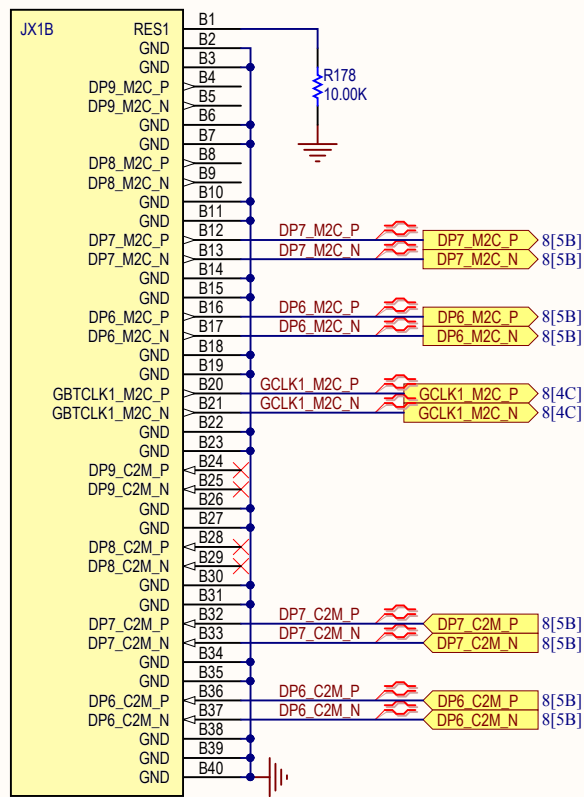
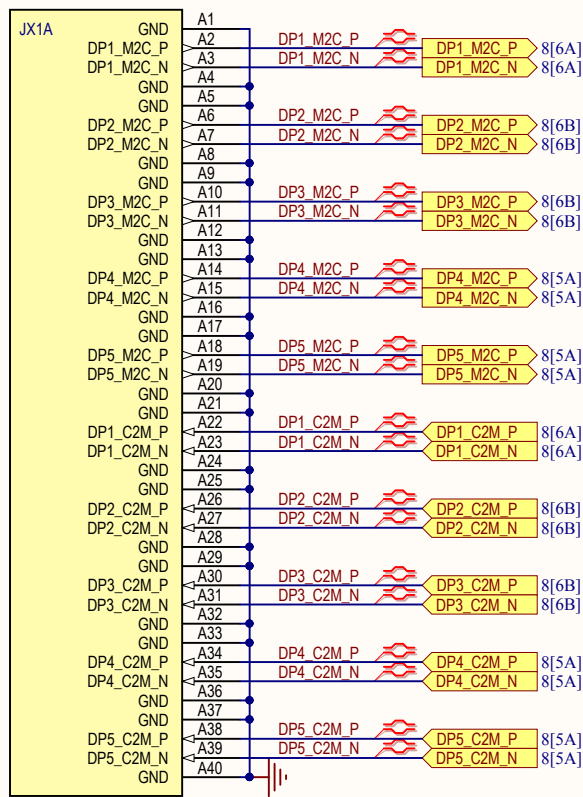
To Implement Spansion QSPI:

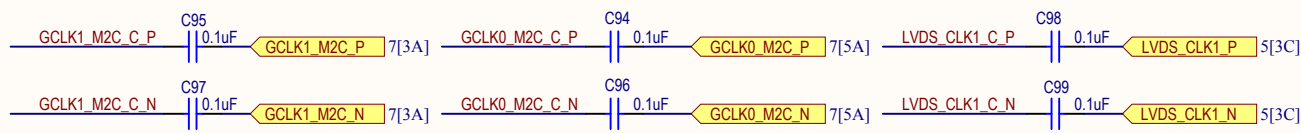
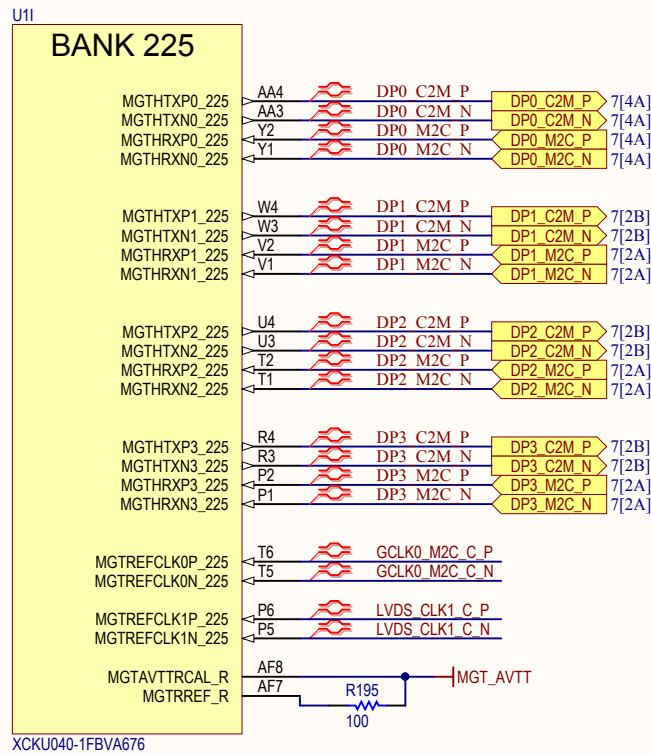
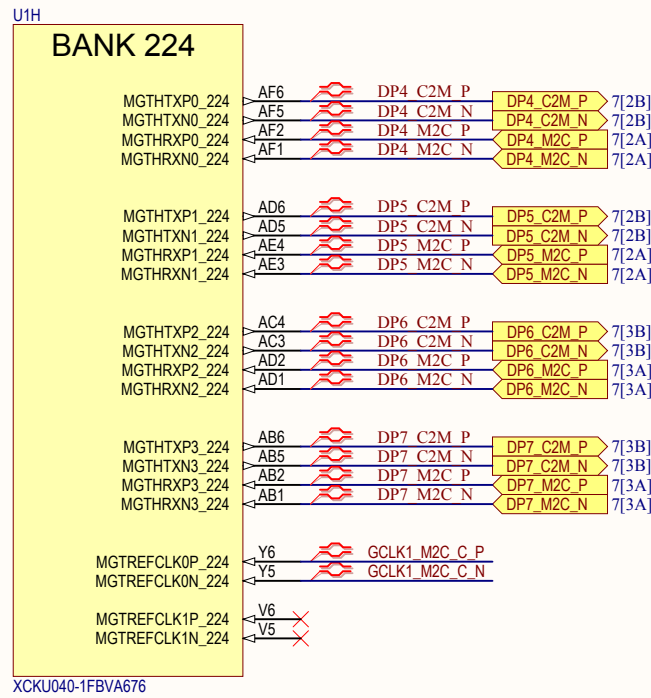
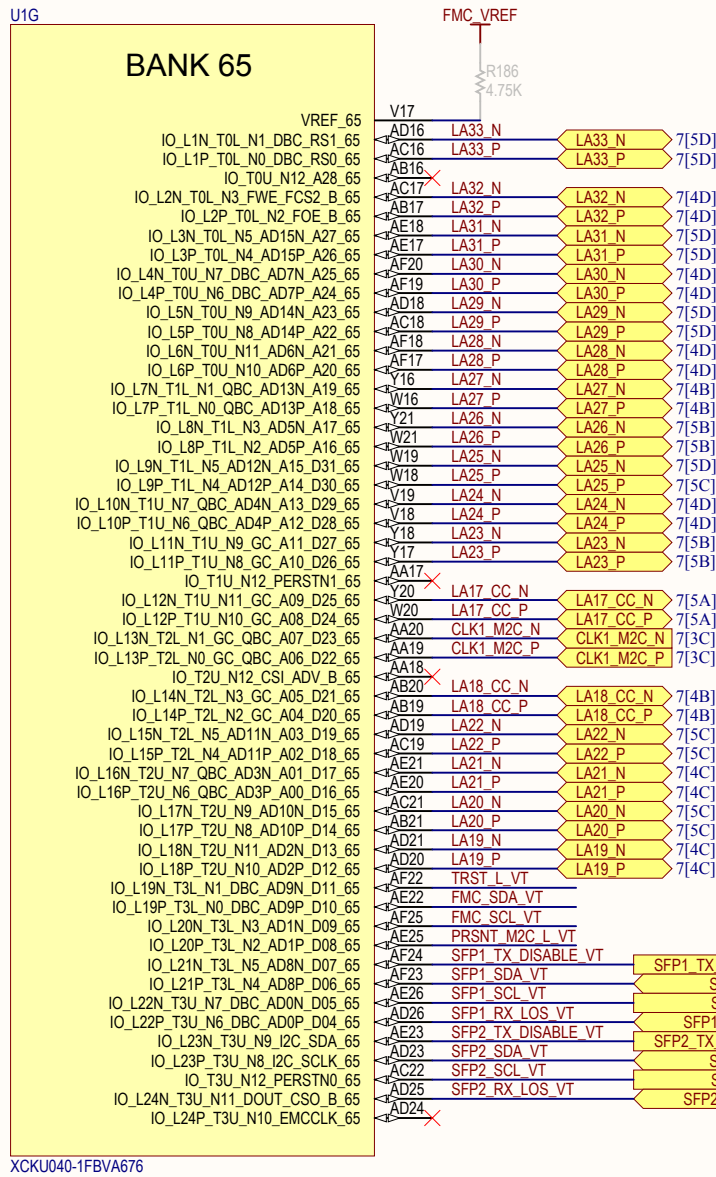
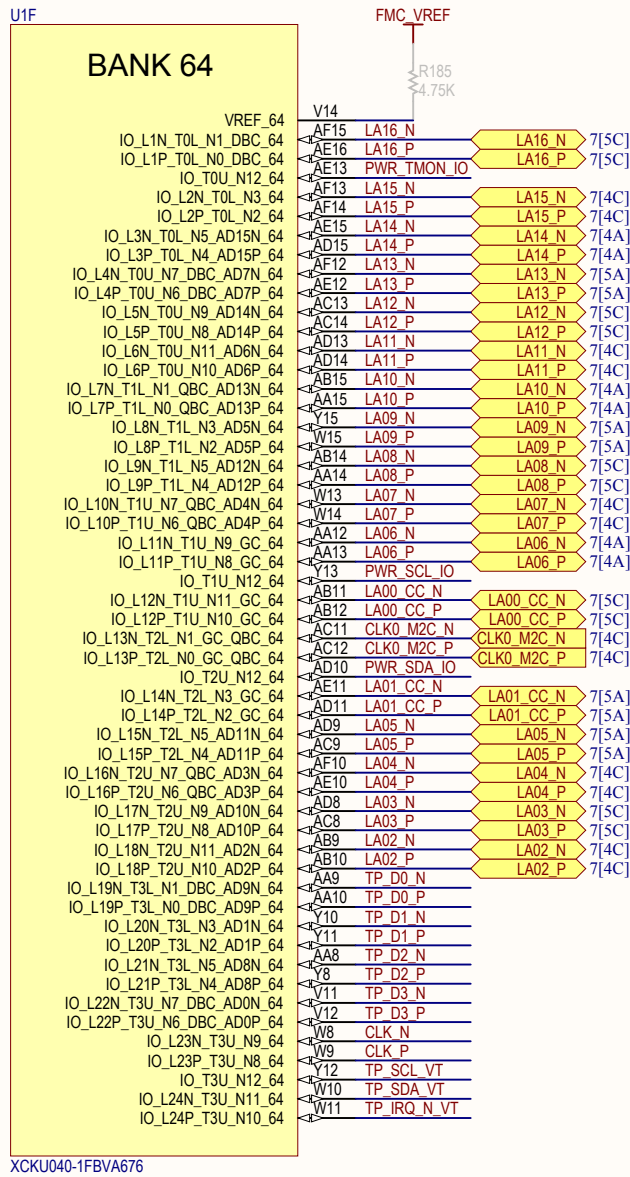
DNP: R150, R163

Place: R153, R154, R166, R167





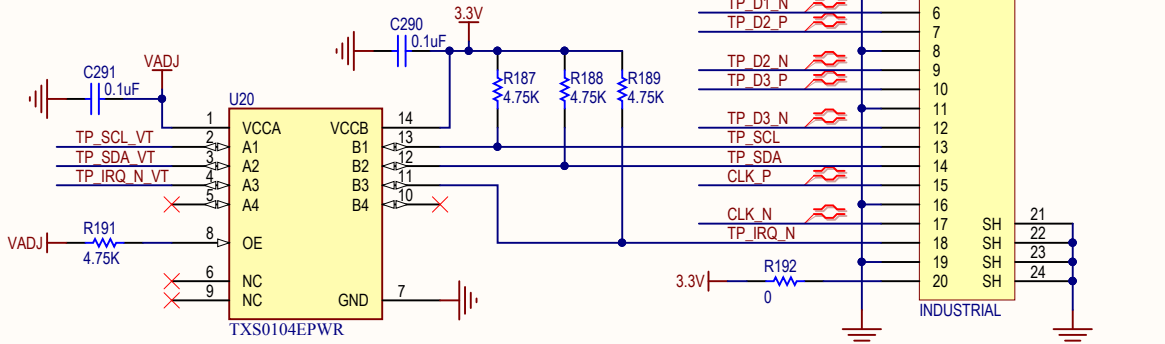




**LVDS Touch Panel Interface**

**User Note:**

VADJ must be set to 2.5V when the LVDS Touch Panel is used



**Layout Note:**

DisplayPort routing should adhere to the following guidelines:

1. Diff pair lengths matched to within 10 mils
2. Vias should be avoided on all diff pairs
3. All trace angles should be > 135°
4. All pairs should use symetric routing within the pair
5. Do not route traces of plane splits or anti-pads
6. Target impedance is 100 ohm differential



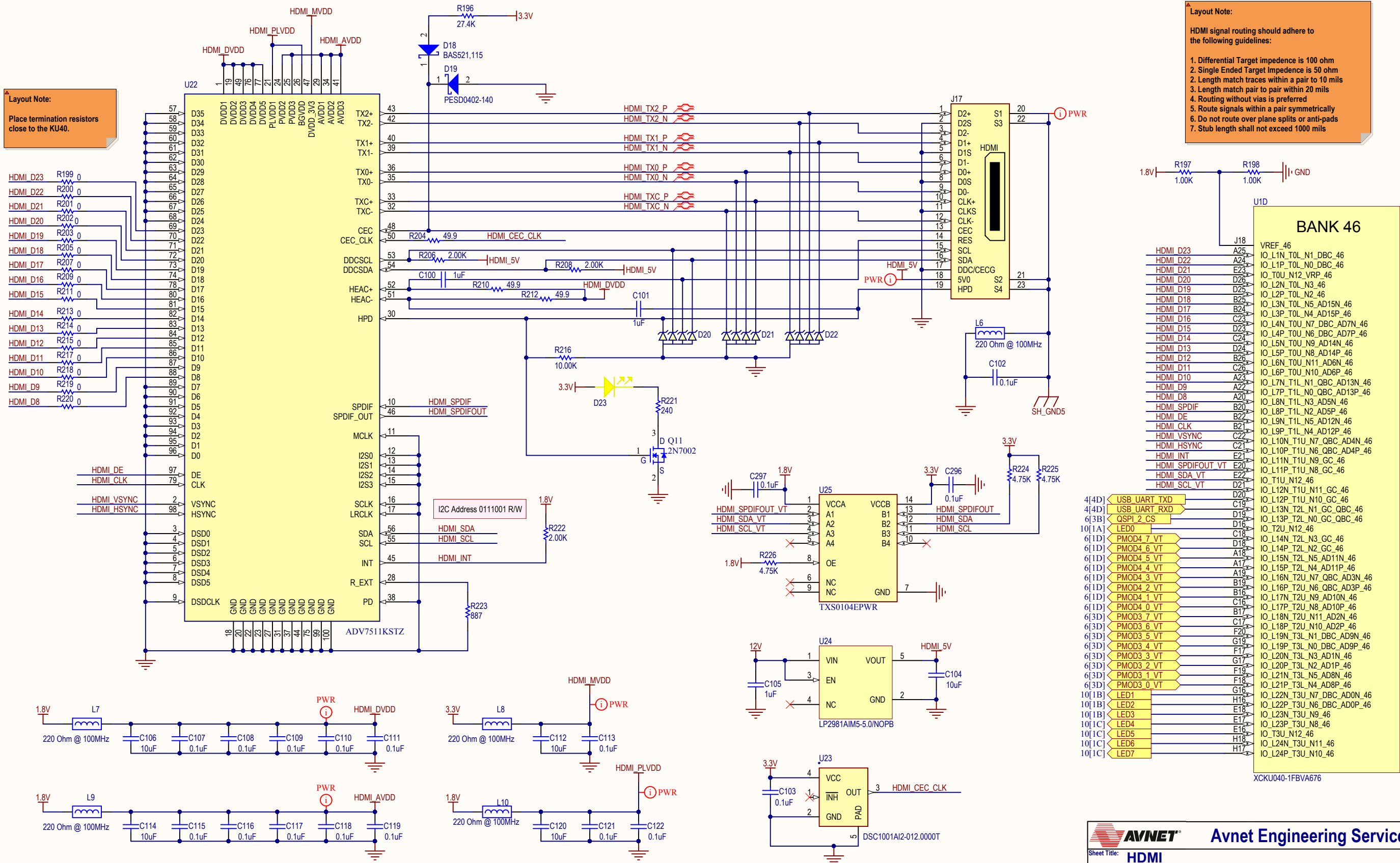
**Layout Note:**

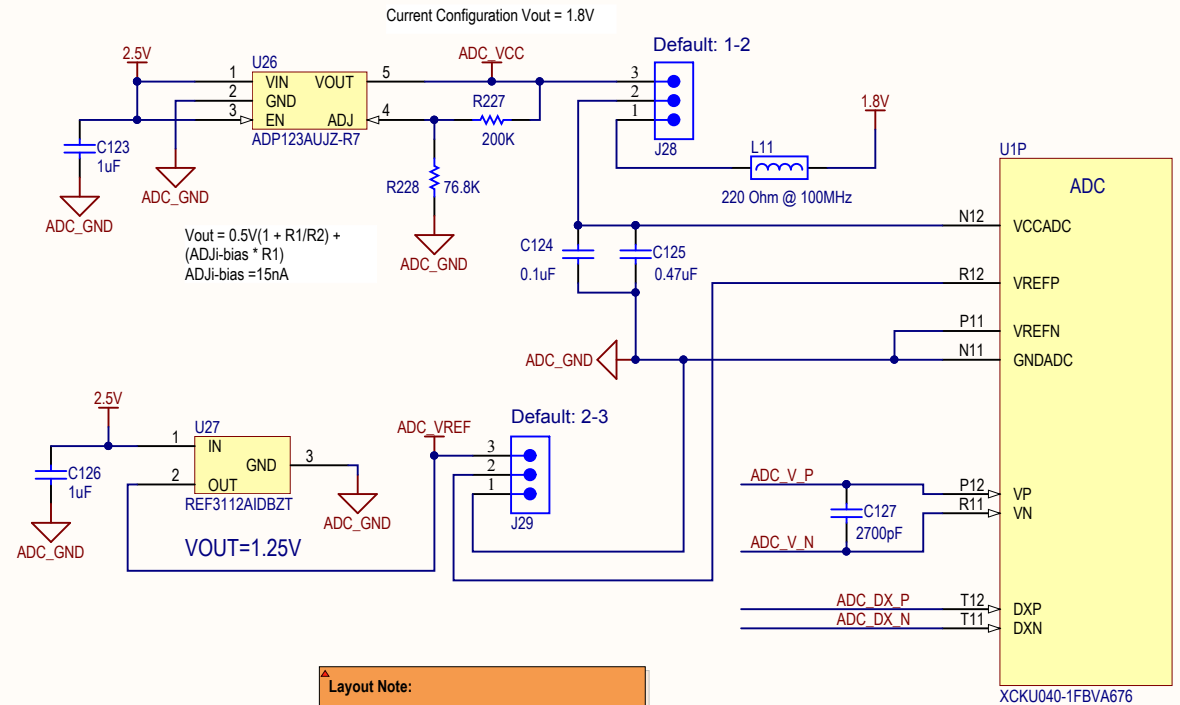
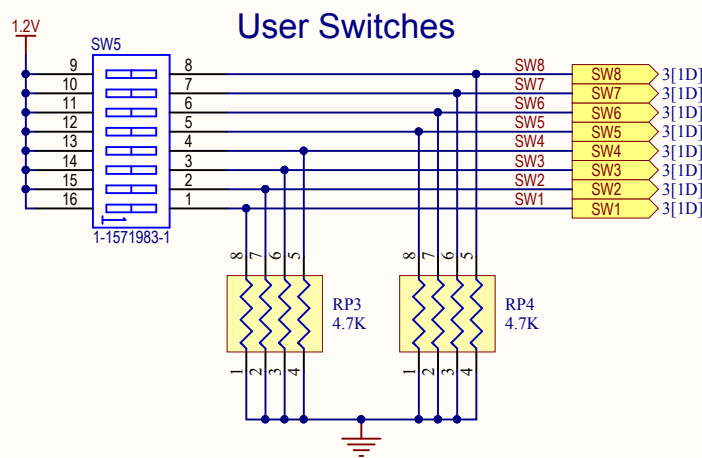
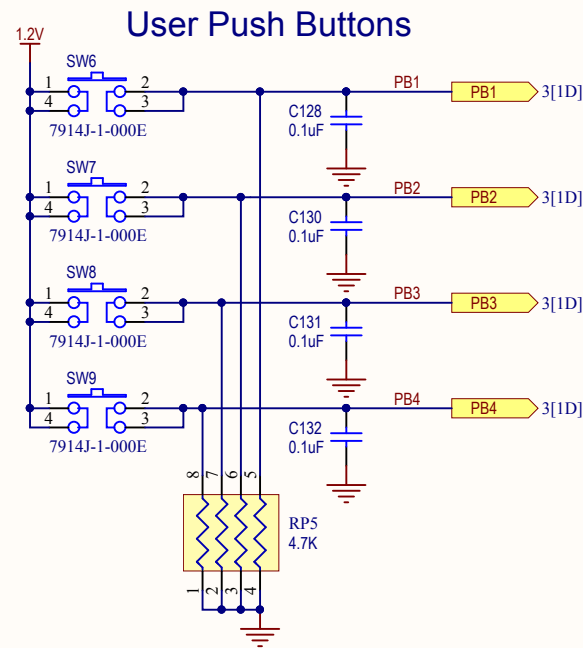
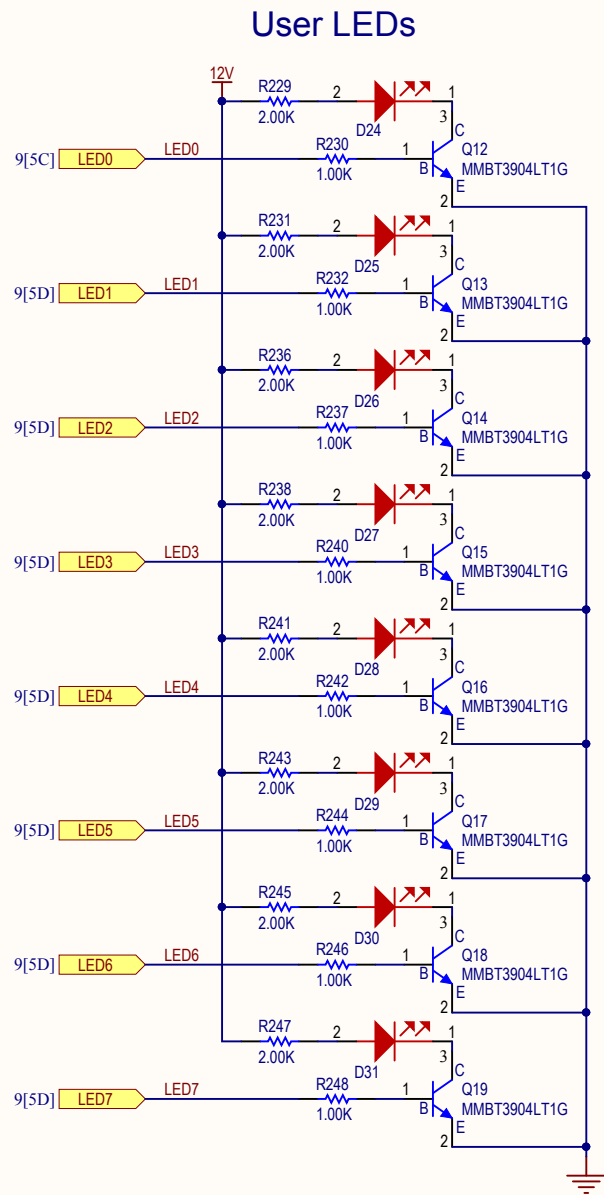
Place termination resistors close to the KU40.

**Layout Note:**

HDMI signal routing should adhere to the following guidelines:

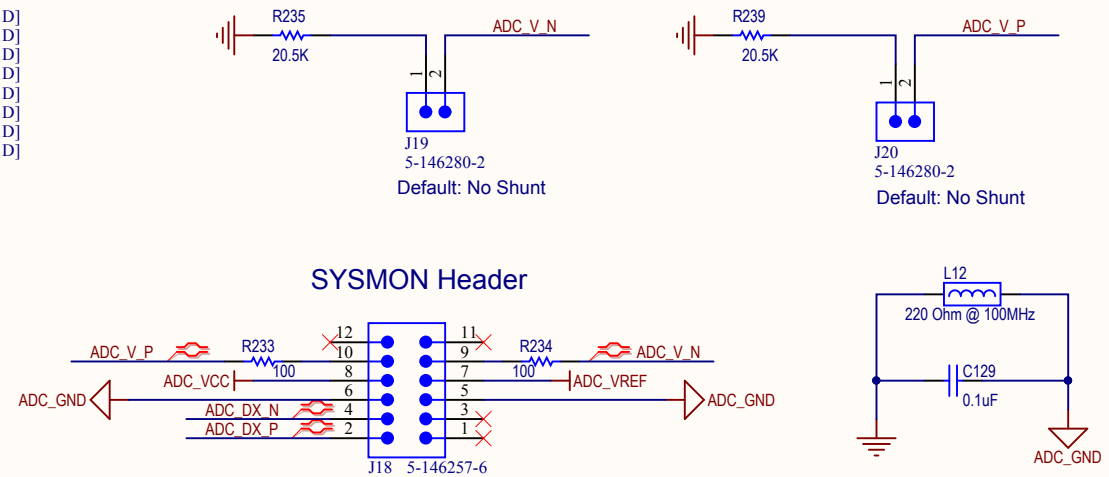
1. Differential Target impedance is 100 ohm
2. Single Ended Target Impedance is 50 ohm
3. Length match traces within a pair to 10 mils
4. Length match pair to pair within 20 mils
5. Routing without vias is preferred
6. Do not route over plane splits or anti-pads
7. Stub length shall not exceed 1000 mils

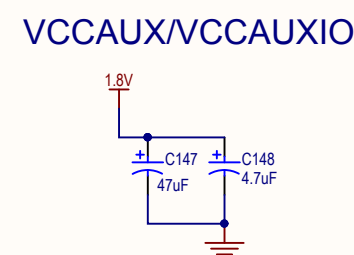
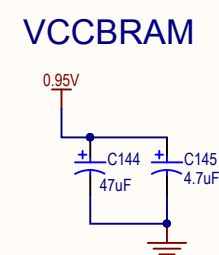
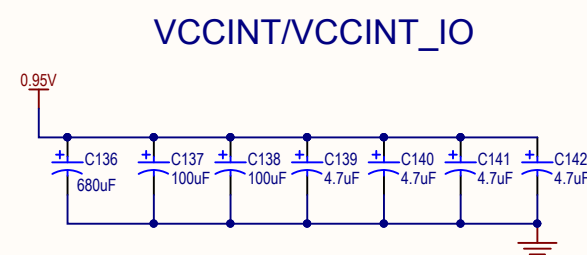
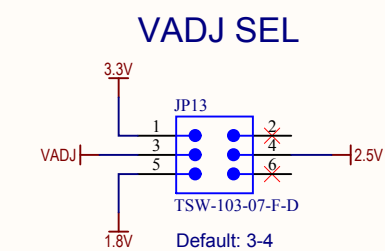
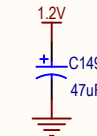
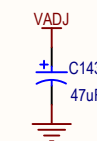
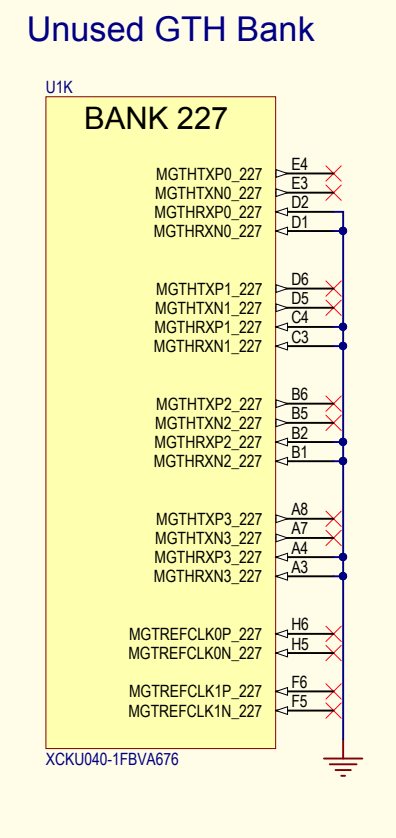
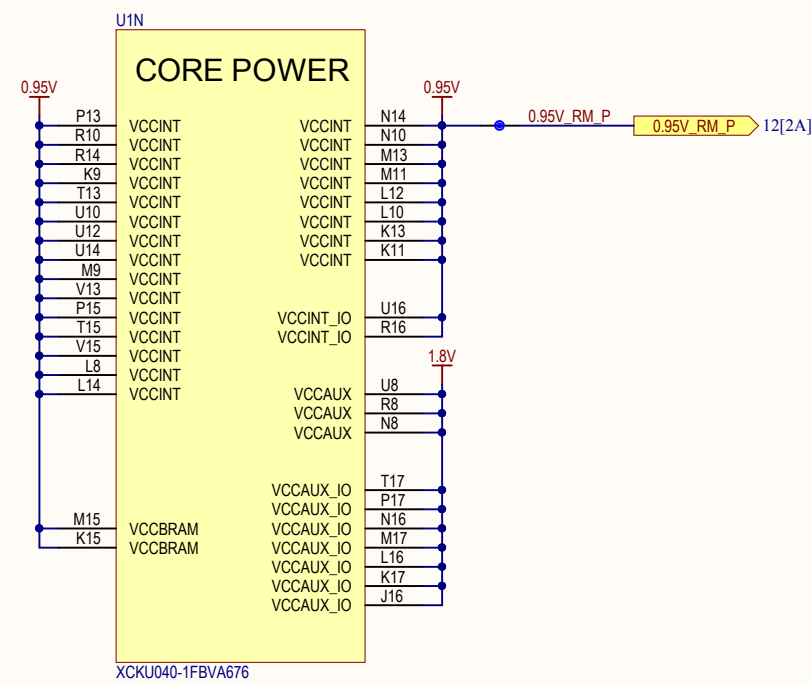
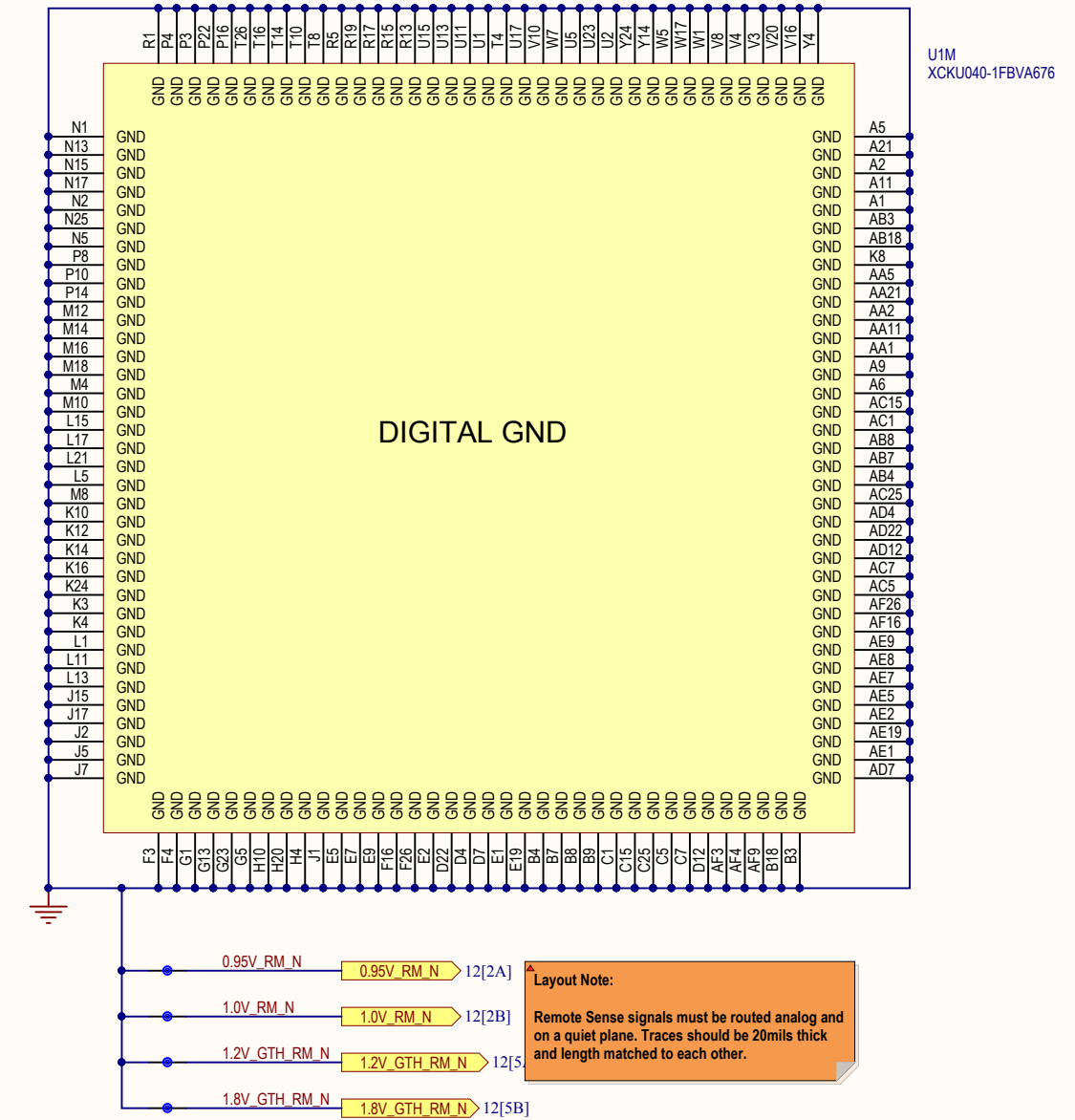
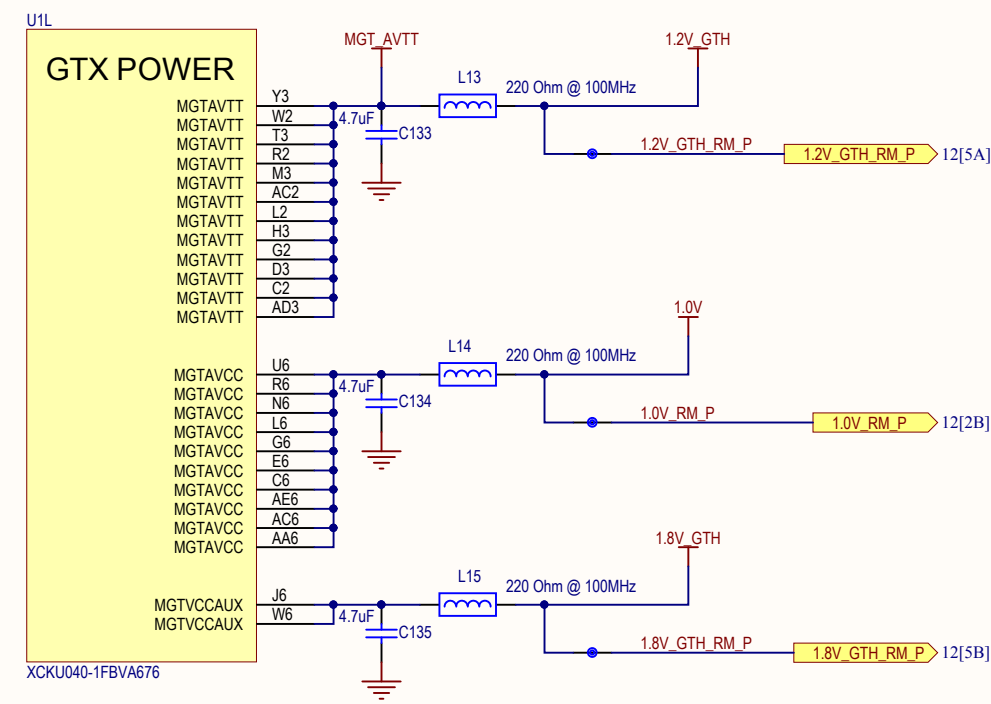
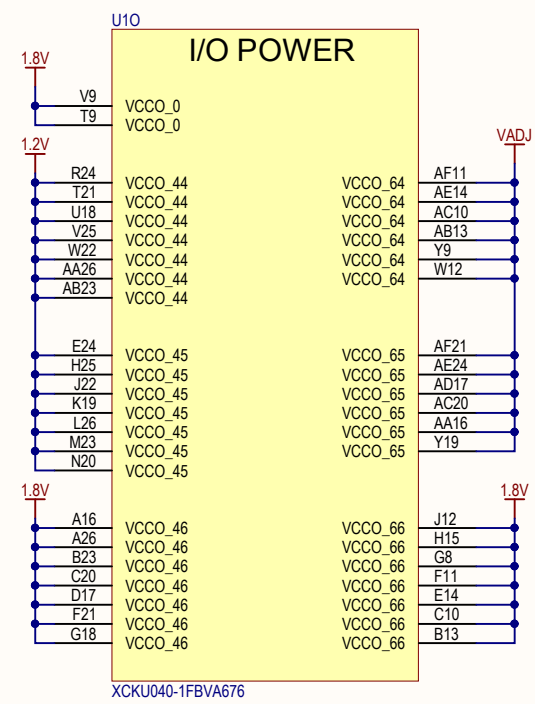




**Layout Note:**

Place 100 ohm resistors and 2700pF cap filter close to FPGA.

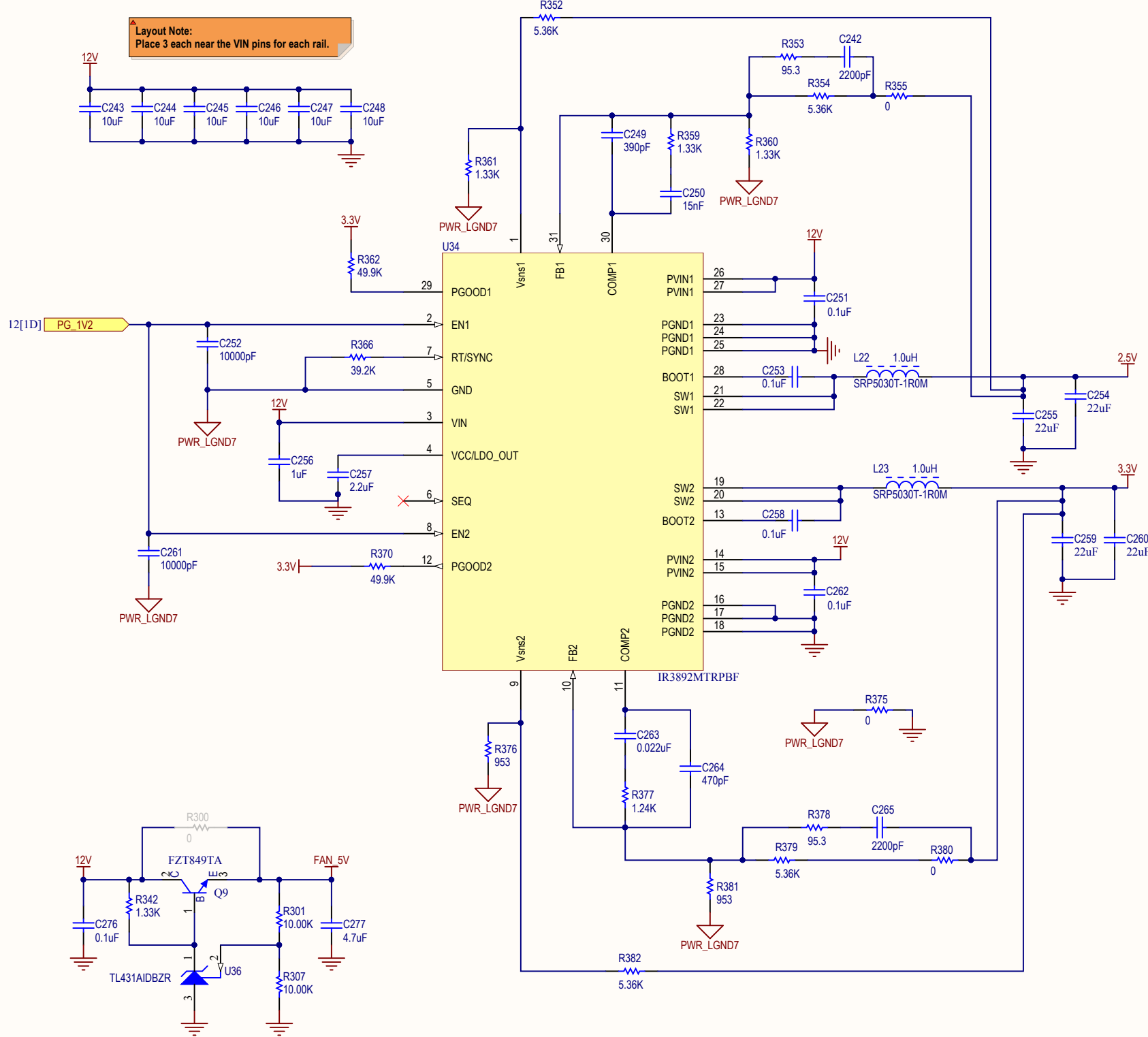




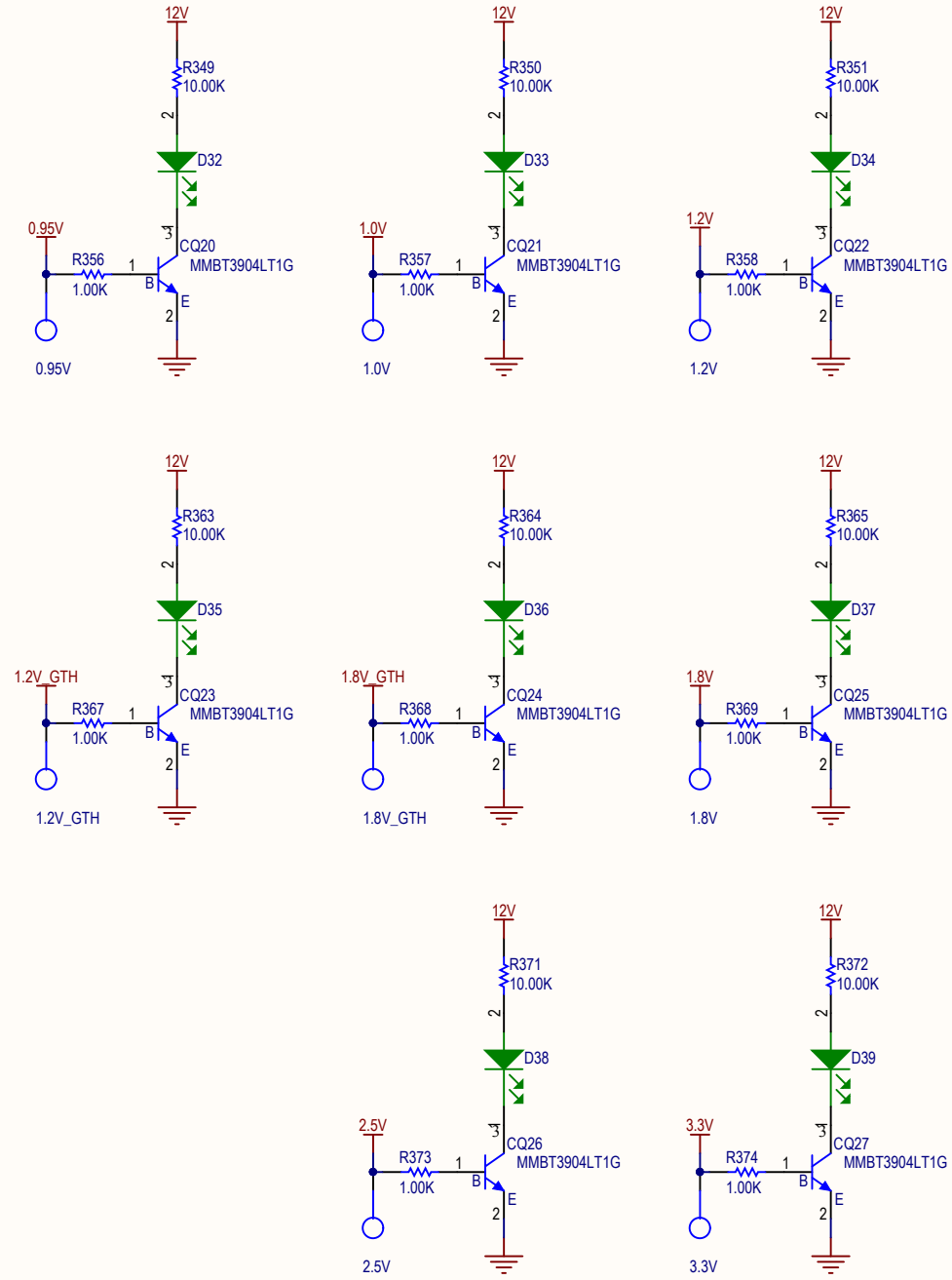




# 2.5V and 3.3V Dual Buck



## Power Rail LEDs



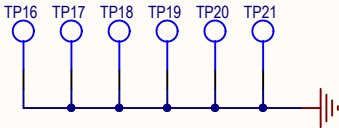
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KU040 DB Revision: B  
Initial Product Release

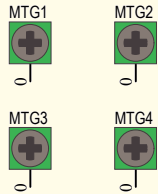
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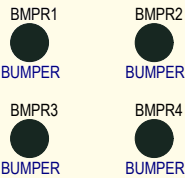
GND TEST POINTS



Mounting Holes




Bumper Standoffs



Assembly:

Label1  
BD-XXXX-XXXX-G  
Label, Product



Label2  
  
XXXXXXX  
Label, Serial Number



ESD Bag



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Sheet Title: Back Page

|                 |  |   |        |
|-----------------|--|---|--------|
| Size: B         | Document Name: Kintex UltraScale Development Board | Variant Description: KU040-DB-PRJ-B-01-00 | Rev: B |
| Date: 10/2/2015 | Doc Num: KU040-DB-SCH-B                            | Sheet: 14 of 14                           |        |