Thermal Evaluation: Comparison of Standard and Exposed Pad DSO Package

Example of SPOC Devices

BTS5682E, BTS5672E, BTS5662E

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Never stop thinking

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1 Abstract

The aim of this application note is to provide a thermal performance evaluation of standard and exposed pad DSO packages with the example of SPI Power Controller SPOC devices BTS5682E, BTS5672E and BTS5662E. The comparisons are done on the same printed circuit board (PCB).

The maximum power dissipation, which can be applied, is defined by two limiting factors: Junction temperature and PCB temperature.

Additionally to that, the basics of the two DSO package groups are described, which have been considered in this application note.

This paper is focusing on DSO packages with and without exposed pad, mounted on standardized JEDEC PCBs. Other package types and application specific scenarios like “heat slug up” and comparison with application specific PCBs are not considered in this application note.

Please note:

- *The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.*
- *All results stated in this application note are based on calculations done by simulation software ANSYS®. This application note can be changed without information.*
- *Please refer to the official SPOC data sheet for detailed technical description.*

2 Introduction

The BTS5682E, BTS5672E and BTS5662E are six channel high-side power switches, which are especially designed to control standard exterior front and rear lighting in automotive applications.

Configuration and status diagnosis is done via SPI. Additionally, there is a current sense signal available for each channel that is routed via a multiplexer to one diagnostic pin.

The maximum power dissipation, which can be distributed, can be defined with the following limiting factors on a high conductivity JEDEC PCB used in most applications. The limiting factors are:

- Standard Package: The maximum junction temperature has to be considered (<150°C). The temperature of 150°C is related to the maximum junction temperature the semiconductor device.
- Exposed pad (ePad) Package: The maximum PCB temperature has to be considered (<130°C). Due to the very low thermal resistance between the junction and the exposed pad of the device, the maximum junction temperature should be below the glass transition temperature of the PCB material. This application note refers to standard FR4 material only, which has a glass transition temperature of about 130°C. PCB materials with higher glass transition temperatures are not considered.

2.1 Boundary Conditions

Ambient temperature: T_a = +85°C
Free convection and radiation

Table 1 Attributes of JEDEC PCB

Dimensions	76.2 × 114.3 × 1.5 mm³	λ_{therm} [W/m·K]
Material	FR4	0.3
Metalization	JEDEC 2s2p (JESD 51-7) + (JESD 51-5)	388

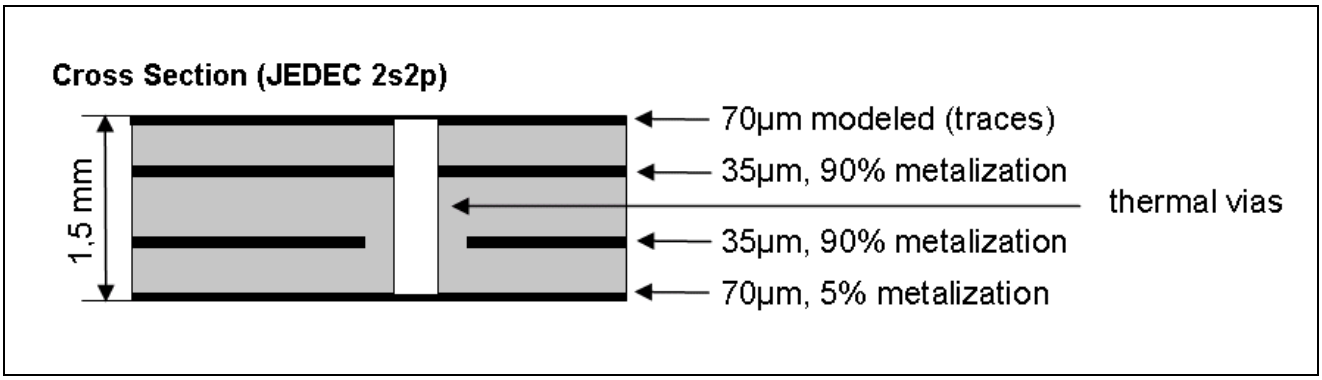


Figure 1 Cross Section High conductivity PCB (JEDEC JESD 51-5 and JESD 51-7)

As shown in Figure 1 the thermal vias are connected only to the first inner layer. According to the JEDEC standard the second inner layer is not connected.

In the high thermal conductivity standard the PCB is described as 2s2p board. This means, that the board is composed by two signal layers (70µm) and two inner planes (35µm).The buried planes should simulate a V_{BB} or ground potential layer with the dimensions of 74.2 x 74.2 mm.

For both packages the same via grid was used in the simulation. The maximum PCB temperature was analyzed below the hottest channel. For the calculation of the thermal resistances the maximum temperatures are used.

3 Chip Layout and Power Dissipation Impressed

In both packages the same product chip SPOC BTS5682E was considered. The layout can be seen in Figure 2.

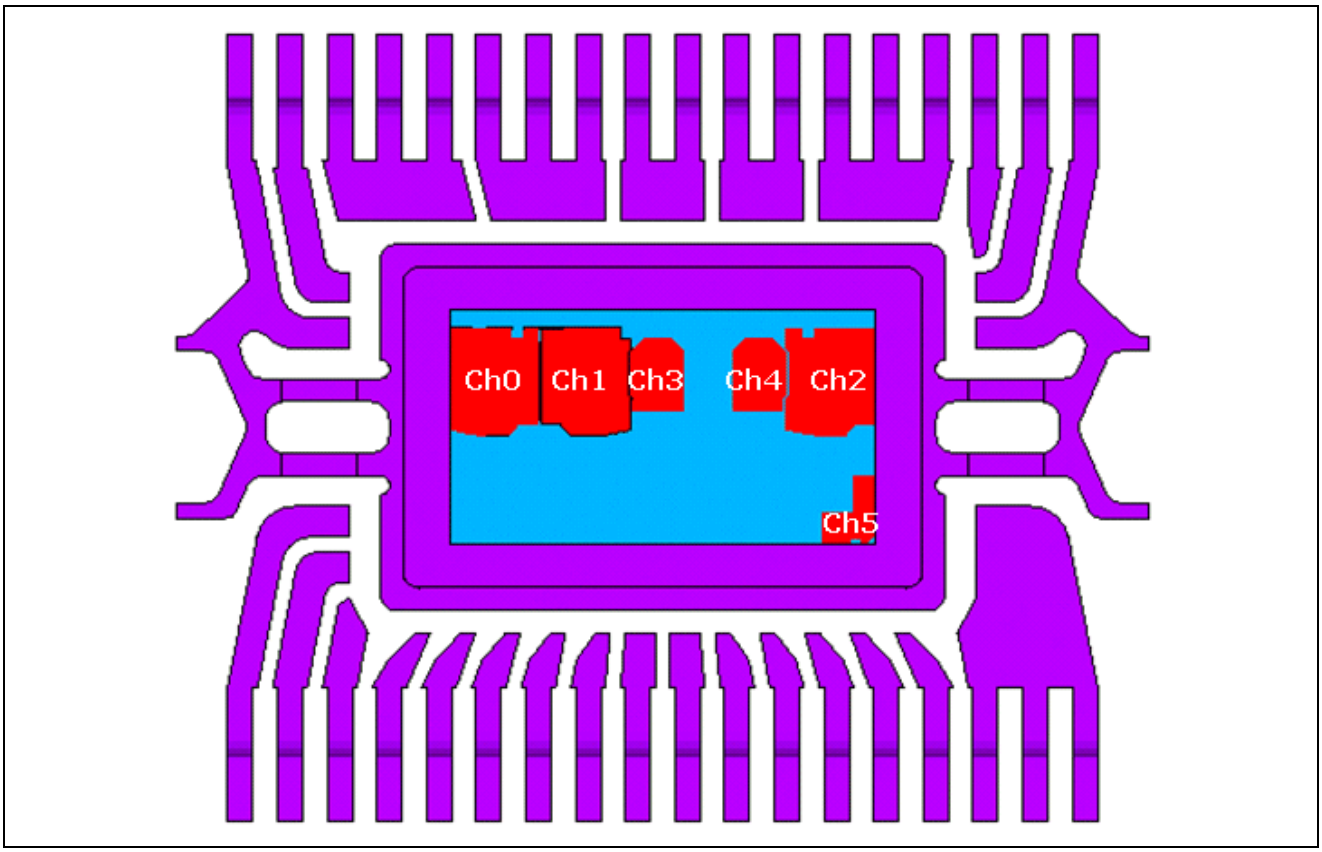


Figure 2 Layout of the considered product chip

The power dissipation levels are only applied in the red pigmented channels (channel 0 to 5). The other colors represent the logic part of the chip. The applied power dissipation levels are dependent on the dimensions of the different channels. The biggest channels (Channel 0, Channel 1 and Channel 2) with the lowest On-State resistances are stressed with the highest power dissipation levels. The other channels are stressed with a lower power dissipation level:

Table 2 Power distribution

Channel	P_d
Channel 0, 1, 2	P_d
Channel 3, 4	P_d / 2
Channel 5	P_d / 4

The used power dissipation pattern is similar to the real application case.

4 DSO Packages used for the Comparison

4.1 Thermally enhanced standard DSO Package

In this assembly, in addition to the bond-wires physical connections between the die and some pins are provided. Thus, a higher heat flow from the junction to the pins can be achieved. The assortment of the connected pins is simple - the pins with the highest power dissipation should be selected. Thus an improvement of the thermal behavior compared to standard packages can be achieved.

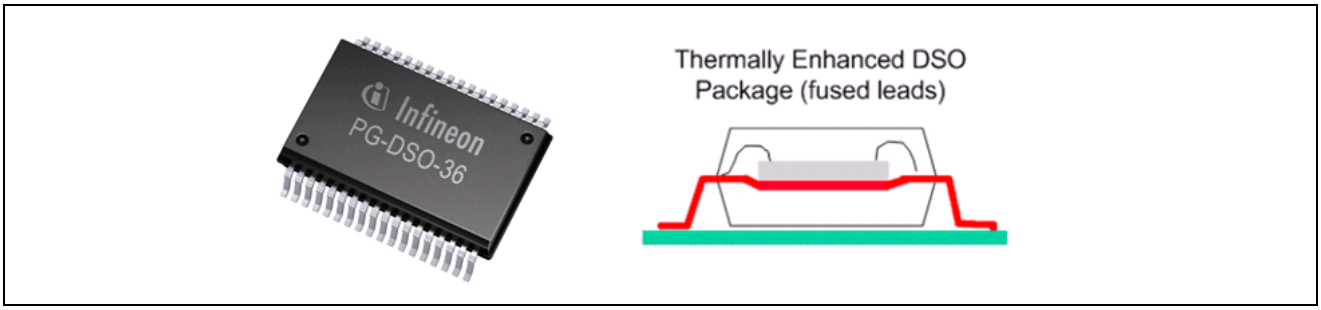
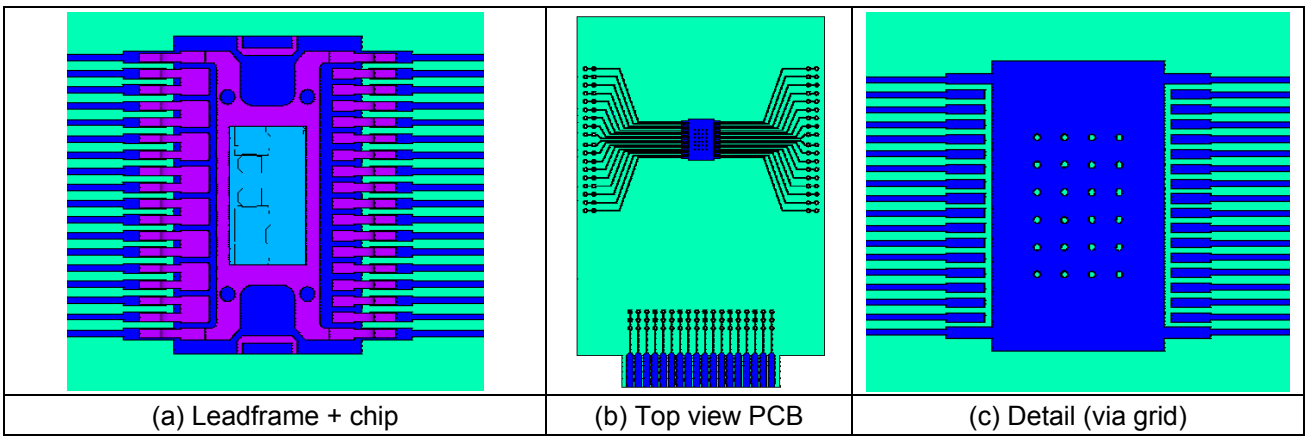


Figure 3 General Schematic of Thermally Enhanced Package



(a) Leadframe + chip	(b) Top view PCB	(c) Detail (via grid)

Figure 4 Schematic of the Leadframe and JEDEC PCB Used for Thermally Enhanced DSO Package

Figure 4a displays the top view of the leadframe with the chip. The corner pins are called fused leads because they are directly connected to the leadframe. In that case the main heat flow path is from the leadframe to the fused leads. Thus it makes sense to connect the fused pins to the via grid (Figure 4c) to improve the steady state thermal performance. Two different simulations are shown below, one with and one without the connection of the top layer with the first inner layer. Figure 4b shows the top view of the used JEDEC high conductivity PCB. Figure 5 shows that the main heat flow path, besides others like radiation from mold surface to the ambient, will appear from the junction to the fused pins.

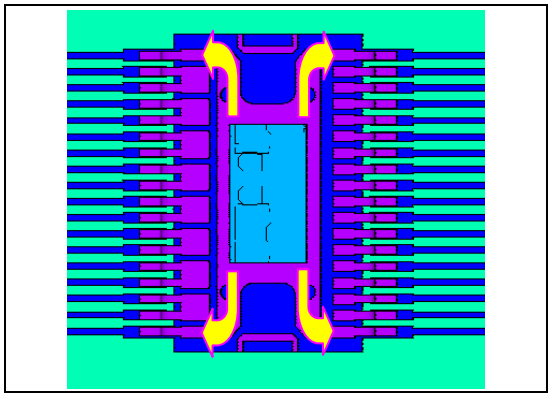


Figure 5 Main heat flow path of Thermally Enhanced DSO Package

4.2 Exposed Pad DSO Package

To satisfy the future trend of miniaturization Infineon developed an exposed Pad package, which should bridge the gap between thermally enhanced DSO packages and power DSO packages. The body size is comparable with before mentioned standard DSO packages. The die is directly soldered or glued on the exposed pad. Thus, a main heat flow path from the die to the exposed pad and the PCB cooling area is realized.

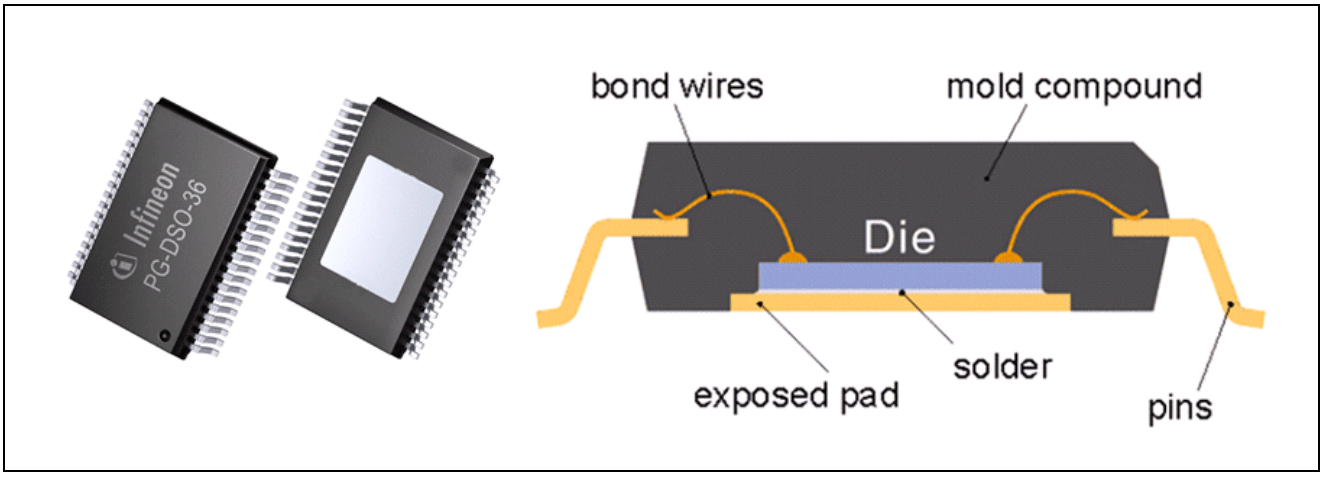


Figure 6 General Schematic of Exposed Pad Package

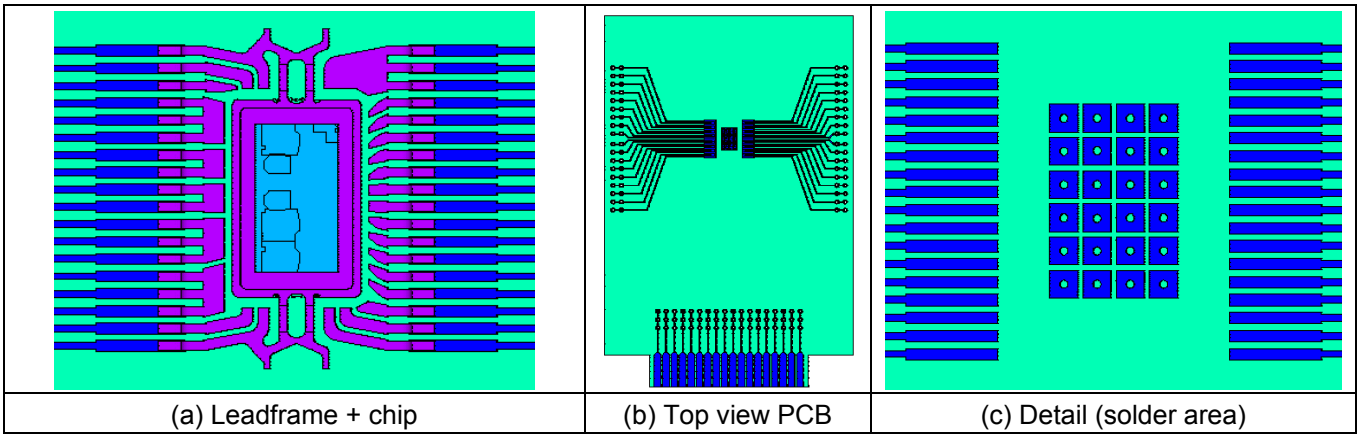


Figure 7 Schematic of the Leadframe and JEDEC PCB Used for ePad Package

Figure 7a displays the top view of the leadframe with the chip. The main heat flow will appear in the lowest thermal resistive path. In this case nearly 90% of the heat generated flows away from the junction to the PCB via the ePad. Thus a high thermal conductivity PCB with thermal vias should be used to get a good heat flow into the PCB. The ePad should be soldered to the thermal vias to get a good thermal connection.

5 Results

The following diagram shows the $Z_{th\text{-}JA}$ curves for the channel heating situation of Table 2. The Z_{th}-curves were calculated for all channels active. The total power loss can be seen in Table 4:

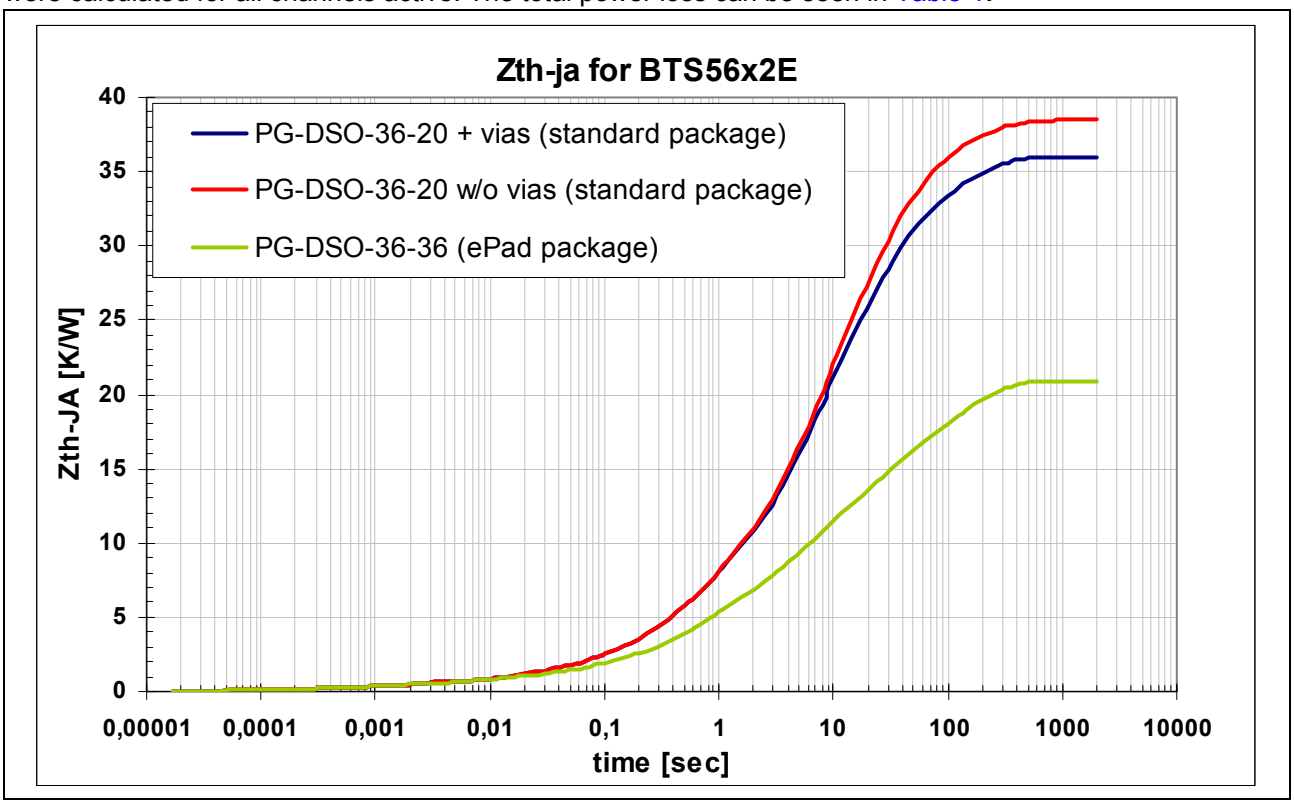


Figure 8 $Z_{th\text{-}JA}$ of different packages with SPOC II product chip

The green curve represents the ePad package. In this case the ePad is soldered to the thermal vias. That means there is a good thermal connection. The thermal package performance can not be done by the comparison of the $Z_{th\text{-}JA}$ curves, because for the ePad package the limiting factor is the maximum PCB-temperature of 130°C (for standard FR4 PCB material). The temperature of the ePad is nearly equal to the PCB temperature. The junction temperature is only slightly higher (≈1°C) than the ePad temperature, because the thermal resistance between the junction and the thermal vias is very low. The heat dissipation from the junction to the ePad is very high which results to a low $R_{th\text{-}JA}$ value: 21 K/W

For the standard package the maximum junction temperature of 150°C has to be considered as maximum.The red curve without vias at the standard package (PG-DSO-36-20) in Figure 8 was produced to see the difference of the Z_{th}-curve compared to the standard package with thermal vias. In this case no thermal connection from the package to the vias are given. The difference of the static $R_{th\text{-}JA}$ can be seen in the following table:

Table 3 Comparison of $R_{th\text{-}JA}$ of standard package

Standard package	$R_{th\text{-}JA}$ [K/W]
without thermal vias	38.5
with thermal vias	36

As it can be seen in Figure 8 in case of the standard package there is no difference of Z_{th} value up to 10 seconds. The explanation is that the effects of the thermal vias on the PCB are not visible at these short times. The difference of the static thermal resistance is about 2.5 K/W (that are 6.5%). The difference can be explained that the traces of the fused pins of the leadframe (corner pins in Figure 4) are connected to the thermal vias on the PCB.

6 Conclusion

For a serious comparison between both packages (package with JEDEC PCB) the maximum power dissipation levels needs to be evaluated according the following explanations.

The temperature rise of the product in the steady state can be calculated by:

(1) $\Delta T = R_{th} * P_d$

ΔT *temperature difference [K]*
R_{th} *static thermal resistance [K/W]*
P_d *power dissipation level [W]*

In case of the standard package the limiting factor is the maximum junction temperature of 150°C. For example the maximum power dissipation level of the standard package without vias can be calculated:

$$\Delta T = T_{j,\max} - T_a = 150°C - 85°C = 65°C$$

$$\Delta T = R_{th} * P_d \Rightarrow P_d = \frac{\Delta T}{R_{th}} = \frac{65°C}{38.5\frac{°C}{W}} = 1.7W$$

Furthermore for the ePad package the limiting factor is the maximum PCB temperature of 130°C:

$$\Delta T = T_{FR4,\max} - T_a = 130°C - 85°C = 45°C$$

$$\Delta T = R_{th} * P_d \Rightarrow P_d = \frac{\Delta T}{R_{th}} = \frac{45°C}{20.9\frac{°C}{W}} = 2.2W$$

The maximum power dissipation levels of each package are summarized in Table 4:

Table 4 Maximum power levels

Package	Total P_d [W]
Standard without thermal vias	1.7
Standard with thermal vias	1.8
ePad with thermal vias	2.2

With those boundary conditions the ePad package is able to handle the highest total power dissipation level. The ePad package is able to handle 20% more power compared to the standard package with vias.

Further improvement of the $R_{th\text{-}JA}$ can be achieved by reducing the thermal resistance between the solderpoint and the ambience. The resulting reduction of the $R_{th\text{-}JA}$ for the exposed pad package will be significantly higher than for the standard package, because of the lower thermal resistance junction to solderpoint of the ePad package.

7 Additional Information

7.1 Simulation Power Conditions

The table below shows the power dissipation values, which were applied for the thermal simulations:

Table 5 Power distribution per each chanel

Package	Total P_d [W]	Pd (Ch0,1,2) [W]	Pd (Ch3,4) [W]	Pd (Ch5) [W]
Standard without thermal vias	1.7	0.4	0,2	0.1
Standard with thermal vias	1.8	0.42	0.21	0.105
ePad with thermal vias	2.2	0.52	0.26	0.13

7.2 Table of Abbreviations

PCB	**P**rinted **C**ircuit **B**oard
DSO	**D**ual **S**mall **O**utline
JEDEC	**J**oint **E**lectron **D**evice **E**ngineering **C**ouncil
ePad	**E**xposed **Pad** Package
P_d	**P**ower **D**issipation Level
R_{th}	Static **Th**ermal **R**esistance
Z_{th}	Transient Thermal Impedance
FR4	**F**lame **R**etardant **4**

- More information regarding SPI Power Controllers and Semiconductor devices can be found at **http://www.infineon.com/spoc**

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