Title - ZU104 Validation Plan/Procedure/Analysis

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Table of Contents

Introduction

This document is used to document and record the power supply programming, bringup, and validation for Xilinx ZU104 program.

Documents

The following documents are used for this validation plan.

Table 1 – Document and File Description

Originator	Title	Description
Xilinx	0381794_HW-Z1-ZCU104_REV_A_SCHEMATIC_20170516_145101	Schematic
Xilinx	ZCU104_REVA_PATCHES	Rev A PCB Rework
Xilinx	HW-Z1-ZCU104-final	Layout
Infineon	IRPS5401MXI04TRP_MTPplus3_0.85_1.8_1.2CD_0.9_800k_Rev0_8_DRC	U179 Configuration
Infineon	IRPS5401MXI04TRP_MTPplus3_3.3_1.13_5.0_1.8_0.85_800k_Rev0_7_drc	U180 Configuration
Infineon	Xilinx ZU104 Programming and Bringup_LL_6_22_17	Programming Instructions

Test Equipment

The following is the test equipment used for validation purposes.

Table 2 – Test Equipment

Item	Manufacturer	Function	Model/Description
1		Power Supply	
2	Fluke	DMM	
3	Tek	Oscilloscope	
4	Tek	Differential Probe	
5	Tek	Passive Probe	
6	N/A	Coax Probe	
7	Infineon	Comms	USB005
8	Infineon	GUI	Power Center
9	Chroma	Electronic Load	

DC/DC Converter Overview

The below reference designators are the voltage regulators designed onto the ZU104 platform and tested as part of the validation plan/procedure. The voltage rails associated with each are listed. Note there are multiple ref des associated with a few voltage rails due to the use of power stages.

Table 3 - Ref Des Description

Ref Des	Manufacturer	Schematic Page	Voltage Rail
U179	Infineon	47	VCCINT
			VCC1V8
			VCC1V2
			MGTAVCC
U175	Infineon	48	*VCCINT (power stage)
U180	Infineon	49	UTIL_3V3
			UTIL_1V13
			UTIL_5V0
			VADJ_FMC
			MGTRAVCC
U176	Infineon	50	*UTIL_3V3 (power stage)
U173	Infineon	51	VCC3V3
U171	Infineon	52	MGT1V2
U174	Infineon	53	MGT1V8
U172	Infineon	54	UTIL_2V5
U177	Infineon	55	PL_DDR4_VTT
U178	Infineon	55	PS_DDR4_VTT

Programming

The programming procedure assumes a board populated with an IRPS5401, U179 and U180, having no pre-programmed configuration in the NVM.

Please confirm all REVA_PATCHES are complete. In addition, ensure the bootstrap cap near the power stages are present, C1370 and C1367.

Follow steps in “Xilinx ZU104 Programming and Bringup_LL_6_22_17.doc”.

Power Sequencing

The following table must be adhered to in order to meet POR sequence requirements.

DCDC Converter Validation Results

The following sections document the DCDC converters with respect to the following test conditions and measurements.

1. DC Voltage
    a. All DC measurements are recorded by use of a true RMS DMM to ensure accuracy and validation with the GUI reported results.
2. DC Ripple (Steady-State)
    a. DC ripple is measured with a differential active probe or an analog coax probe (ac coupled) where precision noise floor measurements are required. Note o-scope offsets are in effect and absolute DC reference point must be measured by the DMM and are recorded as the DC voltage.
3. ac transient response (Large Signal Analysis)
    a. All ac transient measurements are measured with respect to the valley/valley or peak/peak for loading and releasing events respectively. Note 0-scope offsets are in effect and absolute DC reference point must be measured by the DMM and are recorded as the DC voltage.
4. Current Sense Accuracy
    a. Where telemetry is available, the calibrated E-load is used to verify the telemetry reporting accuracy.
5. Protection (OCP)
    a. Where the programmability occurs, magnetic ratings on Isat allow, and test access allows, OCP protections are checked for accurate triggering. In some instances, the OCP rating may be artificially adjusted to check the operation of OCP but may not be the final programmed rating due to other HW limitations.
6. Sequence Timing

Acceptance test parameters are as follows:

1. DC Ripple
    a. 10mV
        i. MGTAVCC, MGTRAVCC, MGT1V2, and MGT1V8
    b. 30mV
        i. VCCINT
    c. 50mV
        i. Others
2. Vac Transient
    a. ±20 mV @ 50% step, 1A/us
        i. MGTAVCC, MGTRAVCC, MGT1V2, MGT1V8
    b. ±30 mV @ 25% step, 1A/us
        i. VCCINT
    c. ±50 mV @ 50% step, 0.5A/us
        i. Others

3. OCP
    a. Where circuit allows, ensure OCP meets design
    b. Else, ensure ample margin to prevent for false OCP
4. Sequencing
    a. POR guidelines met

Design Change Recommendations

Any design change recommendations are embedded within the subsections to follow and are denoted in **RED**.

VCCINT

Vin, 12V
Vout, 0.85V
Iout(pk), 15A
Istep, 3.75A
Iramp, 1A/us

Vout Measurement Location, C1216
Load Test Location, J25/C696/C697
SW Node Measurement Location, L82

Jitter = 31ns (0A load) – 49ns (15A load)
** note - large pigtail loop present due to load equip location*

Design Recommendations:

- **Add 10 ohm BODE 0603 resistor with test points for soldering**

Rev B Tuning (for IFX)

- Slightly reduce PI strength

Table 4 – VCCINT Results

Measurement	Result	Pass/Fail	Test Condition	Notes
Vout	0.849V (0.852V) 0.840V (0.848V)	Pass	0A 15A	DMM (GUI)
DC Ripple	11.2mV 10.8mV	Pass	0A 15A	
Isense	0.25A 5.13A 10A 14.25A	Pass	0A 5A 10A 14.5A	Telemetry/E-load *(ISCALE updated to 59 decimal (0x3B))*
Vac(droop)	4.4mV	Pass	10.75A to 14.5A	
Vac(overshoot)	5.0mV	Pass	14.55A to 10.75A	Increased to 5A step to measure quantitative excursion

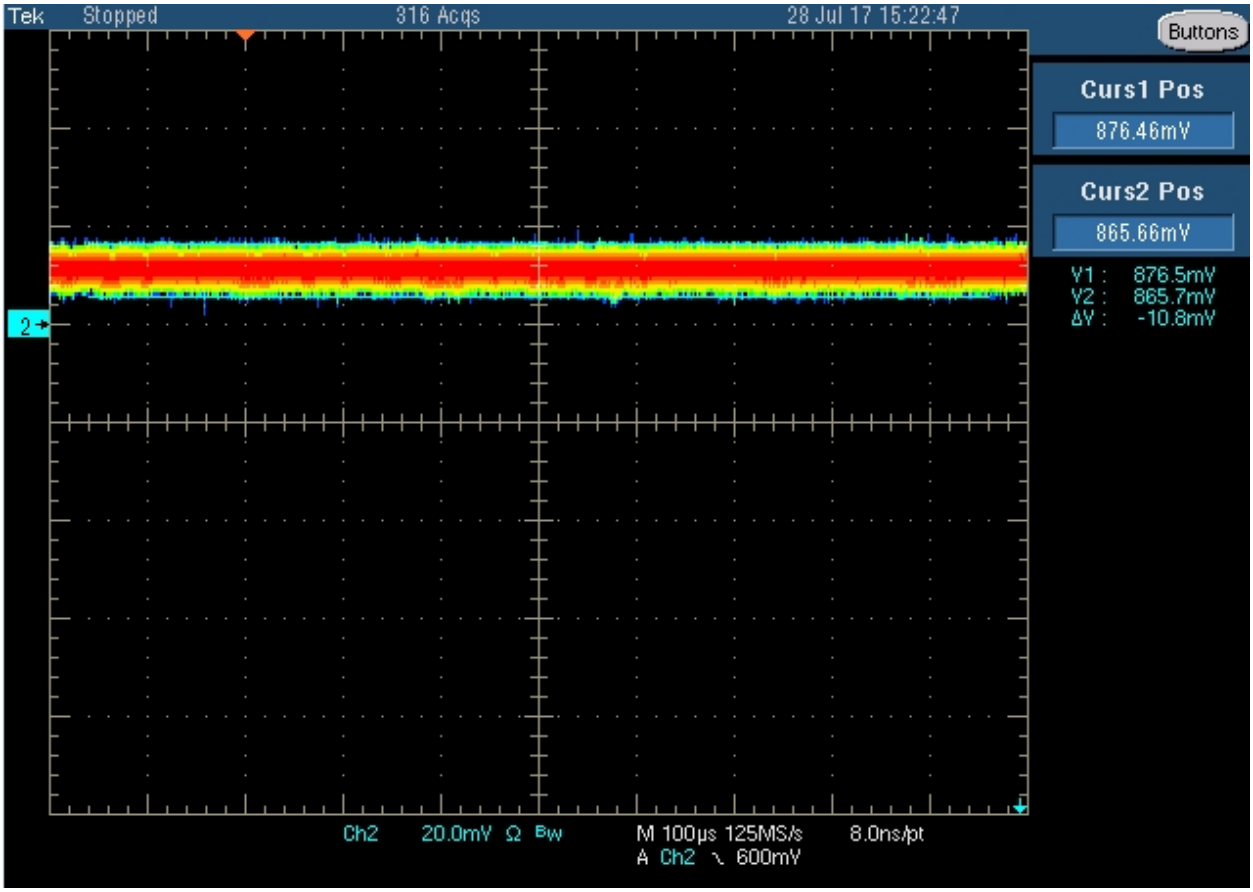

Figure 1 - VCCINT DC Ripple, 15A

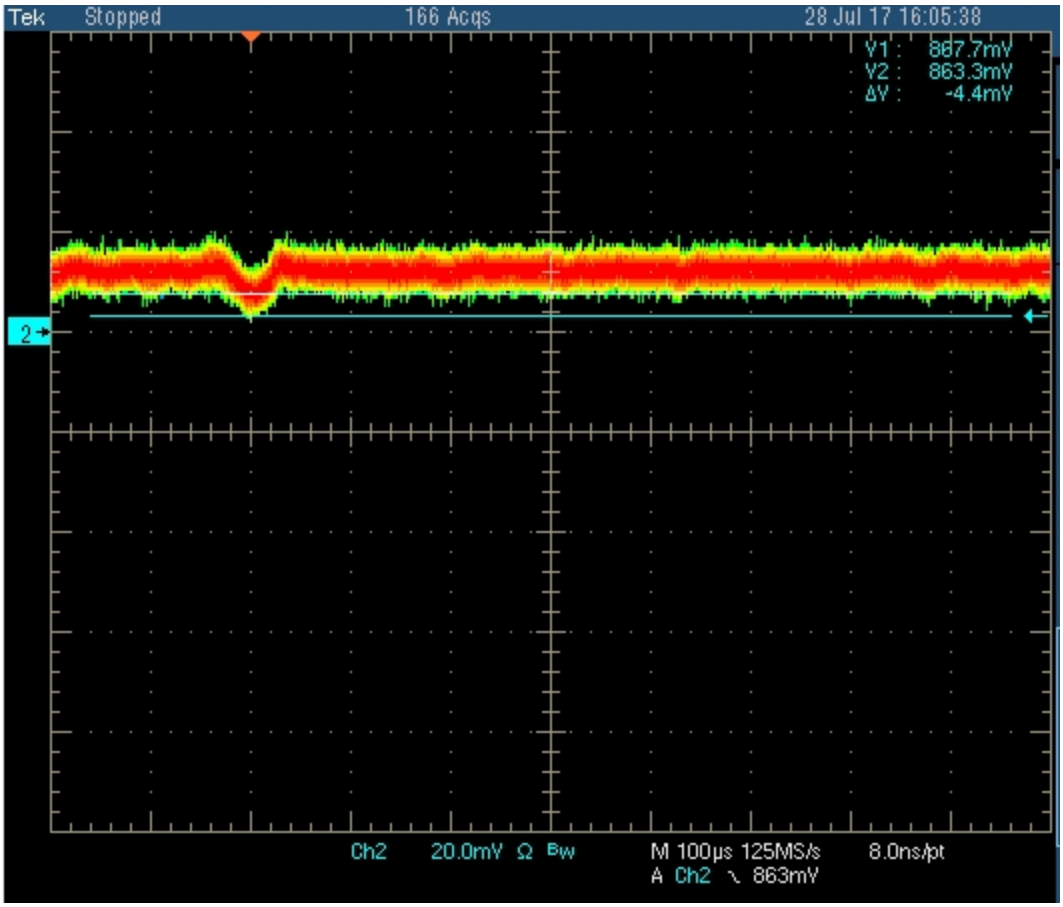

Figure 2 - VCCINT ac ripple load

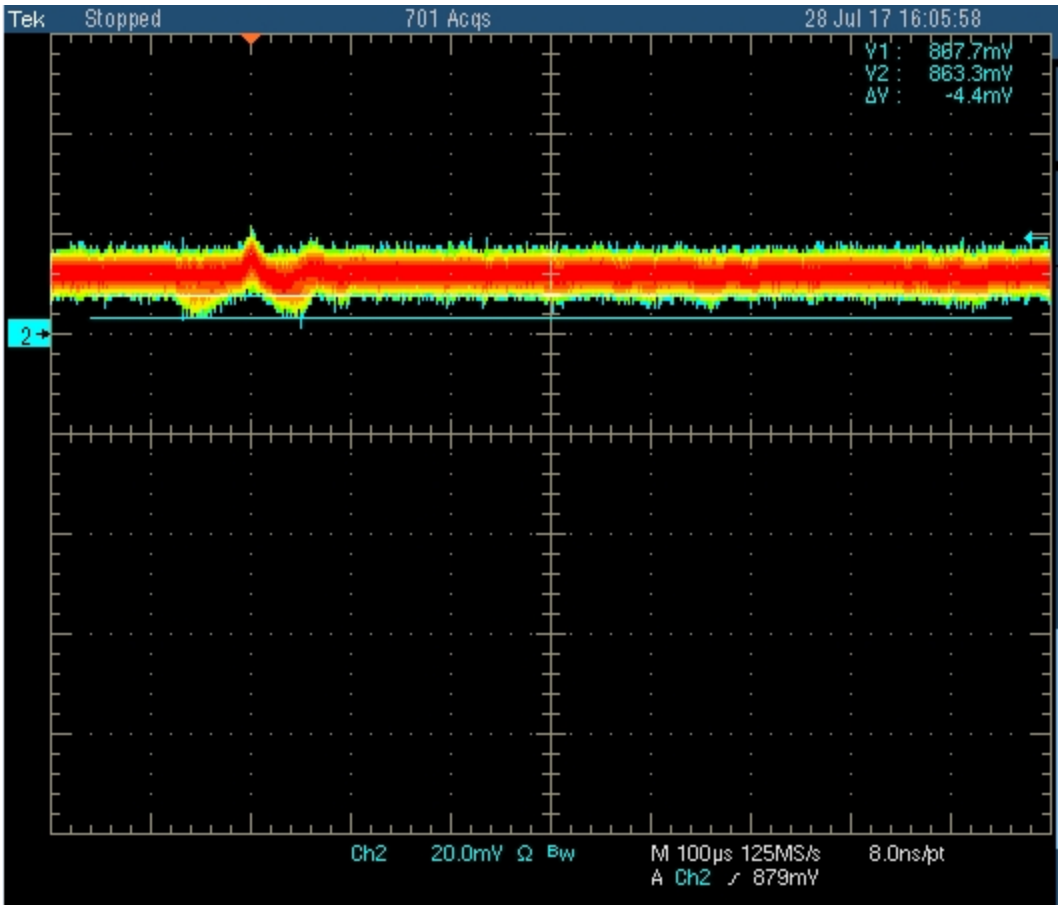

Figure 3 - VCCINT ac ripple release

Figure 4 - VCCINT Jitter, 15A

VCC1V8

Vin, 12V
Vout, 1.8V
Iout(pk), 2A
Istep, 1A
Iramp, 0.5A/us

Vout Measurement Location, J44
Load Test Location, J44
SW Node Measurement Location, L75

Current Sense Measurement – Power Center validated with E-Load
OCP = 2.5A

Jitter = 51.2ns (2A load)

Design Recommendations:

- **Add 10 ohm BODE 0603 resistor with test points for soldering**

Table 5 – VCC1V8 Results

Measurement	Result	Pass/Fail	Test Condition	Notes
Vout	1.799V (1.797V) 1.798V (1.797V)	Pass	0A 2A	DMM (GUI)
DC Ripple	10.4mV 10.8mV	Pass	0A 2A	
Isense	0A 0.97A 1.98A	Pass	0A 1A 2A	Telemetry/E-load
Vac(droop)	20.0mV	Pass	1A to 2A	
Vac(overshoot)	18.0mV	Pass	2A to 1A	

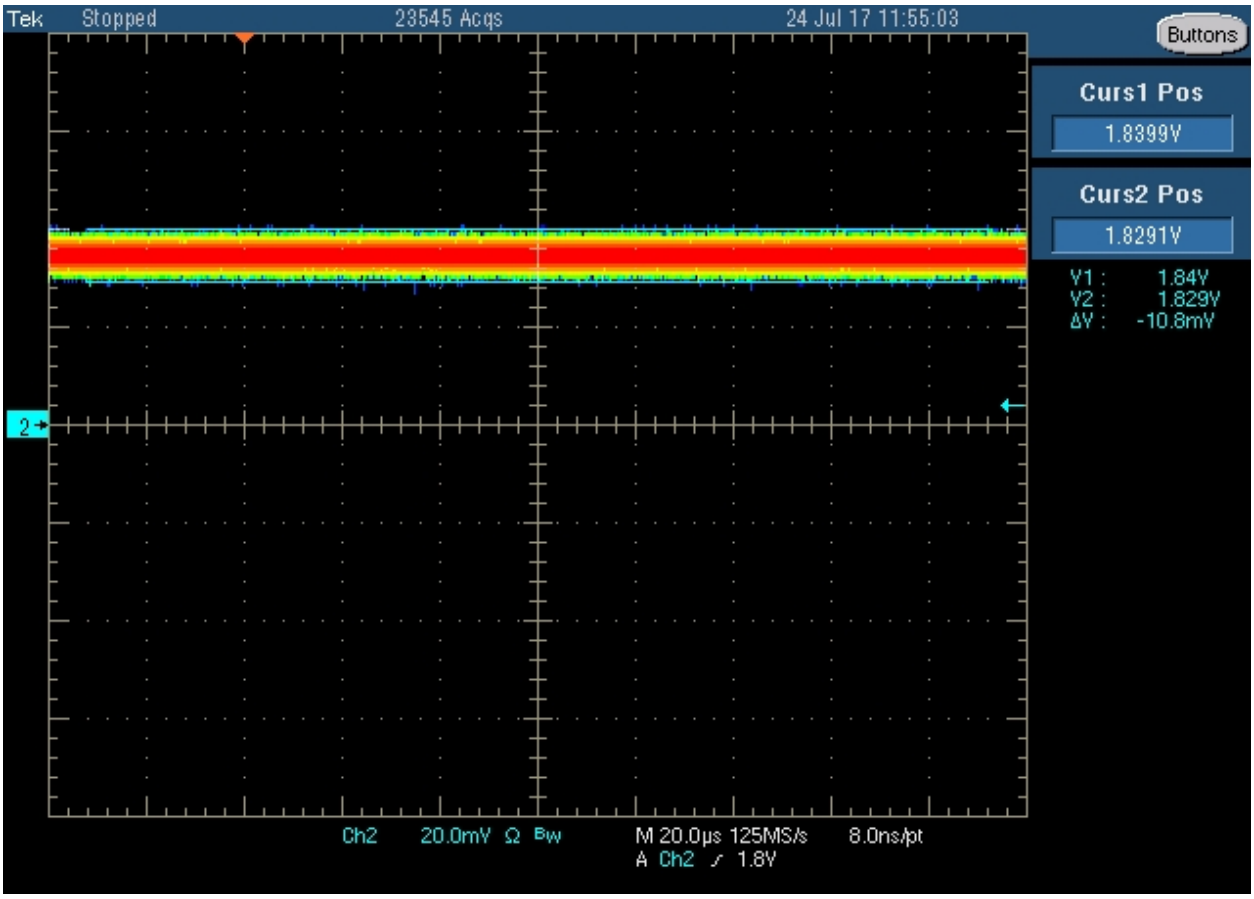

Figure 5 - VCC1V8 DC Ripple, 2A

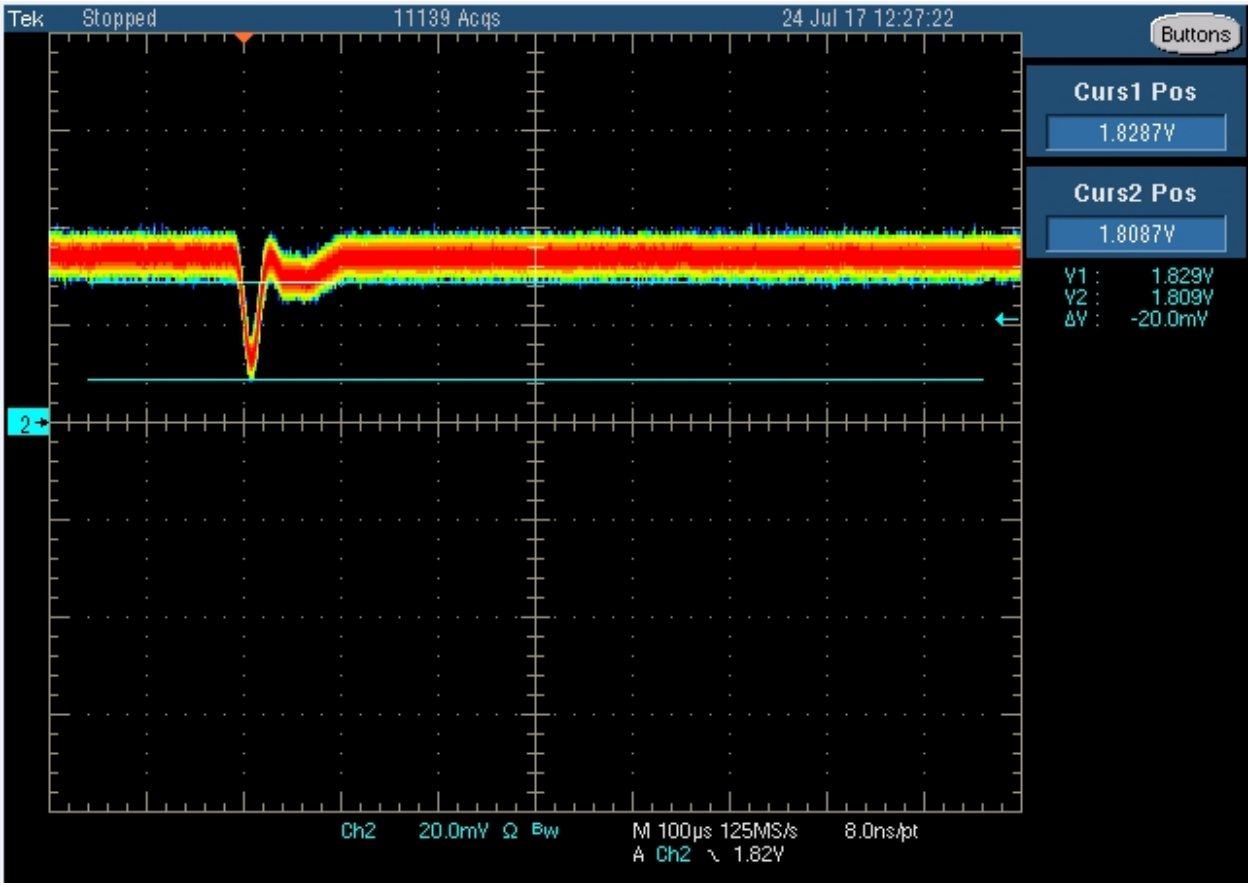

Figure 6 - VCC1V8 ac ripple load

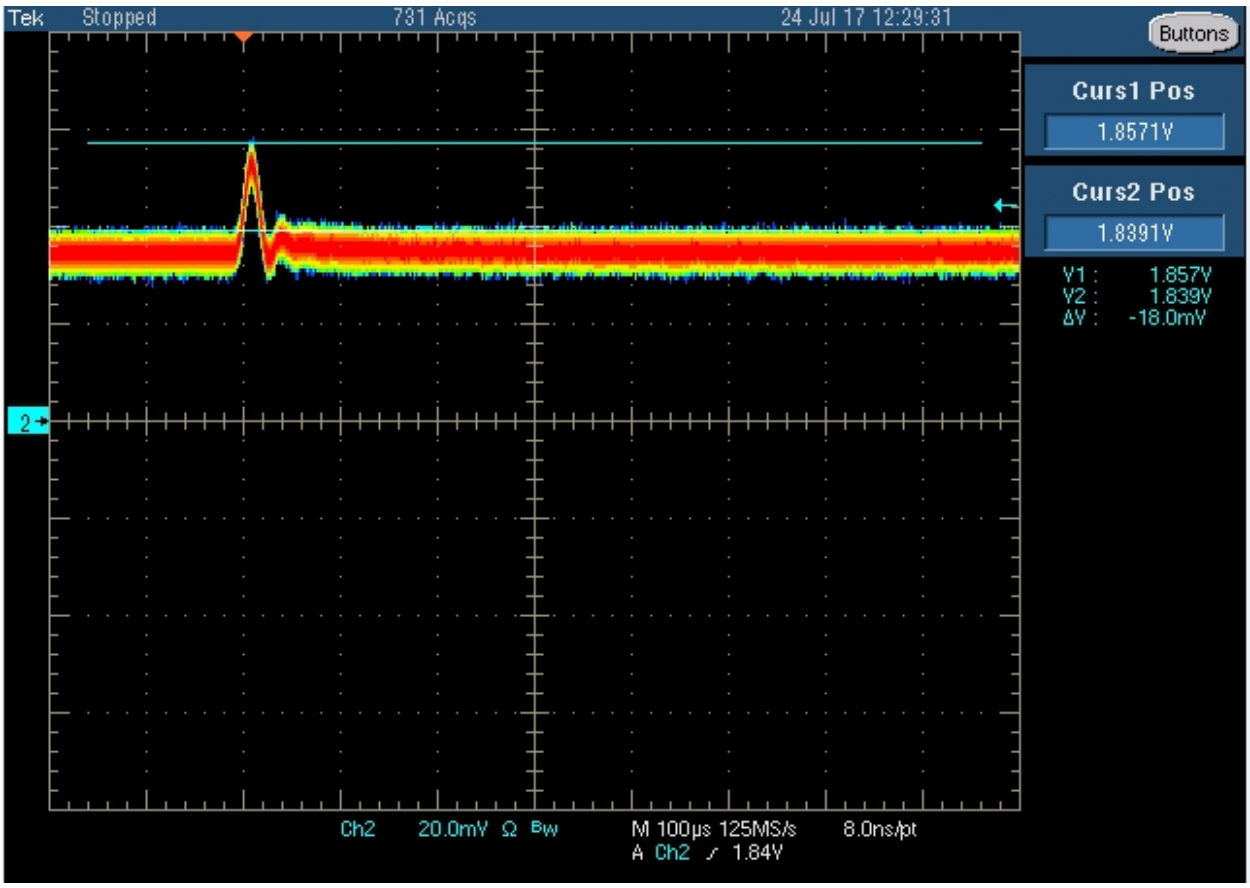

Figure 7 - VCC1V8 ac ripple release

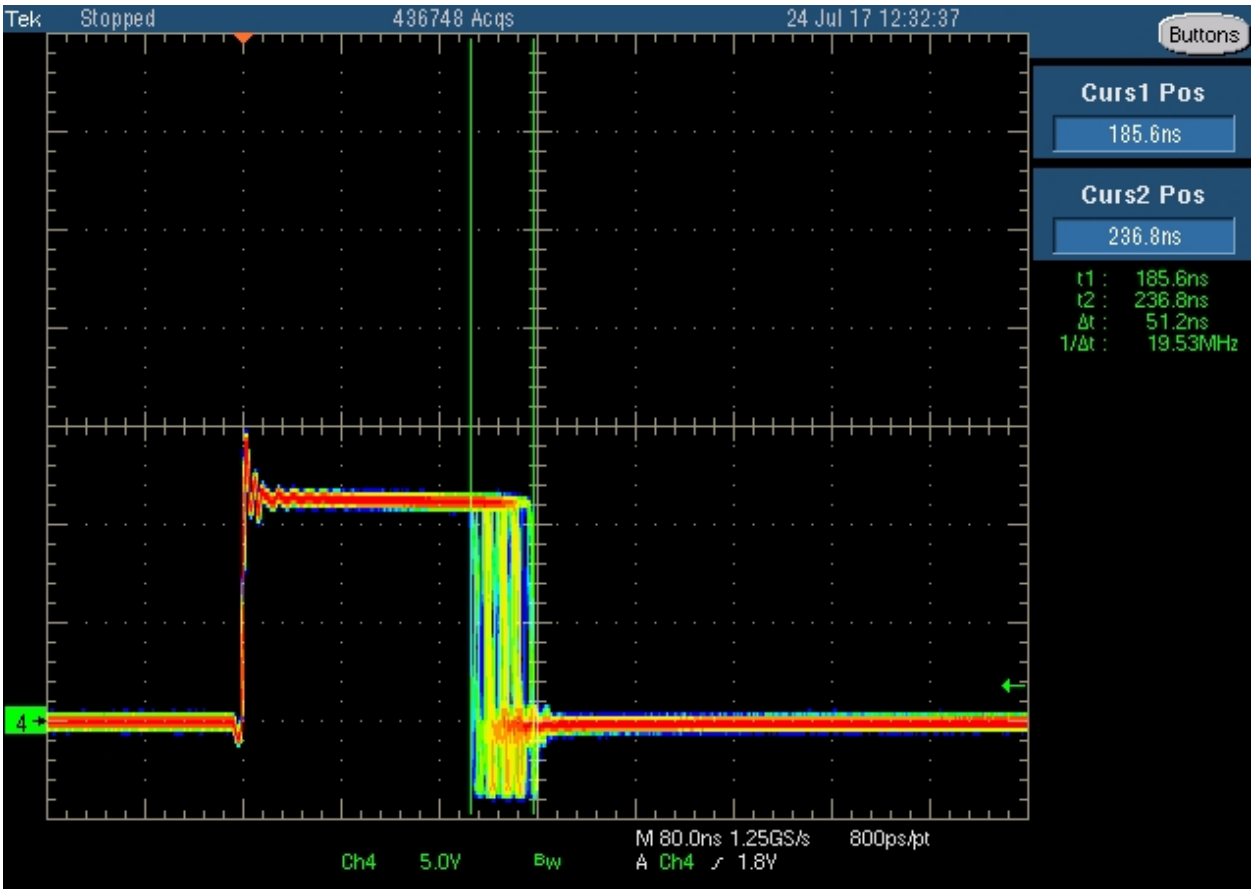

Figure 8 - VCC1V8 Jitter, 2A

VCC1V2

Vin, 12V
Vout, 1.2V
Iout(pk), 5A (8A future)
Istep, 2.5A (4A future)
Iramp, 0.5A/uS

Vout Measurement Location, J167
Load Test Location, J167
SW Node Measurement Location, L76, L77

Jitter = 63ns (5A load)

Design Recommendations:

- **Add 10 ohm BODE 0603 resistor with test points for soldering**
- **Add to Cout at VR for increased load demand to 8A, 4x 22uF**

Rev B Tuning (for IFX)

- Slightly reduce PI strength

Table 6 – VCC1V2 Results

Measurement	Result	Pass/Fail	Test Condition	Notes
Vout	1.203V (1.203V) 1.197V (1.199V)	Pass	0A 5A	DMM (GUI)
DC Ripple	12.0mV 15.6mV	Pass	0A 5A	
Isense	0.0A 0.97A 4.97A	Pass	0.0A 1.0A 5.0A	Telemetry/E-load
Vac(droop)	12.0mV	Pass	2.5A to 5.0A	
Vac(overshoot)	19.6mV	Pass	5.0A to 2.5A	

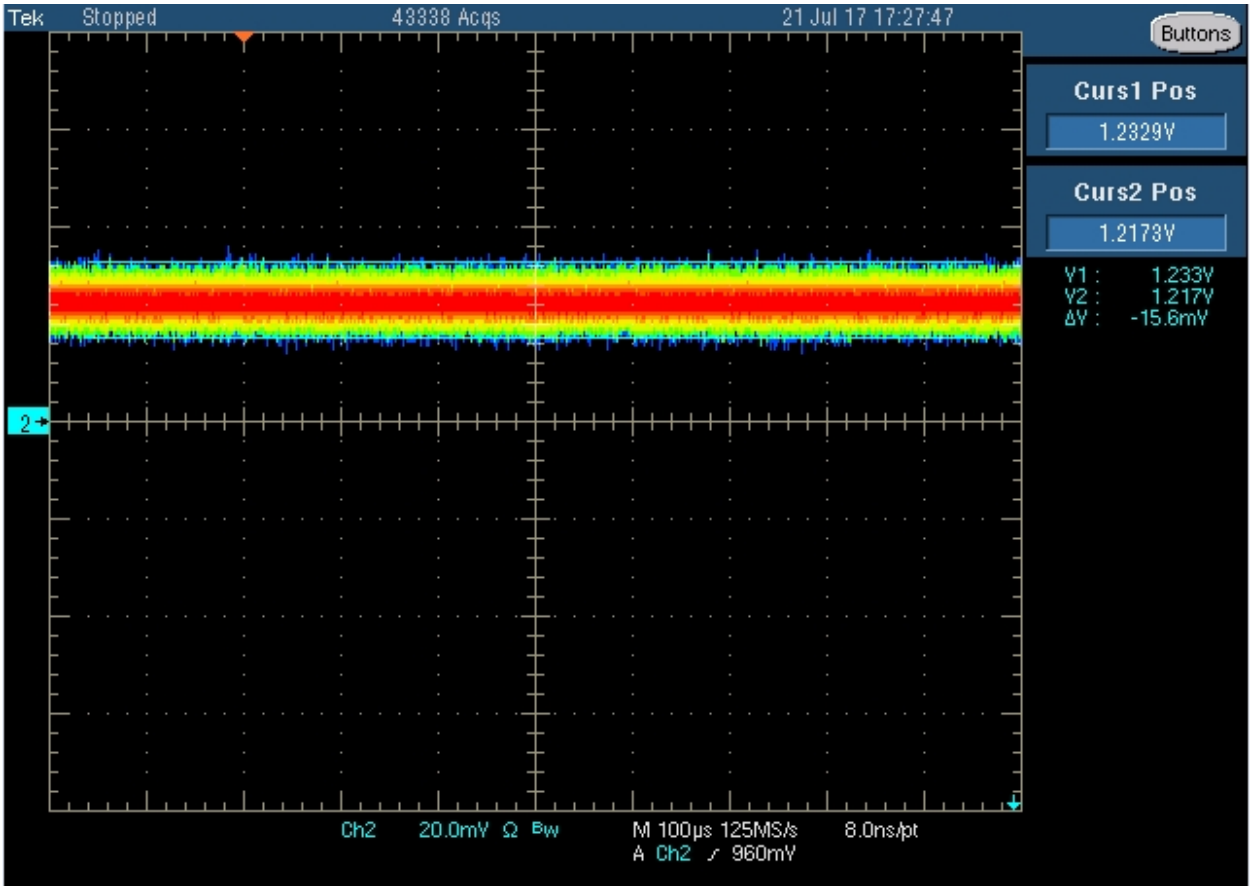

Figure 9 - VCC1V2 DC Ripple, 5A

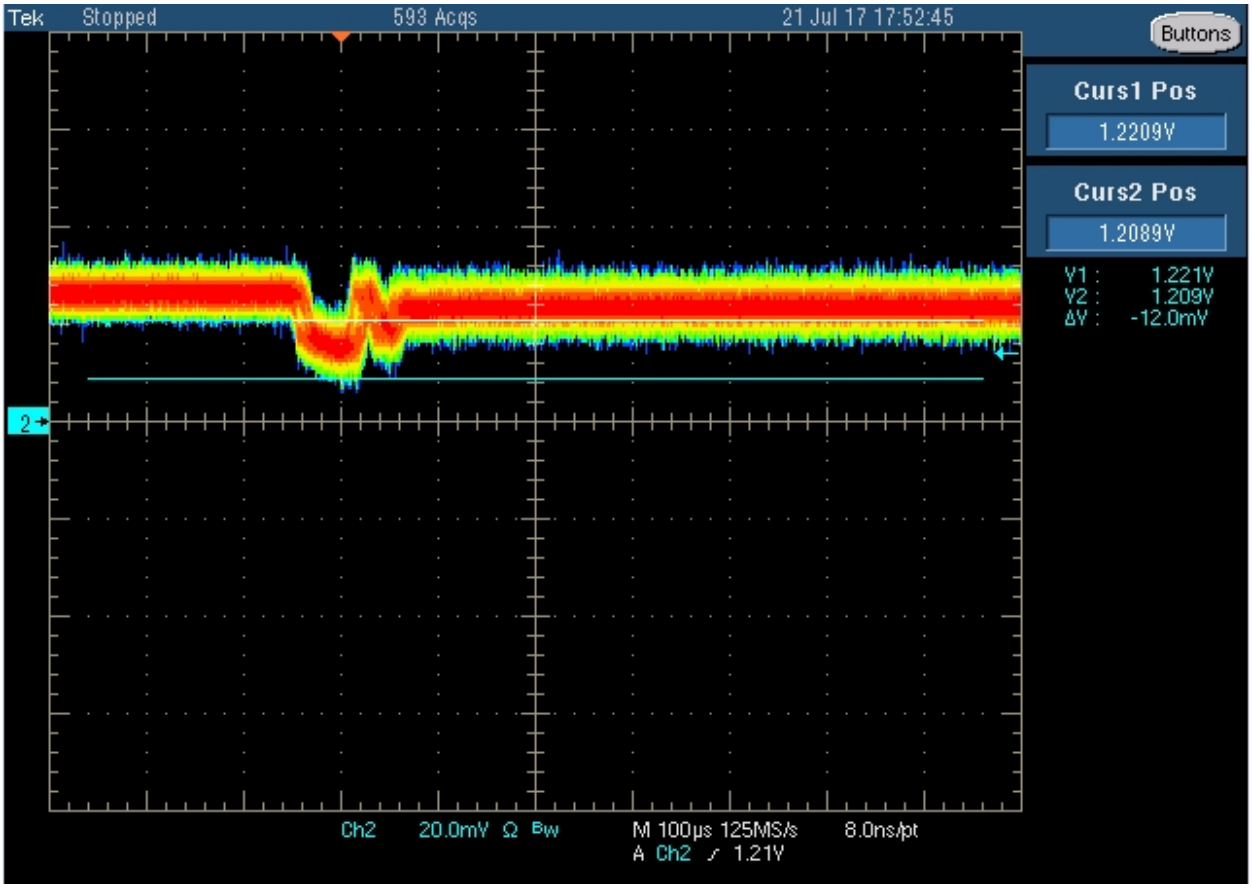

Figure 10 - VCC1V2 ac ripple load

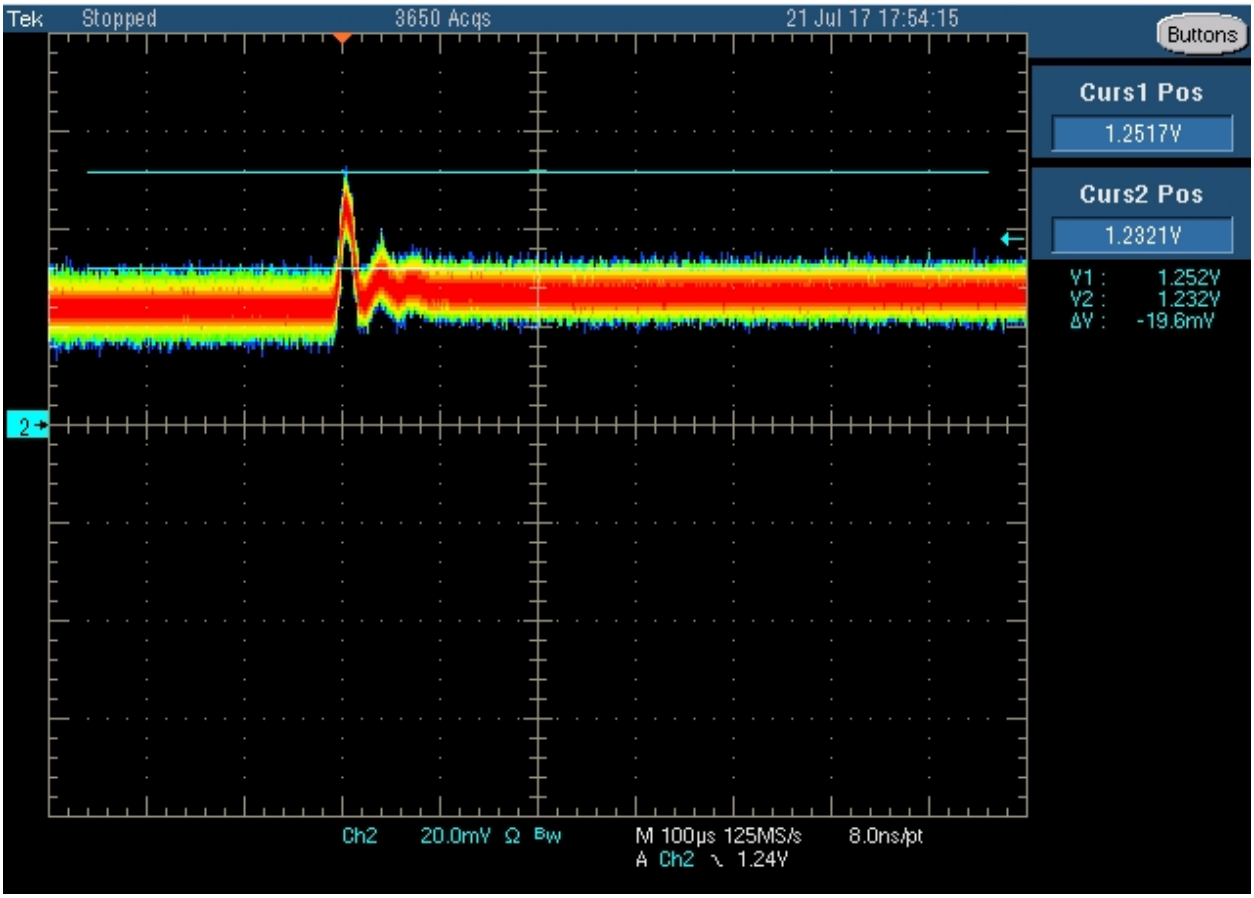

Figure 11 - VCC1V2 ac ripple release

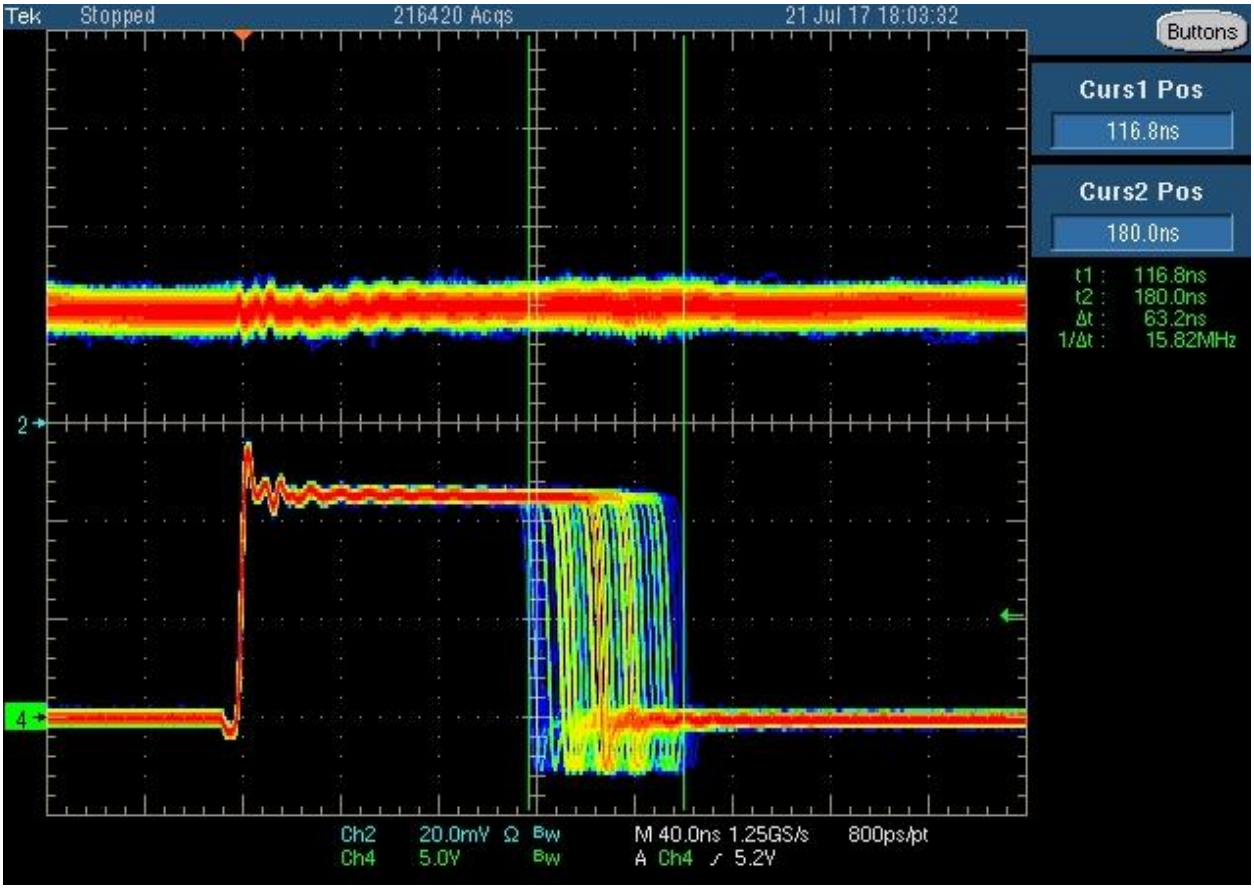

Figure 12 - VCC1V2 Jitter, 5A

MGTAVCC

Vin, 2.5V
Vout, 0.9V
Iout(pk), 0.5A
Istep, 0.25A
Iramp, 1A/us

Vout Measurement Location, J165
Load Test Location, J165

Table 7 – MGTAVCC Results

Measurement	Result	Pass/Fail	Test Condition	Notes
Vout	0.9V 0.899V	Pass	0A 0.5A	DMM (GUI)
DC Ripple	9.6mV 9.6mV	Pass	0A 0.5A	Coax Probe ac coupled
Isense	0A 0.49A	Pass	0A 0.5A	Telemetry/E-load
Vac(droop)	4.0mV	Pass	0.25A to 0.5A	
Vac(overshoot)	4.0mV	Pass	0.5A to 0.25A	

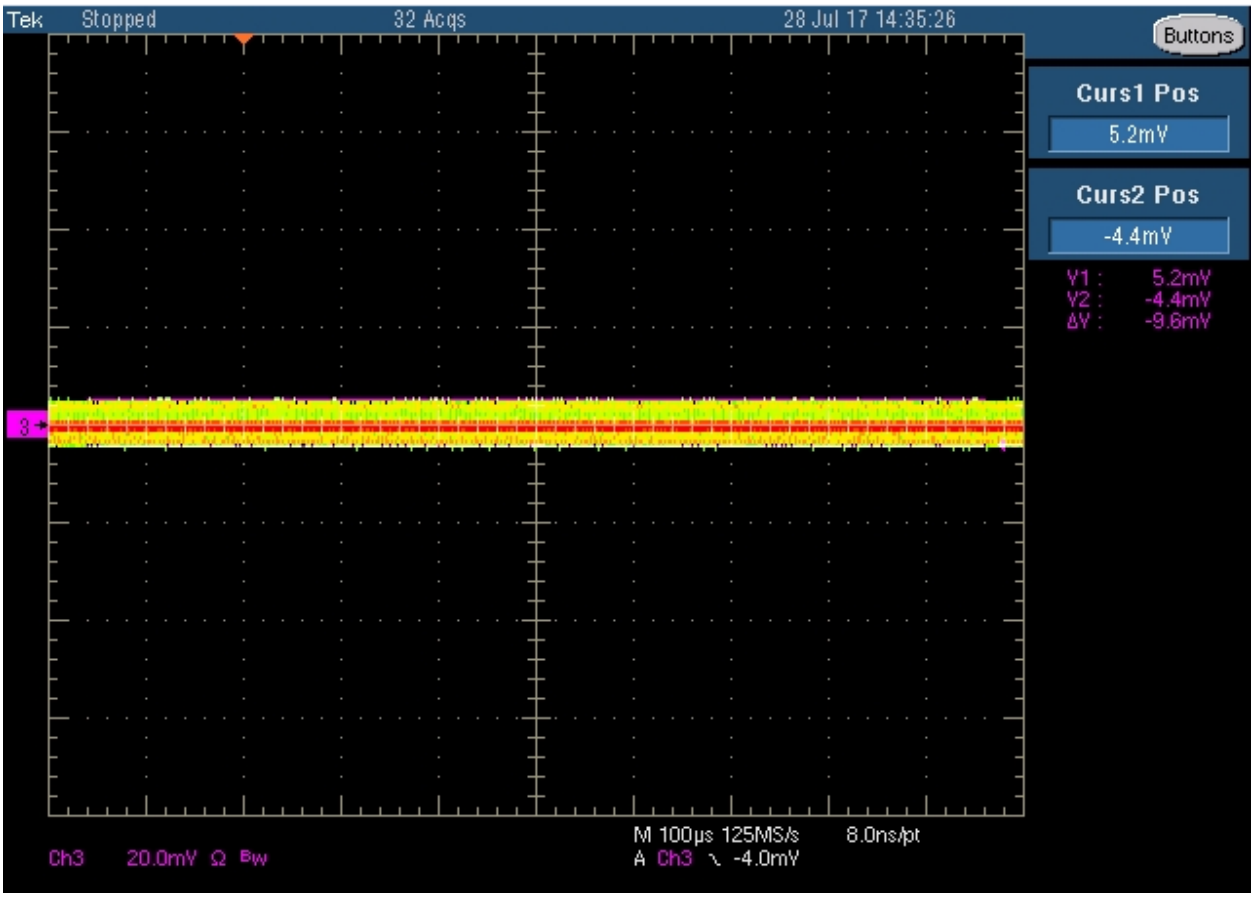

Figure 13 - MGTAVCC DC Ripple, 0.5A

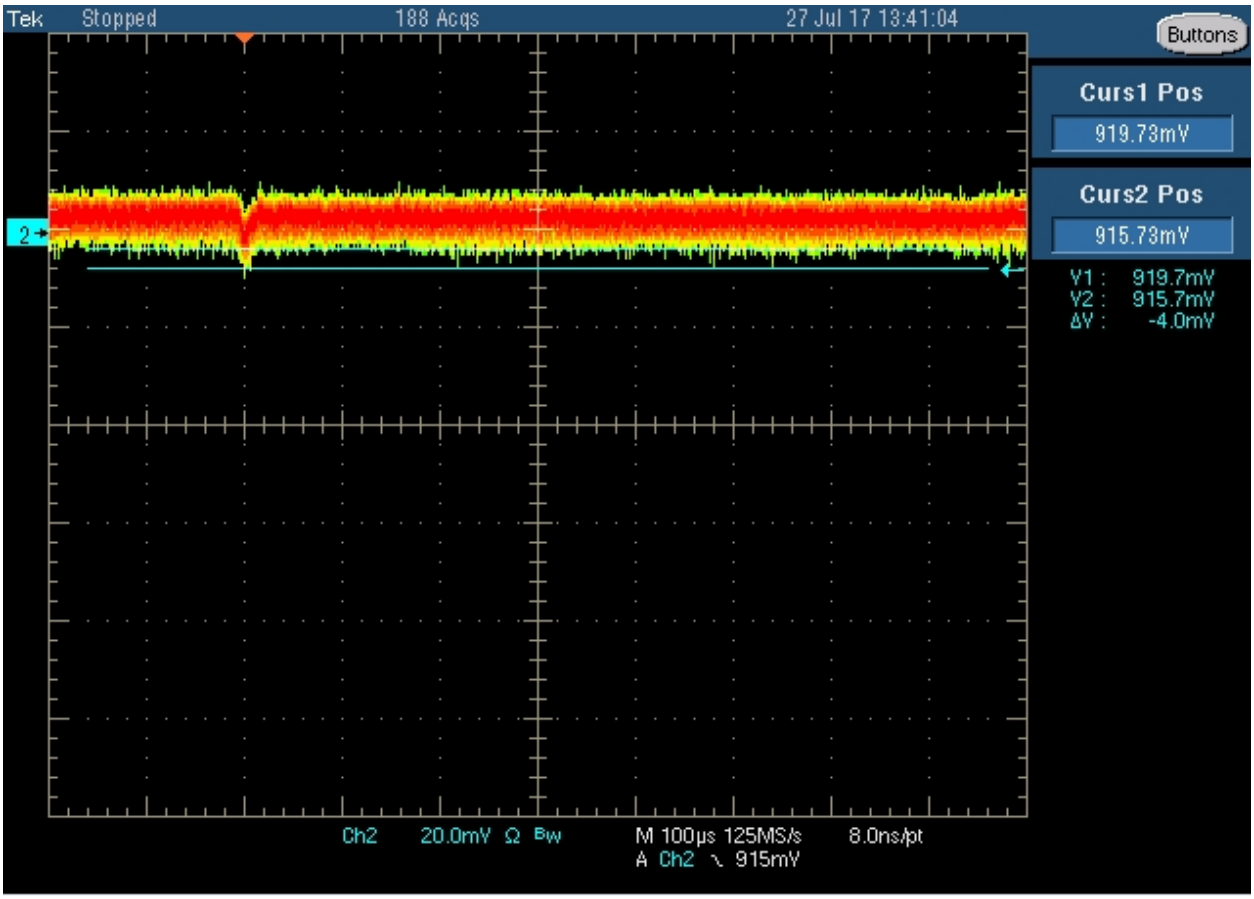

Figure 14 - MGTAVCC ac ripple load

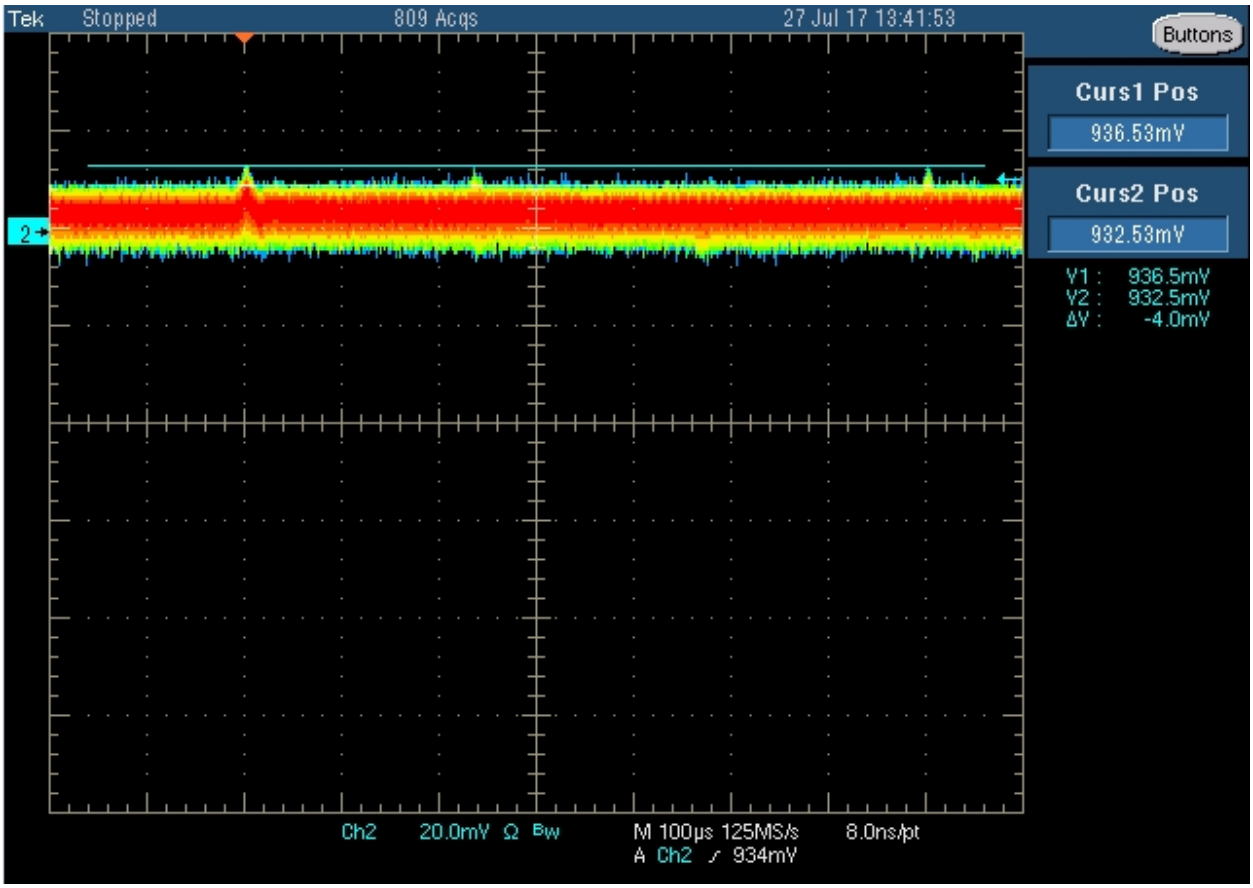

Figure 15 - MGTAVCC ac ripple release

UTIL_3V3

Vin, 12V
Vout, 3.3V
Iout(pk), 10A
Istep, 5A
Iramp, 0.5A/us

Vout Measurement Location, J168/C1418
Load Test Location, J168
SW Node Measurement Location, L83

Jitter = 160ns (10A load)

Design Recommendations:

- **Change location for voltage sense tap to be further from Lout and closer to load(s) across high frequency cap**
- **Remove skinny UTIL_3V3 connections to load and pull from plane (ie layer 2, 5, 14)**
- **Increase Cout**
    - **changing Cout at VR (C1300) to 1x100uF or 2x47uF on top**
    - **adding 2-3 x 47uF/22uF output of VR on bottom**
- **R1158 and R1159 were ~97k. Change to appropriate values in final build.**
- **Add high frequency cap at VR output next to C1300.**
- **Add 10 ohm BODE 0603 resistor with test points for soldering**

PCB Mods Completed for Tests

- Stacked 2x 22uF on C1300 reduced DC ripple and smoothed 1kHz ripple
- Further analysis and test on tuning for secondary LC interactions

Rev B Tuning (for IFX)

- Slightly reduce PI strength after Cout changes

Table 8 – UTIL_3V3 Results

Measurement	Result	Pass/Fail	Test Condition	Notes
Vout	3.314V (3.328V) 3.3072V (3.313V)	Pass	0A 10A	DMM (GUI)
DC Ripple	15.6mV 42.4mV 14.4mV 48.8mV	Pass	0A 0A 10A 10A	C1418 Sense C1418 Sense
Isense	0.63A 5.13A 9.75A	Pass	0A 5A 10A	Telemetry/E-load *(ISCALE updated to 20 decimal (0x14))*
Vac(droop)	21.2mV 25mV	Pass	5A to 10A	C1418 Sense
Vac(overshoot)	35mV	Pass	10A to 5A	Sense

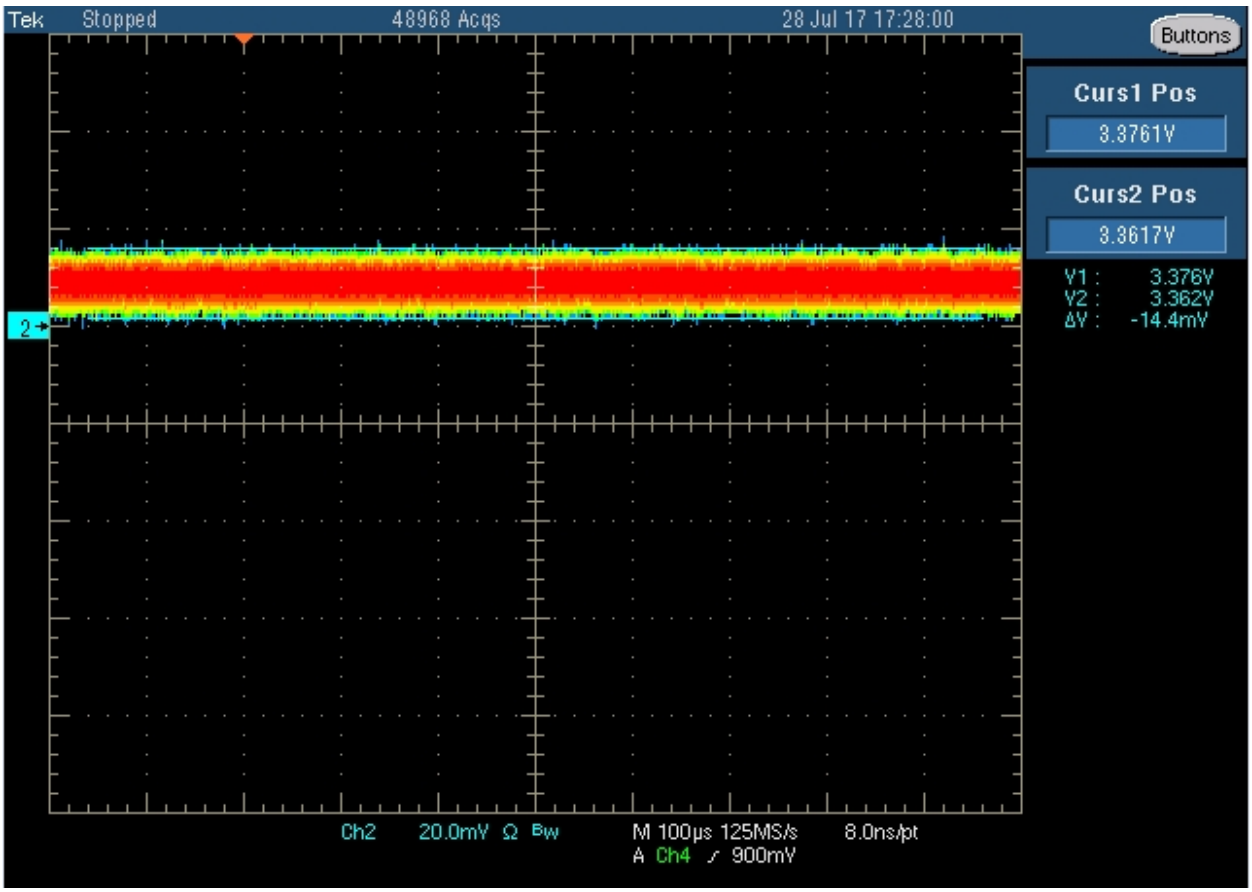

Figure 16 - UTIL_3V3 DC Ripple, 10A, C1418

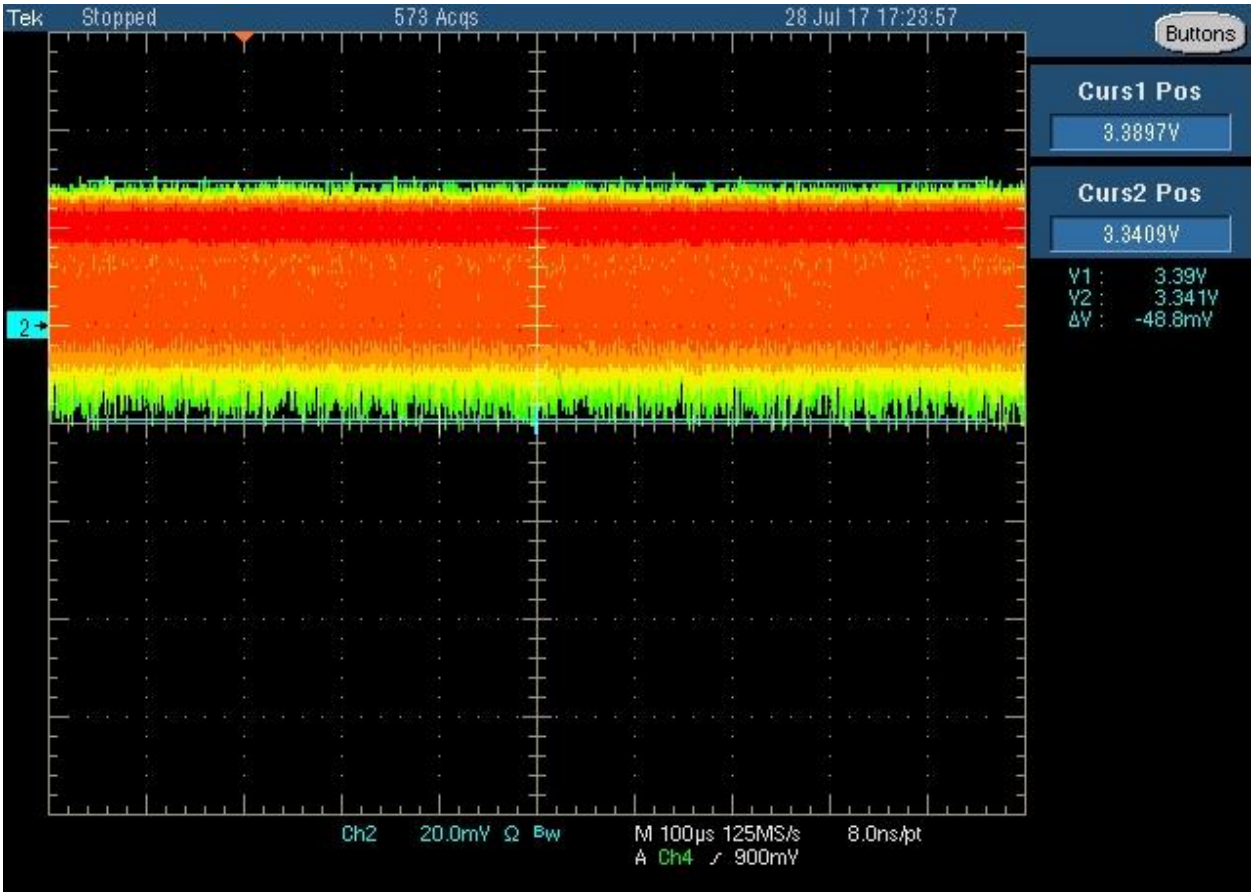

Figure 17 - UTIL_3V3 DC Ripple, 10A, sense

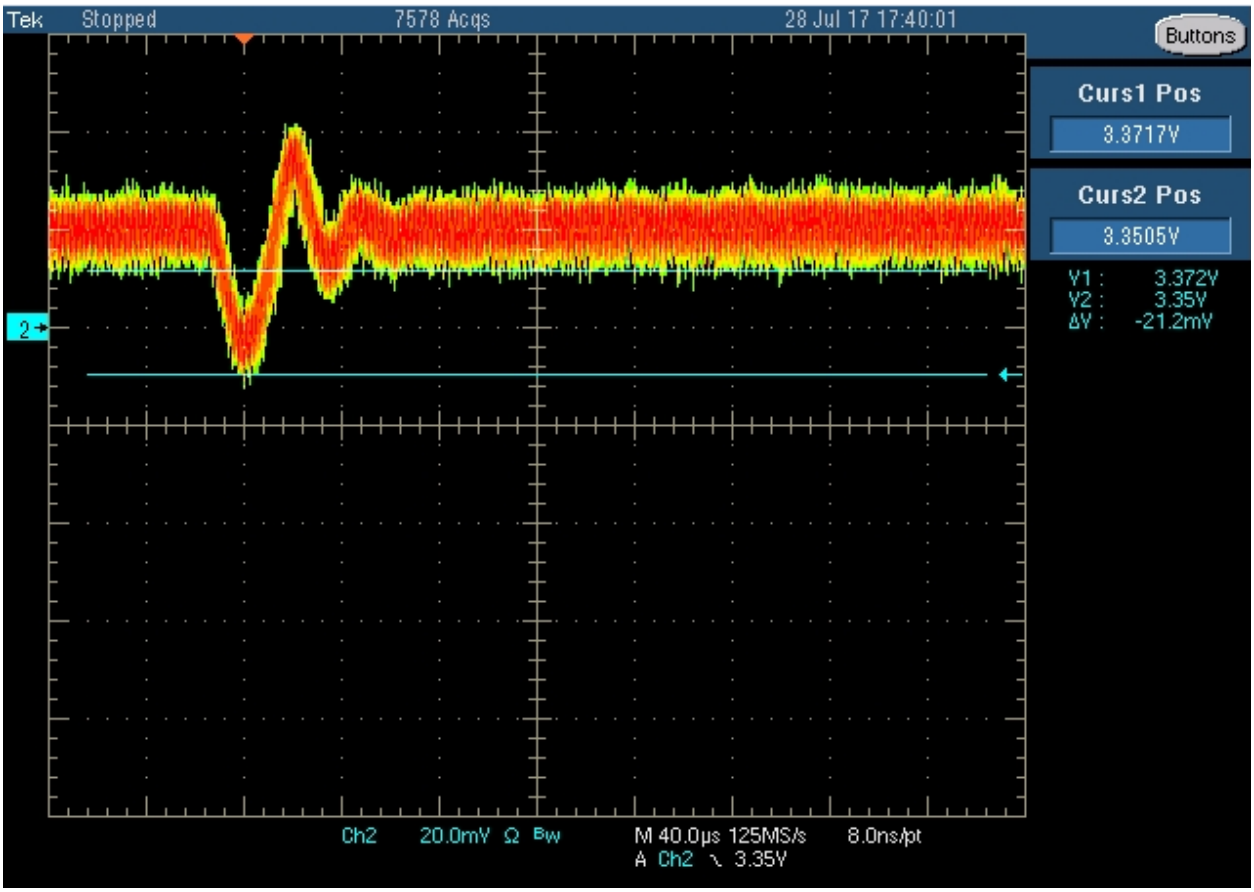

Figure 18 - UTIL_3V3 ac ripple load, C1418

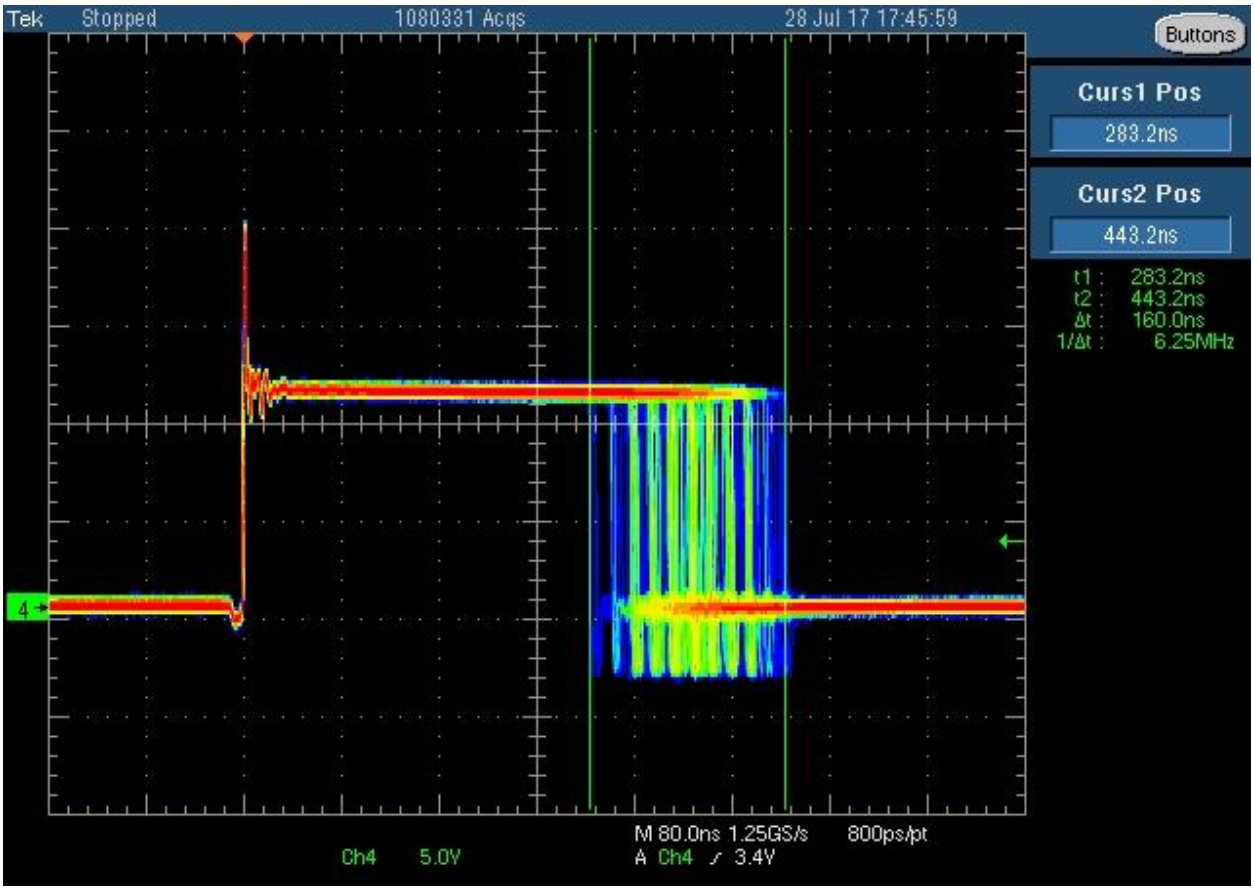

Figure 19 - UTIL_3V3 Jitter, 10A

UTIL_1V13

Vin, 12V
Vout, 1.13V
Iout(pk), 1A
Istep, 0.5A
Iramp, 0.5A/us

Vout Measurement Location, J163
Load Test Location, J163
SW Node Measurement Location, L78

Jitter = 39ns (1A load)

Design Modifications

- **Add 10 ohm BODE 0603 resistor with test points for soldering**

Table 9 – UTIL_1V13 Results

Measurement	Result	Pass/Fail	Test Condition	Notes
Vout	1.13V (1.133V) 1.129V (1.129V)	Pass	0A 1A	DMM (GUI)
DC Ripple	21.6mV 20.8mV	Pass	0A 1A	
Isense	0A 0.97A	Pass	0A 1A	Telemetry/E-load
Vac(droop)	23.6mV	Pass	0.5A to 1A	
Vac(overshoot)	24.8mV	Pass	1A to 0.5A	

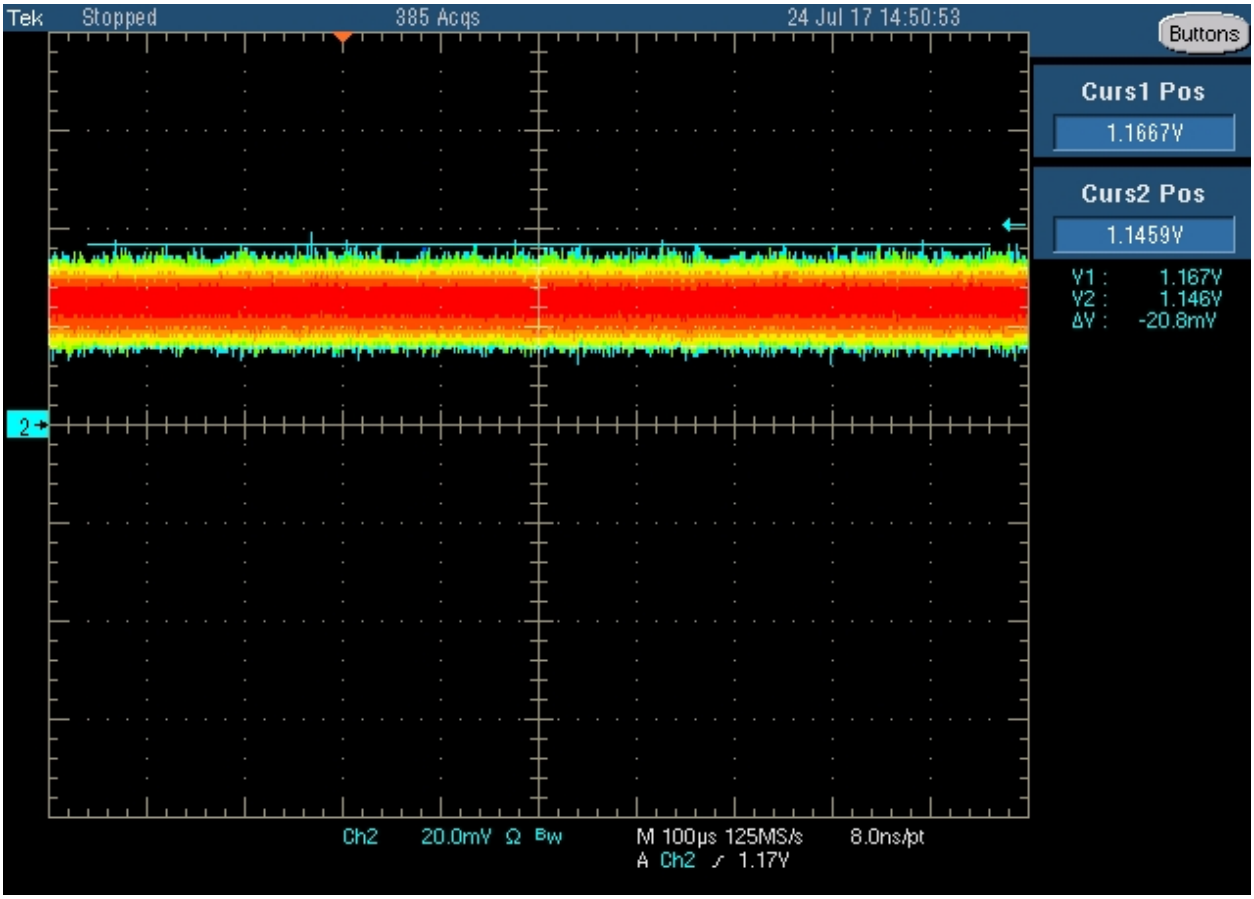

Figure 20 - UTIL_1V13 DC Ripple, 1A

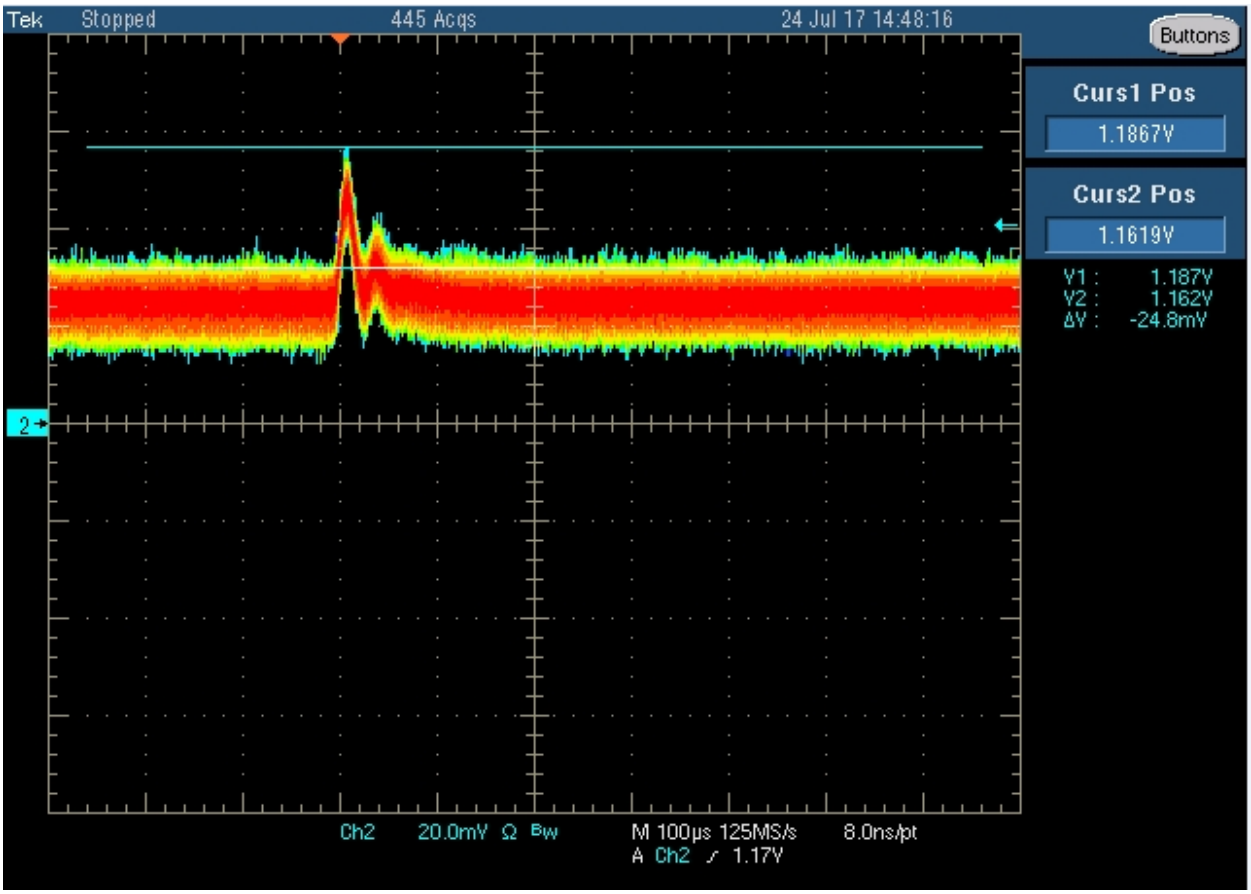

Figure 21 - UTIL_1V13 ac ripple release

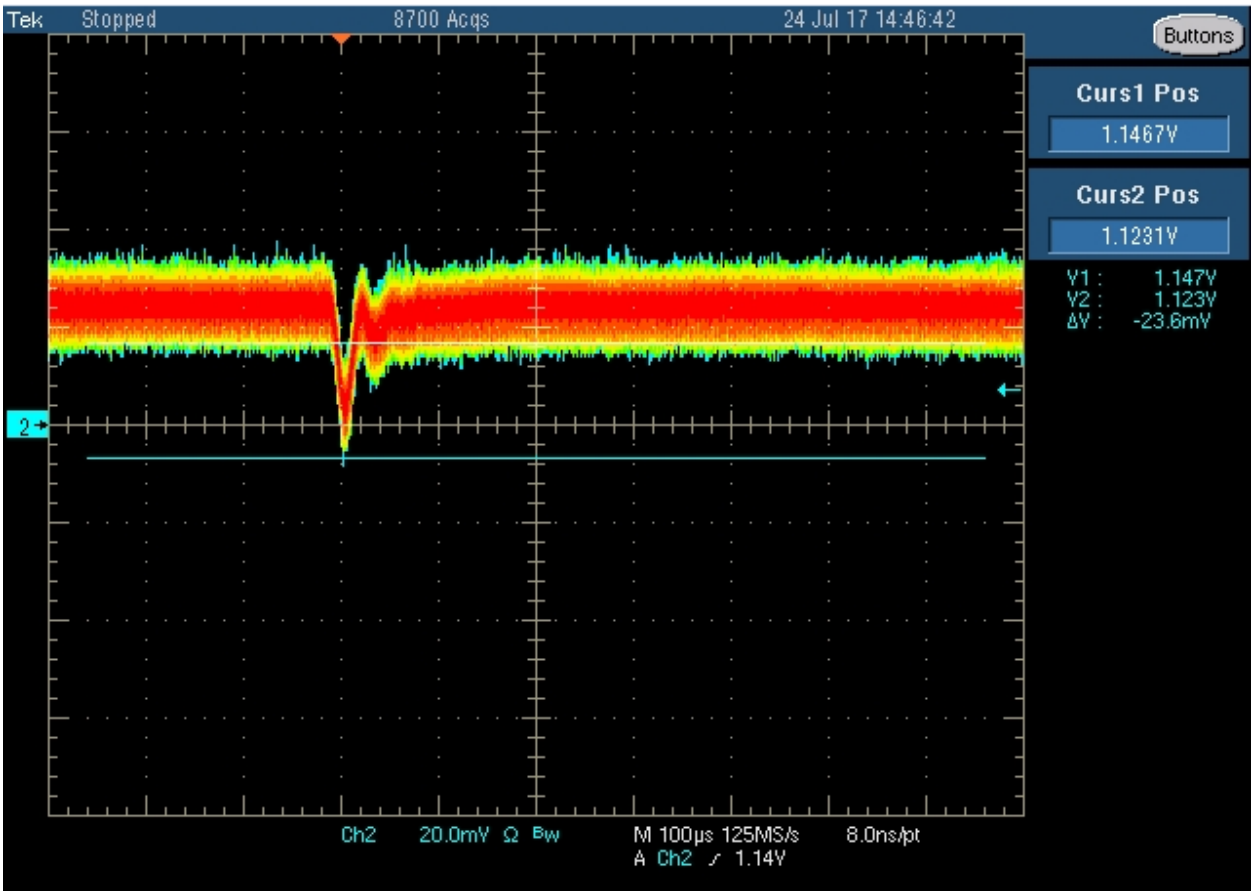

Figure 22 - UTIL_1V13 ac ripple load

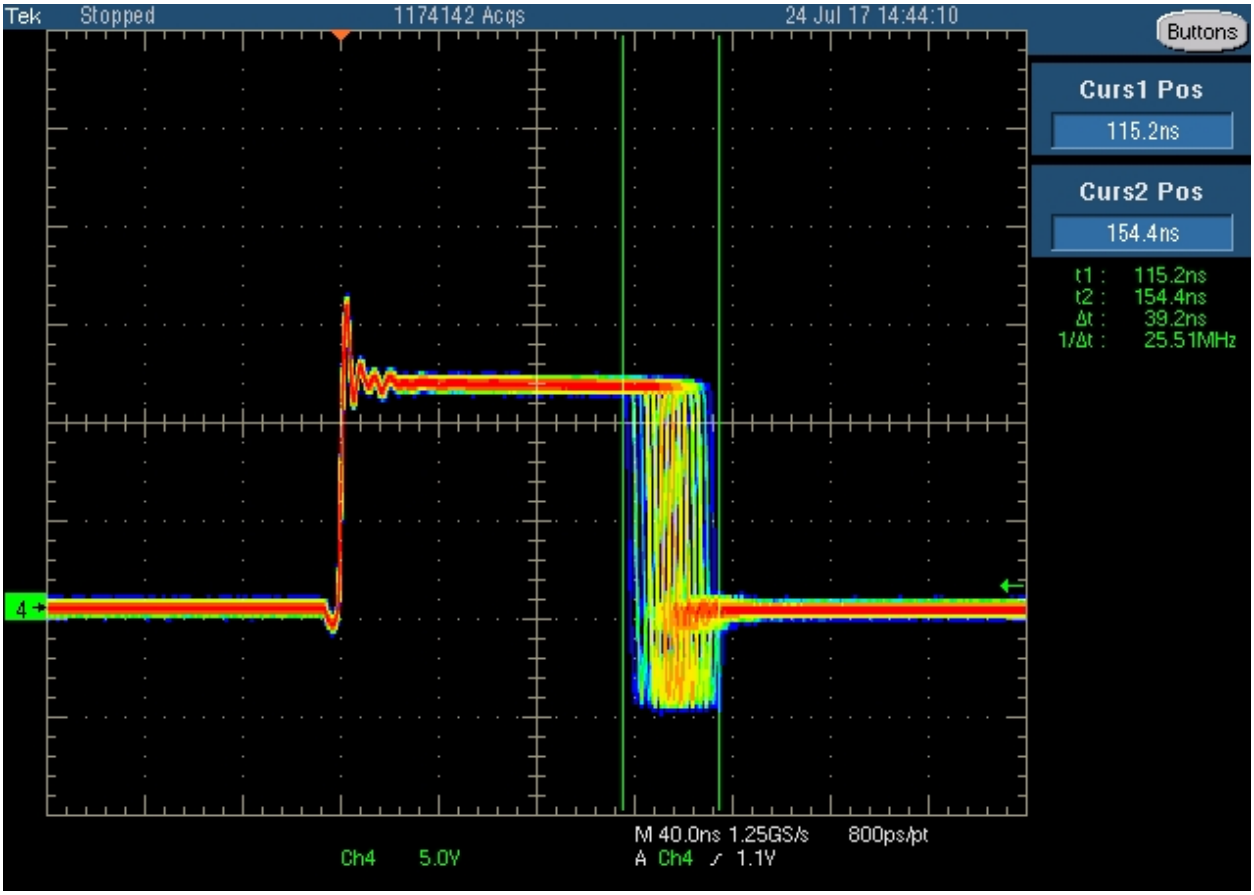

Figure 23 - UTIL_1V13 Jitter, 1A

UTIL_5V0

Vin = 12V
Vout = 5.0V
Iout(pk) = 2.1A
Istep, 1A
Iramp, 0.5A/us

Vout Measurement Location, J171
Load Test Location, J171
SW Node Measurement Location, L78

Jitter = 158ns (2.1A load)

Design Recommendations:

- **ADD 1x 100uF or 2x 47uF or 3x 22uF caps at VR output(reduce jitter/bandwidth for lower Vdroop)**
- **Add 10 ohm BODE 0603 resistor with test points for soldering**
- **Remove skinny traces to loads tapped from this rail**

Rev B Tuning (for IFX)

- Slightly reduce PI strength after increasing Cout

Table 10 – UTIL_5V0 Results

Measurement	Result	Pass/Fail	Test Condition	Notes
Vout	5.04V	Pass	0A	DMM
DC Ripple	23.6mV 23.6mV	Pass	0A 2.1A	Coax Probe ac coupled
Isense	0A 2.06A	Pass	0A 2.1A	Telemetry/E-load
Vac(droop)	40mV	Pass	1.1A to 2.1A	
Vac(overshoot)	42mV	Pass	2.1A to 1.1A	

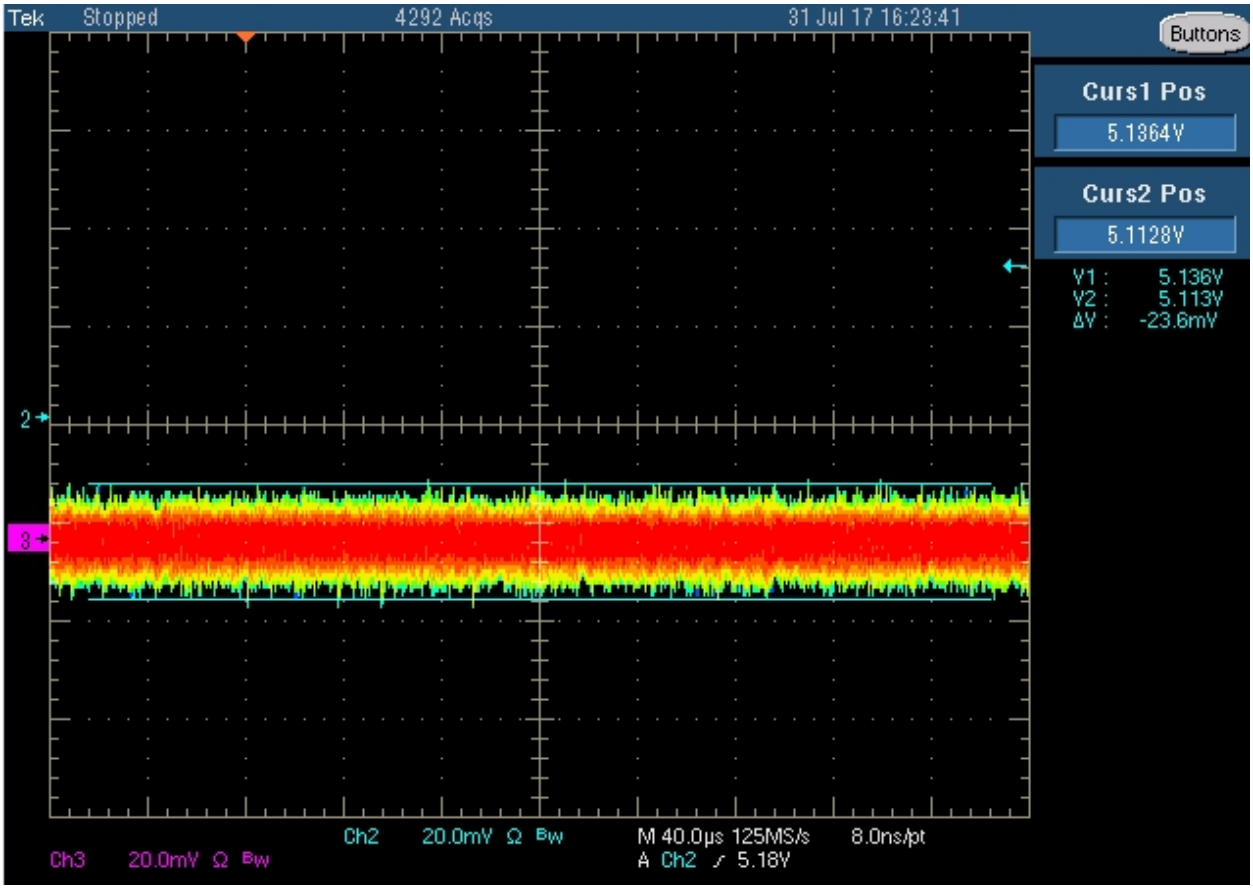

Figure 24 - UTIL_5V0 DC Ripple, 2.1A

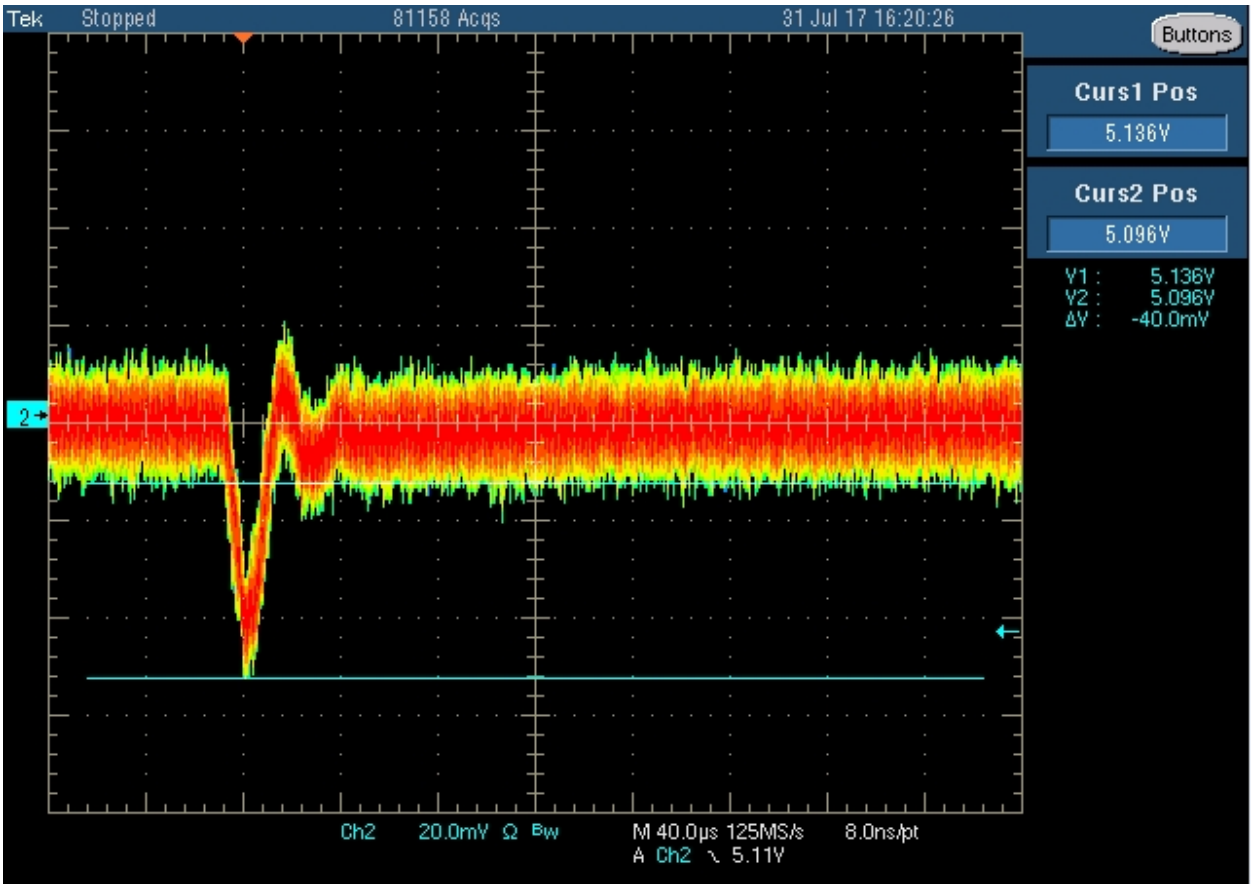

Figure 25 - UTIL_5V0 ac ripple load

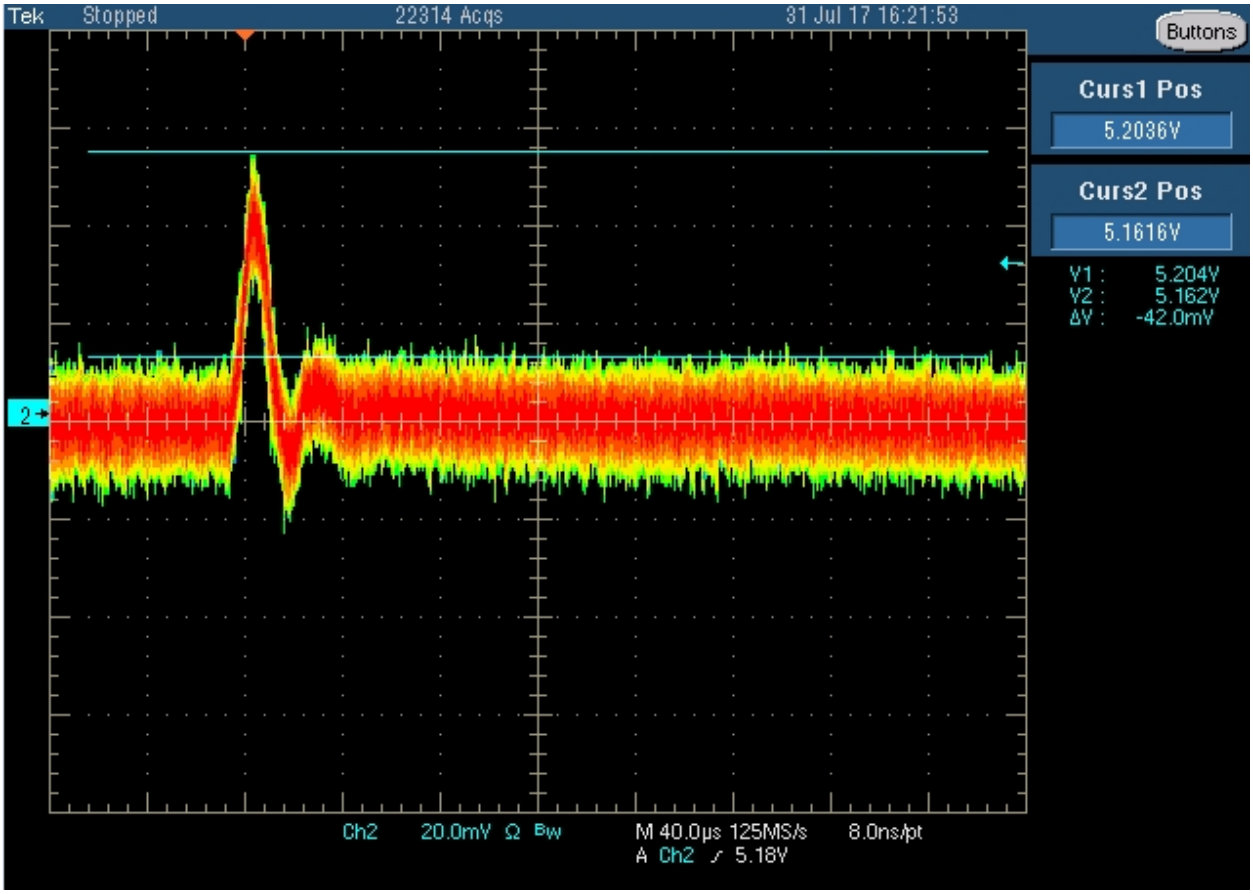

Figure 26 - UTIL_5V0 ac ripple unload

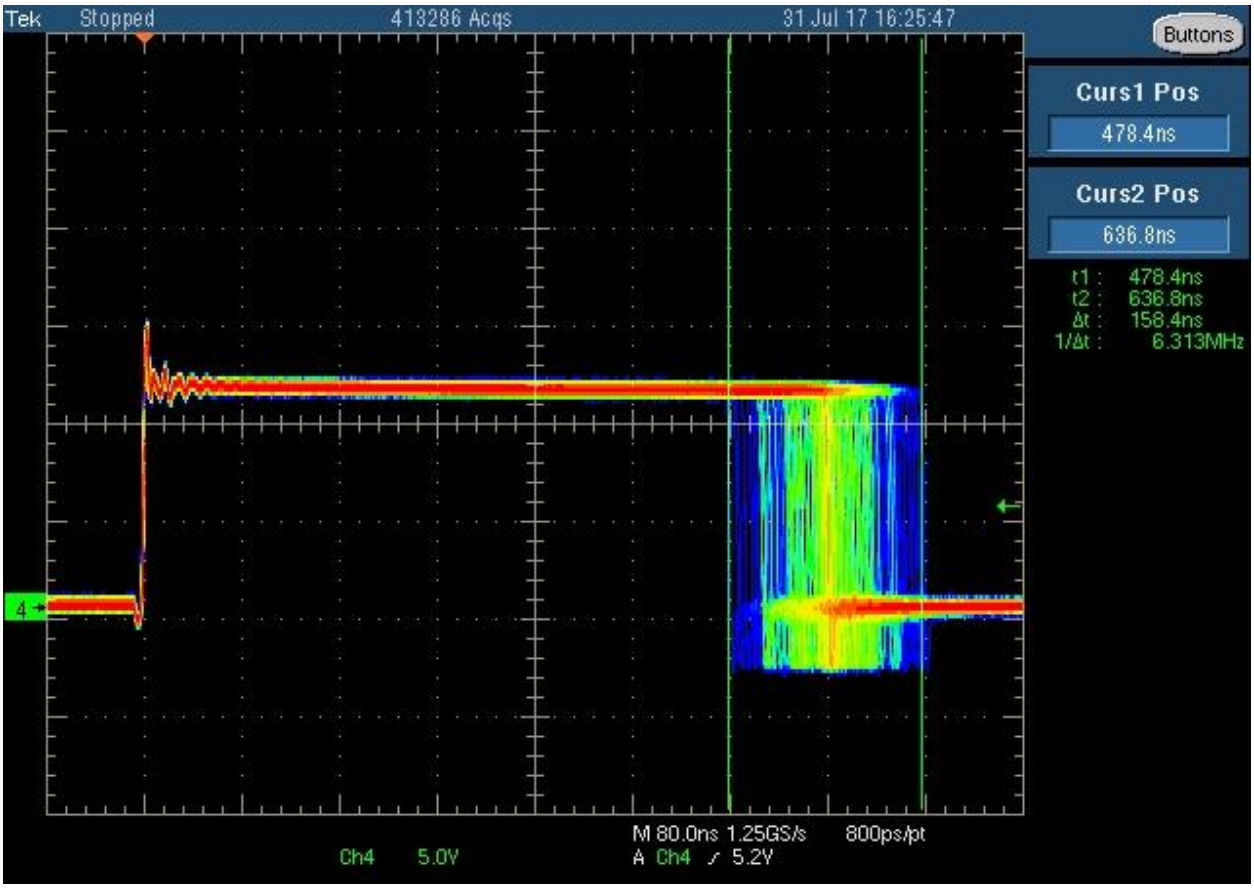

Figure 27 - UTIL_5V0 Jitter, 2.1A

FMC_VADJ

Vin, 12V
Vout, 1.8V
Iout(pk), 3A
Istep, 1.5A
Iramp, 0.5A/us

Vout Measurement Location, J172
Load Test Location, J172
SW Node Measurement Location, L80

Jitter = 111ns (3A load)

Table 11 – FMC_VADJ Results

Measurement	Result	Pass/Fail	Test Condition	Notes
Vout	1.179 1.795V (1.797V)	Pass	0A 3A	DMM (GUI)
DC Ripple	19.6mV 26.8mV	Pass	0A 3A	
Isense	0A 2.94A	Pass	0A 3A	Telemetry/E-load
Vac(droop)	28mV	Pass	1.5A to 3A	
Vac(overshoot)	20.8mV	Pass	3A to 1.5A	

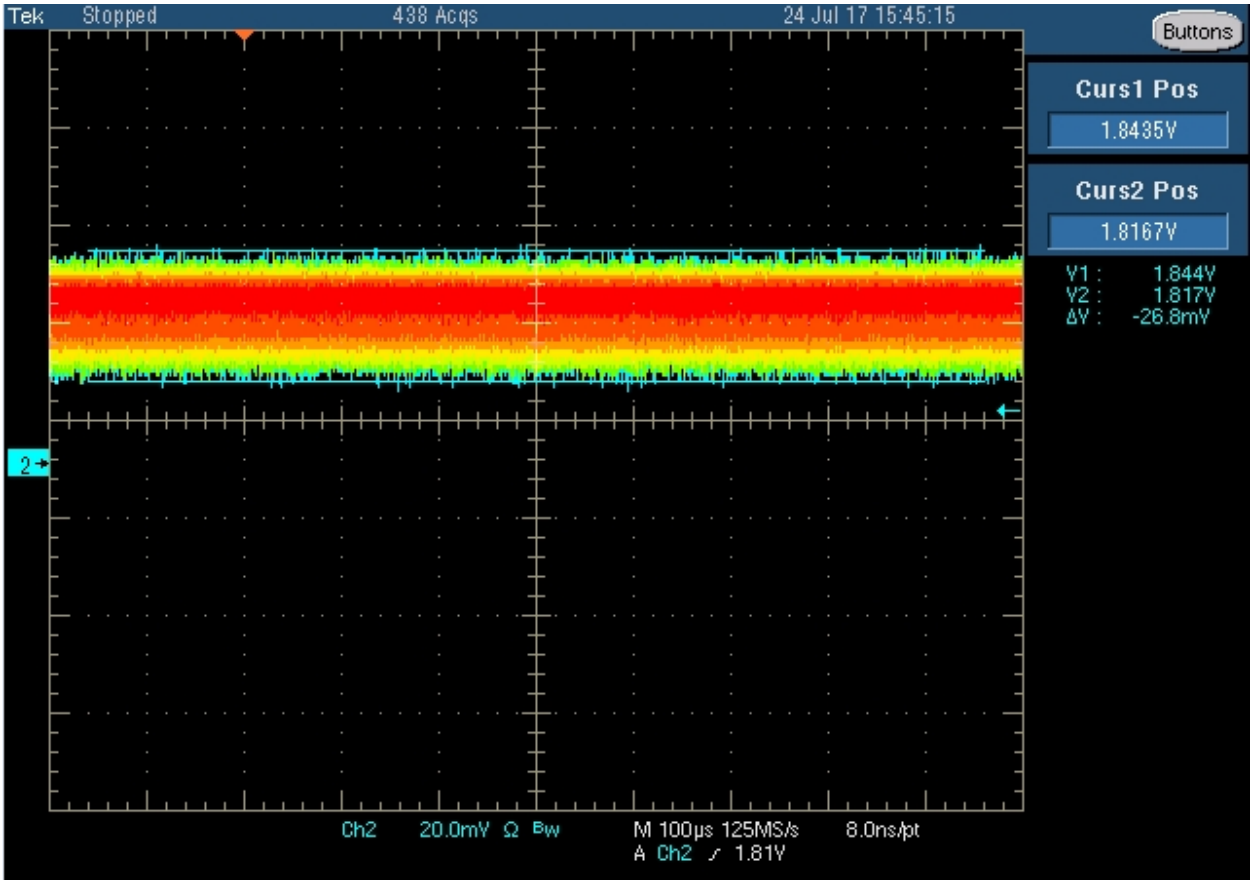

Figure 28 - FMC_VADJ DC Ripple, 3A

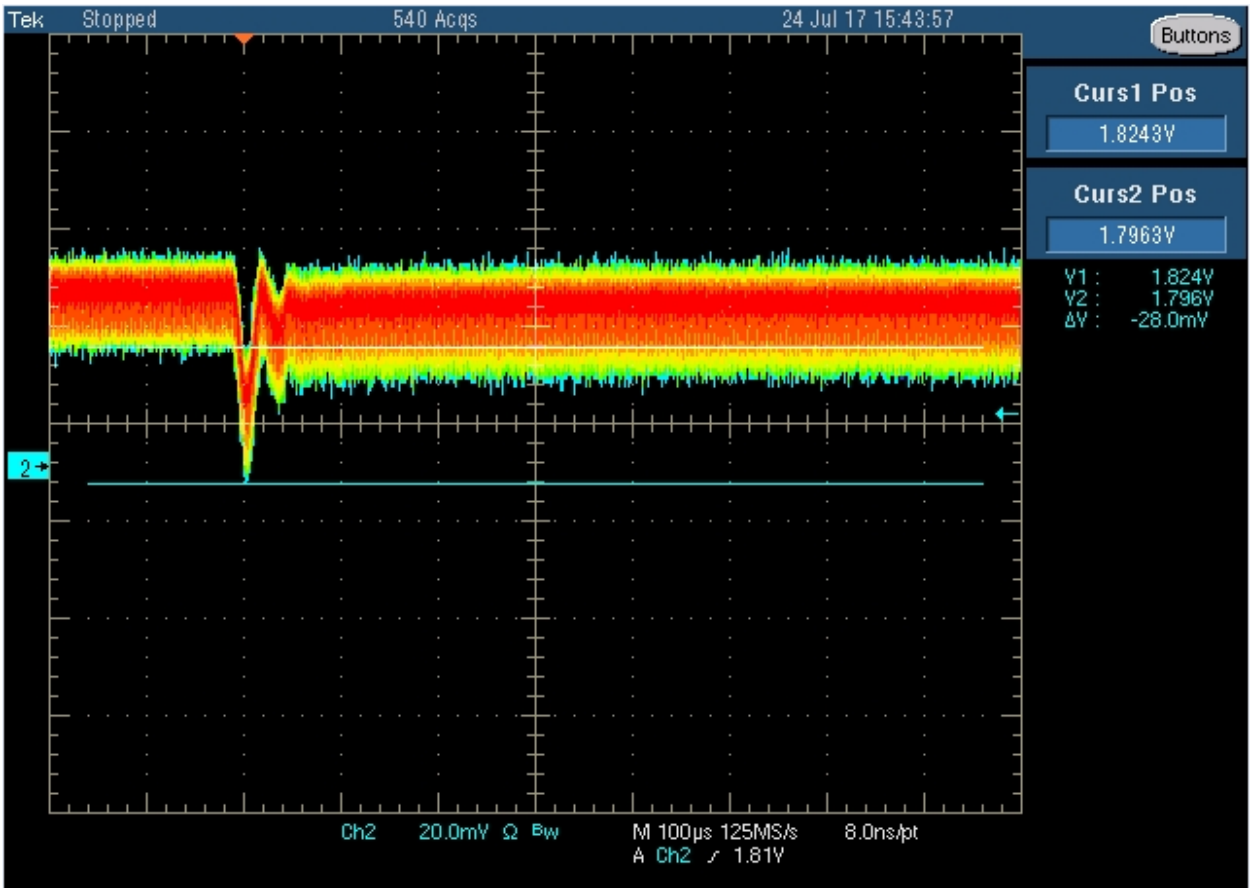

Figure 29 - FMC_VADJ ac ripple load

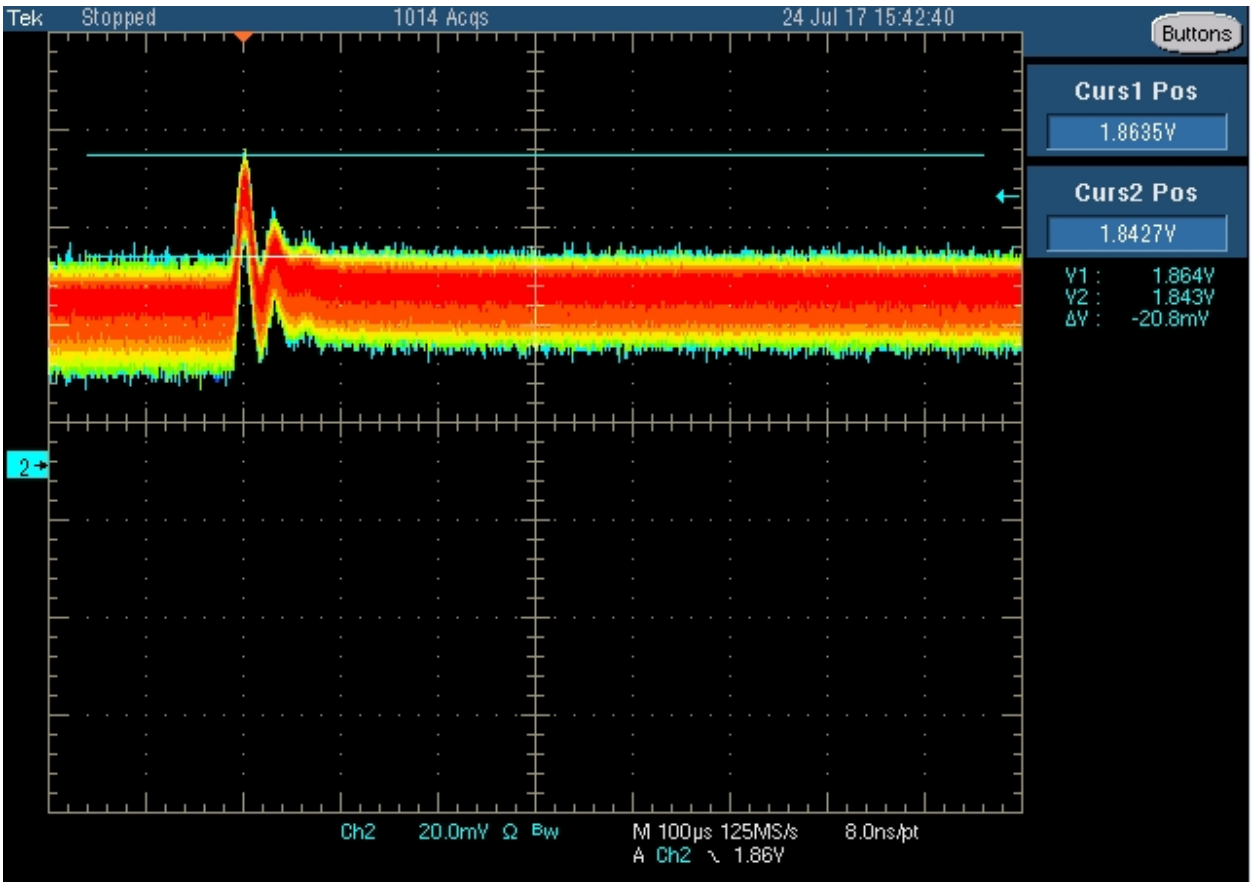

Figure 30 - FMC_VADJ ac ripple release

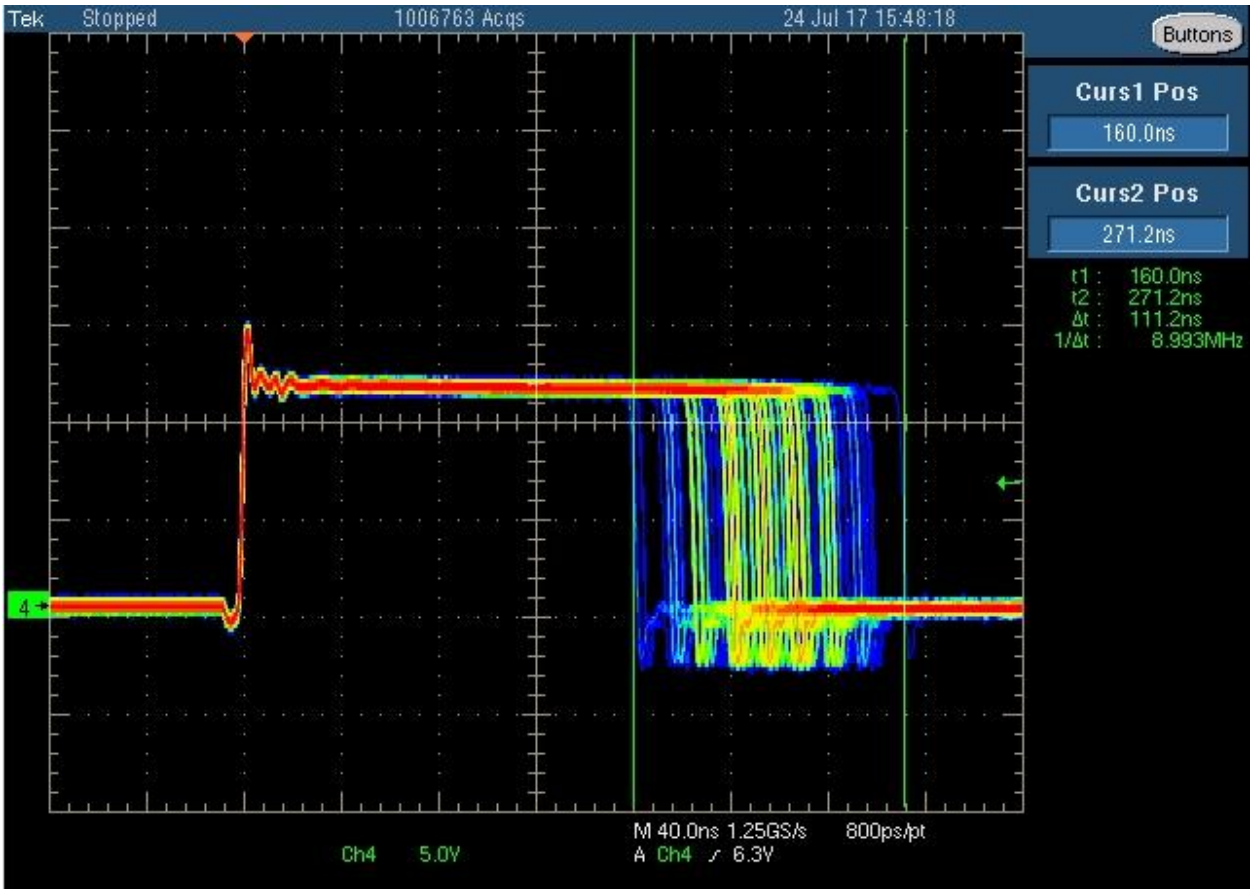

Figure 31 - FMC_VADJ Jitter, 3A

MGTRAVCC

Vin, 2.5V
Vout, 0.85V
Iout(pk), 0.5A
Istep, 0.25A
Iramp, 1A/us

Vout Measurement Location, J40
Load Test Location, J40

Table 12 – MGTRAVCC Results

Measurement	Result	Pass/Fail	Test Condition	Notes
Vout	0.847V (0.852V)	Pass	0A	DMM (GUI)
DC Ripple	6.8mV 6.8mV	Pass	0A 0.5A	Coax Probe ac coupled
Isense	0A 0.5A	Pass	0A 0.5A	Telemetry/E-load
Vac(droop)	3.6mV	Pass	0.25A to 0.5A	
Vac(overshoot)	4.0mV	Pass	0.5A to 0.25A	

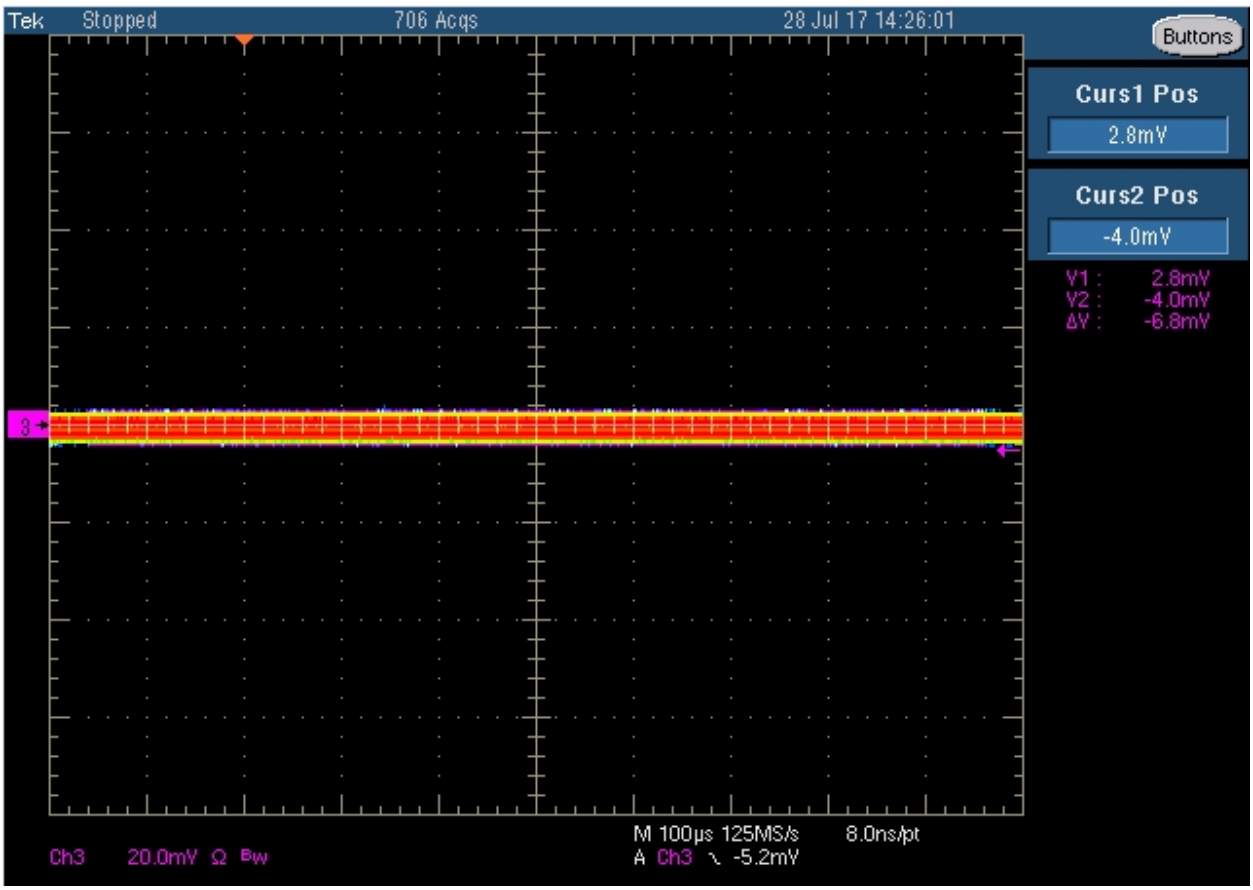

Figure 32 - MGTRAVCC DC Ripple, 0.5A

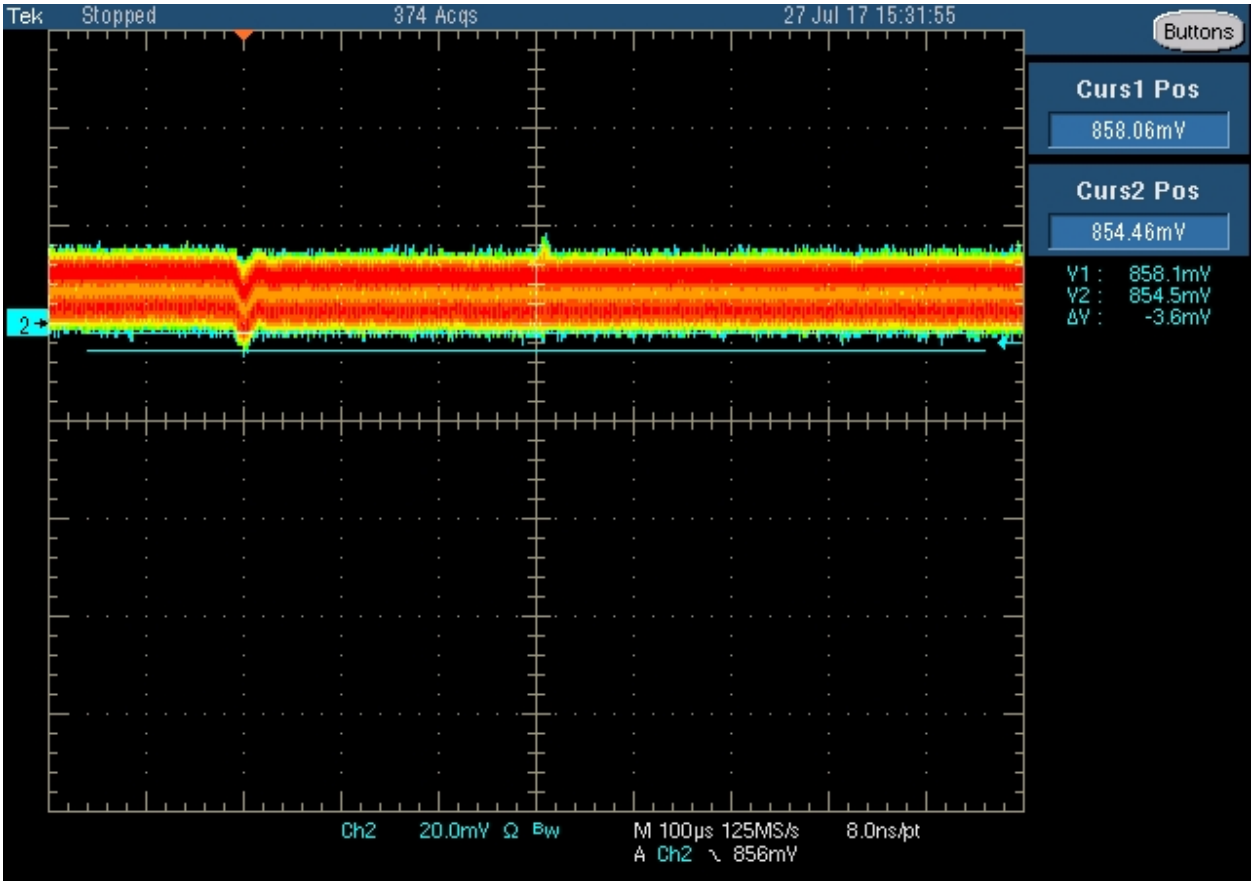

Figure 33 - MGTRAVCC ac ripple load

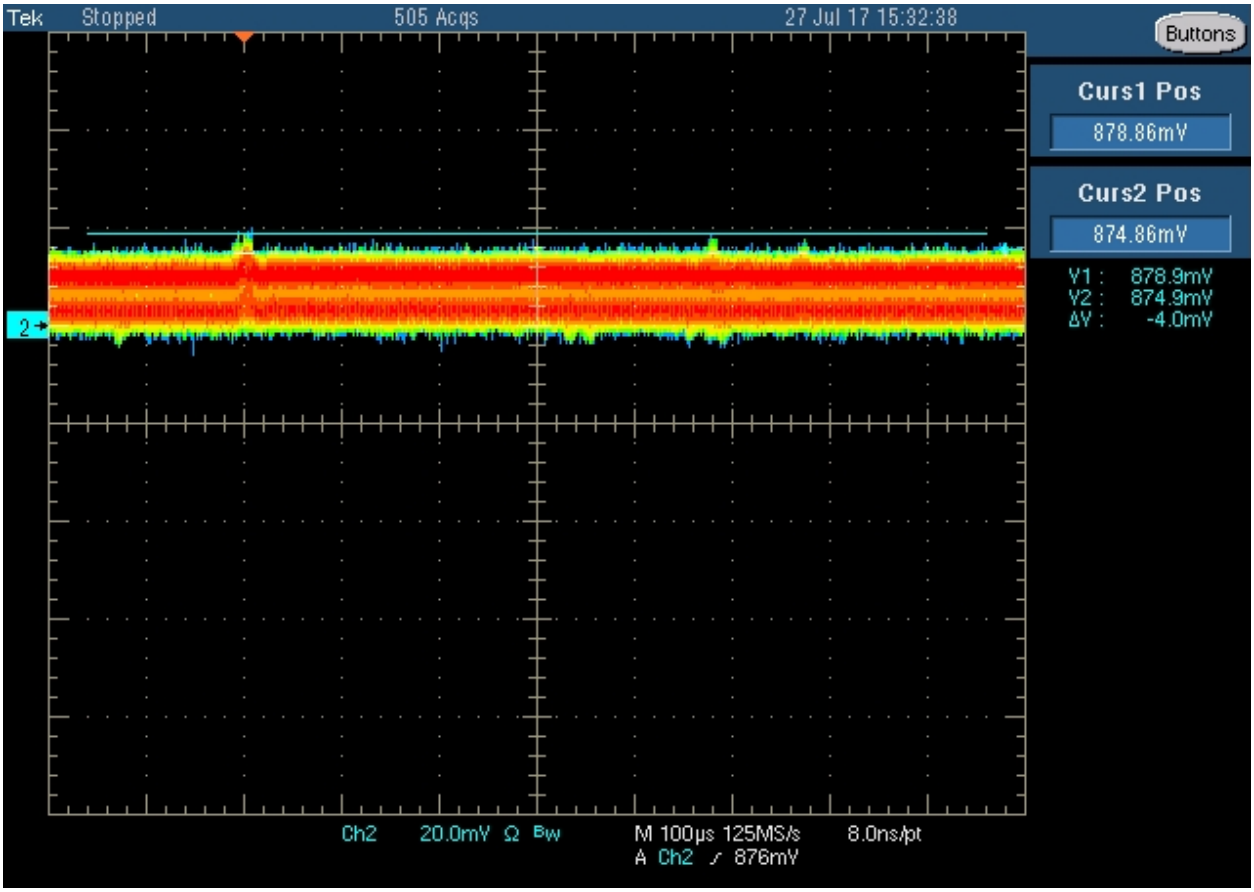

Figure 34 - MGTRAVCC ac ripple release

VCC3V3

Vin, 12V
Vout, 3.3V
Iout(pk), 0.5A
Istep, 0.25A
Iramp, 0.5A/us

Vout Measurement Location, J170
Load Test Location, J170
SW Node Measurement Location, L74

Table 13 – VCC3V3 Results

Measurement	Result	Pass/Fail	Test Condition	Notes
Vout	3.321V 3.314V	Pass	0A 0.5A	DMM
DC Ripple	18mV 17.6mV	Pass	0A 0.5A	
Isense	NA			
Vac(droop)	11.2mV	Pass	0.25A to 0.5A	
Vac(overshoot)	5.6mV	Pass	0.5A to 0.25A	

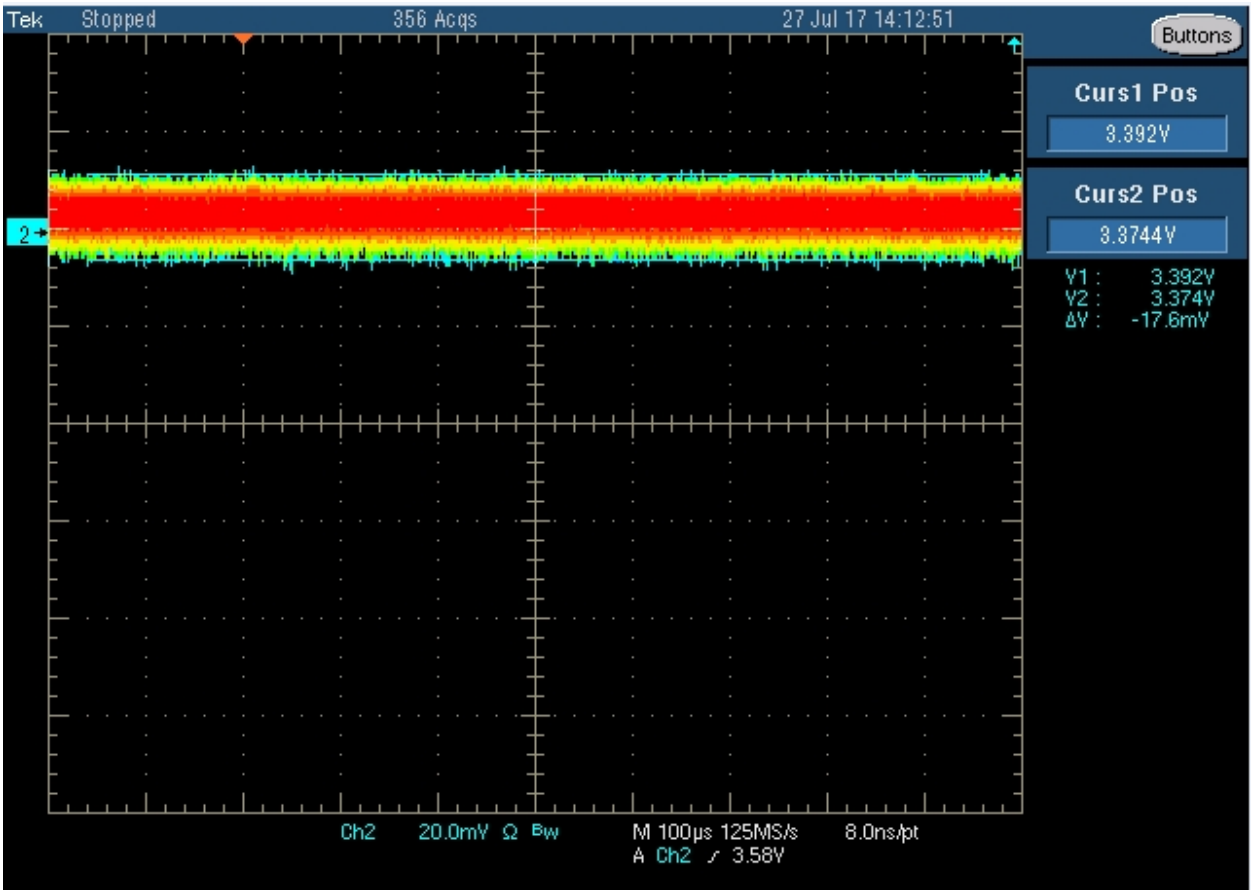

Figure 35 - VCC3V3 DC Ripple, 0.5A

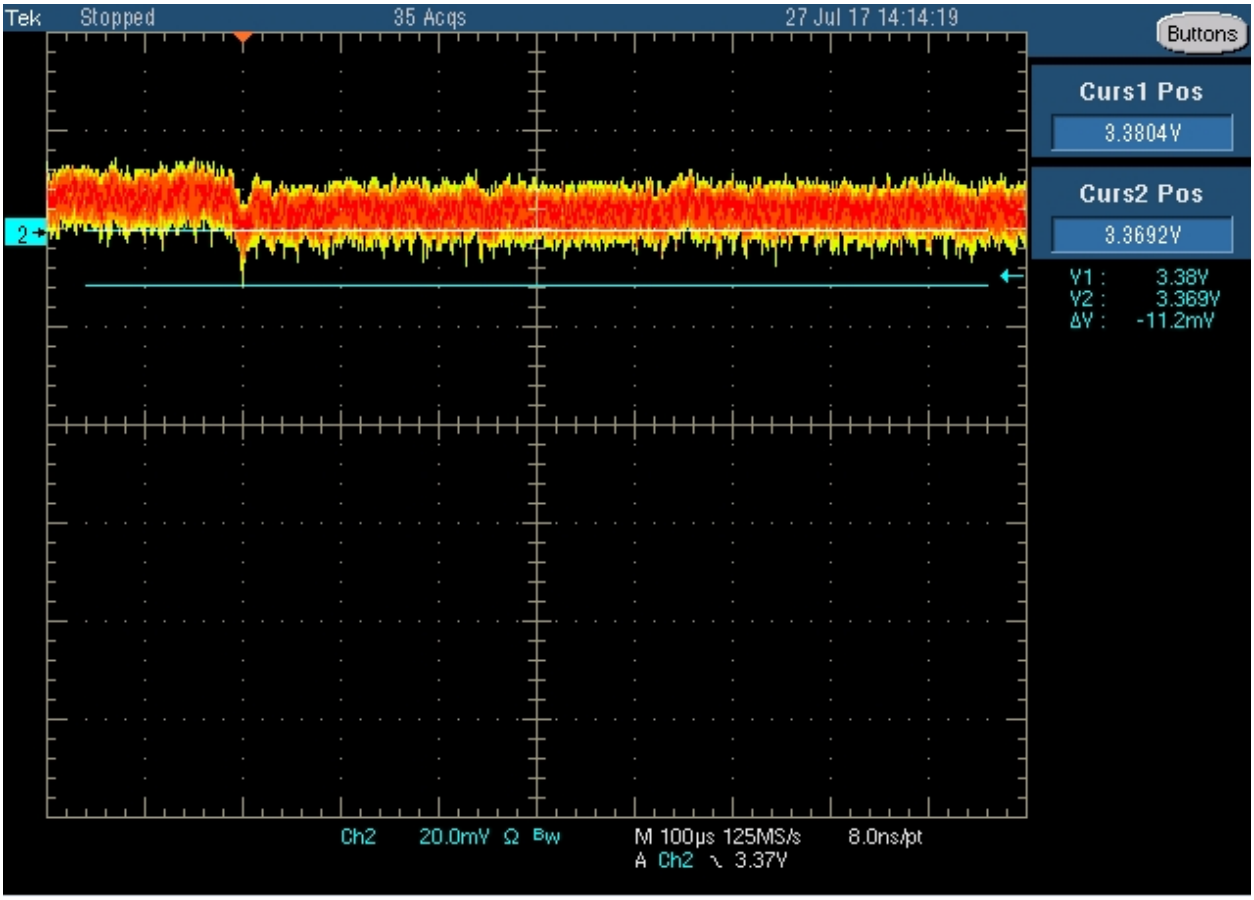

Figure 36 - VCC3V3 ac ripple load

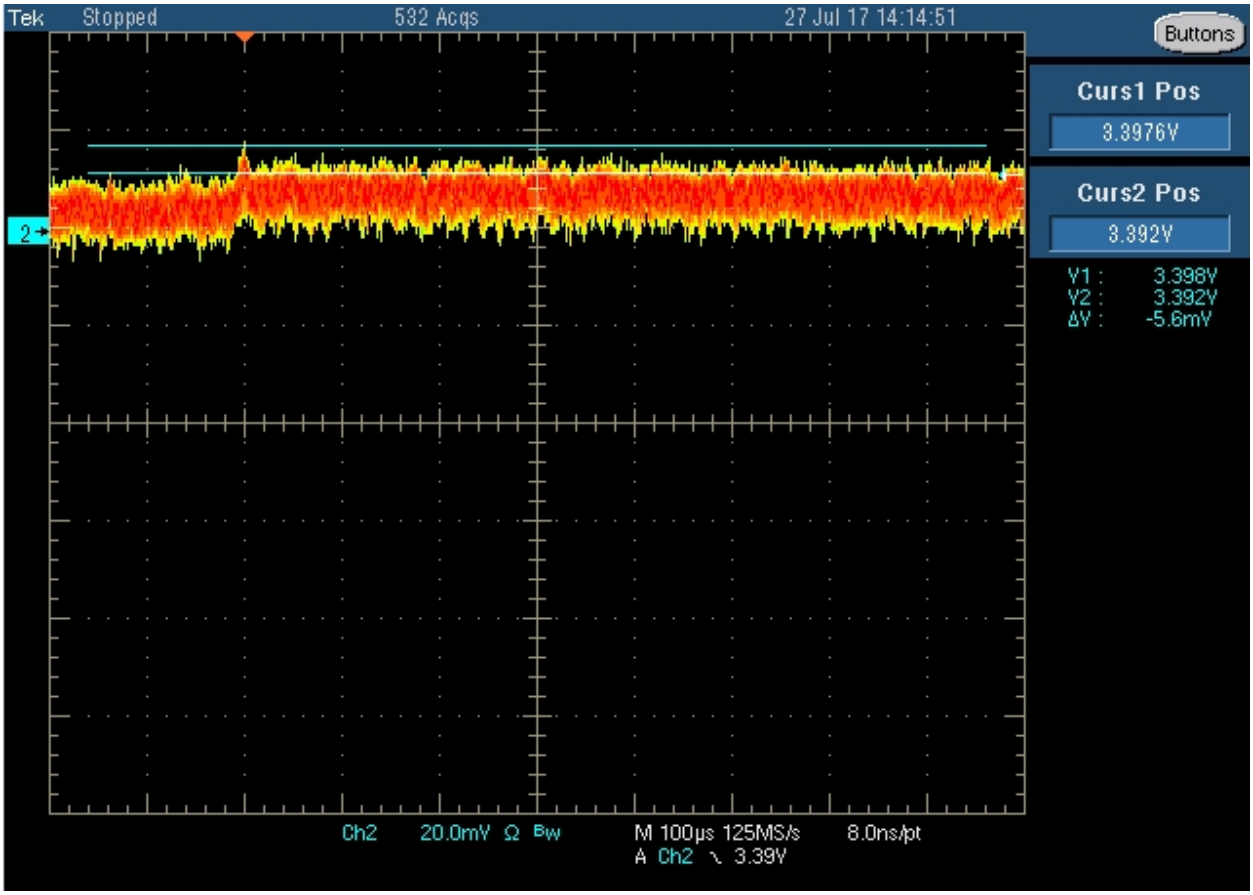

Figure 37 - VCC3V3 ac ripple release

MGT1V2

Vin, 12V
Vout, 1.2V
Iout(pk), 0.5A
Istep, 0.25A
Iramp, 1A/us

Vout Measurement Location, J166
Load Test Location, J166
SW Node Measurement Location, L81

Jitter = 16ns (0.5A)

Table 14 – MGT1V2 Results

Measurement	Result	Pass/Fail	Test Condition	Notes
Vout	1.196V 1.196V	Pass	0A 0.5A	DMM
DC Ripple	8.8mV 10mV	Pass	0A 0.5A	Coax Probe ac coupled
Isense	N/A			
Vac(droop)	4.4mV	Pass	0.25A to 0.5A	
Vac(overshoot)	4.0mV	Pass	0.5A to 0.25A	

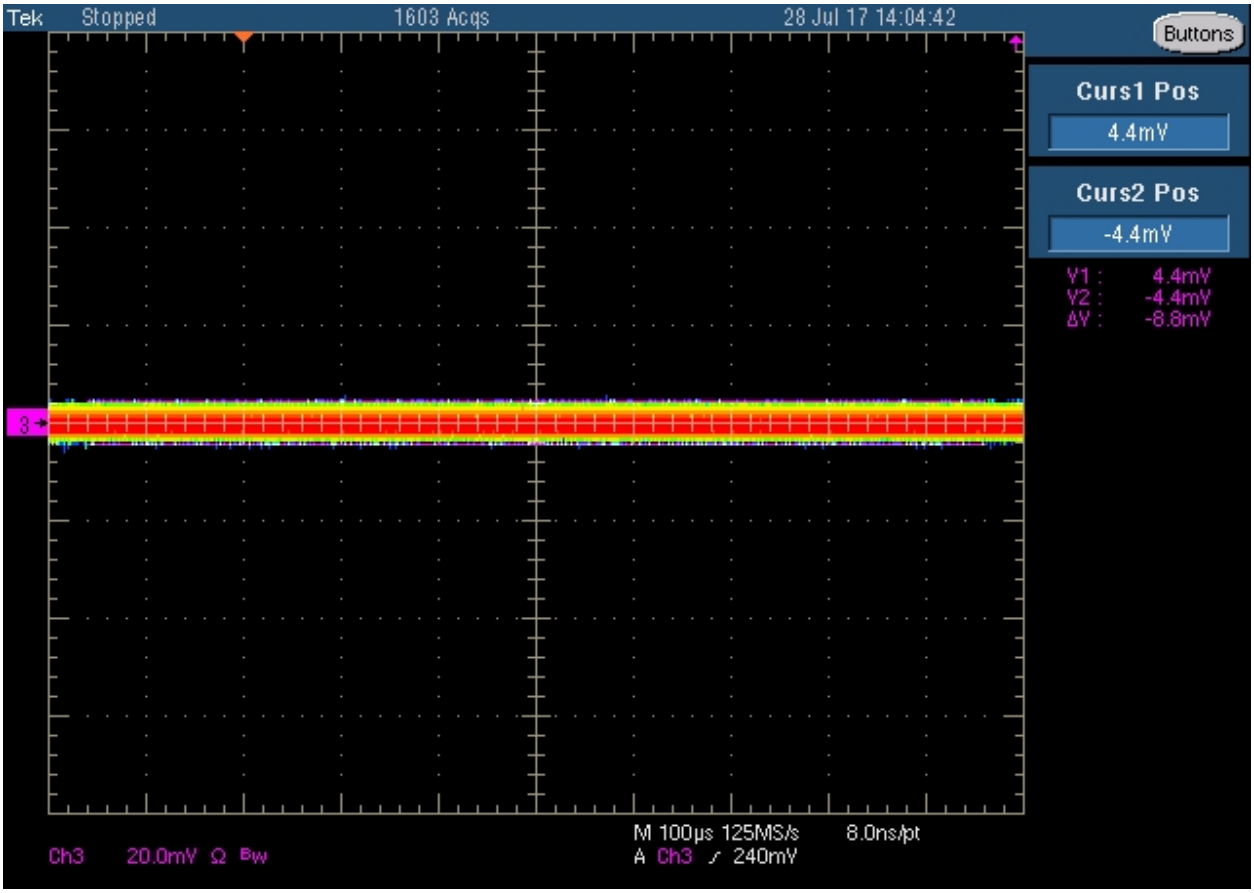

Figure 38 - MGT1V2 DC Ripple, 0A

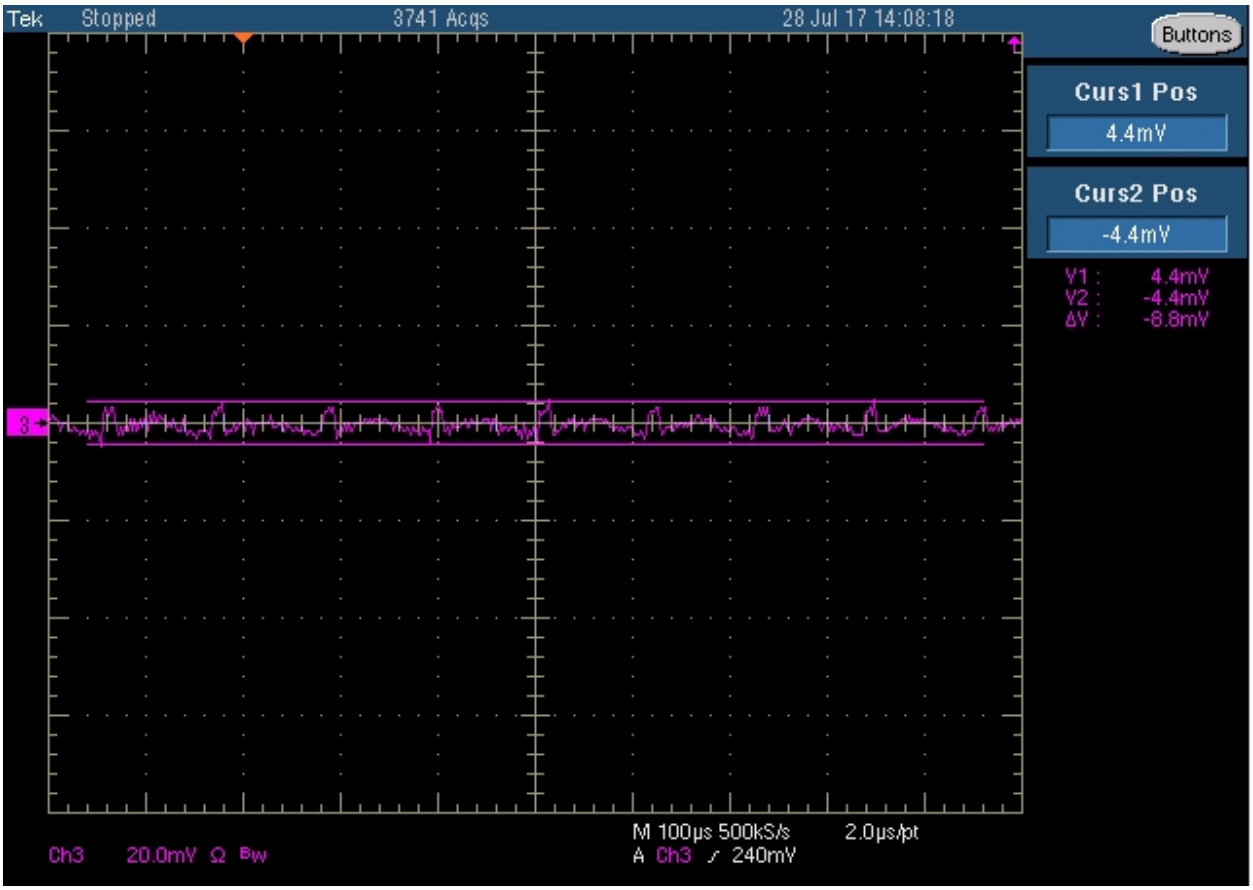

Figure 39 - MGT1V2 DC Ripple, 0.5A

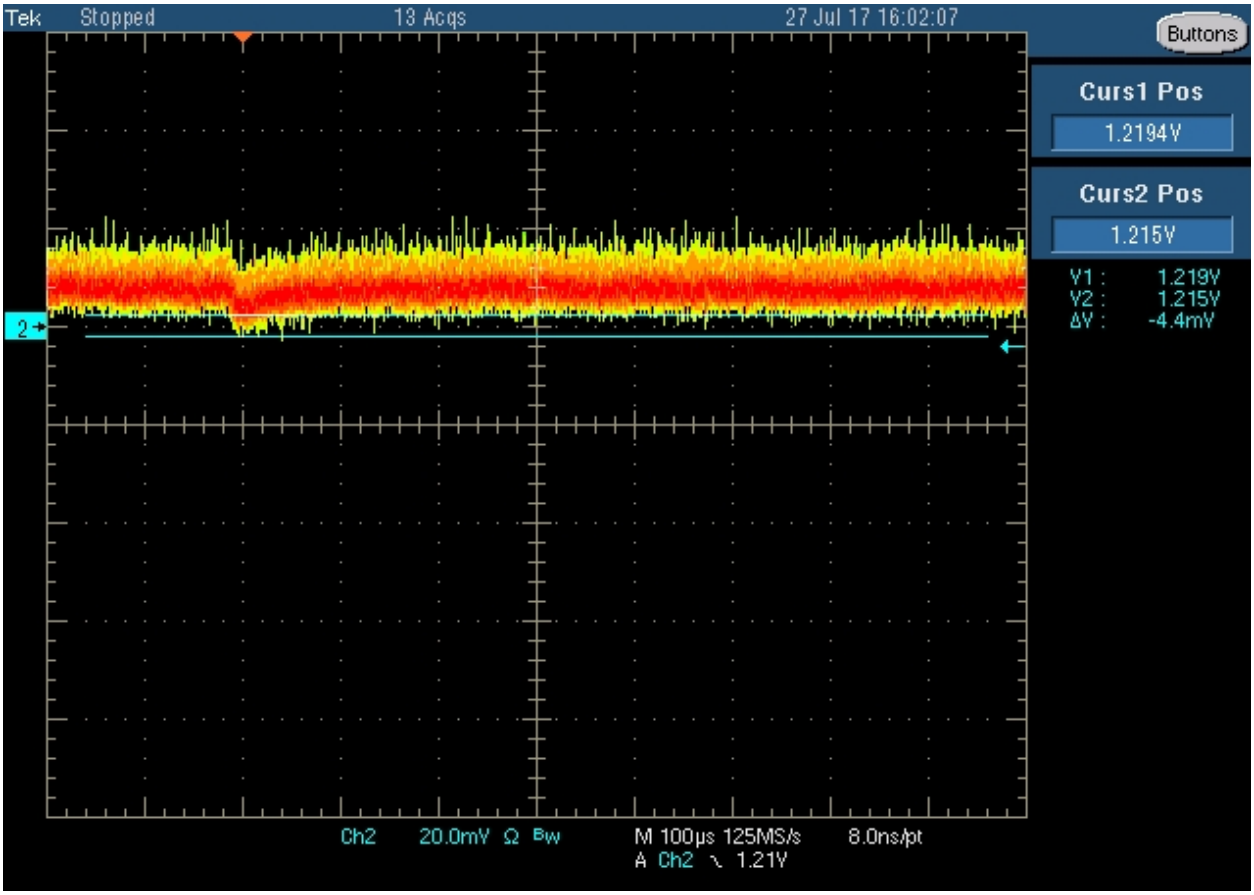

Figure 40 - MGT1V2 ac ripple load

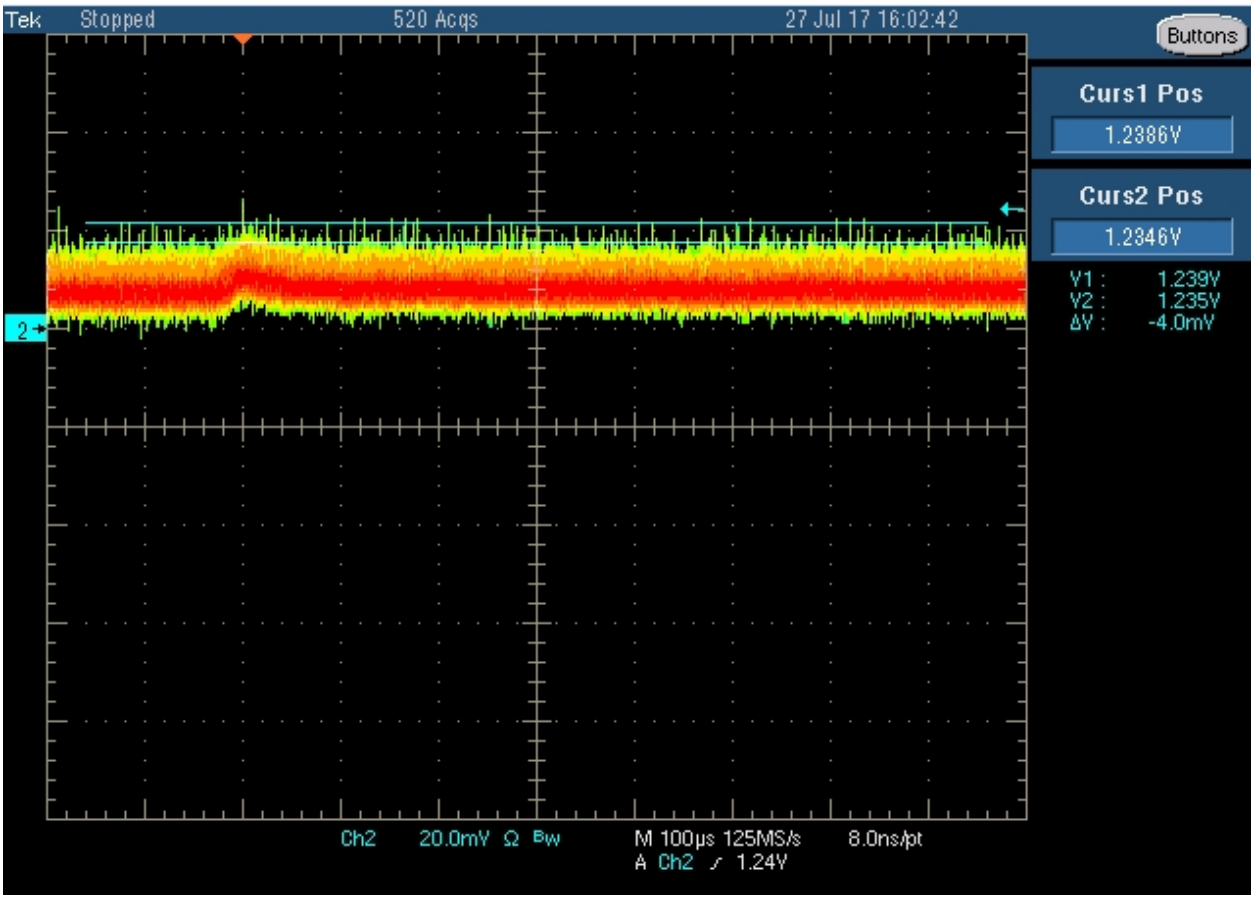

Figure 41 - MGT1V2 ac ripple release

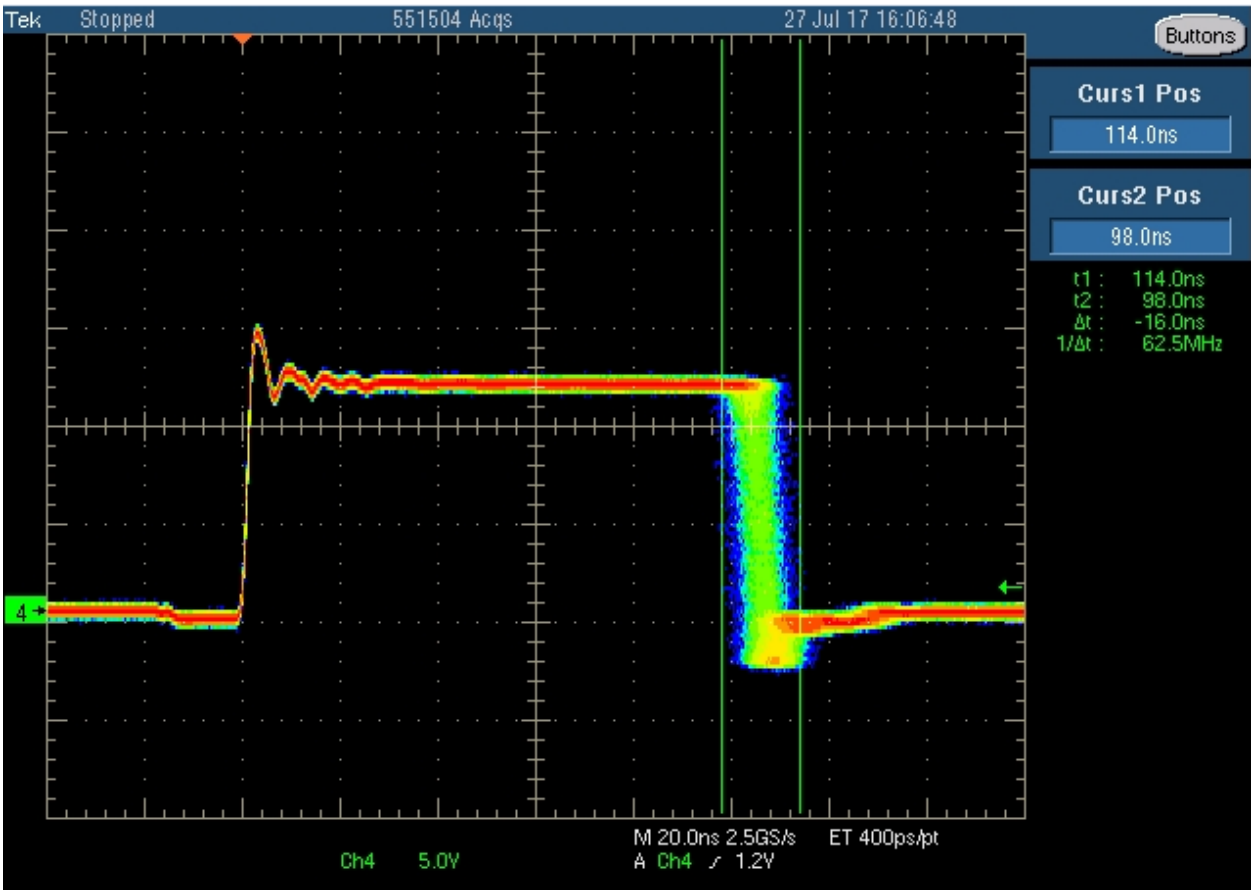

Figure 42 - MGT1V2 Jitter, 0.5A

MGT1V8

Vin, 2.5V
Vout, 1.8V
Iout(pk), 0.1A
Istep, 0.05A
Iramp, 1A/us

Vout Measurement Location, J41
Load Test Location, J41

BOARD HAS INCORRECT SKU OF LDO PN – IN DROPOUT MODE

Table 15 – MGT1V8 Results

Measurement	Result	Pass/Fail	Test Condition	Notes
Vout				
DC Ripple				
Isense	N/A			
Vac(droop)				
Vac(overshoot)				

UTIL_2V5

Vin, 12V
Vout, 2.5V
Iout(pk), 2A
Istep, 1A
Iramp, 0.5A/us

Vout Measurement Location, J169
Load Test Location, J169
SW Node Measurement Location, L73

Table 16 – UTIL_2V5 Results

Measurement	Result	Pass/Fail	Test Condition	Notes
Vout	2.51V 2.50V 2.49V	Pass	0A 1A 2A	DMM
DC Ripple	16.8mV 16.8mV	Pass	0A 2A	
Isense	N/A			
Vac(droop)	16.4mV	Pass	1A to 2A	
Vac(overshoot)	21.2mV	Pass	2A to 1A	

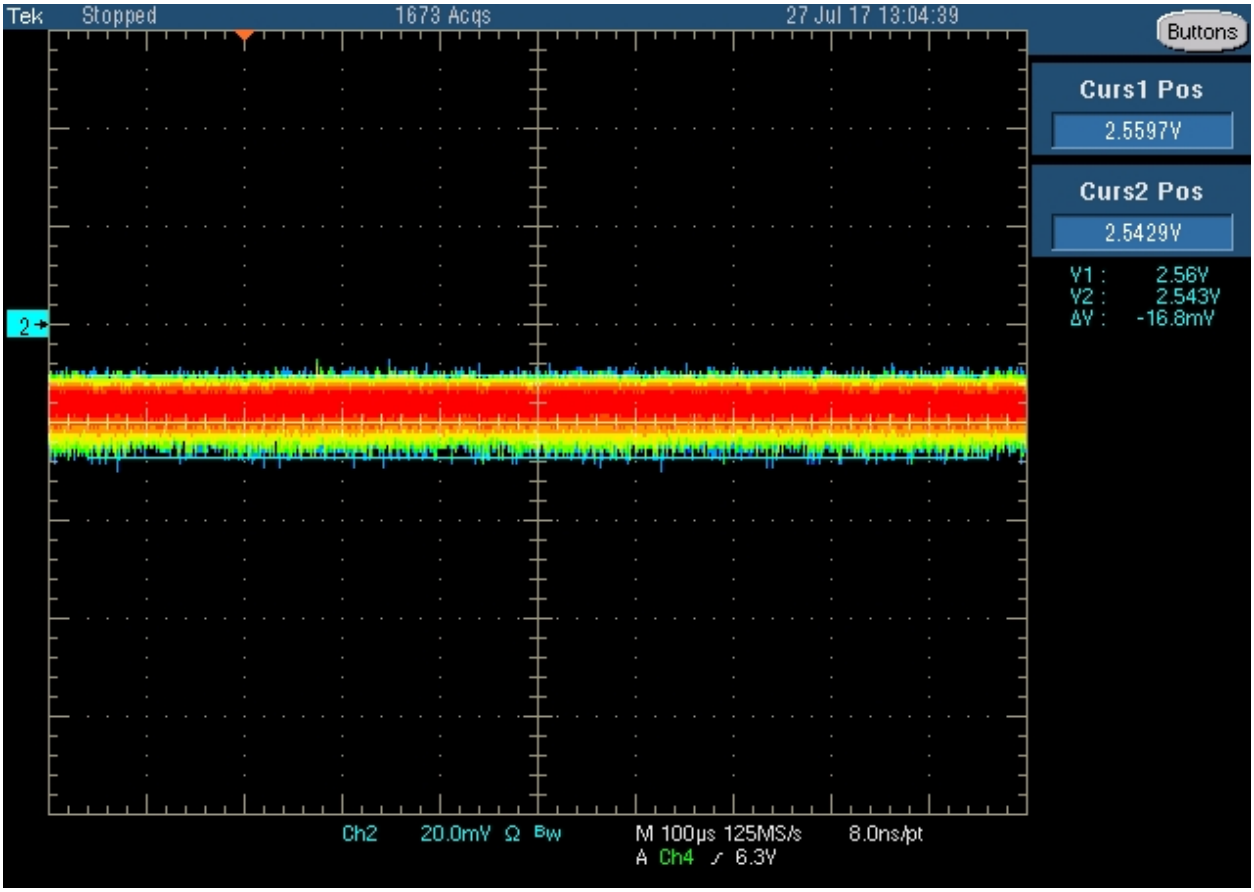

Figure 43 - UTIL_2V5 DC Ripple, 2A

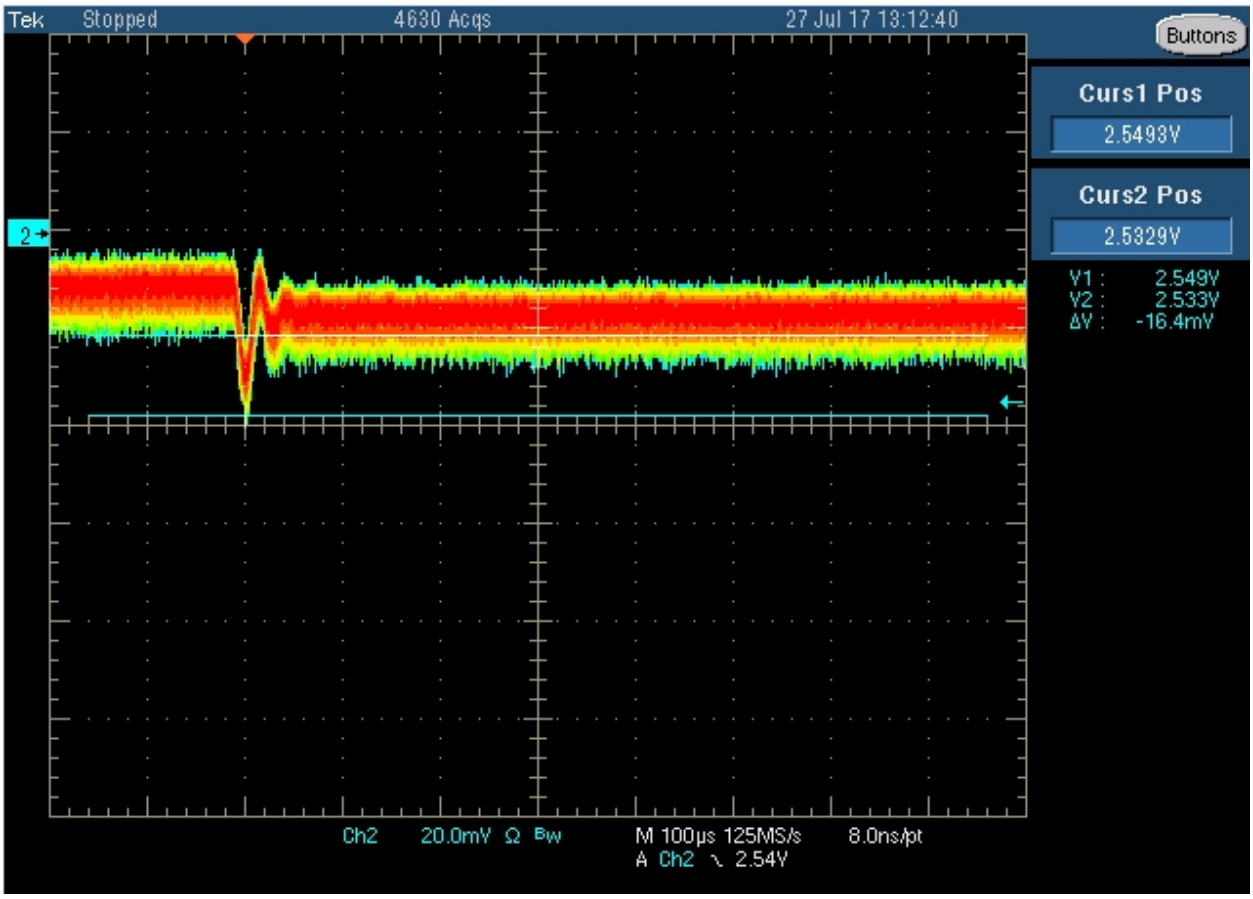

Figure 44 - UTIL_2V5 ac ripple load

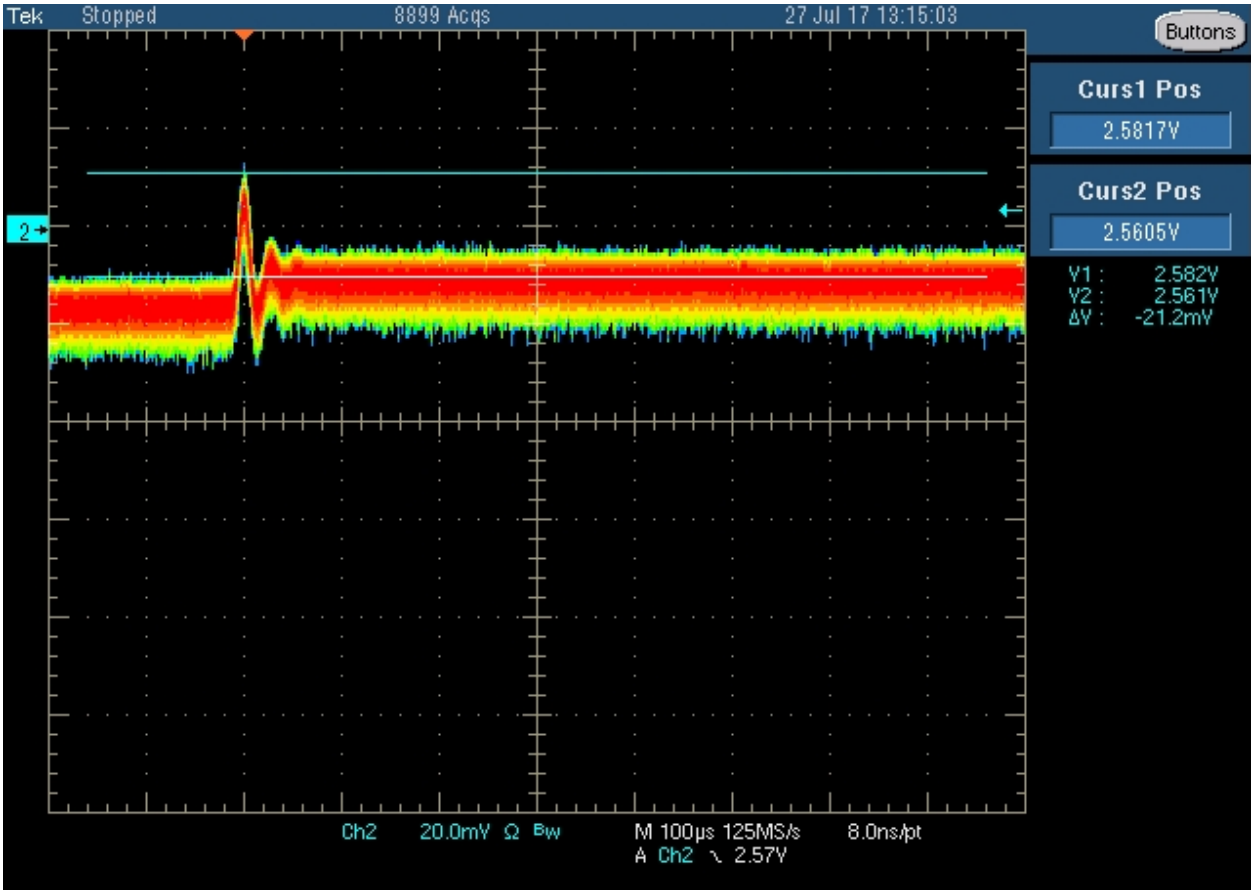

Figure 45 - UTIL_2V5 ac ripple release

PL_DDR4_VTT

Vin, 12V
Vout, 0.6V
Iout(pk), 3A
Istep, 1.5A
Iramp, 0.5A/us

Vout Measurement Location, J19
Load Test Location, J19
SW Node Measurement Location, L71

Jitter = 6.4ns (3A load)

Table 17 – PL_DDR4_VTT Results

Measurement	Result	Pass/Fail	Test Condition	Notes
Vout	0.6V 0.6V	Pass	0A 3A	DMM
DC Ripple	13.6mV 16.8mV	Pass	0A 3A	
Isense	N/A			
Vac(droop)	6.0mV	Pass	1.5A to 3.0A	
Vac(overshoot)	15.6mV	Pass	3.0A to 1.5A	

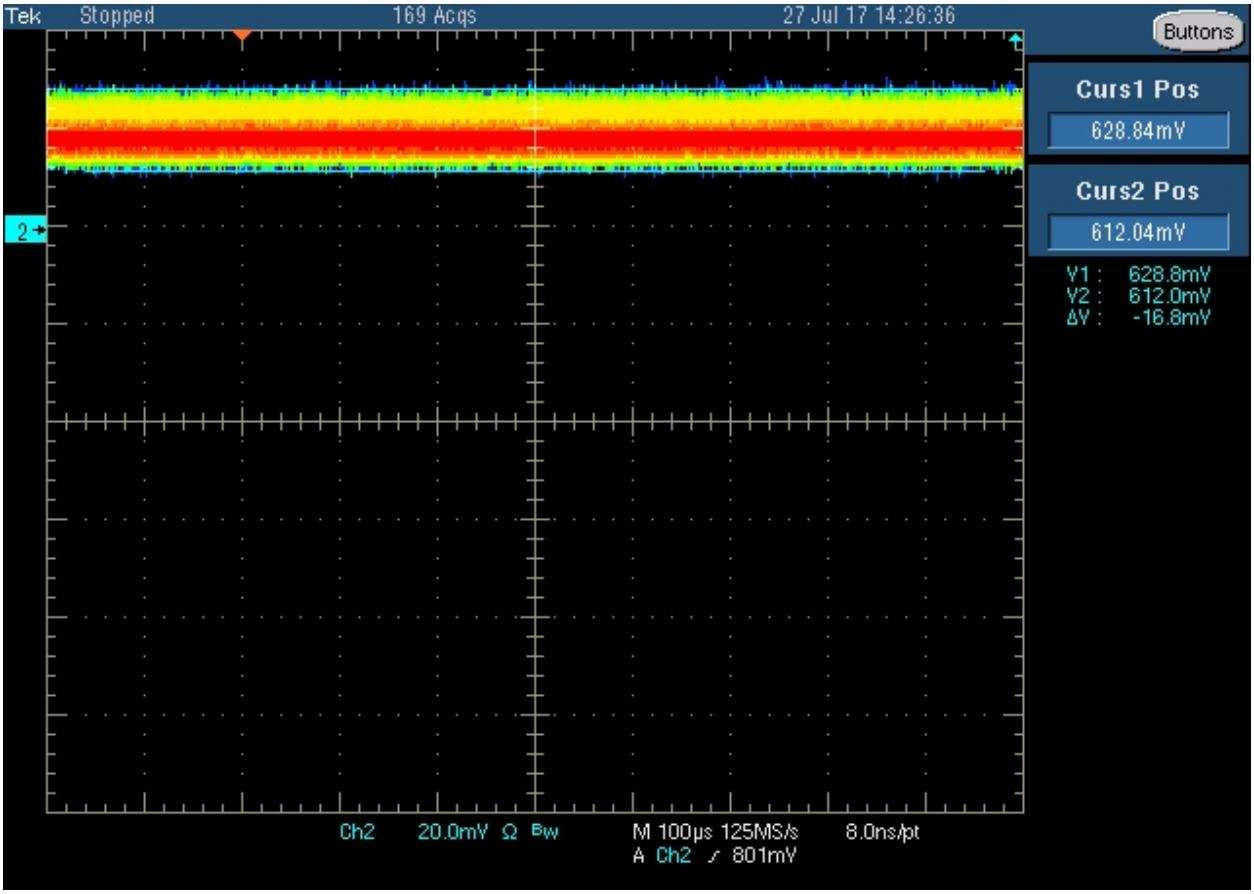

Figure 46 - PL_DDR4_VTT DC Ripple, 3A

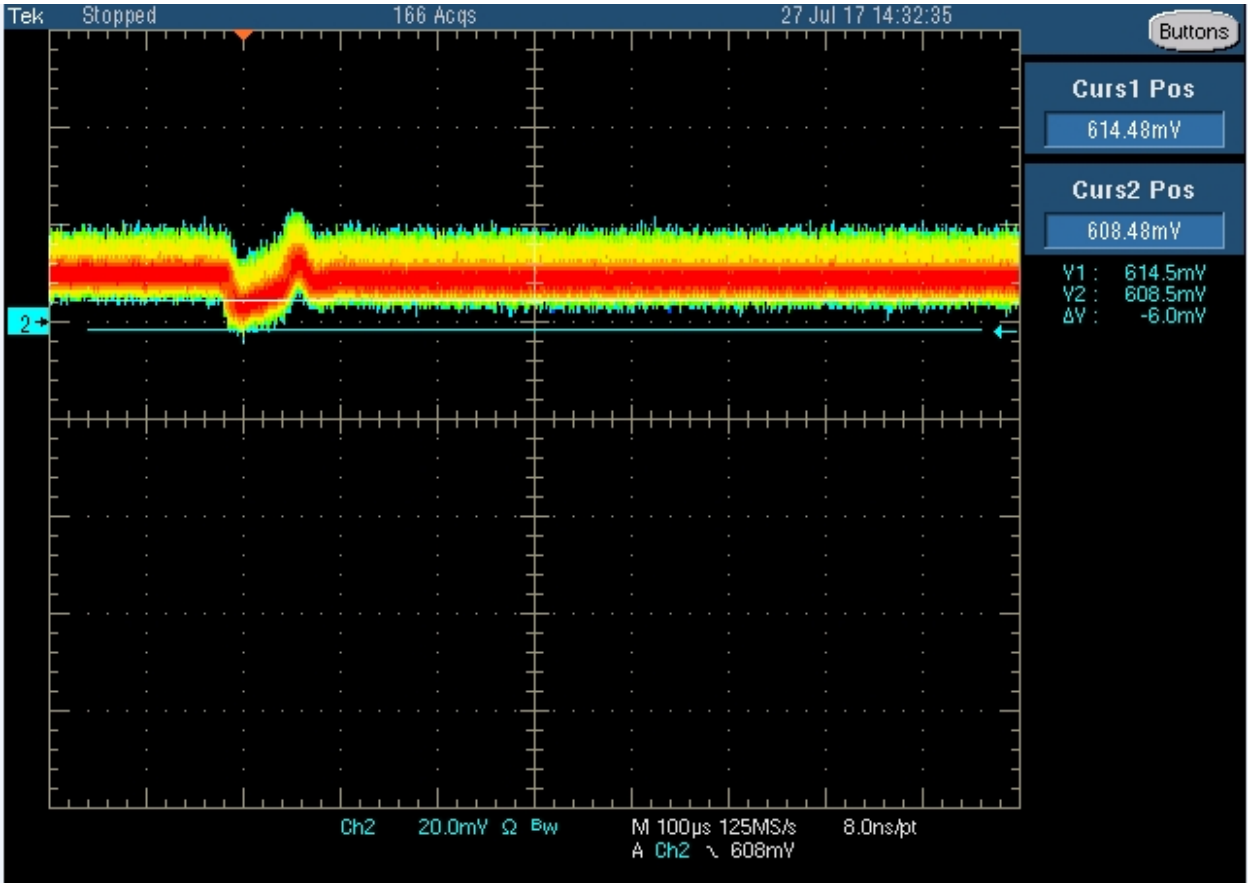

Figure 47 - PL_DDR4_VTT ac ripple load

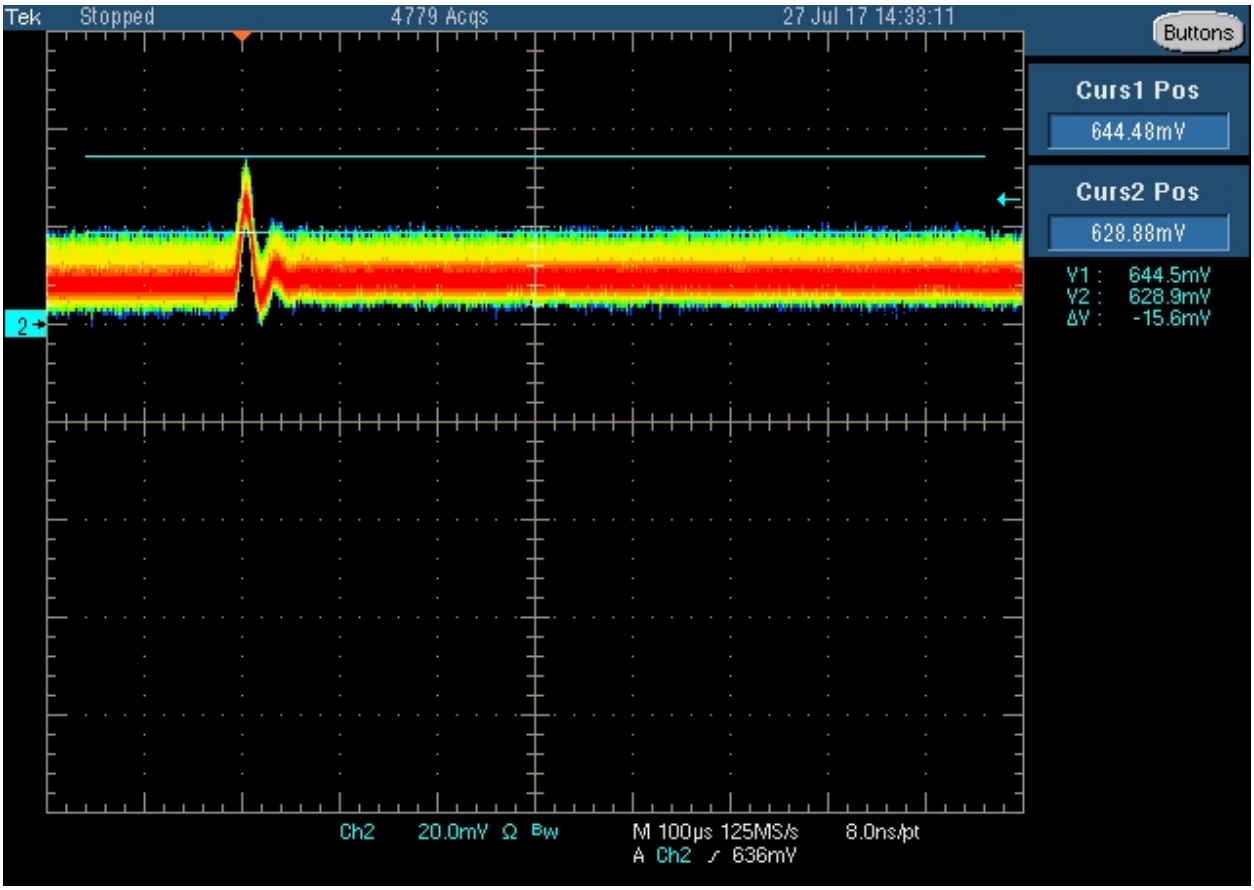

Figure 48 - PL_DDR4_VTT ac ripple release

Figure 49 - PL_DDR4_VTT Jitter, 3A

PS_DDR4_VTT

Vin, 12V
Vout, 0.6V
Iout(pk), 3A
Istep, 1.5A
Iramp, 0.5A/us

Vout Measurement Location, J18
Load Test Location, J18
SW Node Measurement Location, L72

Jitter = 5.2ns

Table 18 – PS_DDR4_VTT Results

Measurement	Result	Pass/Fail	Test Condition	Notes
Vout	0.6V 0.599V	Pass	0A 3A	DMM
DC Ripple	15.6mV 16.4mV	Pass	0A 3A	
Isense	N/A			
Vac(droop)	6mV	Pass		
Vac(overshoot)	14.8mV	Pass		

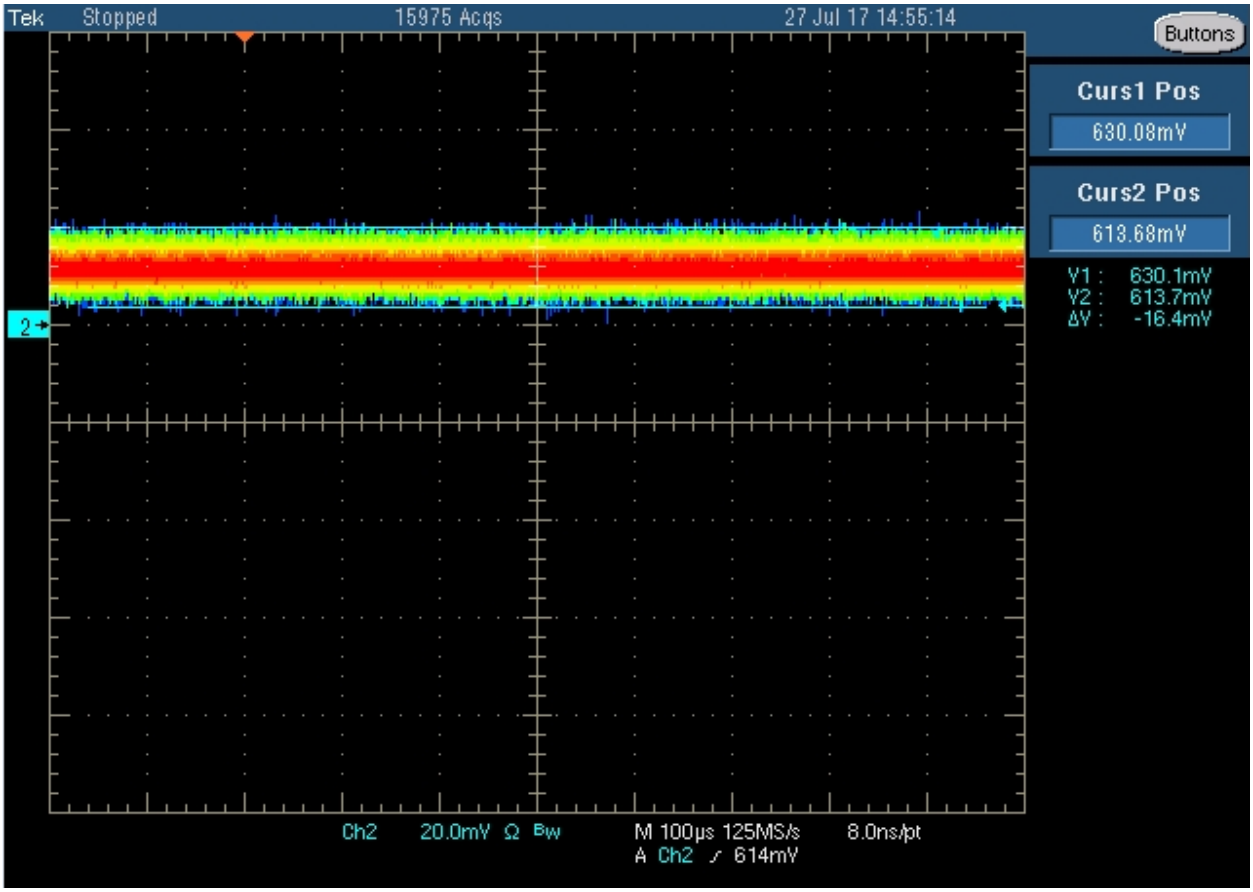

Figure 50 - PS_DDR4_VTT DC Ripple, 3A

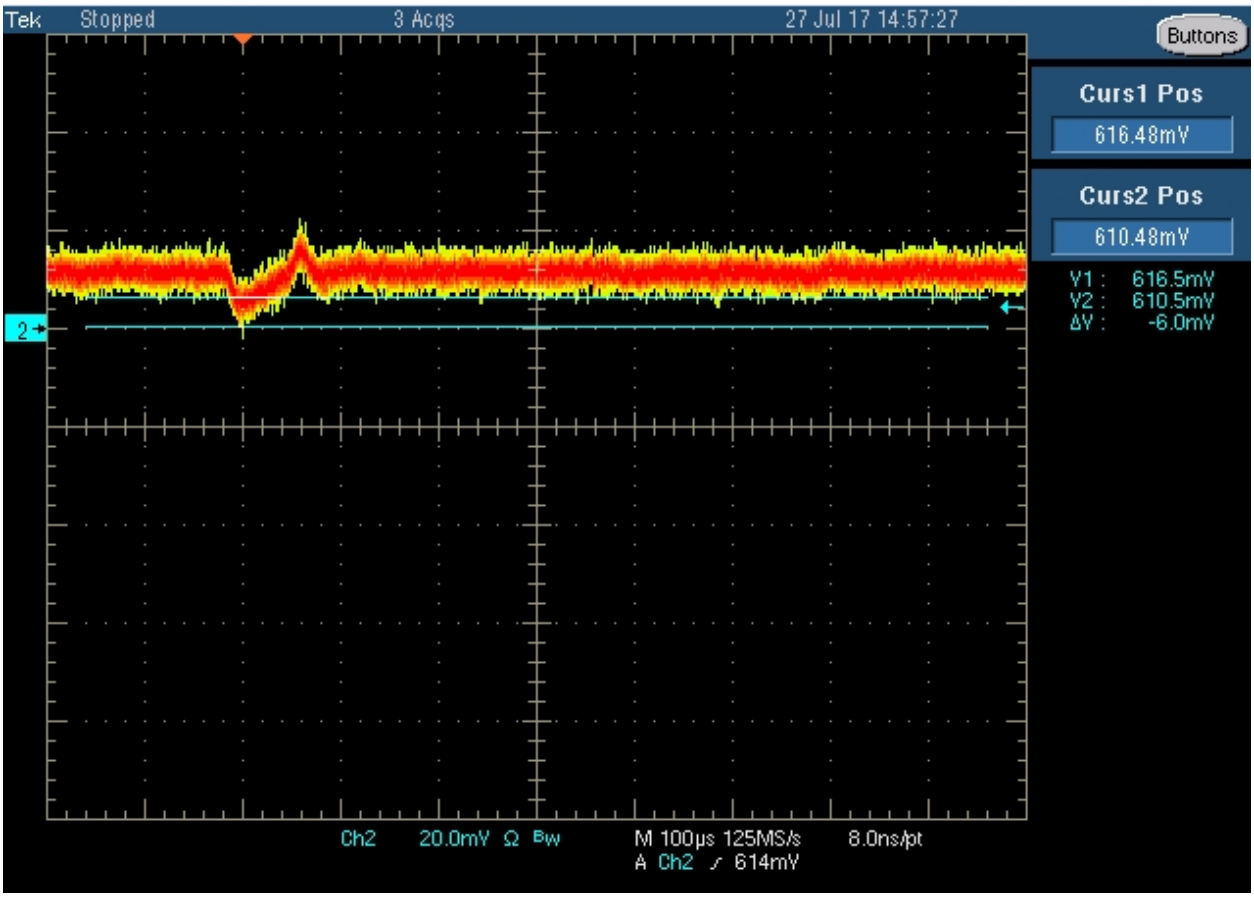

Figure 51 - PS_DDR4_VTT ac ripple load

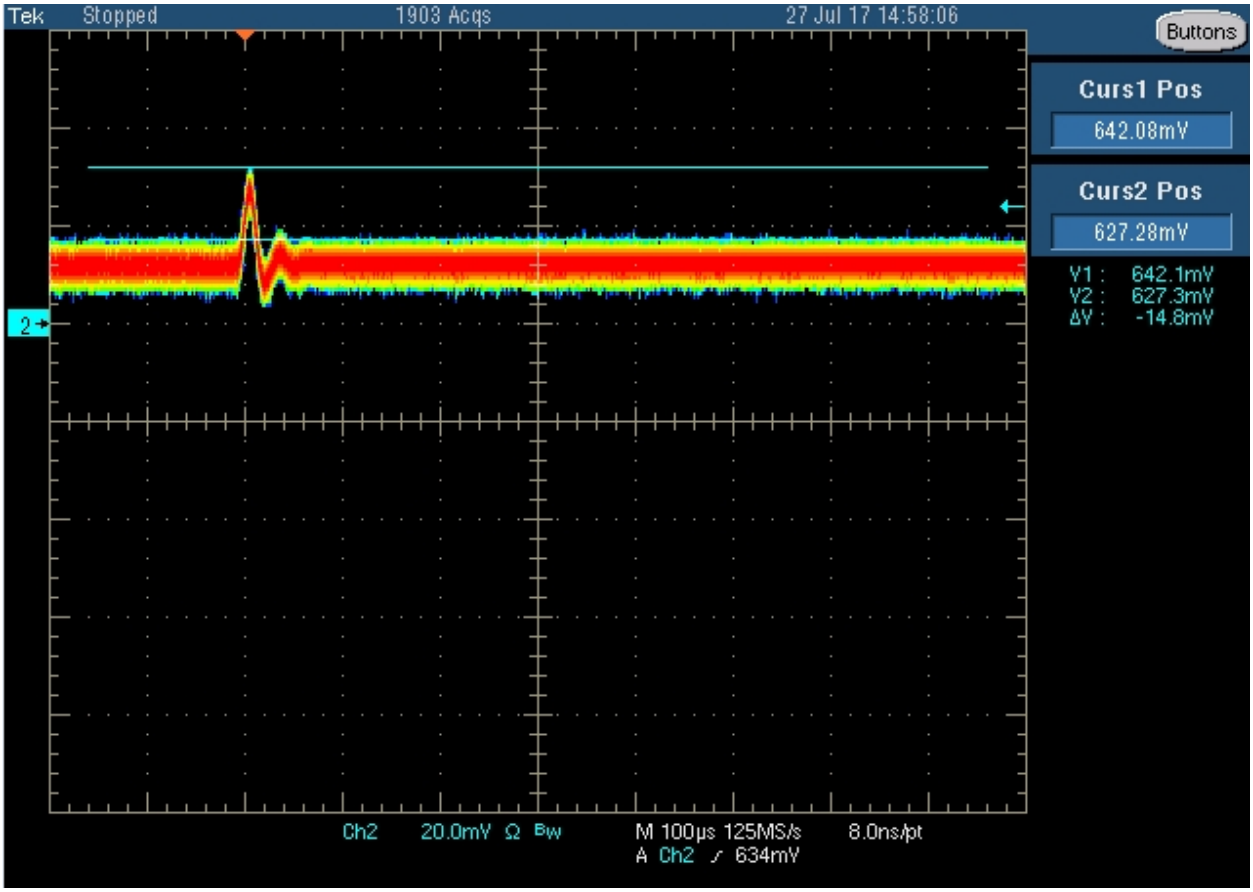

Figure 52 - PS_DDR4_VTT ac ripple release

Figure 53 - PS_DDR4_VTT Jitter, 3A