

# Package comparison

## OPTIREG™ SBC MidRange+

### About this document

#### Scope and purpose

The OPTIREG™ SBC MidRange+ can benefit of a dual site strategy. This comes with minor differences on the package. This document gives additional information on these two packages which are fully compatible. Both packages can be delivered when ordering the below mentioned Orderable Part Number (OPN).

#### Intended audience

Customers who use the OPTIREG™ SBC MidRange+ in their application.

#### Applicable products

**Table 1**      **Applicable products**

Sales name	OPN
TLE9261-3BQX	TLE92613BQXXUMA2
TLE9261-3BQX V33	TLE92613BQXV33XUMA2
TLE9261BQX	TLE9261BQXXUMA2
TLE9261BQX V33	TLE9261BQXV33XUMA2
TLE9262-3BQX	TLE92623BQXXUMA2
TLE9262-3BQX V33	TLE92623BQXV33XUMA2
TLE9262BQX	TLE9262BQXXUMA2
TLE9262BQX V33	TLE9262BQXV33XUMA2
TLE9263-3BQX	TLE92633BQXXUMA2
TLE9263-3BQX V33	TLE92633BQXV33XUMA2
TLE9263BQX	TLE9263BQXXUMA2
TLE9263BQX V33	TLE9263BQXV33XUMA2

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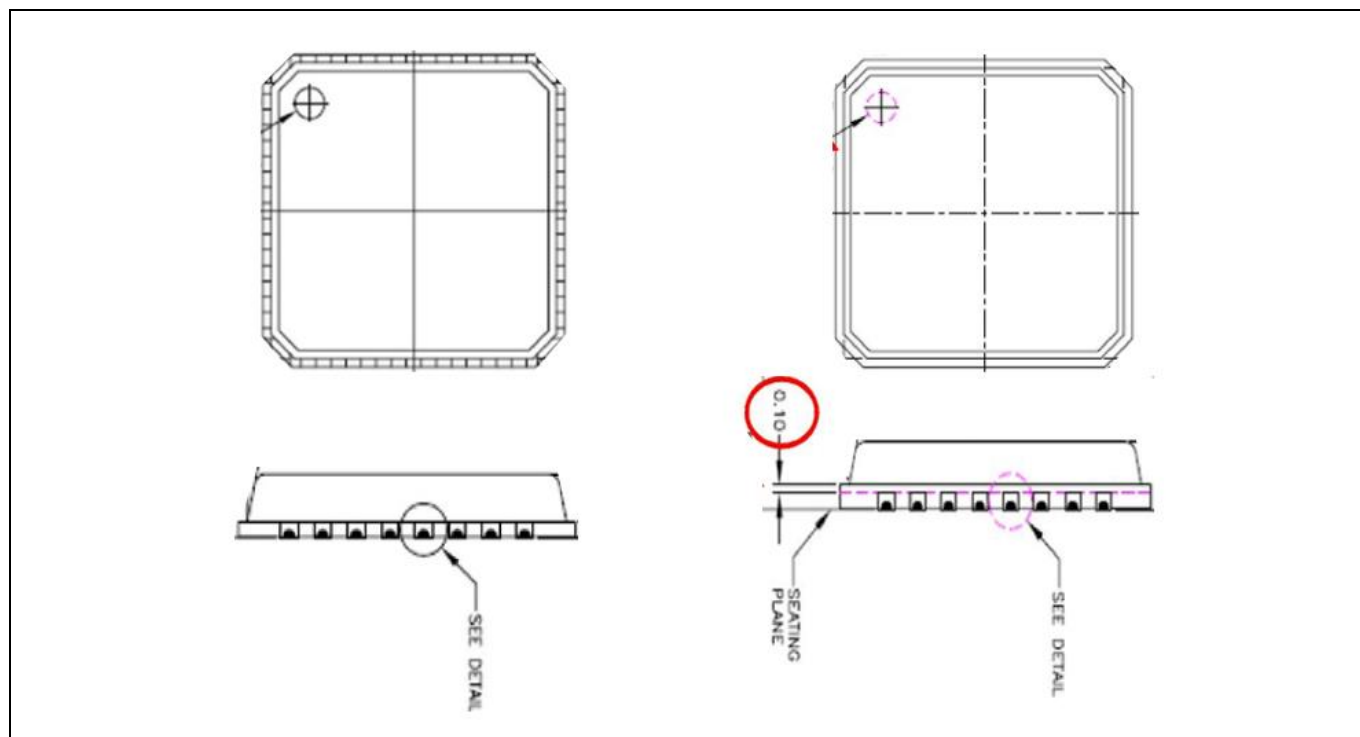
# Package comparison

## OPTIREG™ SBC MidRange+

### 1 Package outline

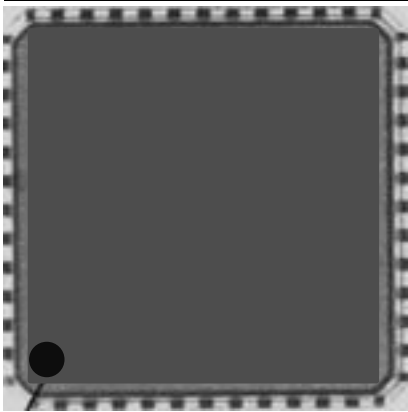
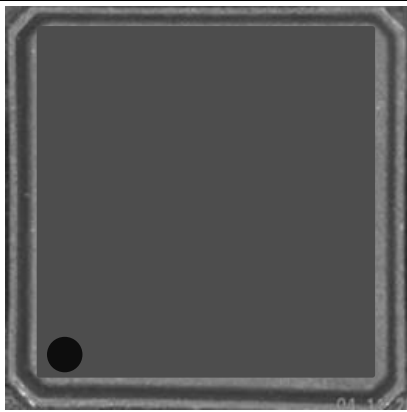
## 1 Package outline

The package outline differs in additional 0.10 mm of mold compound on top of the lead in the flange area as illustrated below. The board footprint dimensions are equal. And as such, there is no impact on the SMT process. Verification and possible adjustment of the incoming inspection may be required, subject to the customer inspection system.



**Figure 1** Package outline comparison

**Table 2** Comparison of the flange area of the two package options

PG-VQFN-48-37	PG-VQFN-48-79
	
Peripheral edge of package is exposed with leads	Peripheral edge of package is covered with mold compound

**Note:** The package outline which is included in the datasheets in revision 1.2 is covering both package variants in one drawing.

## Package comparison

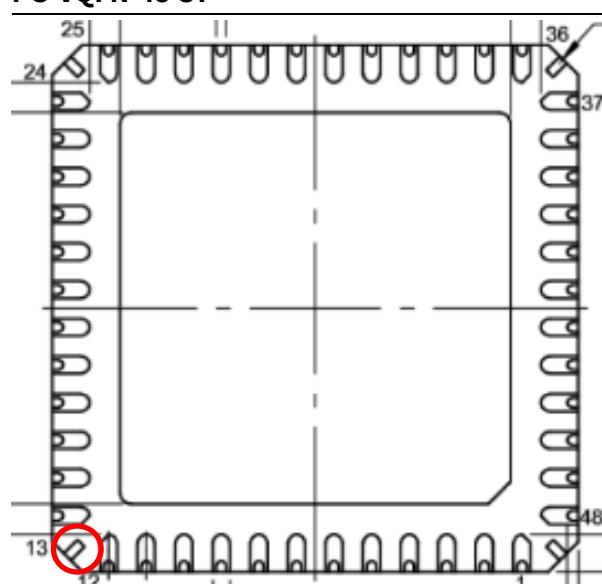
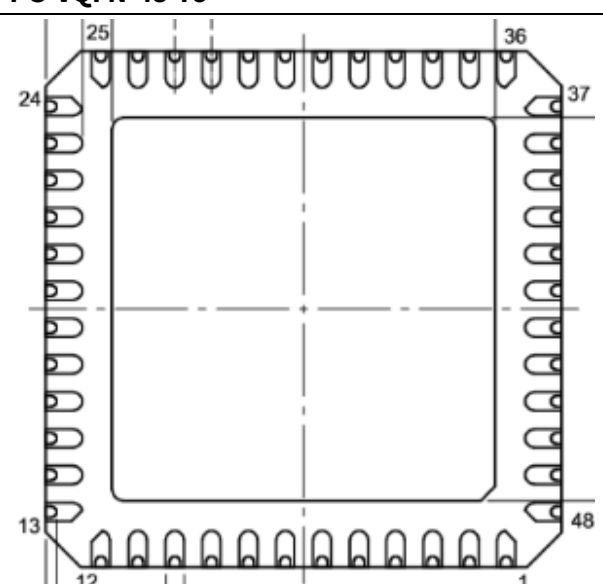
### OPTIREG™ SBC MidRange+

#### 2 Open metal from tie-bar

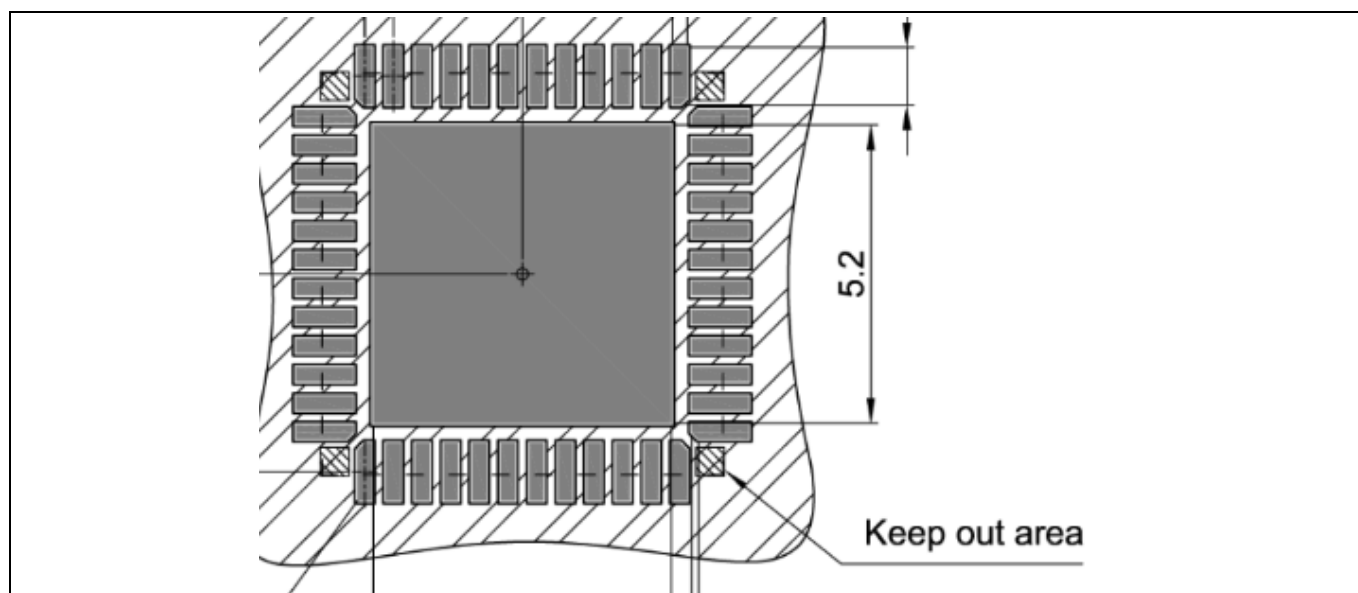
## 2 Open metal from tie-bar

One package shows open metal from the tie-bar, whereas the other package doesn't. See Table 3.

**Table 3 Comparison of the open metal from the tie-bar**

PG-VQFN-48-37	PG-VQFN-48-79
	
Red circle shows open metal from the tie-bar	No open metal in the corners

Because either of this package options can be delivered, it is recommended to have the keep out area implemented in the PCB footprint, which is initially only recommended for PG-VQFN-48-37 package. See Figure 2.



**Figure 2 Keep out area in footprint**

*Note: The package outline which is included in the datasheets in revision 1.2 is covering both package variants in one drawing.*

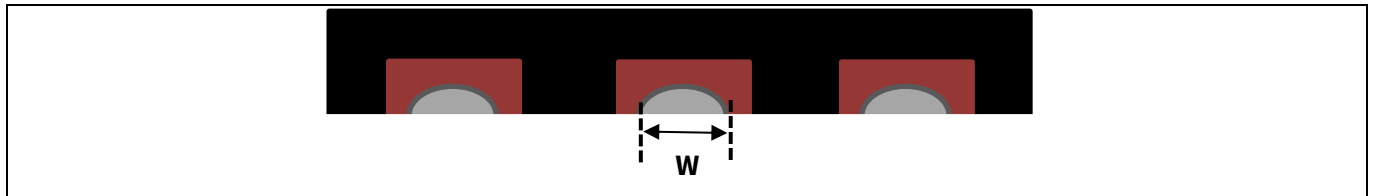
## Package comparison

### OPTIREG™ SBC MidRange+

#### 3 Dimple dimension

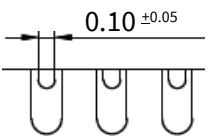
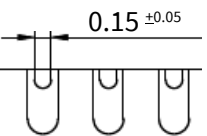
### 3 Dimple dimension

Infineon Automotive VQFN provide a solderable sidewall on lead tip to enable Automated Optical Inspection (AOI) and enhance board reliability. To further enhance robust AOI in mass production where low escape rates and low false alarm rates are both necessary, dimple nominal width  $W$  has increased from 0.10 mm to 0.15 mm. This will help to improve the surface contour of solder to distinguish between the good solder wetted pins and the non-wetted pins. This feature does not affect the footprint and SMT process at the customer assembly.

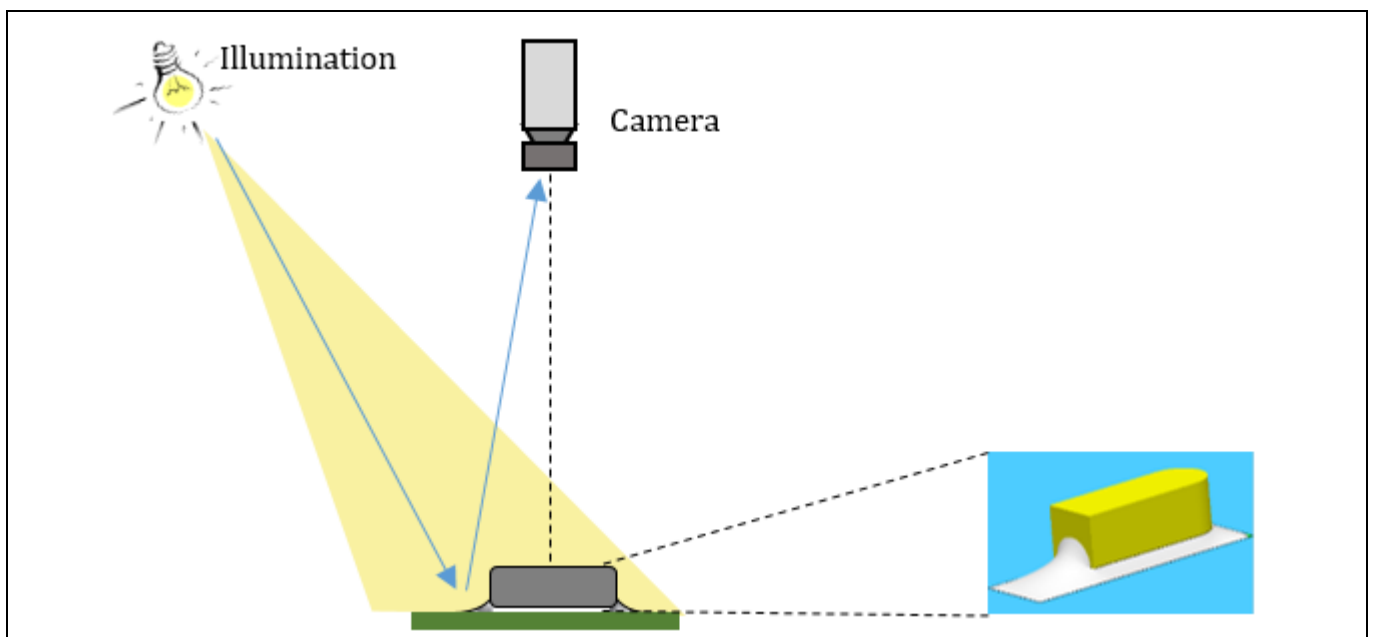


**Figure 3** Dimple width side view

**Table 4** Dimple width bottom view

PG-VQFN-48-37	PG-VQFN-48-79
	

AOI result is depending on the wetting of the sidewalls to ensure a reliable AOI image. Dimple width will increase the dimple depth due to the etching process of the leadframe. As such, enlarging the dimple width will help to improve the dimple height and therefore improve the surface contour of solder for a robust AOI. No changes to AOI setup is expected through this improved dimple size.



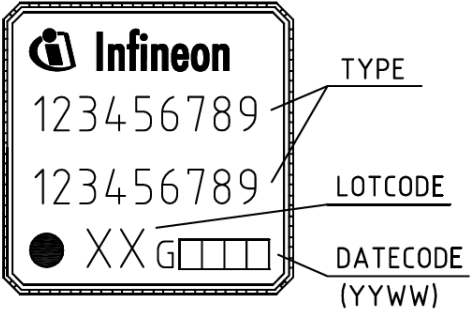
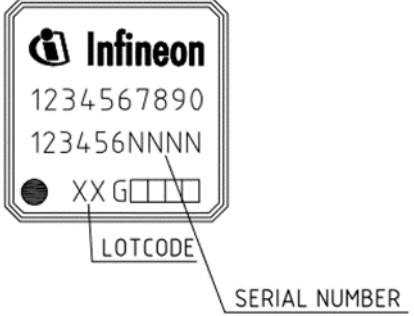
**Figure 4** AOI concept and surface contour of solder

## 4 Serialized marking

### 4 Serialized marking

Apart from the date code, Infineon introduces unit serialized marking for the new package. This will help to improve traceability. Together with the lot and date code it provides a unique marking per device. The unit serialized marking will be positioned above the date code on line 3.

**Table 5 Comparison of markings**

OPN	...XUMA2	
Package	PG-VQFN-48-37	PG-VQFN-48-79
	 <p>The diagram shows a rectangular marking area with the Infineon logo at the top. Below the logo, there are three lines of text: '123456789', '123456789', and 'XX G□□□'. Labels with arrows point to these lines: 'TYPE' points to the first line, 'LOT CODE' points to the second line, and 'DATE CODE (YYWW)' points to the third line.</p>	 <p>The diagram shows a rectangular marking area with the Infineon logo at the top. Below the logo, there are three lines of text: '1234567890', '123456NNNN', and 'XX G□□□'. Labels with arrows point to these lines: 'LOT CODE' points to the second line, and 'SERIAL NUMBER' points to the third line.</p>
Example of marking for TLE9263-3BQX V33	Infineon TLE9263-3 BQXV33 XX GYYWW	Infineon TLE9263-3 BQXV33NNNN XX GYYWW
Example of marking for TLE9261BQX	Infineon TLE9261 BQX XX GYYWW	Infineon TLE9261 BQXNNNN XX GYYWW

## **5 Conclusion**

# **5 Conclusion**

In summary,

- No impact expected on SMT process (such as stencils and temperatures).
- No impact to soldering lead-tip inspection settings expected.
- Minor adjustment may be required in case of incoming inspection in order to match the new marking (if applicable).

## **References**

- [1] <https://www.infineon.com/cms/en/product/packages/PG-VQFN/PG-VQFN-48-31/>
- [2] <https://www.infineon.com/cms/en/product/packages/PG-VQFN/PG-VQFN-48-79/>



## **Revision history**

<b>Document revision</b>	<b>Date</b>	<b>Description of changes</b>
1.0	2022-06-30	Initial release

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**Document reference**

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