

TLE9185QX/TLE9185QXV33

Step-by-step MOSFET driver setting guide and calculator description

About this document

Scope and purpose

This application note explains:

- the parameters and calculations needed to set the MOSFET driver of the TLE9185QX/TLE9185QXV33
- how to use the calculation tool for the settings of the gate drivers in PWM operation

It provides a step-by-step process to configure the MOSFET driver, based on the MOSFET datasheet, to control the MOSFET switching times in PWM operation:

- rise and fall times
- turn-on and turn-off delay times
- recommendations for the settings of the cross-current protection time and of the blank times

It also gives guidelines to use the "TLE9185 gate driver settings" tool.

Intended audience

This document is intended for users who develop application with the motor gate driver ICs products TLE9185QX and TLE9185QXV33.

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1 Introduction

1 Introduction

The TLE9185xx is a multi-half-bridge MOSFET driver, which combines power, communication and supply. The TLE9185QX features a low-dropout voltage regulator with an output current of 250 mA/5 V. The TLE9185QXV33 features a low-dropout voltage regulator with an output current of 250 mA/3.3 V.

Both devices are available in a VQFN-48 (7 mm x 7 mm) package.

The devices offer a wide range of diagnostic features for the bridge driver.

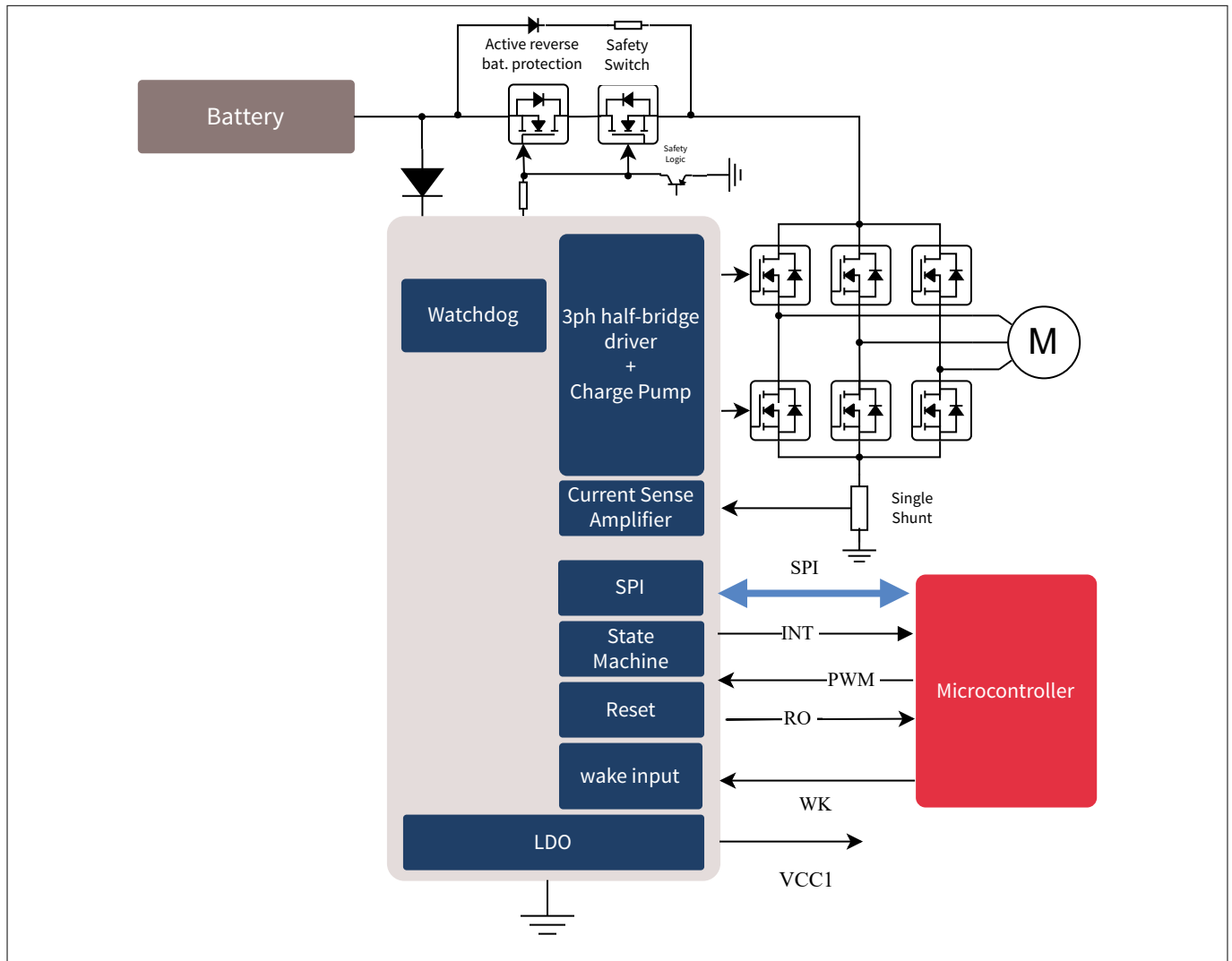


Figure 1 Block diagram – TLE9185QX/TLE9185QXV33

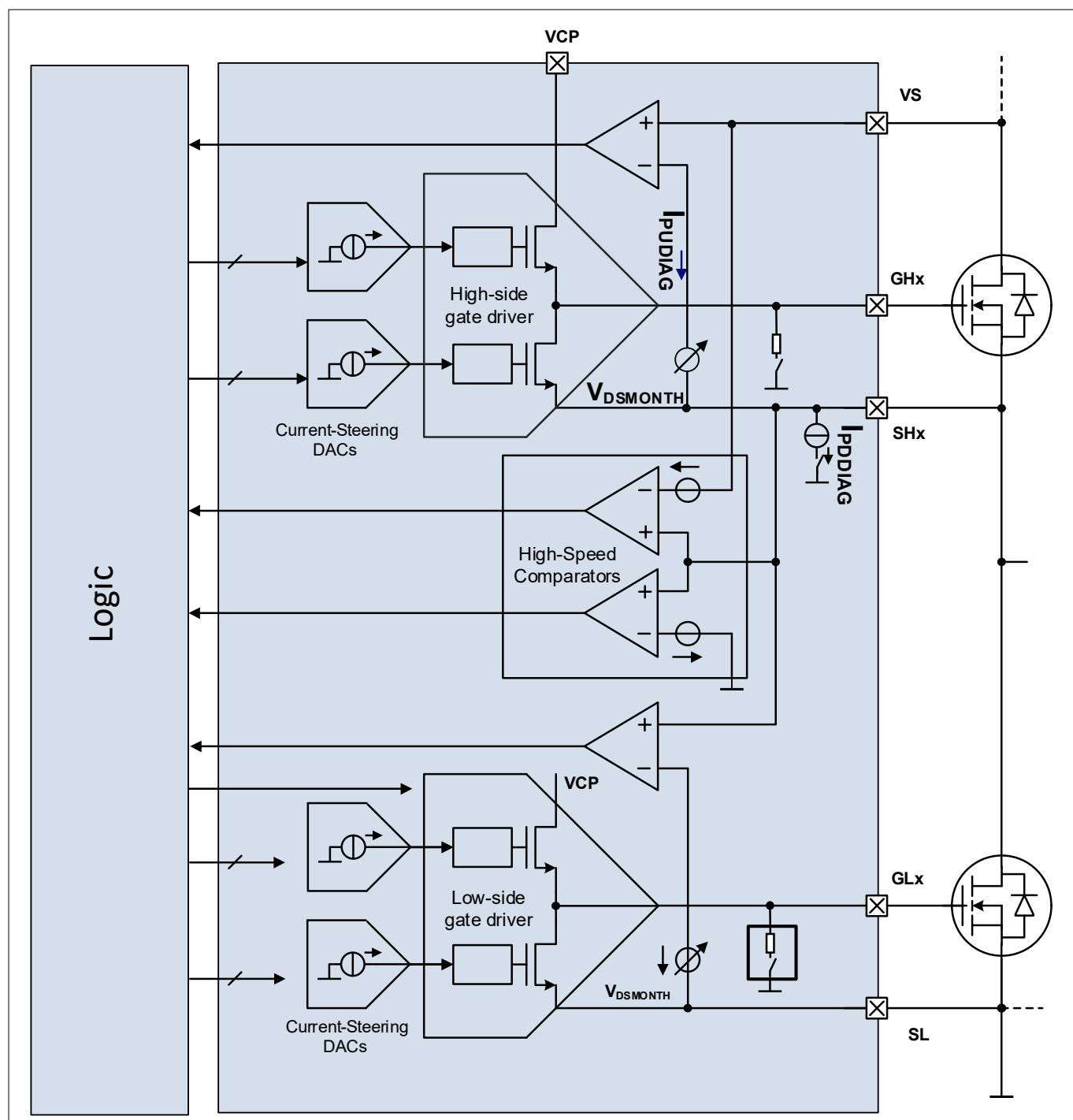


Figure 2 **Block diagram of one half-bridge gate driver**

2 General information

2 General information

2.1 Conditions

The calculations and considerations of this document are valid for an inductive load controlled in half-bridge/ full-bridge configuration with active freewheeling in PWM operation.

It is assumed that no external gate-drain/gate-source capacitance is placed at the MOSFET gate.

Note: Electrical parameters of the TLE9185xx and of the MOSFETs are subject to variations such as production spread, supply voltage, temperature drift etc... The proposed calculation and settings are done with typical values for a specific MOSFET operating condition (e.g. supply voltage, load current etc...), uses small-signal MOSFET capacitances and may differ from the tested devices under different test conditions. The calculations do not have the precision of a simulation and do not replace measurements.

2.2 Overview of the calculation steps

In this calculation tool, the user enters:

- MOSFET parameters extracted from the datasheet
- The application specific parameters and MOSFET driver's pre-charge and pre-discharge times

The calculation tool provides:

- The adapted MOSFET gate charges ($V_{ds} = V_s$, [Figure 5](#))
- The recommended settings of the MOSFET driver:
 - Gate driver currents
 - Cross-current protection times and blank times
 - Resulting switching times

2 General information

USER INPUT	
Datasheet MOSFET parameters:	
Qgs_typ	7.7 nC
Qgd_typ	7.1 nC
Qg_typ	31.0 nC
Vdd_typ	32.0 V
Vgh_typ	10.0 V
Vplateau_typ	4.4 V
Vgs_th	2.8 V
Ciss_vs	1740.0 pF
Crss_vs	100.0 pF
Crss_typ	27.0 pF

Figure 3 MOSFET input parameters (example with IPZ40N04S5-3R1)

Application conditions:	
Vs	14.0 V
Vgp	4.2 V
FET_LVL	0
Active MOSFET	LS active
trise_target	600.0 ns
tfall_target	800.0 ns
toff_fw_target	800.0 ns
tdon_min_margin	300.0 ns
tdoff_min_margin	300.0 ns
t_margin	30.0 %
tpchg	160 ns
tpdchg	267 ns
Adaptive Gate Control	1

Figure 4 Application and MOSFET driver input parameters

2 General information

Calculated MOSFET parameters:		
Q_{gs}	7.308	nC
Q_{gd}	5.957	nC
Q_g	34.382857	nC
V_{gh_active}	11.5	V
V_{gh_FW}	10	V
C_{iss_0V}	2893	pF

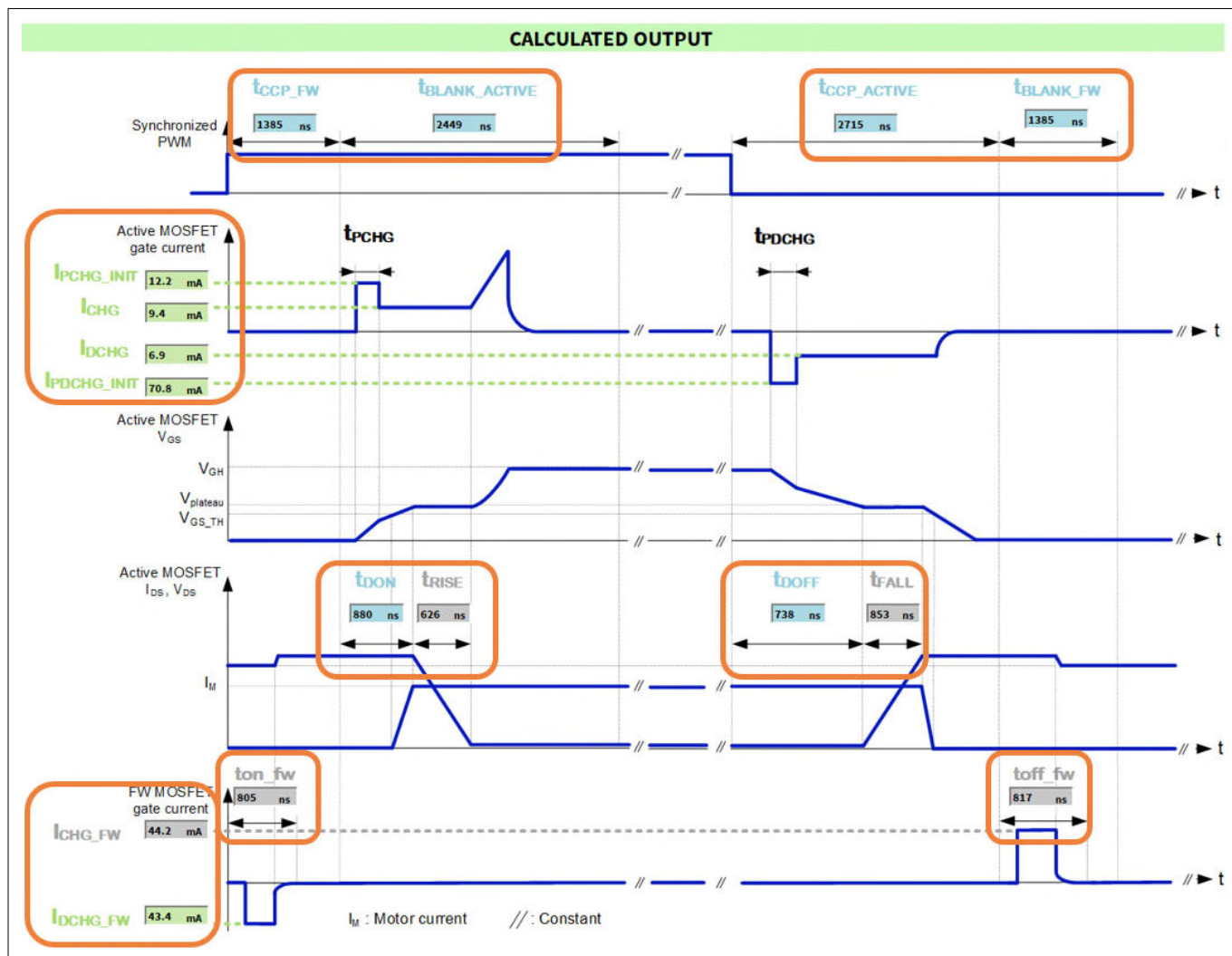
Figure 5 Outputs: MOSFET adapted gate charges (to $V_{ds} = V_s$)

Figure 6 Outputs: recommended cross-current protection time, blank time, gate driver currents and resulting switching times

2 General information

2.3 Notations

Table 1 List of notations

Abbreviation	Definition	Comment
V_{ds}	MOSFET drain-source voltage	
V_{gs}	MOSFET gate-source voltage	
I_{ds}	MOSFET drain-source current	
V_{gh}	MOSFET gate-source voltage when the gate is fully charged	
$t_{d_gdrv_on}$	TLE9185xx gate driver turn-on delay time	150 ns
$t_{d_gdrv_off}$	TLE9185xx gate driver turn-off delay time	150 ns
C_{iss_0V}	MOSFET input capacitance for drain-source voltage with $V_{ds} \sim 0$ V and $V_{gs} > V_{plateau}$	Chapter 6.3

V_{gh} is a TLE9185xx parameter which depends on the high-side MOSFET, and on the setting of the FET_LVL bit (refer to [Table 2](#) and Datasheet chapter 9.7). That is the reason why FET_LVL and the position of the active MOSFET must be entered ([Figure 4](#)).

Table 2 Typical V_{gh} depending on FET_LVL bit and the considered high-side/low-side MOSFET

	Typ. V_{gh} high-side	Typ. V_{gh} low-side
FET_LVL = 0	10 V	11.5 V
FET_LVL = 1	11.5 V	11.5 V

2.4 Software setup

The GUI requires the installation of the Infineon Development Center Launcher.

The download link and installation instructions can be found [here](#).

1. Launch the Infineon Development Center Launcher on your PC
2. Go to "Manage Tools" and search and install the tool: "Config Wizard for MOTIX™ motor gate driver ICs"
3. Start the "Config Wizard for MOTIX™ motor gate driver ICs"
4. Click on "TLE9185GATE DRIVER SETTINGS"

2 General information

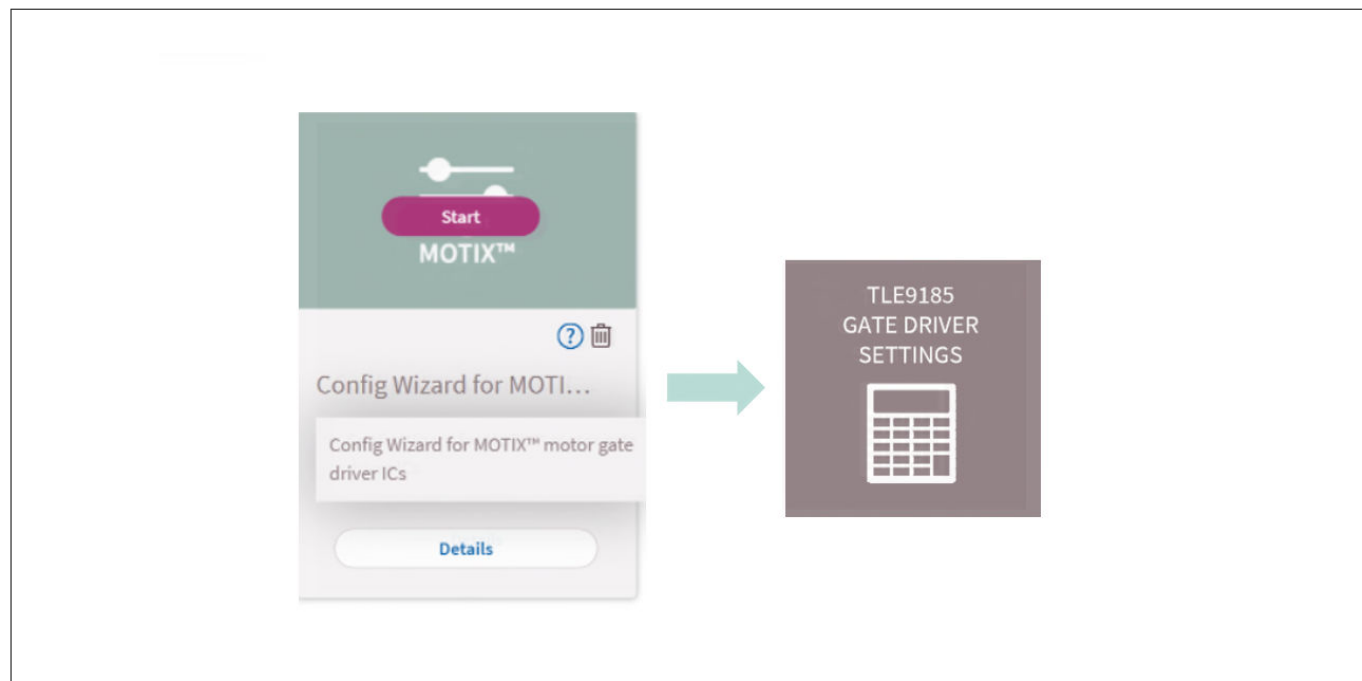


Figure 7 Start of the TLE9185 gate driver settings tool

3 Input parameters

3 Input parameters

This chapter explains the meaning of the required input parameters.

3.1 MOSFET input parameters

This section describes the required MOSFET input parameters, and how to extract them from the MOSFET datasheet.

Table 3 List of MOSFET input parameters

Abbreviation	Definition	Unit	Comment
Q_{gs_typ}	Typical MOSFET gate-source charge	nC	According to the datasheet conditions, Figure 9
Q_{gd_typ}	Typical MOSFET gate-drain charge	nC	According to the datasheet conditions, Figure 9
Q_{g_typ}	Typical MOSFET total gate charge	nC	According to the datasheet conditions (in general @ $V_{gs} = 10$ V), Figure 9
V_{dd_typ}	V_{ds} at which Q_{gd_typ} is specified	V	For example for IPZ40N04S5-3R1: $V_{dd_typ} = 32$ V, Figure 9
V_{gh_typ}	V_{gs} at which Q_{g_typ} is specified for full turn-on	V	For example for IPZ40N04S5-3R1: $V_{gh_typ} = 10$ V, Figure 9
$V_{plateau_typ}$	V_{gs} plateau at which Q_{gs_typ} is specified	V	For IPZ40N04S5-3R1: $V_{plateau_typ} = 4.4$ V @ $I_{ds} = 40$ A, Figure 9
V_{gs_th}	V_{gs} threshold according to the typical application conditions (I_{ds} , etc...)	V	According to the datasheet conditions, Figure 9
C_{iss_vs}	MOSFET input capacitance for drain-source voltage with $V_{ds} = V_s$	pF	Figure 12 , corresponding to the nominal application conditions ($V_s = 14$ V in this application note)
C_{rss_vs}	MOSFET reverse transfer capacitance with $V_{ds} = V_s$	pF	Figure 12
C_{rss_typ}	MOSFET reverse transfer capacitance at $V_{ds} = V_{dd_typ}$	pF	Figure 12

3.1.1 Gate charges Q_{gs_typ} , Q_{gd_typ} , Q_{g_typ}

Q_{gs_typ} , Q_{gd_typ} , Q_{g_typ} are required parameters for the control of the switching times of the active MOSFET. Refer to [Figure 8](#) for the definition.

In general, the gate charges are specified for a very specific condition (32 V, 40 A, V_{gs} from 0 to 10 V, [Figure 9](#)).

3 Input parameters

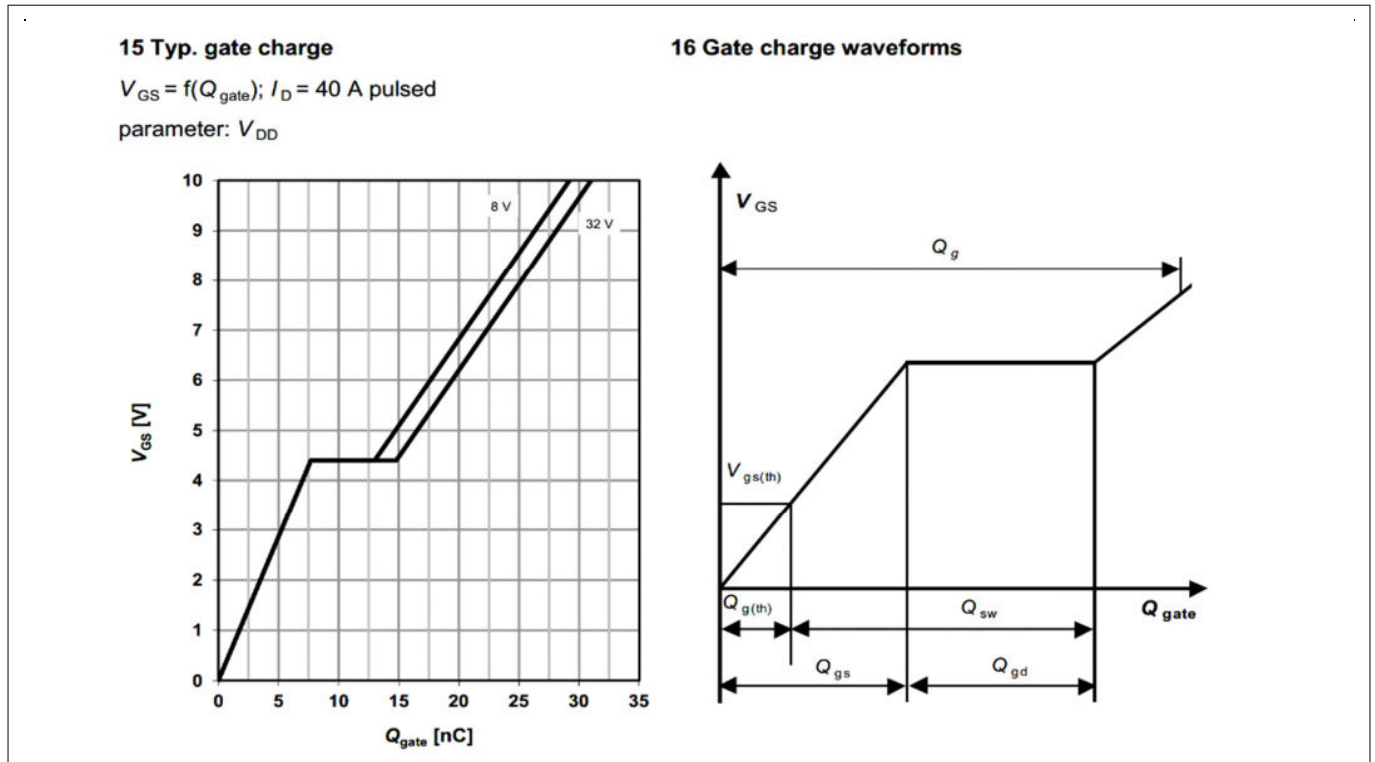


Figure 8 Gate charge definition and example

The figure above shows the gate charge definition as well as an example (IPZ40N04S4-3R1, Infineon OptiMOS™ 5 MOSFET, [4]).

Gate Charge Characteristics ²⁾						
Gate to source charge	Q_{gs}	$V_{DD}=32\text{V}, I_D=40\text{A},$ $V_{GS}=0 \text{ to } 10\text{V}$	-	7.7	10.2	nC
Gate to drain charge	Q_{gd}		-	7.1	10.6	
Gate charge total	Q_g		-	31	41	
Gate plateau voltage	$V_{plateau}$		-	4.4	-	V

Figure 9 Example of gate charge specification (IPZ40N04S4-3R1) under specific conditions (32 V, 40 A, V_{gs} from 0 to 10 V)

Note: The specified gate charges in Figure 9 correspond to Q_{gs_typ} , Q_{gd_typ} , and Q_{g_typ} .

These parameters depend on the working point of the active MOSFET. Indeed, these gate charges vary (among others) with:

- the applied drain-source voltage
- the MOSFET I_{ds} current
- the applied gate-source voltage, when the MOSFET is turned on (V_{gh})

Note: Q_g in the MOSFET datasheets is often given for $V_{gs} = 0 \text{ V to } 10 \text{ V}$. However, the typical V_{gh} of the TLE9185xx depends on the setting of the FET_LVL bit and on the high-side/low-side MOSFET. Therefore, Q_g is re-calculated by the tool (for the applicable V_{gh} instead of V_{gs_typ} , refer to Chapter 6.3).

3 Input parameters

For a more accurate control of the switching times, the gate charges must be adapted to the specific application conditions. Refer to [Chapter 6](#).

3.1.2 Gate threshold voltage V_{GS_th} (or $V_{GS(th)}$)

V_{GS_th} : typical MOSFET threshold voltage (Refer to [Figure 8](#) and [Figure 10](#)).

Static characteristics						
Drain-source breakdown voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=1mA$	40	-	-	V
Gate threshold voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=30\mu A$	2.2	2.8	3.4	

Figure 10 IPZ40N04S4-3R1 gate threshold voltage

3.1.3 MOSFET input capacitances at $V_{ds} = V_s$

C_{iss_vs} is the input capacitance under the following conditions: $V_{ds} = V_s$ and $V_{gs} = 0V$

C_{iss_vs} is needed to set conditions on the gate driver configurations for the pre-charge phase (AGC = 1 or 2), in order to avoid a too fast current increase of I_{ds} (i.e. high dI_{ds}/dt) during the turn-on of the MOSFET.

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Dynamic characteristics ²⁾						
Input capacitance	C _{iss}	V _{GS} =0V, V _{DS} =25V, f=1MHz	-	1740	2310	pF
Output capacitance	C _{oss}		-	490	650	
Reverse transfer capacitance	C _{rss}		-	35	55	

Figure 11 Specification of C_{iss} at $V_{gs} = 0V$ and $V_{ds} = 25V$ (IPZ40N04S4-3R1)

The IPZ40N04S5-3R1 shows no substantial variation for the C_{iss} between 14 V and 25 V ([Figure 12](#)). Therefore C_{iss_vs} can be considered to be equal to 1740 pF for this MOSFET.

Note: The MOSFET input capacitance depends on V_{ds} (and V_{gs}). This parameter is in general specified under a specific condition, which may differ from the typical application conditions.

3 Input parameters

10 Typ. capacitances

$$C = f(V_{DS}); V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$$

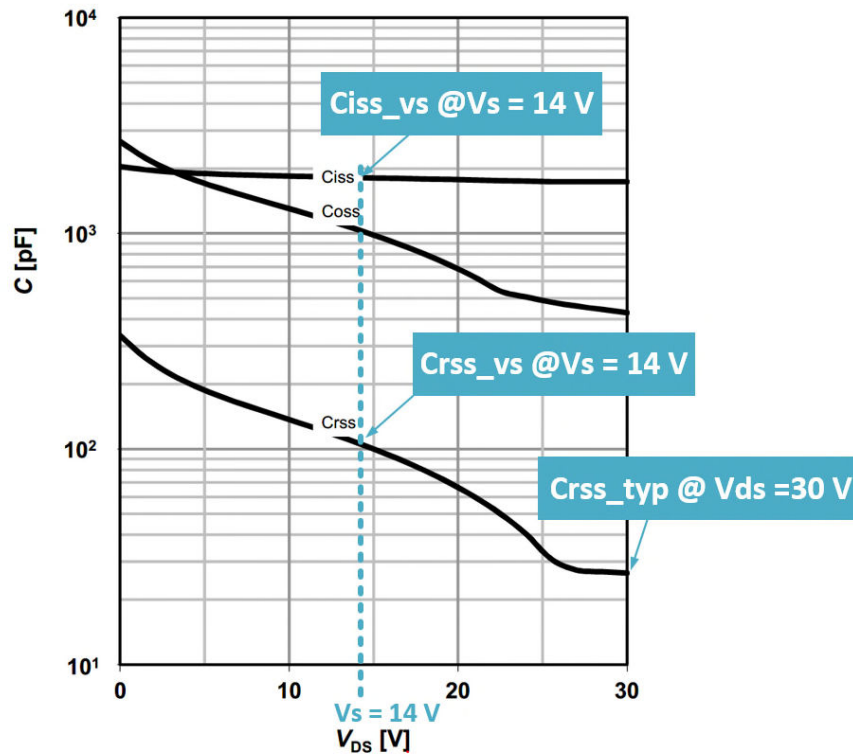


Figure 12 Determination of C_{iss_vs} , C_{rss_vs} (IPZ40N04S5-3R1, $V_s = 14 \text{ V}$)

3.1.4 MOSFET reverse transfer capacitances at $V_{ds} = V_s$ and $V_{ds} = V_{dd_typ}$

C_{rss_vs} is the reverse transfer capacitance at $V_{ds} = V_s$ and $V_{gs} = 0 \text{ V}$.

C_{rss_typ} is the reverse transfer capacitance at $V_{ds} = V_{dd_typ}$ and $V_{gs} = 0 \text{ V}$.

C_{rss_vs} and C_{rss_typ} are required to estimate Q_{gd} at $V_{ds} = V_s$, using Q_{gd_typ} (at $V_{ds} = V_{dd_typ}$).

The value of these capacitances can be read from [Figure 12](#) for the IPZ40N04S5-3R1. C_{rss_typ} at $V_{ds} = 30 \text{ V}$ is a good estimation of C_{rss_typ} (at $V_{ds} = V_{dd_typ} = 32 \text{ V}$), because the C_{rss} curve is flat in this range for this MOSFET.

3.2 Application related input parameters

This section describes the application related input parameters, which are listed in the table below.

Table 4 List of inputs parameters in the application conditions

Abbreviation	Definition	Unit	Comment
V_s	Nominal application supply voltage	V	$V_s = 14 \text{ V}$ in this document
V_{gh}	MOSFET driver gate-source voltage when the gate is fully charged	V	Refer to Table 2
$V_{plateau}$	V_{gs} plateau in the application conditions	V	Refer to Figure 14

(table continues...)

3 Input parameters

Table 4 (continued) List of inputs parameters in the application conditions

Abbreviation	Definition	Unit	Comment
$t_{\text{rise_target}}$	Active MOSFET target rise time	ns	–
$t_{\text{fall_target}}$	Active MOSFET target fall time	ns	–
$t_{\text{off_fw_target}}$	FW MOSFET target turn-off time	ns	–
$t_{\text{don_min_margin}}$	Additional delay between the end of the pre-charge phase and the moment when V_{gs} reaches $V_{\text{gs_th}}$	ns	300 ns in the examples
$t_{\text{doff_min_margin}}$	Additional delay between the end of the pre-discharge phase and the moment when V_{ds} decreases (V_{gs} reaches V_{plateau})	ns	300 ns in the examples
t_{margin}	Margin in % added to the min. required cross-current protection time and blank time	%	30% in the examples
t_{pchg}	Gate driver pre-charge time	ns	TPRECHG register
t_{pdchg}	Gate driver pre-discharge time	ns	TPRECHG register
AGC	Adaptive gate control bit	–	GENTCTRL register

Figure 13 shows the switching times, the cross-current protection time and blank time of the active and FW MOSFETs during PWM operation (the control scheme of the active MOSFET represented on Figure 13 corresponds to AGC = 1 and AGC = 2).

3 Input parameters

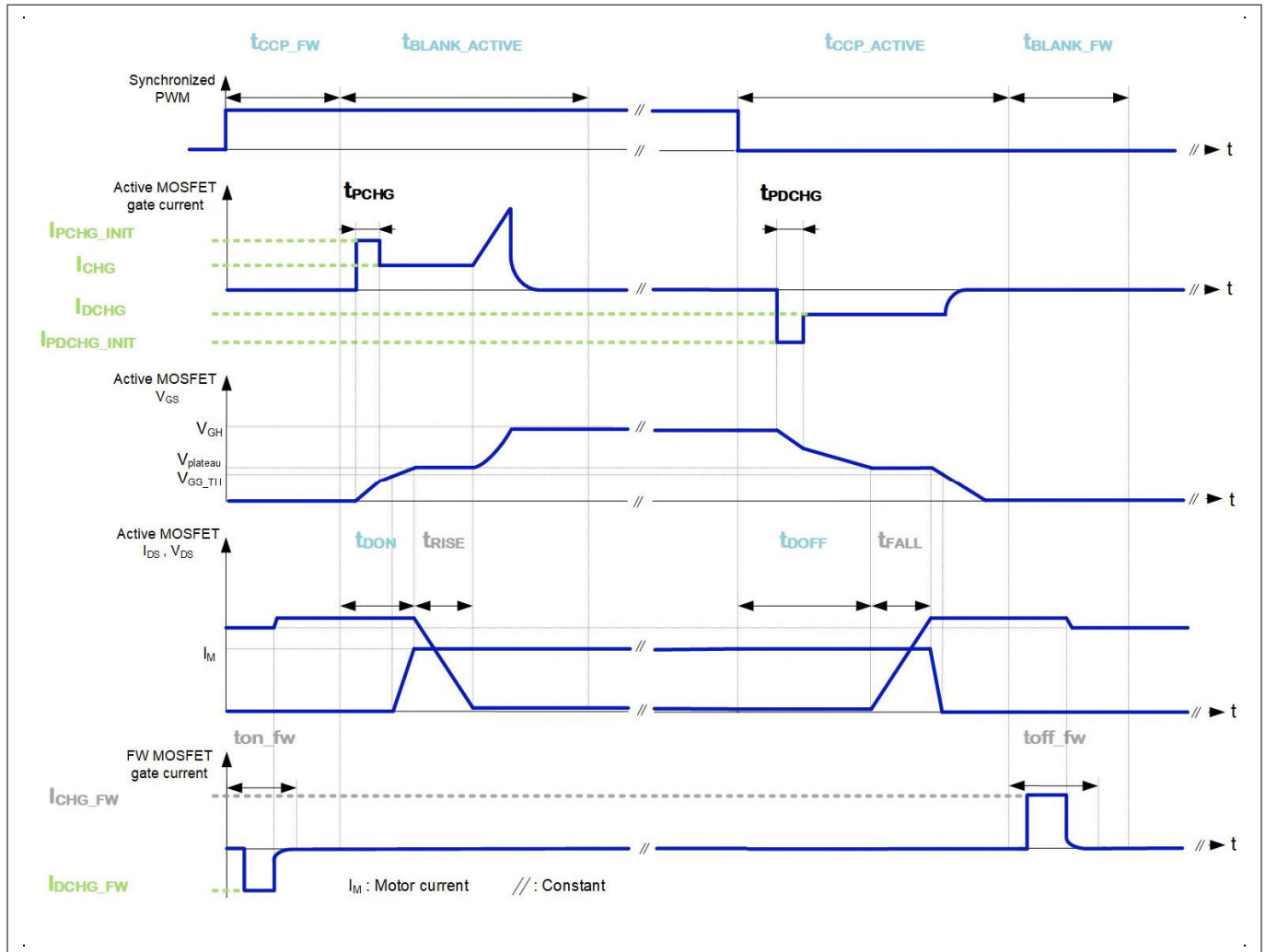


Figure 13 Switching times and timings definition

- t_{rise_target} is the target rise time of the active MOSFET. This parameter is defined as the duration of the V_{ds} slope at the turn-on of the active MOSFET (Refer to [Figure 13](#)).
- t_{fall_target} is the target fall time of the active MOSFET. This parameter is defined as the duration of the V_{ds} slope at the turn-off of the active MOSFET (Refer to [Figure 13](#)).
- $t_{off_fw_target}$ is the target switch-off time of the FW MOSFET.
- t_{ccp_active} is the cross-current protection time of the active MOSFET. The gate driver must be configured so that active MOSFET is off before the end of the t_{CCP_ACTIVE} .
- t_{ccp_fw} is the cross-current protection time of the FW MOSFET. The gate driver must be configured so that the FW MOSFET is off before the end of the t_{CCP_FW} .
- t_{margin} is the margin (in percent) added to the minimum required cross-current protection times and the blank times for the active MOSFET and for the FW MOSFET.
- $t_{don_min_margin}$ is relevant for AGC = 1 and 2 (refer to the datasheet for information about the AGC bit). It is a minimum delay between the end of the pre-charge phase and the moment when V_{gs} reaches V_{gs_th} . Refer to [Chapter 4](#).
- $t_{doff_min_margin}$ is relevant for AGC = 1 or 2. It is the minimum delay between the end of the pre-discharge phase and the beginning of t_{fall} . Refer to [Chapter 4](#).

3 Input parameters

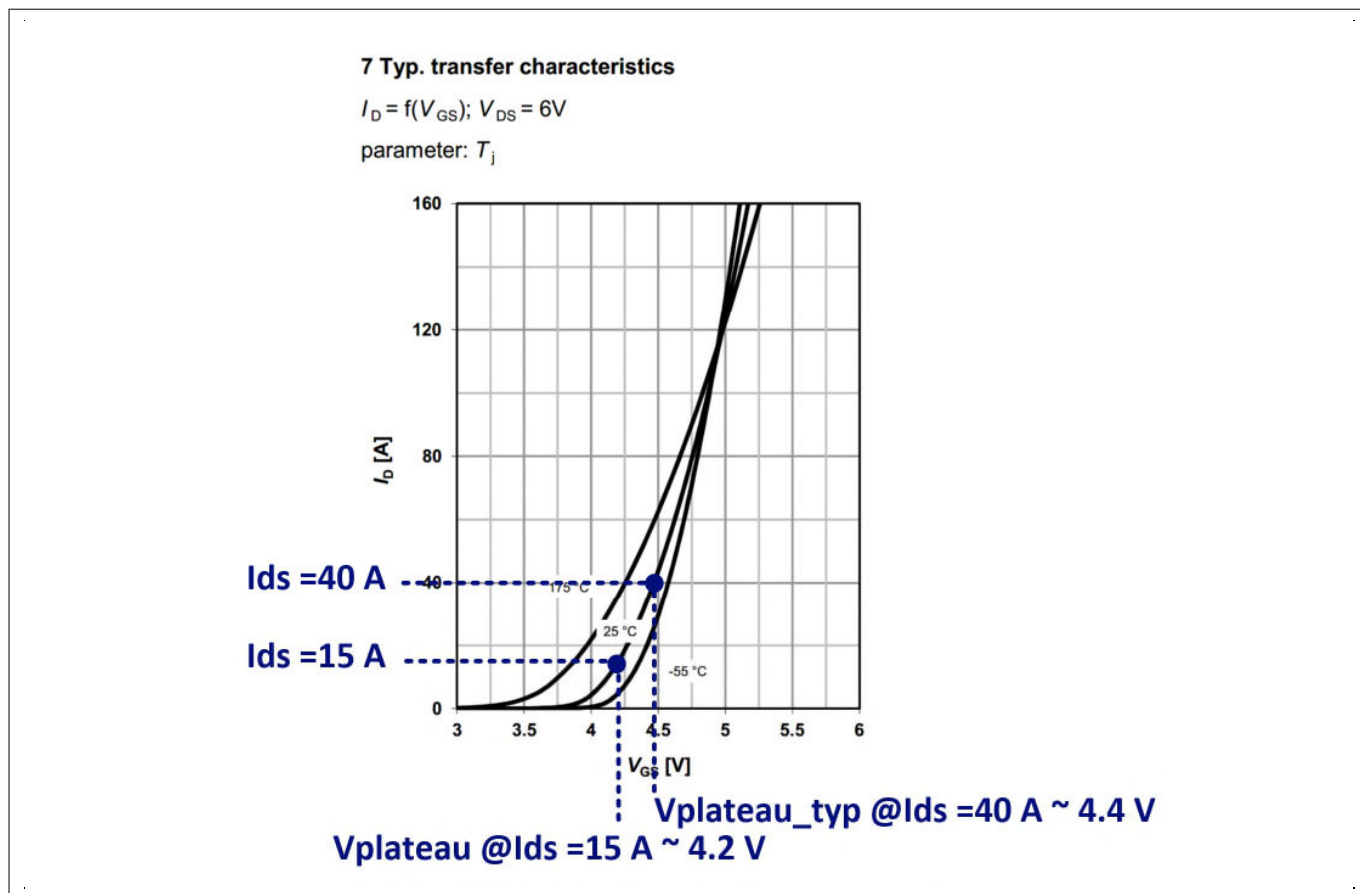


Figure 14 Determination of $V_{plateau}$ in the application conditions – IPZ40N04S5-3R1, $I_{DS} = 15\text{ V}$

3.3 Output parameters

The calculation tool provides the recommended charge and discharge currents for the active and FW MOSFETs and the expected switching times. The user will also find the recommendations for the blank time and cross-current protection times.

The MOSFET gate charges Q_g , Q_{gs} and Q_{gd} are adapted by the calculation tool according to the description in [Chapter 6](#).

Note that the maximum allowed pre-charge current and pre-discharge currents (for AGC = 1 or 2) is supposed to be set to 100 mA typ.

Table 5 List of output parameters

Abbreviation	Definition	Unit	Control register
ICHG	Active MOSFET charge current	mA	HB_ICHG
IDCHG	Active MOSFET discharge current	mA	
ICHG_FW	FW MOSFET charge current	mA	
IDCHG_FW	FW MOSFET discharge current	mA	
IPCHG_INIT	Active MOSFET initial pre-charge current	mA	HB_PCHG_INIT
IPDCHG_INIT	Active MOSFET initial pre-discharge current	mA	
t_{don}	Active MOSFET turn-on delay time	ns	–

(table continues...)

3 Input parameters

Table 5 (continued) List of output parameters

Abbreviation	Definition	Unit	Control register
t_{doff}	Active MOSFET turn-off delay time	ns	–
t_{rise}	Active MOSFET effective rise time	ns	–
t_{fall}	Active MOSFET achievable fall time	ns	–
$t_{\text{on_fw}}$	FW MOSFET turn-on time	ns	–
$t_{\text{off_fw}}$	FW MOSFET turn-off time	ns	–
$t_{\text{blank_active}}$	Active MOSFET selected blank time	ns	CCP_BLK
$t_{\text{ccp_active}}$	Active MOSFET current-cross protection time	ns	
$t_{\text{blank_fw}}$	FW MOSFET blank time	ns	
$t_{\text{ccp_fw}}$	FW MOSFET current-cross protection time	ns	

Notes:

1. t_{rise} , t_{fall} , $t_{\text{on_fw}}$, $t_{\text{off_fw}}$ may differ from $t_{\text{rise_target}}$, $t_{\text{fall_target}}$, $t_{\text{on_fw_target}}$ and $t_{\text{off_fw_target}}$. This difference is due to the fact that the calculation of t_{rise} , t_{fall} , $t_{\text{on_fw}}$, $t_{\text{off_fw}}$ considers the nearest available gate driver's charge and discharge currents
2. t_{don} , t_{doff} , $t_{\text{on_fw}}$ and $t_{\text{off_fw}}$ include the gate driver delay times $t_{\text{d_gdrv_on}}$ and $t_{\text{d_gdrv_off}}$
3. $t_{\text{blank_active}}$ is selected so that its minimum value fulfills [0.12], [1.12]. The calculation tool displays the corresponding typical value
4. $t_{\text{ccp_active}}$ is selected so that its minimum value fulfills [0.13], [1.13]. The calculation tool displays the corresponding typical value
5. $t_{\text{ccp_fw}}$ is selected so that its minimum value fulfills [0.14], [1.14]. The calculation tool displays the corresponding typical value
6. $t_{\text{blank_fw}}$ is selected so that its minimum value fulfills [0.15], [1.15]. The calculation tool displays the corresponding typical value

4 Recommendations

4 Recommendations

4.1 Conditions on $t_{\text{rise_target}}$ and $t_{\text{fall_target}}$

$t_{\text{rise_target}}$ and $t_{\text{fall_target}}$ are input parameters determined by the application requirements. These parameters are determined by the trade-off between the electromagnetic emissions (EME) and the switching losses, and must be defined for each application according to their specific requirements.

4.2 Conditions on the pre-charge phase (AGC = 1 and AGC = 2)

If the pre-charge phase is activated, the pre-charge phase should be over before the I_{ds} increases in the active MOSFET (i.e. before $V_{\text{gs}} = V_{\text{gs_th}}$). If this condition is not fulfilled, then the possible high pre-charge current causes a fast increase of I_{ds} , resulting in a high EME.

This criteria is taken into account in 5.2.1 Step 3 and gives a condition on IPCHG_INIT.

$t_{\text{don_min_margin}}$ (e.g. 300 ns) further reduces the maximum allowed pre-charge current, in order to avoid a fast increase of I_{ds} .

Note: $t_{\text{don_min_margin}}$ is an additional delay, which is directly reflected on the turn-on delay time, explaining the name of the parameter.

4.3 Recommendation for t_{pchg} (AGC = 1 and AGC = 2)

t_{pchg} must fulfill two conditions:

1. It should be as short as possible in order to avoid an unnecessary increase of t_{don}
2. It should be long enough, so that the charges delivered during the pre-charge phase ($t_{\text{pchg}} \times \text{IPCHG}$) and during the charge phase allow to reach the target t_{don}

For the common MOSFETs used in combination with the TLE9185QX/TLE9185QXV33, $t_{\text{pchg}} = 160$ ns is often a good starting point.

4.4 Conditions on the pre-discharge phase (AGC = 1 and AGC = 2)

When the pre-discharge phase is activated (AGC = 1 or 2), the pre-discharge phase should over before the decrease of V_{ds} . If this condition is not fulfilled, then the possible high pre-discharge current causes a fast decrease of V_{ds} , resulting in a high EME.

This criteria is taken into account in 5.2.1 Step 4 (AGC = 1 or 2) and gives a condition on IPDCHG_INIT.

$t_{\text{doff_min_margin}}$ (e.g. 300 ns) further reduces the maximum allowed pre-discharge current, in order to avoid that the pre-discharge phase is still active during the increase of V_{ds} .

Note: In the calculations of this application note, a symmetrical t_{don} and t_{doff} requires $t_{\text{doff_min_margin}} > t_{\text{don_min_margin}}$.

4.5 Recommendation for t_{pdchg} (AGC = 1 or 2)

t_{pdchg} must fulfill two conditions:

1. It should be as short as possible in order to avoid an unnecessary increase of t_{doff}
2. It should be long enough, so that the charges removed from the MOSFET's gate during the pre-discharge phase ($t_{\text{pdchg}} \times \text{IPDCHG}$) and during the discharge phase allow to reach the target t_{doff}

4 Recommendations

For the common MOSFETs used in combination with the TLE9185QX/TLE9185QXV33 such as the IPZ40N04S5-3R1, $t_{pdchg} = 267$ ns is often suitable.

4.6 Recommendations for $t_{off_fw_target}$

The turn-off (and the turn-on) of the FW MOSFET has a much lower impact on the EME than for the active MOSFET. Therefore, it is possible to turn-off the FW MOSFET faster than the active MOSFET: for example between 600 ns and 1 μ s as a starting point. $t_{off_fw_target}$ determines the suitable FW discharge current.

Note: $IDCHG_FW$ is determined by $t_{off_fw_target}$ and by the MOSFET characteristics. The setting FW MOSFET charge and discharge currents are set by common control bits, therefore the turn-on time of the FW MOSFET is also determined.

5 Calculation of the gate driver currents and timings

5 Calculation of the gate driver currents and timings

This chapter shows the calculations that apply for AGC = 0, AGC = 1 or AGC = 2.

5.1 Calculation with adaptive gate control disabled (AGC = 0)

This section shows the formulas used to calculate the required gate driver settings based on the input parameters when AGC = 0.

In this mode, the pre-charge and pre-discharge phases are disabled. The gate of the active MOSFET is charged, respectively discharged with the constant currents ICHG and IDCHG.

5.1.1 Calculation of gate driver currents with AGC = 0

This section calculates the required ICHG, IDCHG, IDCHG_FW.

Table 6 Calculation of gate driver currents with AGC = 0

Step	Parameters [mA]	Formula	-
1	Active MOSFET Charge current	$ICHG = \frac{Q_{gd}}{t_{rise_target}}$	[0.1]
2	Active MOSFET Discharge current	$IDCHG = \frac{Q_{gd}}{t_{fall_target}}$	[0.2]
3	Active MOSFET initial pre-charge current ¹⁾	IPCHG_INIT = ICHG	[0.3]
4	Active MOSFET initial pre-discharge current ¹⁾	IPDCHG_INIT = IDCHG	[0.4]
5	FW MOSFET discharge current ²⁾	$IDCHG_FW = \frac{C_{iss_0V} \times V_{gh}}{t_{off_fw_target} - t_{d_drv_off}}$	[0.5]

Once the required current is calculated, the nearest available MOSFET driver current of the TLE9185QX/TLE9185QXV33 is selected by the calculation tool. Refer to the datasheet rev. 1.0, Table 24 and Table 25, [1].

5.1.2 Timing calculation with AGC = 0

This section calculates the effective t_{rise} , t_{fall} , t_{don} , t_{doff} , t_{on_fw} , t_{off_fw} , t_{blank_active} , t_{ccp_active} , t_{ccp_fw} , and t_{blank_fw} .

Attention: The nearest available ICHG, IDCHG, ICHG_FW and IDCHG_FW must be used in this calculation step.

¹⁾ These parameters are not relevant if AGC = 0: Therefore the IPCHG_INIT and IPDCHG_INIT must not be programmed when AGC = 0.

²⁾ The FW MOSFET charge current is automatically determined when the FW MOSFET discharge current is selected (the FW MOSFET charge and discharge currents are set by the same control bits, [1]).

5 Calculation of the gate driver currents and timings

Table 7 Timing calculation with AGC = 0

Step	Parameters	Formula	–
6	Effective rise time	$t_{rise} = \frac{Q_{gd}}{ICHG}$	[0.6]
7	Effective fall time	$t_{fall} = \frac{Q_{gd}}{IDCHG}$	[0.7]
8	Turn-on delay time	$t_{don} = \frac{Q_{gs}}{ICHG} + t_{d_gdrv_on}$	[0.8]
9	Turn-off delay time	$t_{doff} = \frac{Q_g - Q_{gs} - Q_{gd}}{IDCHG} + t_{d_gdrv_off}$	[0.9]
10	FW turn-on time	$t_{on_fw} = \frac{C_{iss_0V} \times V_{gh}}{ICHG_FW} + t_{d_gdrv_on}$	[0.10]
11	FW turn-off time	$t_{off_fw} = \frac{C_{iss_0V} \times V_{gh}}{IDCHG_FW} + t_{d_gdrv_off}$	[0.11]
12	Active MOSFET blank time ³⁾	$t_{blank_active} = (t_{don} + t_{rise}) \times (1 + t_{margin})$	[0.12]
13	Active MOSFET CCP ⁴⁾ time	$t_{ccp_active} = \left(t_{doff} + t_{fall} + \frac{Q_{gs}}{IDCHG} \right) \times (1 + t_{margin})$	[0.13]
14	FW CCP time	$t_{ccp_fw} = t_{off_fw} \times (1 + t_{margin})$	[0.14]
15	FW blank time	$t_{blank_fw} = t_{on_fw} \times (1 + t_{margin})$	[0.15]

5.2 Calculation with precharge and predischage enabled (AGC = 1 or 2)

This section shows the formulas used to calculate the required gate driver settings based on the input parameters when AGC = 1 and AGC = 2.

For AGC = 1:

- the pre-charge phase is enabled. The MOSFET is charged with the current IPCHG_INIT during this phase
- the pre-discharge phase is enabled. The MOSFET is discharged with the current IPDCHG_INIT during this phase
- t_{don} and t_{doff} are not regulated by the TLE9185QX/TLE9185QXV33

For AGC = 2:

- t_{don} and t_{doff} are regulated by the TLE9185QX/TLE9185QXV33
- the pre-charge is enabled. The MOSFET is initially charged with the current IPCHG_INIT during this phase for the first PWM period. Then the device adapts IPCHG cycle-by-cycle
- the pre-discharge phase is enabled. The MOSFET is initially discharged with the current IPDCHG_INIT during this phase for the first PWM period. Then the device adapts IPDCHG cycle-by-cycle

³ If the MOSFET must have the full $R_{ds(on)}$ at the end of t_{blank_active} (i.e. $V_{gs} = V_{gh}$) and the postcharge phase is disabled, then [0.12] must be changed to: $t_{blank_active} = (t_{don} + t_{rise} + \frac{Q_g - Q_{gs} - Q_{gd}}{ICHG}) \times (1 + t_{margin})$.

⁴ Cross current protection

5 Calculation of the gate driver currents and timings

5.2.1 Calculation of gate driver currents with AGC = 1 or 2

Table 8 Calculation of gate driver currents with AGC = 1 or 2

Step	Parameters	Formula	-
1	Active MOSFET charge current	$ICHG = \frac{Q_{gd}}{t_{rise_target}}$	[1.1]
2	Active MOSFET discharge current	$IDCHG = \frac{Q_{gd}}{t_{fall_target}}$	[1.2]
3	Active MOSFET initial pre-charge current	$IPCHG_INIT = \frac{Q_g - (t_{don_min} - t_{d_gdrv_on} - t_{pchg}) \times ICHG}{t_{pchg}}$	[1.3]
4	Active MOSFET initial pre-discharge current	$IPDCHG_INIT = \frac{Q_g - Q_{gs} - Q_{gd} - (t_{doff_min} - t_{d_gdrv_off} - t_{pdchg}) \times ICHG}{t_{pdchg}}$	[1.4]
5	FW discharge current 5)	$IDCHG_FW = \frac{C_{iss_OV} \times V_{gh}}{t_{off_fw_target} - t_{d_gdrv_off}}$	[1.5]

The nearest available current must be selected. Refer to the datasheet rev. 1.0, Table 24 and Table 25, [1] and the corresponding datasheet.

Additional information to step 3:

Condition on IPCHG_max to ensure that the pre-charge phase is over before $V_{gs} = V_{gs_th}$:

$$IPCHG_INIT \leq IPCHG_max = \frac{V_{gs_th} \times C_{iss_vss}}{t_{pchg}}$$

The minimum allowed t_{don} (noted t_{don_min}), considering a margin ($t_{don_min_margin}$) is given by:

$$t_{don_min} = \frac{Q_g - t_{pchg} \times IPCHG_max}{ICHG} + t_{d_gdrv_on} + t_{pchg} + t_{don_min_margin}$$

Additional information to step 4:

Condition on IPDCHG_max to ensure that the pre-discharge phase is over before V_{gs} reaches $V_{plateau}$ at the turn-off of the active MOSFET:

$$IPDCHG_INIT \leq IPDCHG_max = \frac{Q_g - Q_{gs} - Q_{gd}}{t_{pdchg}}$$

The minimum allowed t_{doff} (noted t_{doff_min}), considering a margin ($t_{doff_min_margin}$) is given by:

$$t_{doff_min} = \frac{Q_g - Q_{gs} - Q_{gd} - t_{pdchg} \times IPDCHG_max}{IDCHG} + t_{d_gdrv_off} + t_{pdchg} + t_{doff_min_margin}$$

⁵ The FW MOSFET charge current is automatically determined when the FW MOSFET discharge current is selected (the FW MOSFET charge and discharge currents are set by the same control bits, [1] and the corresponding datasheet.)

5 Calculation of the gate driver currents and timings

5.2.2 Timing calculation with AGC = 2

Table 9 Timing calculation with AGC = 2

Step	Parameters [ns]	Formula	-
7	Effective rise time	$t_{rise} = \frac{Q_{gd}}{ICHG}$	[1.7]
8	Effective fall time	$t_{fall} = \frac{Q_{gd}}{IDCHG}$	[1.8]
9	Turn-on delay time	$t_{don} = \frac{Q_{gs} - t_{pchg} \times IPCHG_INIT}{ICHG} + t_{d_gdrv_on} + t_{pchg}$	[1.9]
10	Turn-off delay time	$t_{doff} = \frac{Q_g - Q_{gs} - Q_{gd} - t_{pdchg} \times IPDCHG_INIT}{IDCHG} + t_{d_gdrv_off} + t_{pdchg}$	[1.10]
11	FW turn-on time	$t_{on_fw} = \frac{C_{iss_0V} \times V_{gh}}{ICHG_FW} + t_{d_gdrv_on}$	[1.11]
12	FW turn-off time	$t_{off_fw} = \frac{C_{iss_0V} \times V_{gh}}{IDCHG_FW} + t_{d_gdrv_off}$	[1.12]
13	Active MOSFET blank time	$t_{blank_active} = (t_{don} + t_{rise}) \times (1 + t_{margin})$	[1.13]
14	Active MOSFET CCP ⁶⁾ time	$t_{ccp_active} = (t_{doff} + t_{fall}) \times (1 + t_{margin})$	[1.14]
15	FW CCP time	$t_{ccp_fw} = t_{off_fw} \times (1 + t_{margin})$	[1.15]
16	FW blank time	$t_{blank_fw} = t_{on_fw} \times (1 + t_{margin})$	[1.16]

⁶ Cross current protection

6 Adaption of the gate charges to the application conditions

6 Adaption of the gate charges to the application conditions

The MOSFET Q_{gs} , Q_{gd} and Q_g are specified for specific conditions. Refer to [Figure 9](#): IPZ40N04S5-3R1:

$V_s = 32\text{ V}$, V_{gs} from 0 to 10 V and $I_{ds} = 40\text{ A}$.

However, the value of the gate charge depends on the supply voltage, the load current ([\[2\]](#) [\[3\]](#)), and V_{gh} for the TLE9185QX/TLE9185QXV33.

6.1 Adaption of Q_{gs} (at $V_{ds} = V_s$)

During the turn-on of the active MOSFET until $V_{gs} = V_{plateau}$, the current delivered by the gate driver charges C_{iss} . Therefore the charge injected in the MOSFET gate until V_{gs} reaches $V_{plateau}$ is equal to $C_{iss_vs} \times V_{plateau}$:

$$Q_{gs} \text{ (at } V_{ds} = V_s) = C_{iss_vs} \times V_{plateau}$$

Example: $V_s = 14\text{ V}$, $V_{plateau} = 4.2\text{ V}$

$$C_{iss_vs} \sim 1740\text{ pF}$$

$$Q_{gs} = 1740 \times 10^{-12} \times 4.2 \sim 7.3\text{ nC}$$

6.2 Adaption of Q_{gd} (at $V_{ds} = V_s$)

An estimation of Q_{gd} consist in using Q_{gd_typ} and subtracting the gate charge related to C_{rss} between V_{dd_typ} and $V_{ds} = V_s$ ([\[2\]](#) [\[3\]](#)). The gate charge difference is represented by the highlighted area in [Figure 15](#).

Approximating this area to a trapezoid, gives $Q_{gd_typ} - Q_{gd} \sim (C_{rss_vs} + C_{rss_typ}) \times (V_{dd_typ} - V_s) / 2$.

$$Q_{gd} = Q_{gd_typ} - (C_{rss_vs} + C_{rss_typ}) \times (V_{dd_typ} - V_s) / 2.$$

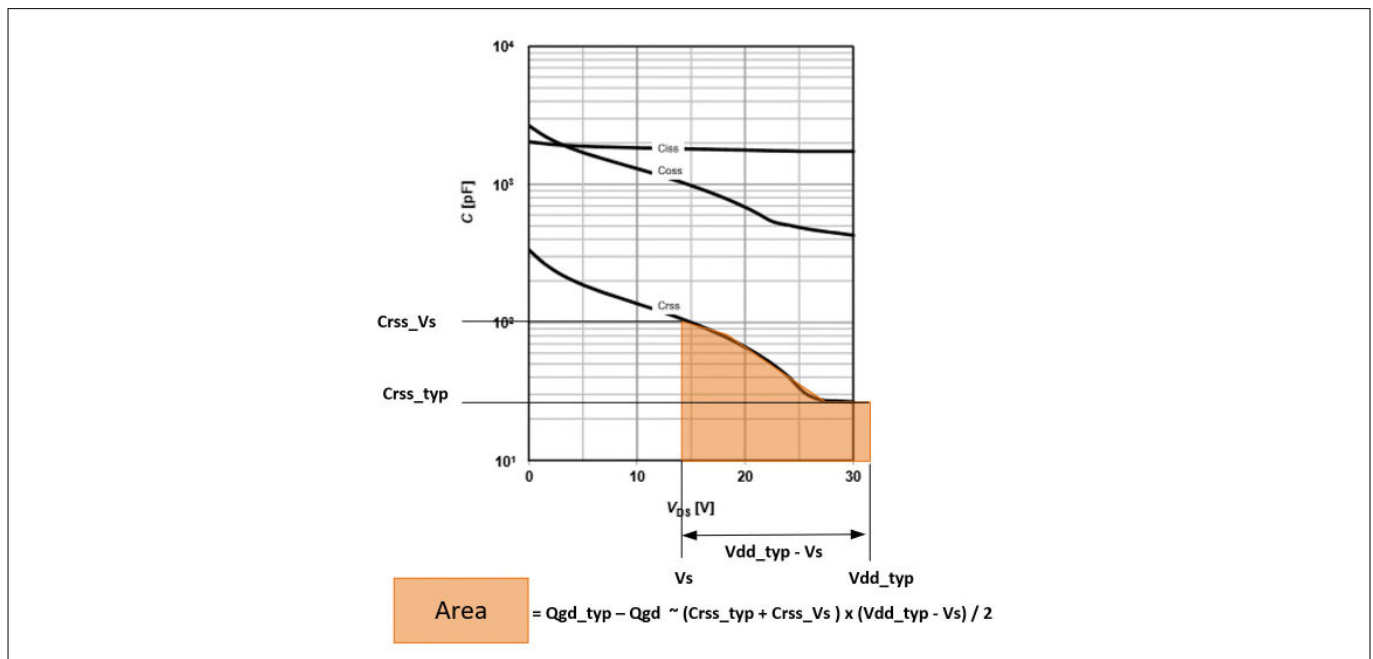


Figure 15 Estimation of the difference between Q_{gd_typ} and Q_{ds}

Example: MOSFET IPZ40N04S5-3R1, $V_s = 14\text{ V}$, $V_{dd_typ} = 32\text{ V}$

$$C_{rss_vs} = 100\text{ pF}, C_{rss_typ} \sim 27\text{ pF}, Q_{gd_typ} = 7.1\text{ nC}$$

$$Q_{gd} = 7.1 \times 10^{-9} - (100 + 27) \times 10^{-12} \times (32 - 14) / 2 \sim 6.0\text{ nC}$$

6 Adaption of the gate charges to the application conditions

6.3 Adaption of Q_g at ($V_{ds} = V_s$) for the active MOSFET

During the turn-on phase of the active MOSFET, the remaining charge delivered by the MOSFET driver between the end of the Miller plateau and $V_{gs} = V_{gh}$ represents the charge required to charge C_{iss_0v} from $V_{plateau}$ to V_{gh} .

$$Q_g - Q_{gd} - Q_{gs} = C_{iss_0v} \times (V_{gh} - V_{plateau})$$

$$Q_g = C_{iss_0v} \times (V_{gh} - V_{plateau})$$

Where C_{iss_0v} is the MOSFET input capacitance with V_{ds} close to 0 V.

This parameter is not directly provided in the MOSFET datasheets. It is the inverse slope of the graph V_{gs} versus gate charge (Figure 16).

$$C_{iss_0v} = (Q_{g_typ} - Q_{gs_typ} - Q_{gd_typ}) / (V_{gh_typ} - V_{plateau_typ})$$

$$Q_g = Q_{gd} + Q_{gs} + C_{iss_0v} \times (V_{gh} - V_{plateau})$$

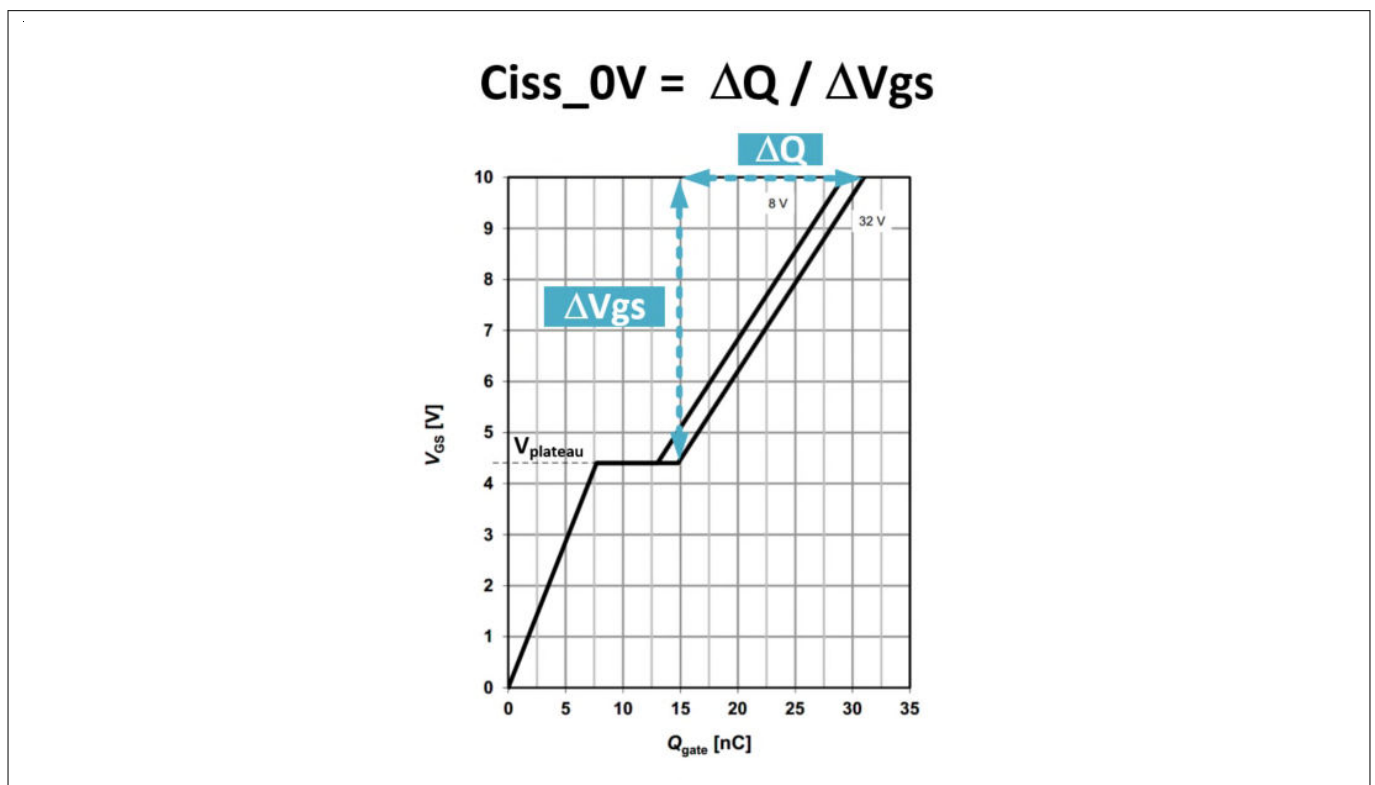


Figure 16 Determination of C_{iss_0v} (IPZ40N04S5-3R1)

Example:

MOSFET IPZ40N04S5-3R1, $V_s = 14$ V,

$V_{gh_typ} = 10$ V, $V_{gh} = 11.5$ V (low-side PWM or high-side PWM with FET_LVL = 0)

$Q_{gs_typ} = 7.7$ nC, $Q_{gd_typ} = 7.1$ nC, $Q_{g_typ} = 31$ nC

$V_{plateau_typ} = 4.4$ V, $V_{plateau} = 4.2$ V

In 6.1 and 6.2, we have seen that $Q_{gs} = 7.3$ nC, $Q_{gd} = 6.0$ nC

$$C_{iss_0v} = \frac{(31 - 7.1 - 7.7) \times 10^{-9}}{(10 - 4.4)} = 2.89 \text{ nF}$$

$$Q_g = 7.3 \times 10^{-9} + 6.0 \times 10^{-9} + 2.89 \times 10^{-9} \times (11.5 - 4.2) \sim 34.4 \text{ nC}$$

7 Conclusions

This application note provides recommendations for the setting of the gate driver of the TLE9185QX/TLE9185QXV33 in PWM operation. It also gives step-by-step calculation details used by the gate driver setting tool for the determination of the MOSFET driver currents and timings and the resulting MOSFET switching times, for an open-loop control.

However, the MOSFET switching times are dependent on the application conditions (e.g. current, voltage timings) and subject to the production spread of the MOSFET and the Muti-MOSFET driver itself.

To overcome the limitations of an open-loop control, the TLE9185QX/TLE9185QXV33 also integrates features which allow a closed-loop regulation of the switching times:

- a self-regulation of t_{don} and t_{doff} can be done by the TLE9185QX/TLE9185QXV33
- a closed loop regulation of t_{rise} and t_{fall} can be done by the microcontroller thanks to measured in-application switching times provided by the TLE9185QX/TLE9185QXV33. The principle is described in the application note [\[2\]](#).

8 References

- [1] Datasheet TLE9185QX/TLE9185QXV33, [Link](#)
- [2] Rise and fall time regulation with current source MOSFET drivers, [Link](#)
- [3] AND9083. MOSFET gate charge origin and its applications, [Link](#)
- [4] Datasheet IPZ40N04S5-3R1, [Link](#)

Revision history

Document version	Date of release	Description of changes
V 1.0	2022-06-03	<ul style="list-style-type: none">First release

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Edition 2022-06-03

Published by

Infineon Technologies AG
81726 Munich, Germany

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Document reference
IFX-oyb1652866212485

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