SSO8 Package Thermal Data Sheet

PG-TDSON-8-33/34/43/53

About this document

Scope and purpose

This document aims at providing information about the thermal characteristics of Infineon's SSO8 packages PG-TDSON-8-33/34/43/53, used for Infineon MOSFETs (Grade-0). The document contains details regarding dimensions, package outline, products involved, and a detailed overview on the thermal resistance characteristics of the package. Please refer to the thermal resistance document if you need more information on thermal resistance calculation and background.

Intended audience

This document is intended for engineers who would like to have information of the thermal characteristics of the package used, and the products making use of it.

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1 Package Dimensions

Figure 1 depicts s the basic package of this application note. On the left the outline of the package is given with all dimensions in mm. On the right the internal package construction with clip, leadframe and solder thickness is shown.

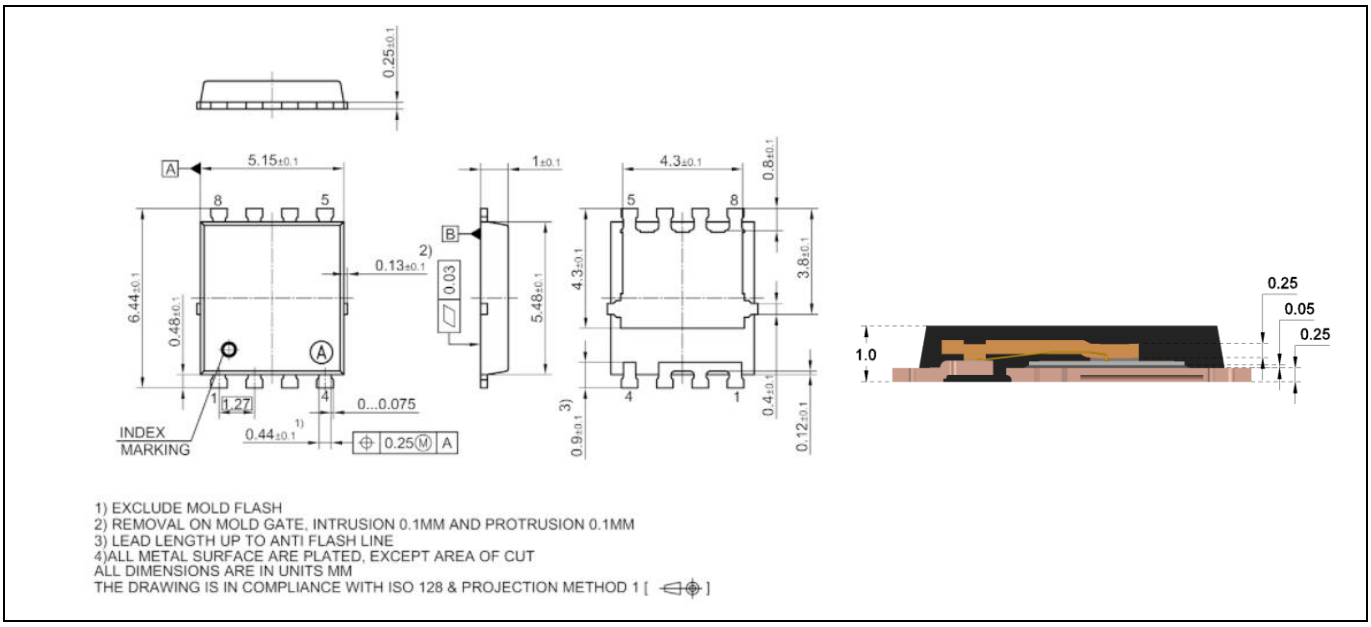

Figure 1 Package outline drawing with dimensions

Figure 2 shows the 3D view of the TDSON with and without mold. The clip, die and gate bond wire can be seen.

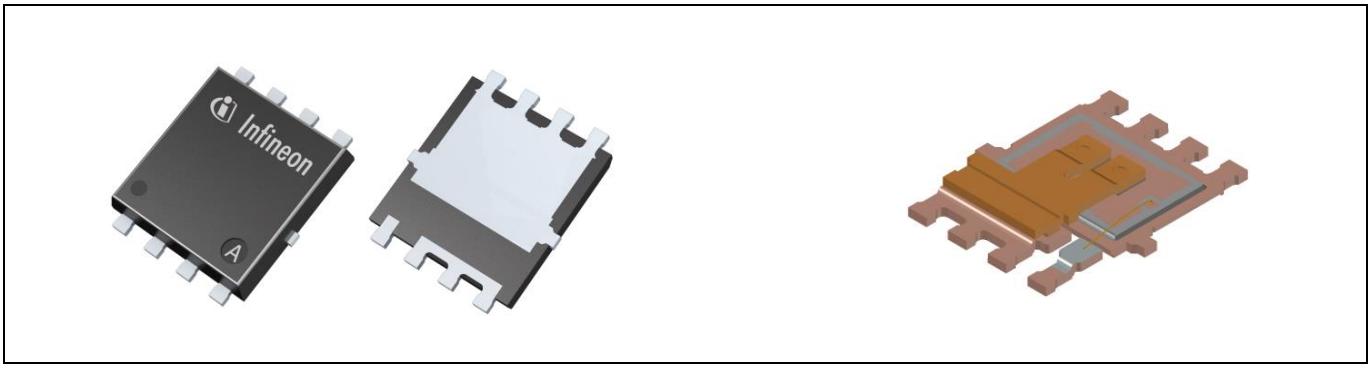

Figure 2 3D view of the package with and without mold

The footprint drawing in figure 3 specifies the dimensions for the copper pads on the PCB (left) as well as the stencil mask for the solder paste (right). This is the recommended footprint by Infineon. An adaption of the footprint may be required by special application requirements and/or specific assembly processes.

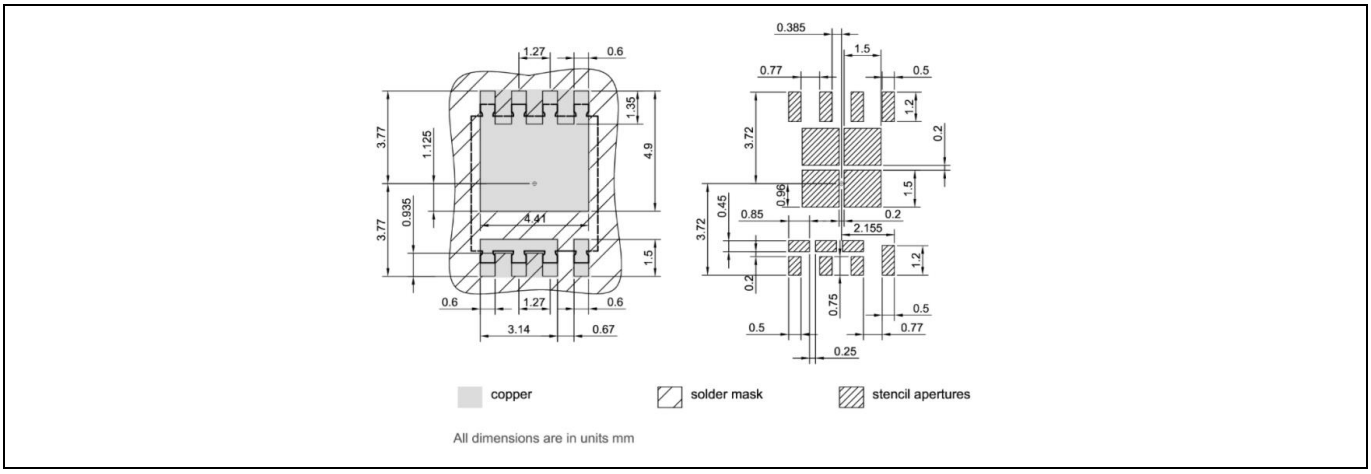

Figure 3 Footprint

General recommendations on board assembly related topics can be found in the application note: General Board Assembly Recommendations

2 List of related products in PG-TDSON-8-33/34/43/53

Table 1 below provides a list of available products from Infineon's OptiMOS™ 6 family in the package versions at the time this document was published.

Table 1 Product list of the related package

Package variant	List of products	Note
PG-TDSON-8-33	IAUC100N04S6L020, IAUC100N04S6N022 IAUC100N04S6L025, IAUC100N04S6N028 IAUC80N04S6L032, IAUC80N04S6N036 IAUC60N04S6L039, IAUC60N04S6N044	Highest R_{DSON}
PG-TDSON-8-34	IAUC120N04S6L009, IAUC120N04S6N010 IAUC120N04S6L012, IAUC120N04S6N013 IAUC100N04S6L014, IAUC100N04S6N015	
PG-TDSON-8-43	IAUC120N04S6L008 IAUC120N04S6N009	
PG-TDSON-8-53	IAUC120N04S6N006 IAUC120N04S6L005	Lowest R_{DSON}

3 Thermal Resistance Definition

The package thermal resistance is the measure of a package'scapability to dissipate heat from the die's active surface (junction) to a specified reference point (case, pin, ambient, etc.). The value of thermal resistance depends on many factors, such as applied power, ambient temperature, PCB board used and much more. This chapter describes in detail boundary conditions we use in the definition of various thermal resistances.

The thermal resistance is divided into two groups: junction-to-case thermal resistance (package only) and junction-to-ambient thermal resistance (package with PCB and housing) as seen in Figure 4 below.

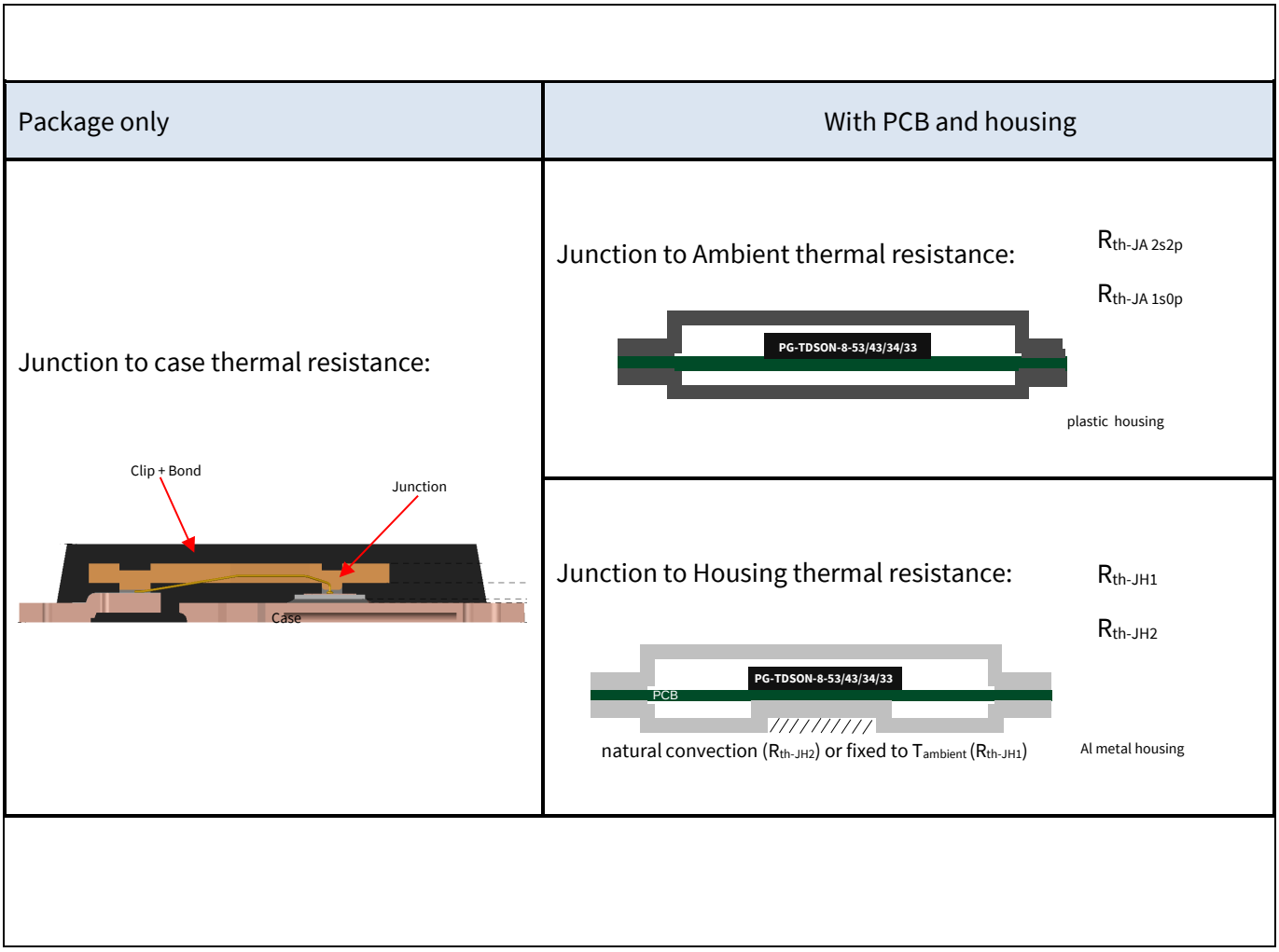

Figure 4 Boundary conditions for thermal resistance definition

3.1 Package only (Junction-to-case thermal resistance $R_{th\text{-}JC}$)

The backside of the exposed pad is fixed to $T_{ambient}$. The other side of the package has an adiabatic boundry condition.

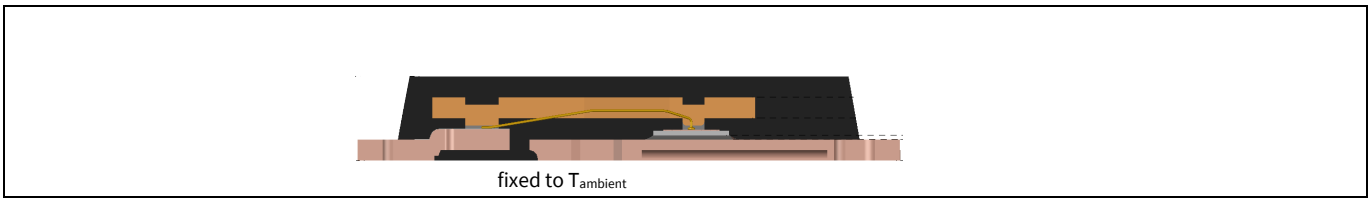

Figure 5 Package only

3.2 With PCB and housing

3.2.1 Junction-to-ambient thermal resistance ($R_{th\text{-}JA\ 1s0p}$)

- PCB construction is according to JEDEC standards 1s0p, without thermal vias (Figure 6) Copper areas can vary in size e.g. 600 or 1000mm^2; see Figure 7.
- Natural Convection

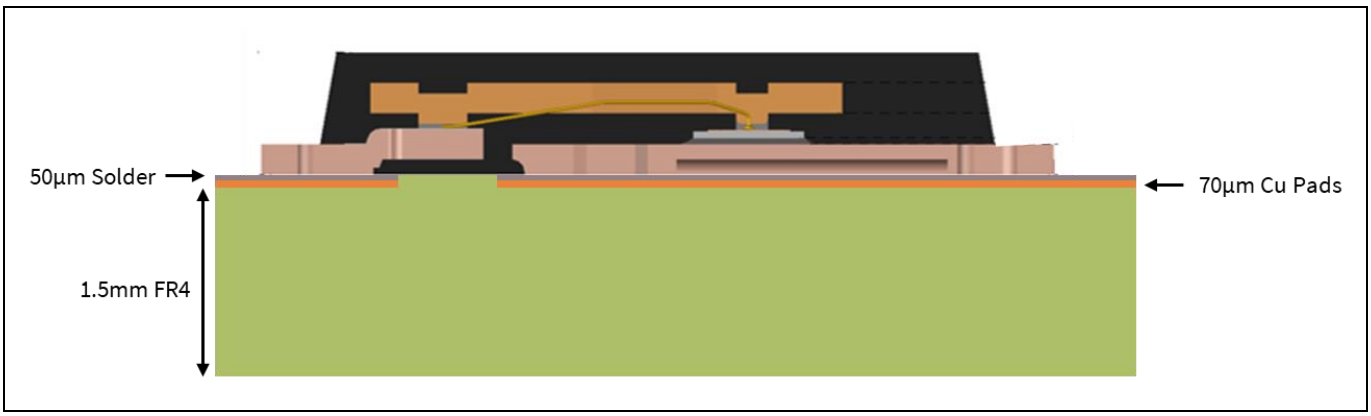

Figure 6 Package on JEDEC 1s0p board

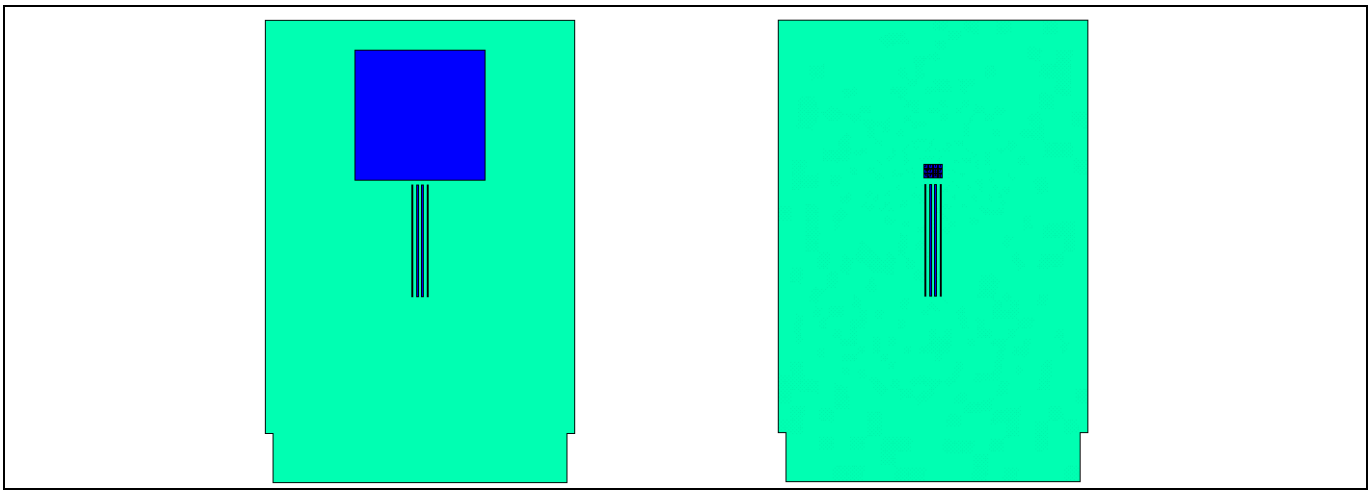

Figure 7 Top view on board with 1s0p 1000mm^2 copper area (left side) and 1s0p footprint only (right side)

3.2.2 Junction-to-ambient thermal resistance ($R_{th\text{-}JA\ 2s2p}$)

- A JEDEC (Joint Electron Device Engineering Council) board is used for thermal assessment. PCB construction is according to JEDEC standards 2s2p, with thermal vias as seen in Figure 8.
- PCB size – 74 mm * 116 mm * 1.5 mm
- Number of thermal vias – 12. Thermal vias are connected to only one Cu inner layer
- Natural Convection

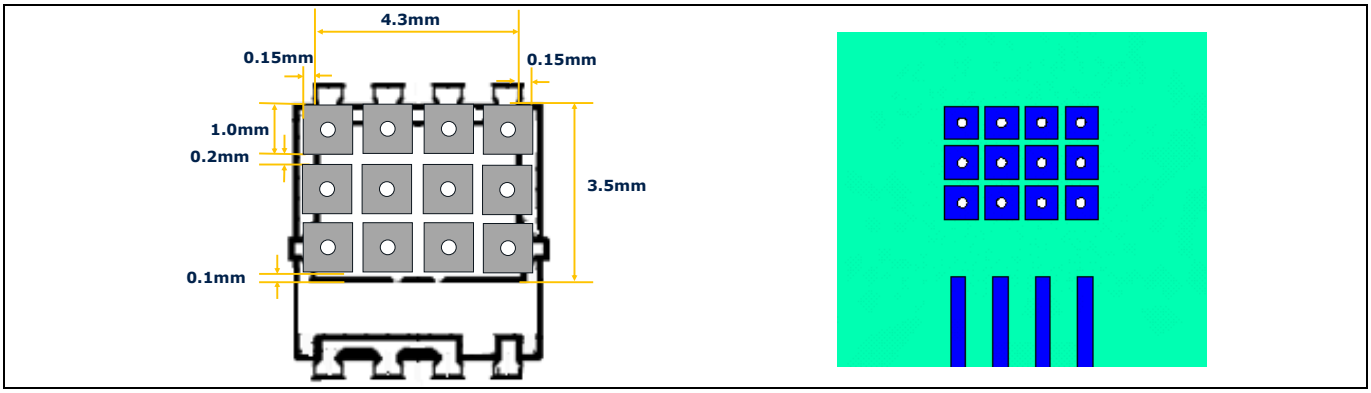

Figure 8 12 JEDEC thermal vias with dimensions (left side) and detailed top view of board (right side)

Note: Thermal vias are only used for multi layer boards such as JEDEC 2s2p. For boards like JEDEC 1s0p it is not applicable as there is no bottom metal layer.

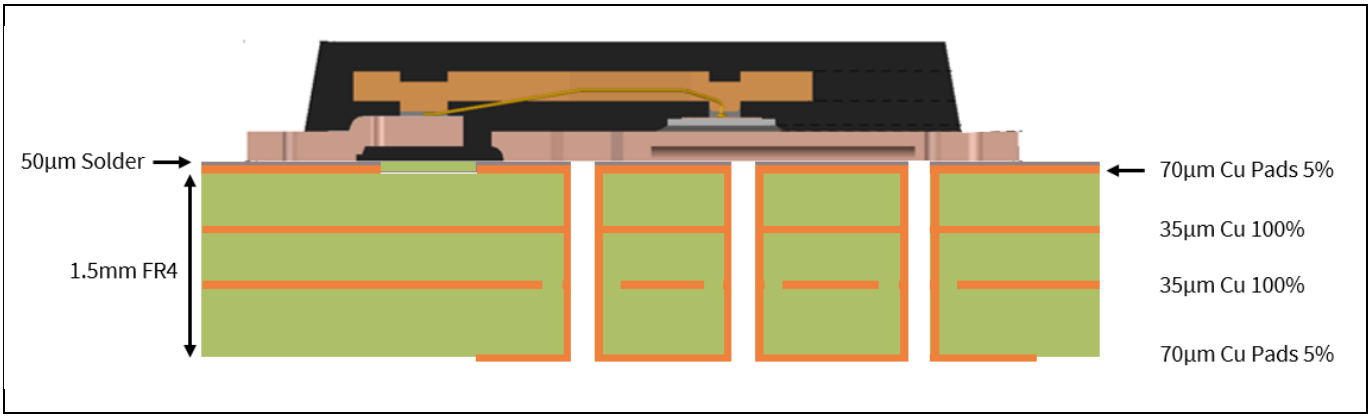

Figure 9 Package on JEDEC 2s2p board

3.2.3 Junction-to-housing thermal resistance ($R_{th\text{-}JH1}$)

- The backside of the housing is fixed to Tambient
- PCB construction is according to JEDEC standards 2s2p with thermal vias as above for $Z_{th\text{-}JA\ 2s2p}$)
- TIM (100µm, 0,7W/mK, X and Y size is double of the package size)
- Housing: 2mm thick, X and Y the same as JEDEC 2s2p board, 92W/mK (alloy name: ADC12)

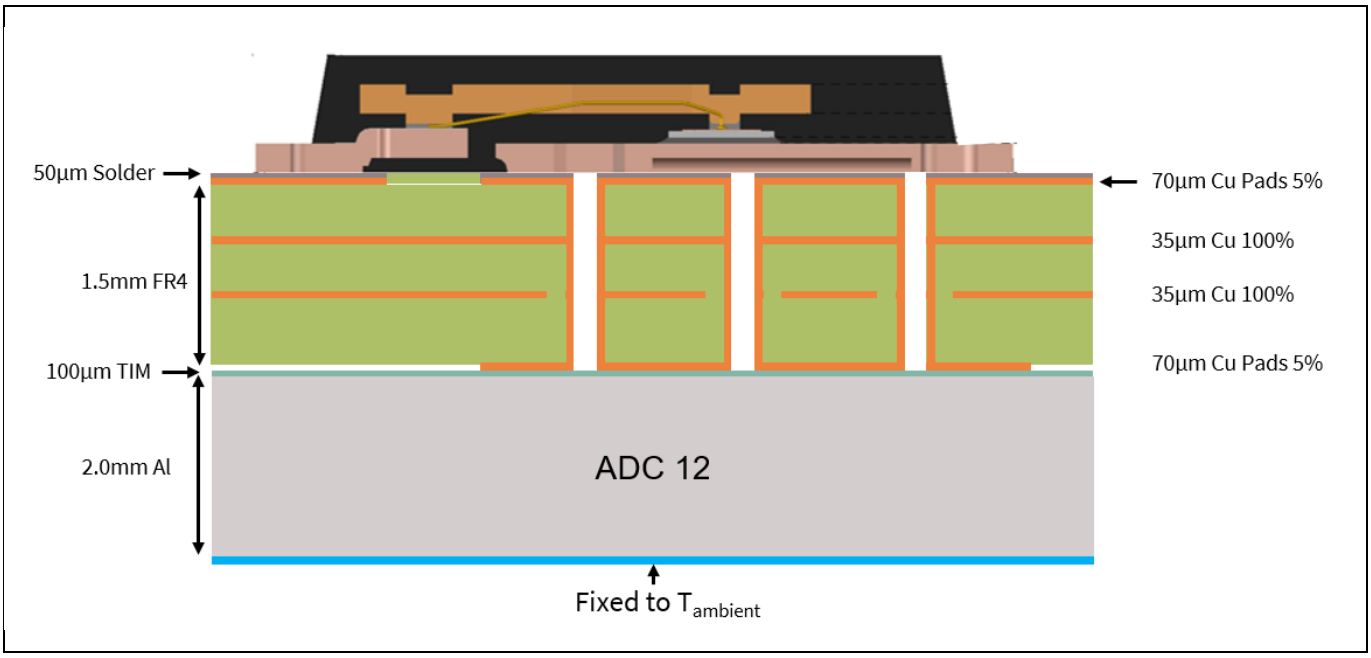

Figure 10 JEDEC 2s2p board in metal housing (fixed $T_{ambient}$)

3.2.4 Junction-to-housing thermal resistance ($R_{th\text{-}JH2}$)

- The backside of the housing has natural convection
- PCB construction is according to JEDEC standards 2s2p, with thermal vias as above for $R_{th\text{-}JA\ 2s2p}$
- TIM (100µm, 0,7W/mK, X and Y size is double of the package size)
- Housing: 2mm thick, X and Y the same as JEDEC 2s2p board, 92W/mK (alloy name: ADC12)

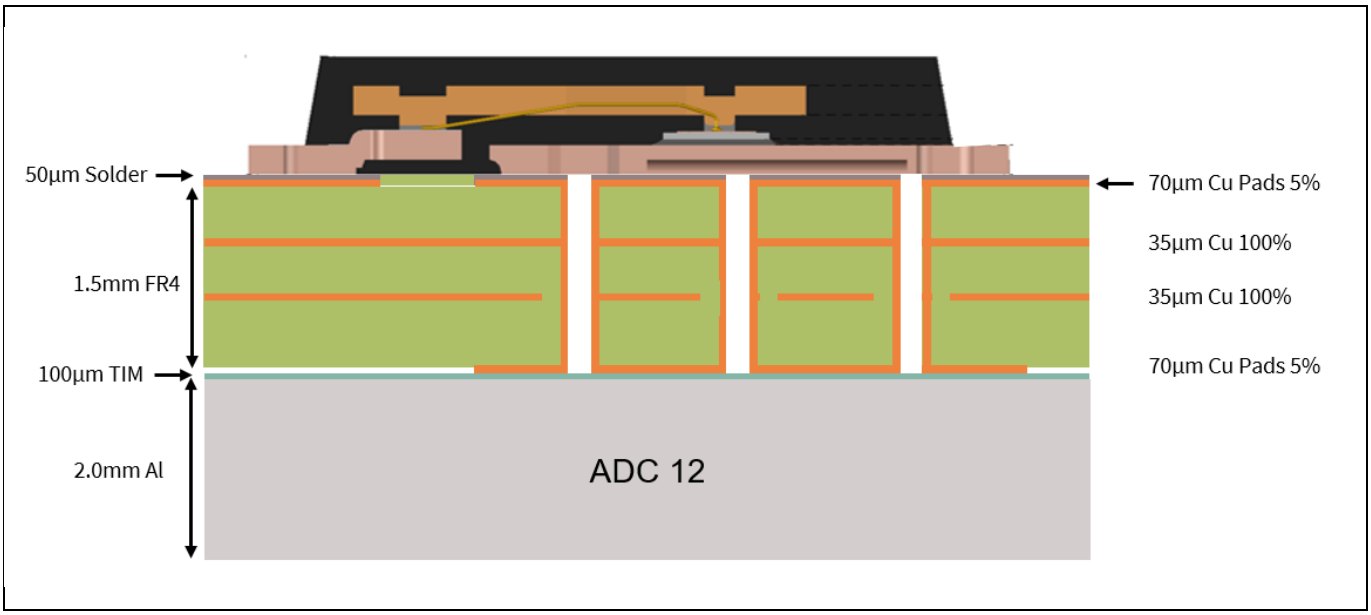

Figure 11 JEDEC 2s2p board in metal housing (natural convection)

3.2.5 Junction-to-housing thermal resistance with IMS board ($R_{th\text{-}JH1\ IMS}$)

- The backside of the housing is fixed to Tambient
- PCB construction is IMS board (Al is 1100H14)

- TIM (100µm, 0,7W/mK, X and Y size is double of the package size)
- Housing: 2mm thick, X and Y the same as JEDEC 2s2p board, 92W/mK (alloy name: ADC12)

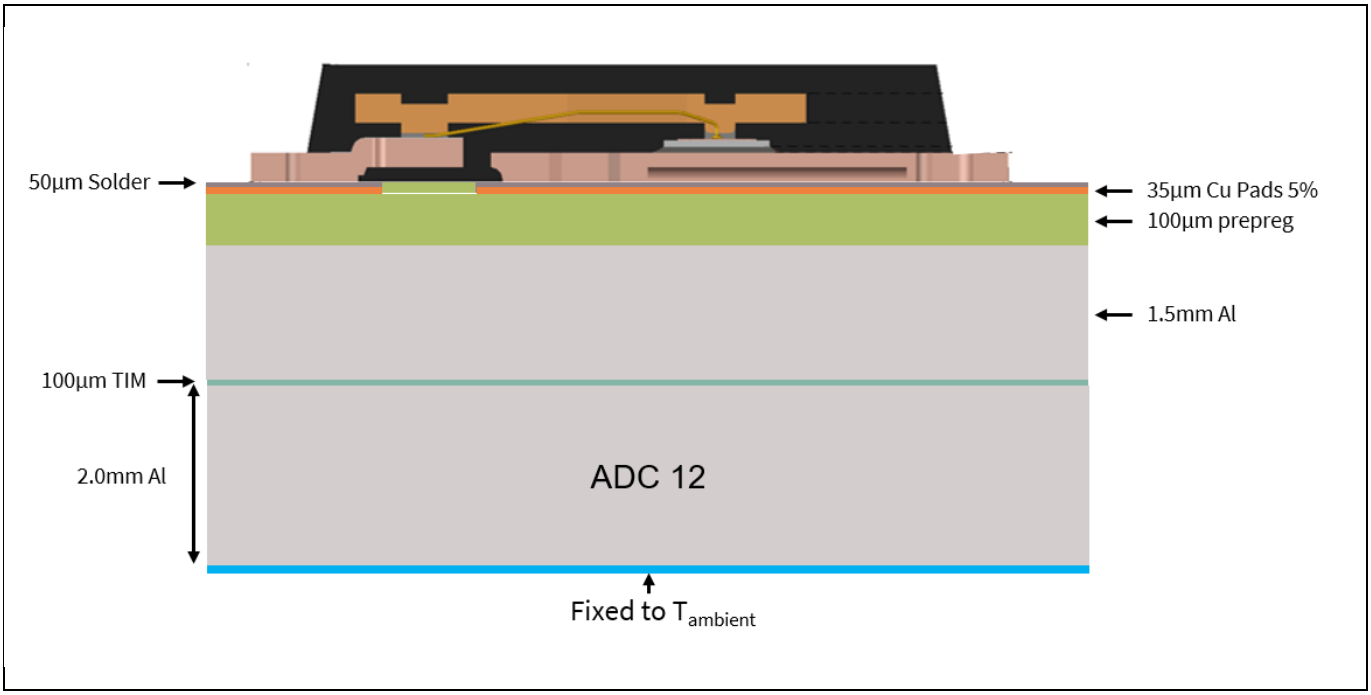

Figure 12 IMS board in metal housing (fixed $T_{ambient}$)

3.2.6 Junction-to-housing thermal resistance with IMS board ($R_{th\text{-}JH2\ IMS}$)

- The backside of the housing has natural convection
- PCB construction is IMS board (Al is 1100H14)
- TIM (100µm, 0,7W/mK, X and Y size is double of the package size)
- Housing: 2mm thick, X and Y the same as JEDEC 2s2p board, 92W/mK (alloy name: ADC12)

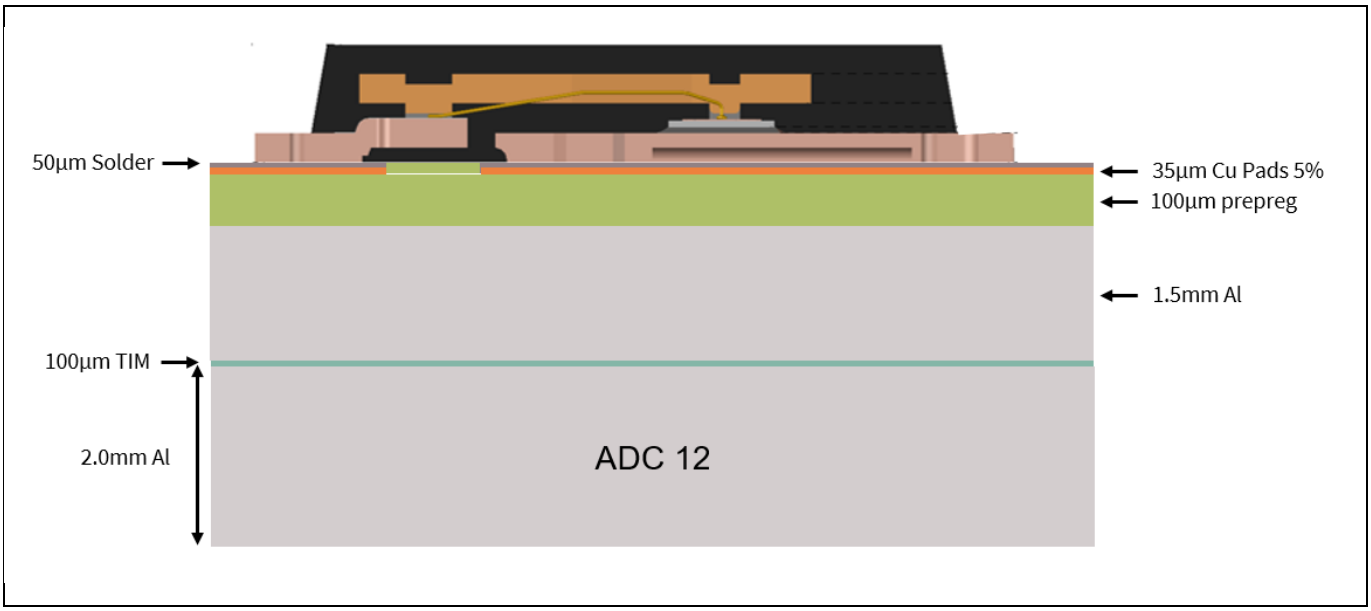

Figure 13 IMS board in metal housing (natural convection)

4 Thermal Characteristics

4.1 Thermal Impedance

The typical transient thermal impedance for products IAUC120N04S6N006 and IAUC60N04S6N044 can be seen in Figures 14 through 17 below according to the boundary conditions described in chapter 3. The results from these products with the largest and smallest silicon die show the typical range of values covering the product family. Chapter 4.2 provides a method for interpolating between the products family.

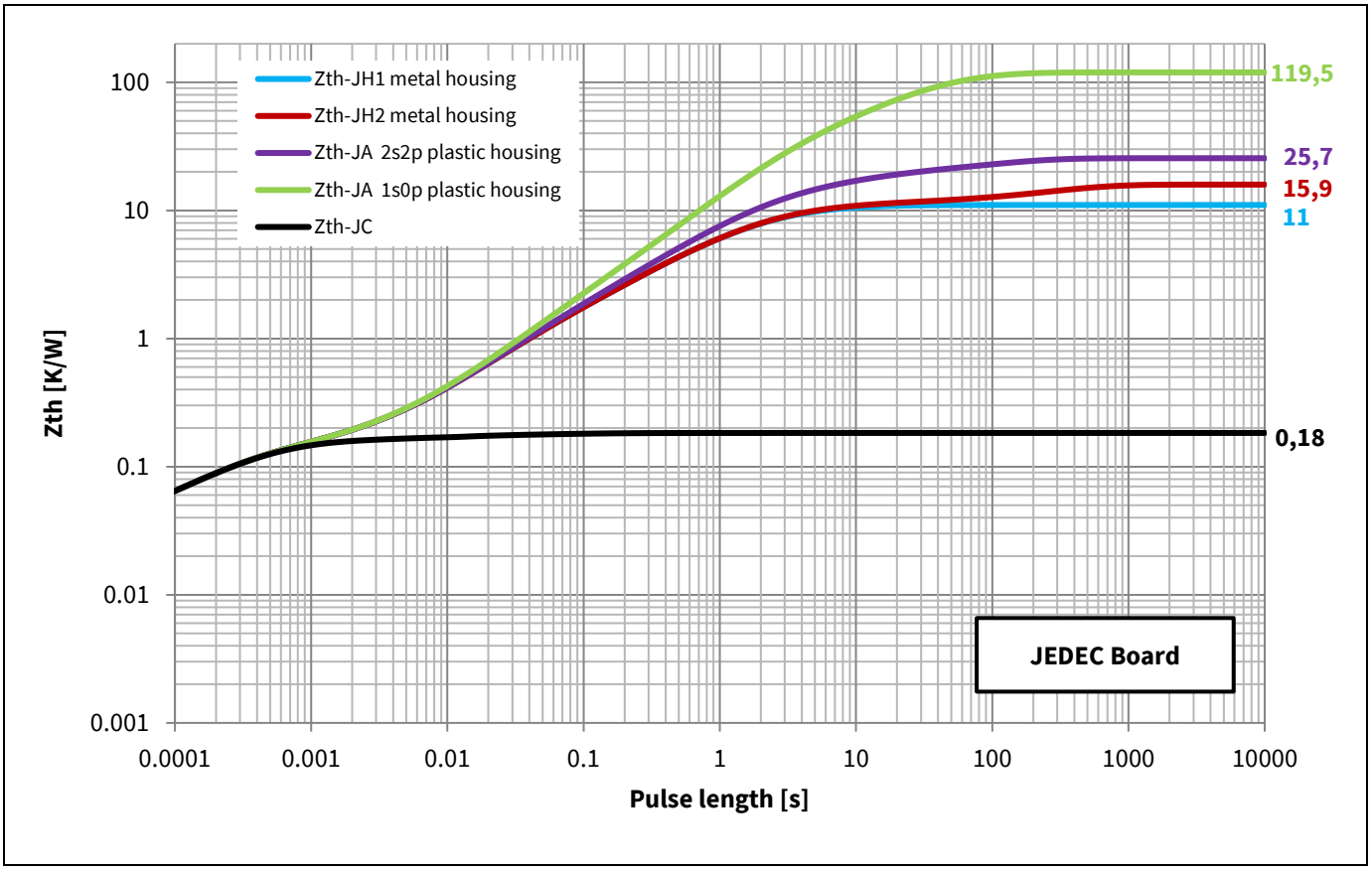

Figure 14 Thermal impedance for IAUC120N04S6N006

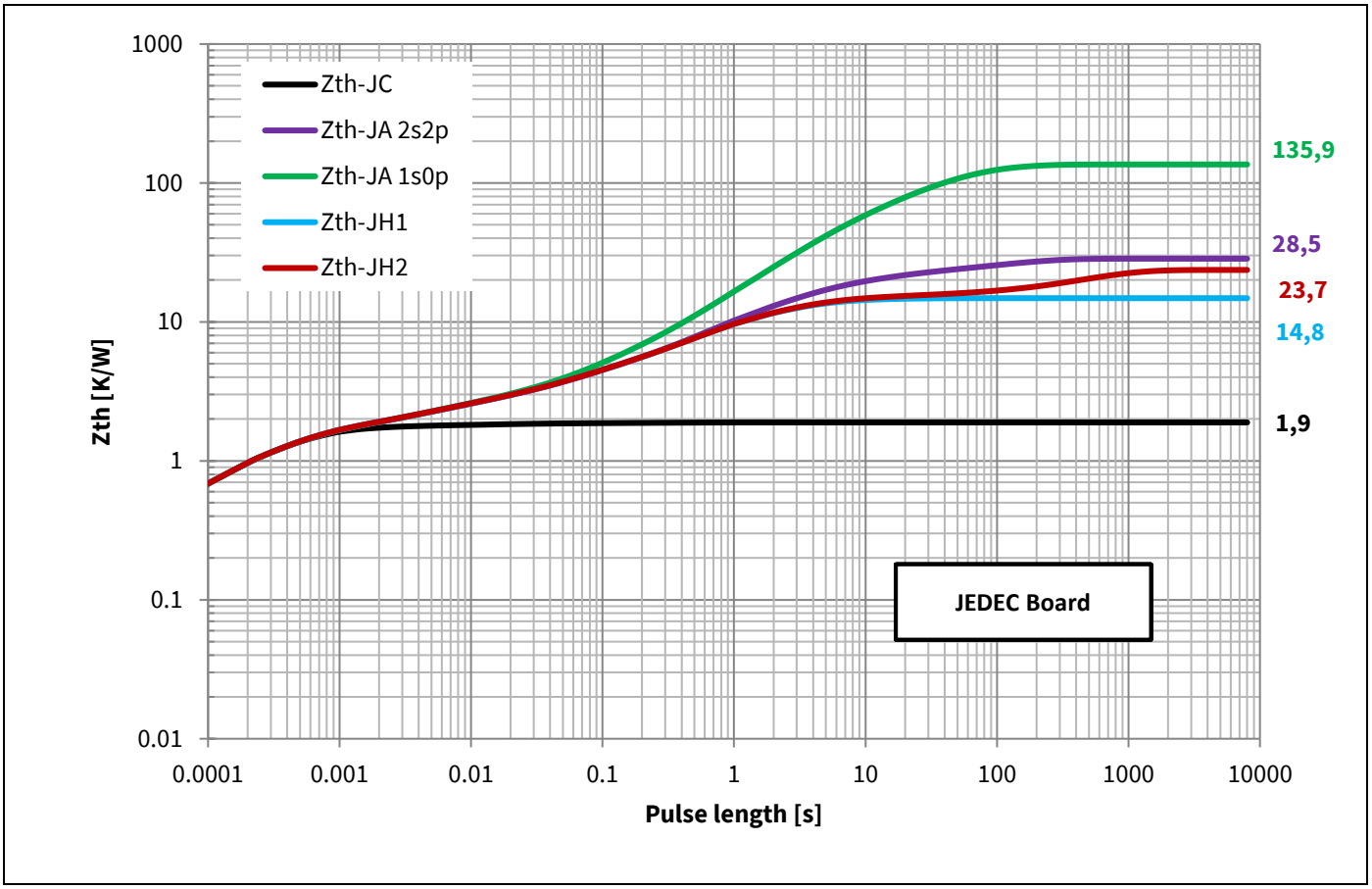

Figure 15 Thermal impedance for IAUC60N04S6N044 (same as IAUC60N04S6L039, IPC50N04S5-5R8)

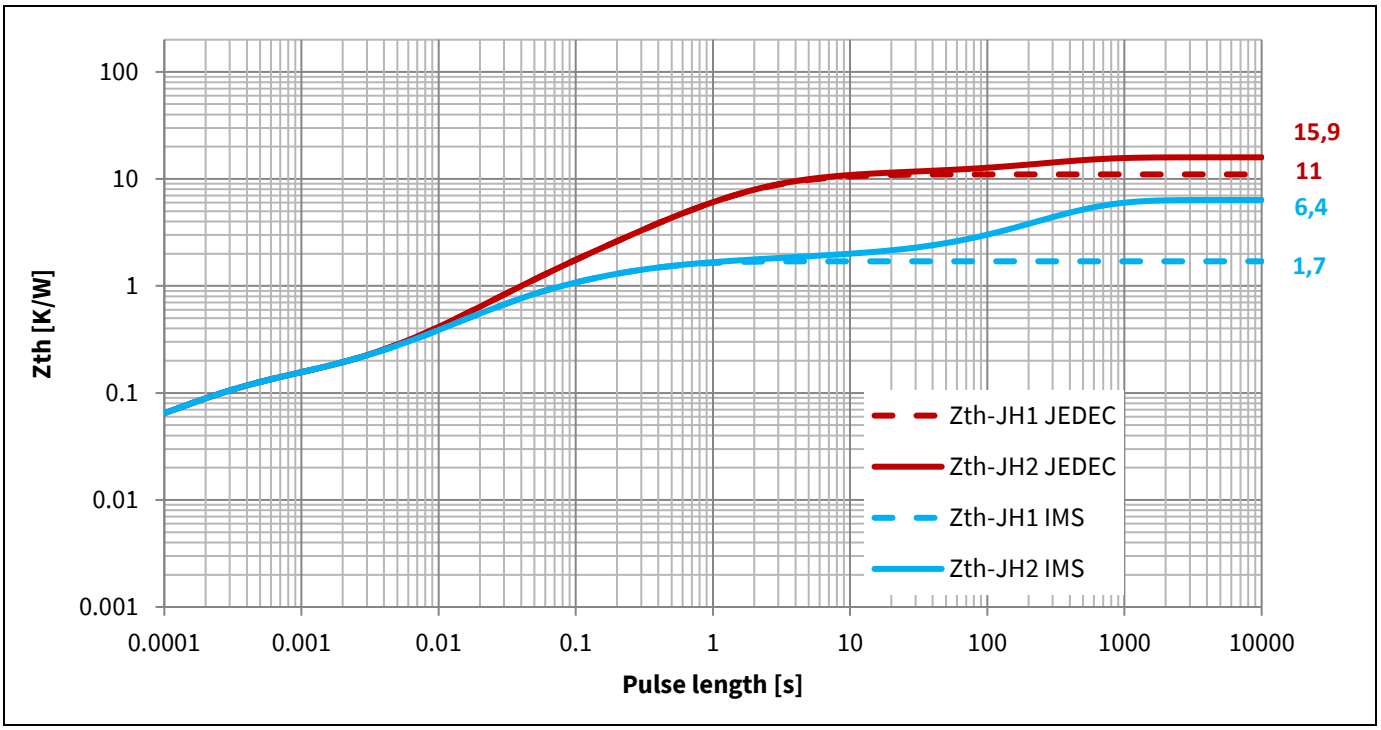

Figure 16 Metal housing board comparison between 2s2p JEDEC & IMS with IAUC120N04S6N006

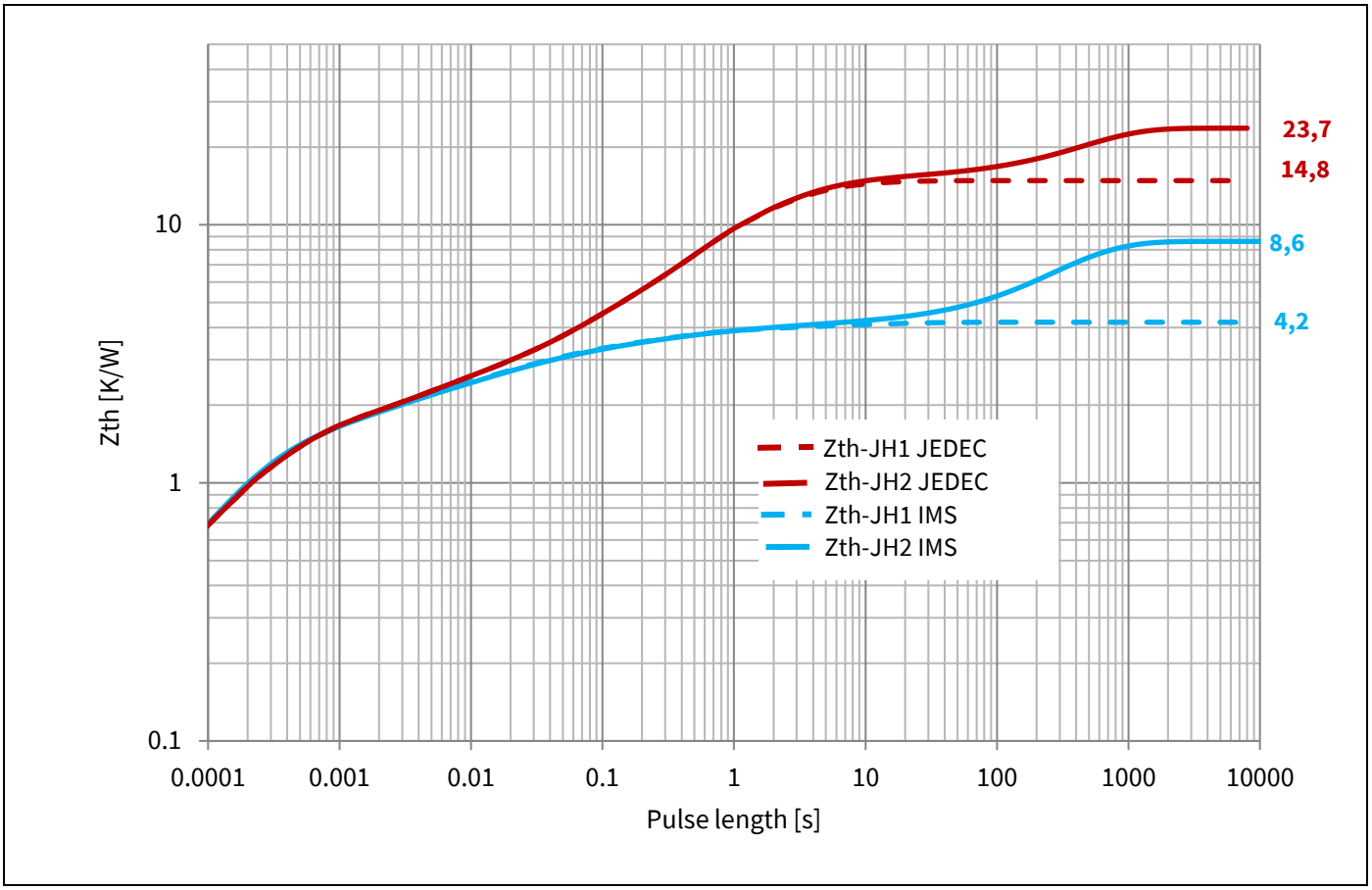

Figure 17 Metal housing board comparison between 2s2p JEDEC & IMS with IAUC60N04S6N044

4.2 Thermal resistance interpolation

As can be seen in section 4.1 the RDSON of the product correlates to its transient thermal impedance. For the same technology, the RDSON value is defined by the size of the silicon die. A larger RDSON, such as the IAUC60N04S6N044 with 4.4mOHm, corresponds to a smaller die and therefore a larger transient thermal impedance when compared to the IAUC120N04S6N006 with 0.6mOhm. Since many products are available in the package, it is useful to interpolate between the largest and smallest dies to estimate the performance of other products from the same family. The formulas provided below can be used for evaluating other products in the same package. As the thermal resistance is taken from the data sheet value (R_{thJC}) it can be used across different technologies (e.g. OptiMOS™ 6 or 5). Please recognize that the thermal resistance was split into a package part (R_{thJC}) and a board level/ ambient part (R_{thCA} or R_{thCHx}, see table 2). By that it becomes easier in use and from the thermal flow perpesctive a change in die size is inside the package and deviations in ambient are averaged. Also note that interpolation between typical values will not result in a typical value for the target device as accuracy is lost in the process and the resulting values should be used as guidelines to select a target device followed by a more robust analysis with available tools.

See below an example for the R_{thC} from data sheet:

IAUC60N04S6N044

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Thermal characteristics[2]						
Thermal resistance, junction - case	R_{thJC}	-	-	-	3.6	K/W
Thermal resistance, junction - ambient	R_{thJA}	6 cm² cooling area[3]	-	-	50	

Figure 18 R_{thJC} from data sheet

Please recognize that this maximum value is already the worst case thermal value of the package, e.g. it gives a good picture whether the device will be a good fit over lifetime.

To get the final R_{thJA} value for your desired application environment you need to add the values from table 2

$R_{th\text{-}JA\text{-}1s0p} = R_{thJC} + R_{th\text{-}CA\text{-}1s0p}$

$R_{th\text{-}JA\text{-}2s2p} = R_{thJC} + R_{th\text{-}CA\text{-}2s2p}$

$R_{th\text{-}JH1\text{-}JEDEC} = R_{thJC} + R_{th\text{-}CH1\text{-}JEDEC}$

$R_{th\text{-}JH2\text{-}JEDEC} = R_{thJC} + R_{th\text{-}CH2\text{-}JEDEC}$

$R_{th\text{-}JH1\text{-}IMS} = R_{thJC} + R_{th\text{-}CH1\text{-}IMS}$

$R_{th\text{-}JH2\text{-}IMS} = R_{thJC} + R_{th\text{-}CH2\text{-}IMS}$

Table 2 Thermal resistance case to ambient

$R_{th\text{-}CA\text{-}1s0p}$	$R_{th\text{-}CA\text{-}2s2p}$	$R_{th\text{-}CH1\text{-}JEDEC}$	$R_{th\text{-}CH2\text{-}JEDEC}$	$R_{th\text{-}CH1\text{-}IMS}$	$R_{th\text{-}CH2\text{-}IMS}$
127.8	26.0	11.9	16.9	1.9	6.4

Glossary

- R_{th}: Thermal Resistance
- Z_{th}: Thermal Impedance
- $T_{ambient}$: Ambient Temperature
- JEDEC: Joint Electron Device Engineering Council
- PCB: Printed Circuit Board
- 2s2p: JEDEC standard two internal copper planes embedded in the circuit board and the trace layer on the top surface of the PCB, ‘s’ refers to the signal layers on both outside surfaces of the board and ‘p’ refers to two power planes in the board (voltage and ground)
- 1s0p: JEDEC standard no internal copper planes embedded in the circuit board and the trace layer on the top surface of the PCB
- ADC: Aluminium Alloy Die Casting
- TIM: Thermal Interface Material
- RDSON: Drain-Source Resistance in ON state (V_{GS} = 10V) of the MOSFET

References

[1] Thermal Resistance Theory and Pactice reference document on the thermal resistance

Revision history

Document version	Date of release	Description of changes
V 1.0	16-02-2022	Final release

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