LITIX™ Power Flex TLD5190

Voltage regulator in buck-boost topology

About this document

This document explains how to design a voltage regulator using the Infineon TLD5190 4-switch buck-boost controller for a powerful and efficient design. The application used as example is a voltage regulator with 12 V, 4 A at the output connected to a 12 V automotive battery power supply.

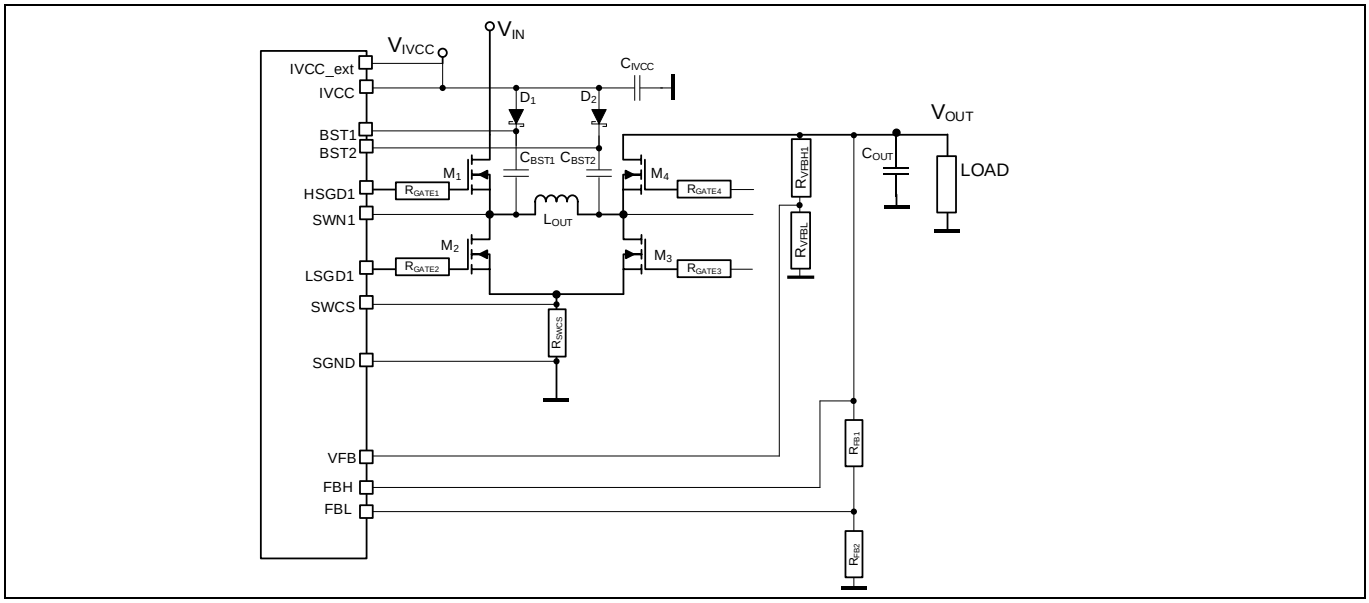

Figure 1 LITIX™ 4-switch buck-boost controller as voltage regulator

Intended audience

HW designers

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1 Introduction

This document explains how to size all TLD5190 external components for a specific constant voltage application.

It is possible to use the *TLD5190 TLD5541-1 LED Component calculator* [1] available on the Infineon TLD5190 webpage [2]. Even if this excel tool is designed for LED drivers, many TLD5190 external components for voltage applications (for example, overvoltage and overcurrent resistor dividers) can be calculated with this tool.

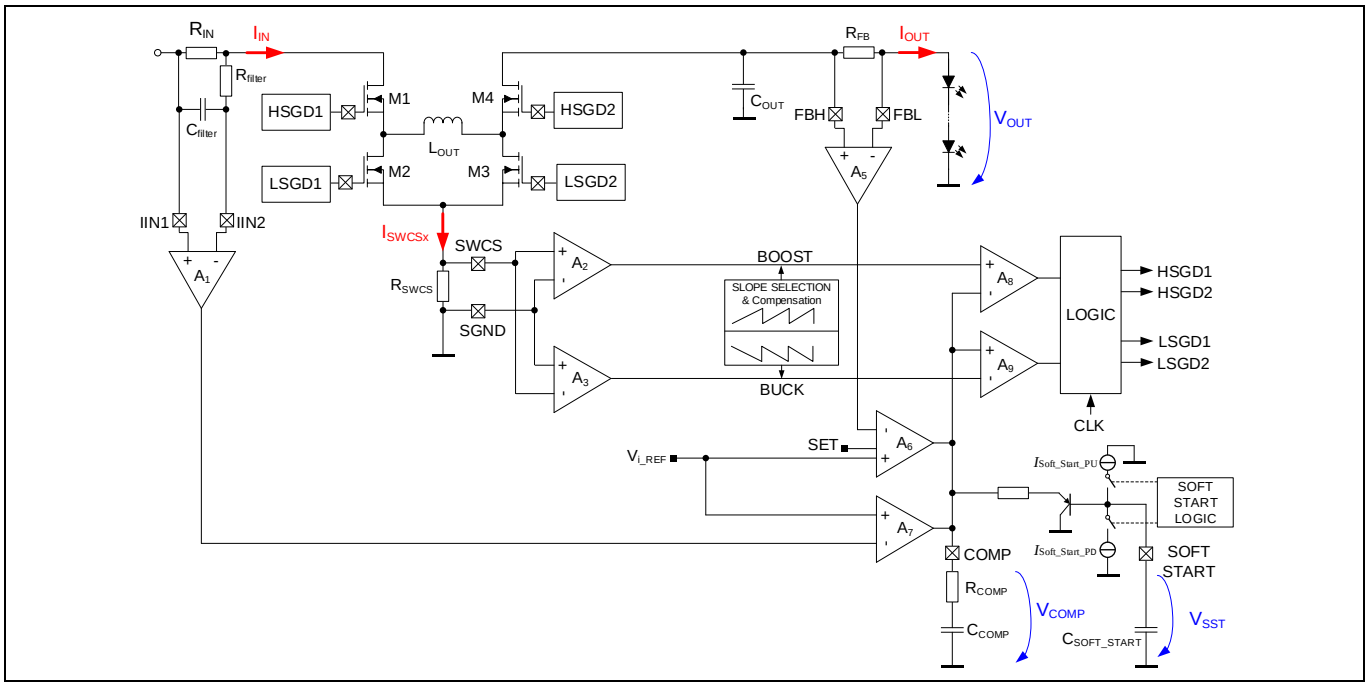

Figure 2 TLD5190 regulator block diagram

The core of the regulator is a current mode controller with compensation capacitor, similar to a standard boost controller.

Careful selection of external components provides the best compromise between efficiency, stability, EMC and cost for the application conditions.

1.1 Application example

The power supply module has the following specifications:

Table 1 LDM requirements

Parameter	Symbol	Value			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Input voltage	V_{IN}	6	13.5	35	V	Extended range
		9	13.5	16	V	Operating range
Output voltage	V_{OUT}	–	12	–	V	–
Output current	I_{OUT}	0	–	4	A	–
Output power	P_{OUT}	–	–	48	W	V_{IN} 9 V to 35 V, T_A = 25°C Power derating applies for V_{IN} < 9 V
Switching frequency	f_{SW}	–	385	–	kHz	–
System efficiency	η	–	95	–	%	V_{IN} = 13.5 V V_{OUT} = 12 V 3 A

2 External component design

2.1 Inductor

The design of the inductor in a buck-boost converter is based on the specified average and ripple current. Usually, the ripple current is within the range of 20% to 40% of the average value at the maximum rated power.

The inductor value depends on the switching frequency. Increasing the switching frequency allows smaller inductor and output capacitors, however increasing the switching frequency increases switching losses.

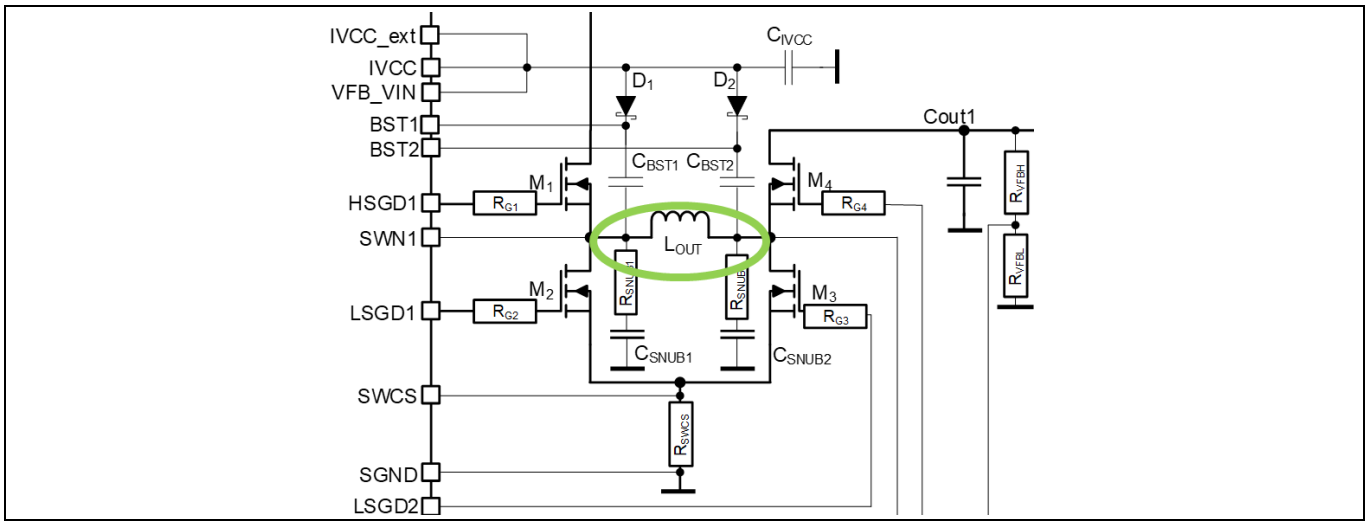

Figure 3 Main switching inductor

In this application 20% ripple current on the inductor is chosen so that there is reduced core loss at light load.

The following equation determines the inductor value to obtain the required ripple current with maximum input voltage and maximum output power (V_{IN} = 16 V, V_{OUT} = 12 V, I_{OUT} = 4 A).

Inductor ripple current varies a lot with the input voltage. It is suggested to check the ripple in corner operating points. In this case we calculated the ripple at the maximum input voltage. In this case the ripple at the maximum input voltage is calculated by:

$$L_{MIN} = D_{BUCK} \cdot \frac{V_{IN_{MAX}} - V_{OUT}}{\Delta I_{L_{pkpk}} \cdot f_{sw}} = 0.75 \cdot \frac{16\,V - 12V}{800mA \cdot 385\,kHz} = 9.7\,\mu H$$

Where

$$D_{BUCK} = \frac{V_{OUT}}{V_{IN\_MAX}} = \frac{12V}{16V} = 0.75$$

$$\Delta I_{L_{pkpk\_typ}} = 20\%\, I_L = \ 0.2 \cdot I_{IOUT} = 800\,mA$$

In order to dimension the inductor peak current, the worst case condition (when minimum input voltage and maximum output power are applied) can be calculated by:

$$I_{L\_peak} = \ I_{IL\_AVG\_MAX} \ + \frac{\Delta I_{Lpkpk_{vinmin}}}{2} = 5.7\,A + 0.58\,A = 6.28\,A$$

where, in boost mode $I_L = I_{IN}$, assuming efficiency is a little lower (approximately 93%) for V_{IN} = 9 V

$$I_{L\_AVG\_MAX} = I_{IN\_AVG\_MAX} = \frac{P_{OUT\_max}}{V_{IN\_min} \cdot \eta} = \frac{48W}{9 \cdot 93\%} = 5.7\ A$$

$$\Delta I_{Lpkpk\_vinmin} = D_{MIN\_VIN} \cdot \frac{V_{IN_{MIN}}}{L \cdot f_{sw}} = 0.25 \cdot \frac{9\ V}{10\ \mu H \cdot 385\ kHz} = 0.58\ A$$

$$D_{MIN\_VIN} \approx \frac{V_{OUT} - V_{IN\_min}}{V_{OUT}} = 0.25$$

The important key parameters to select an inductor are:

- Inductance > 9.7 µH
- RMS current > 5.7 A
- Saturation current > I_{L_PEAK} = 6.28 A

An inductor that fulfills the above mentioned requirements is the **10 µH** TDK SPM10065VT-100M-D.

2.2 Output capacitors

The output capacitor acts as an energy tank when M4 is off. For this reason it is subjected to a high ripple current. This component affects the bandwidth of the system and also the output current ripple performance. For this kind of application, multilayer ceramic capacitors (X7R - MLCC) with low ESR are placed in parallel to the electrolytic capacitors. The ceramic capacitors filter high speed transients, thereby improving EMC emissions. The electrolytic capacitor acts as a low frequency energy reserve and improves stability with higher ESR and capacitance.

Dimensioning of C_{OUT} is mainly driven by the output voltage ripple requirement ΔV_{OUT}. The worst case condition for the output ripple in the application conditions is when the device is in boost mode as well as minimum input voltage, maximum output current and maximum output power is applied.

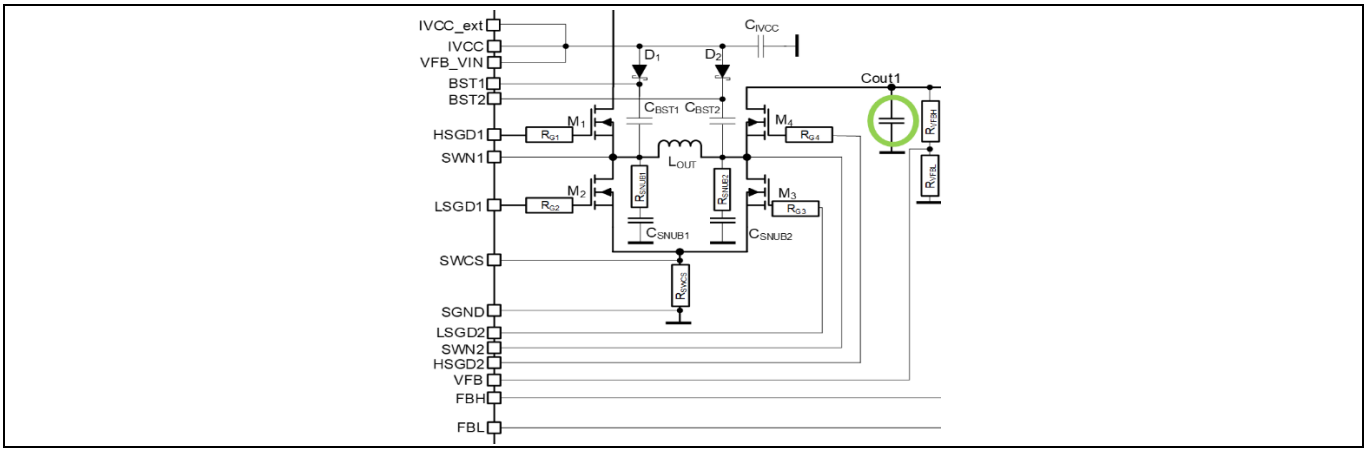

Figure 4 Output capacitors

Boost mode implies that output current is discontinuous. The output capacitor is discharged by a constant current equal to the average output current, for a time equal to $t_{ON} = D_{MAX}/f_{SW}$.

Assuming an ideal capacitor (R_{ESR} = 0 Ω) its value can be calculated from the desired output voltage ripple in worst case condition, for example ΔV_{OUT}=0.2 V at V_{IN_MIN} = 9 V, I_{OUT} = 4 A.

$$C \geq \frac{I_{OUT}}{\Delta V_{OUT}} \cdot \frac{D_{MIN\_VIN}}{f_{sw}} = \frac{4A}{0.1\ V} \cdot \frac{0.25}{385kHz} = 26\ \mu F$$

The ESR of the output capacitor adds more ripple, as shown with the equation:

$$\Delta V_{OUT_{ESR}} = ESR \cdot I_{L\_PEAK} = ESR \cdot \left(\frac{I_{OUT}}{1 - D_{MIN\_VIN}} + \frac{\Delta I_{Lpkpk_{vinmin}}}{2}\right)$$

Referring to the equations above, it is possible to calculate the maximum ESR, so that ESR contributes 20%, as rule of thumb, of C_{OUT} ripple.

$$R_{ESR} \leq \frac{\Delta V_{ESR}}{I_{L_{PEAK}}} = \frac{0.2 \cdot \Delta V_{OUT}}{6.28A} = \frac{0.2 \cdot 0.1\ V}{6.28A} = 3.2\ m\Omega$$

Another important aspect of the output capacitor design, is to consider the output transient response to a load step. The output voltage deviation is given by the time the inductor takes to adapt to the increased or reduced output current needs.

The following formula can be used to calculate the necessary output capacitance for a desired maximum voltage overshoot V_{OS} (e.g. 500 mV), at the maximum possible load step (e.g. 4 A)

$$C_{OUT} \geq \frac{{\Delta I_{OUT}}^2 \cdot L}{2 \cdot V_{OUT} \cdot V_{OS}}$$

This implies that with the described application assumptions we obtain:

$$C_{OUT} \geq \frac{{\Delta I_{OUT}}^2 \cdot L}{2 \cdot V_{OUT} \cdot V_{OS}} = \frac{(4\ A)^2 \cdot 10\ \mu H}{2 \cdot 12\ V \cdot 500\ mV} = 13\ \mu F$$

It is evident that the output capacitor design is driven by the ripple voltage requirement.

A **4 x 4.7 µF X7R ceramic** capacitor and **a 100 µF electrolytic** capacitor in parallel, fulfill required capacitance and series impedance. The additional capacitance helps the regulator during load transients and it improves stability.

Note: MLCC capacitors show a strong variation of the capacitance as a function of the applied voltage. An X7R 50 V capacitor may show 30% drop at 25 V bias voltage.

2.3 MOSFETs

Switching MOSFETs must be on logic level. They must withstand at least the maximum current calculated for the inductor sizing in Chapter 2.1:

$$I_{SW\_peak} \geq I_{L_{peak}} = 6.28\ A$$

Voltage class on the buck (input M1, M2) side must be higher than the maximum input voltage (35 V). At the boost side (output M3, M4), the voltage class must be higher than the maximum output voltage (12 V).

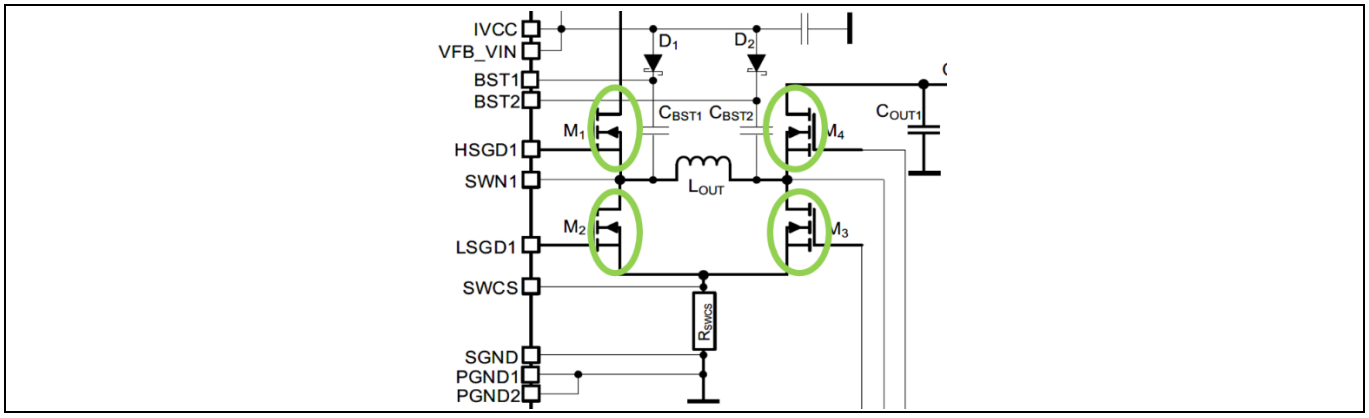

Figure 5 Switching MOSFETs

Note: Choosing a very low $R_{DS(ON)}$ MOSFET is not always the best choice. The optimum $R_{DS(ON)}$ shall balance switching losses and conduction losses, improving the efficiency.

In this design the focus is on efficiency. So a **7 mΩ 40 V MOSFET** (Infineon IPZ40N04S5L-7R4) is chosen for the 4 MOSFETs. These MOSFETs have low parasitic capacitances with low reverse recovery charge (Q_{rr}), providing 95% efficiency at V_{IN} = 12 V, V_{OUT} = 12 V 3 A. The efficiency is even higher when the device operates in boost or in buck, because the switching losses are halved compared to the buck-boost region.

2.4 Switch current limiter R_{SWCS}

The TLD5190 offers a switch current limit protection with the R_{SWCS} resistor.

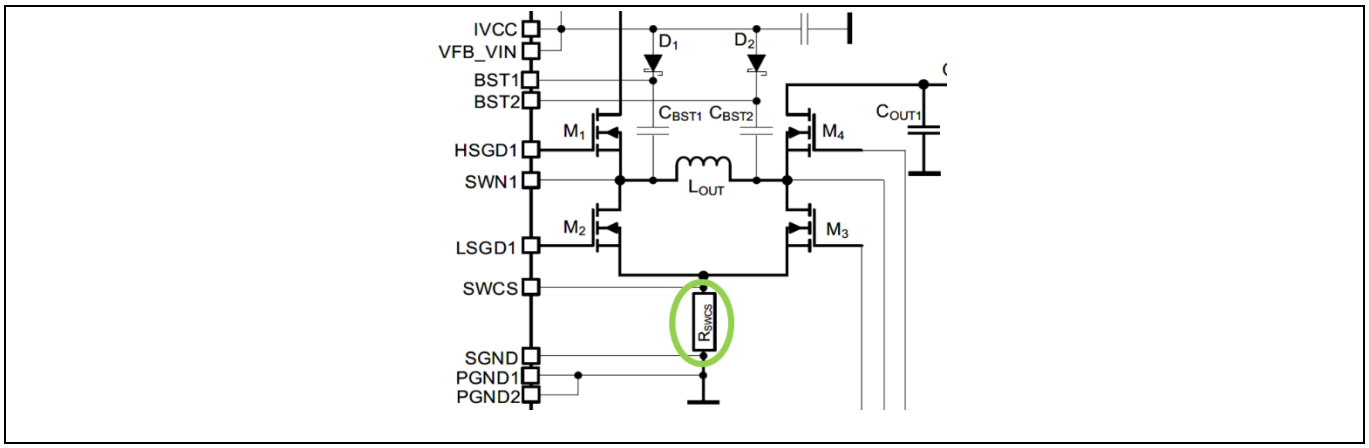

Figure 6 Switch current limiter R_{SWCS}

Please note that the SGND pin is not a ground signal, it is instead a differential input for the R_{SWCS} sense amplifier. Therefore it has to be routed into the PCB as a differential couple with the SWCS track.

The current limit shall be set higher than the previously calculated maximum switch current I_{SW_peak} (6.28 A) and is calculated by the following formula:

$$R_{SWCS} < \frac{V_{SWCS\_boost(min)}}{I_{L\_peak}} = \frac{40\ mV}{6.28\ A} 6.37\ m\Omega$$

R_{SWCS} is also the current mode controller inductor sensing resistor and impacts stability. The larger R_{SWCS} is, the higher the phase margin and PSRR are. Choose the resistor slightly smaller than the required value to fulfill the

minimum switch current limit and maximize the phase margin. For example, a **6 mΩ** Susumu PRL1632-R006-F-T1 (low ESL shunt resistor) provides a switch current limit of:

$$I_{SW\_LIMIT(typ)} = \frac{V_{SWCS_{boost}(typ)}}{R_{SWCS}} = \frac{50\ mV}{6\ m\Omega} = 8.3\ A$$

Note: Use a low inductive resistor on R_{SWCS}, in order to reduce fast transients switching activity noise.

2.5 Output voltage feedback resistor divider

The output voltage is set by a resistor divider which carries a portion of V_{OUT} to the feedback pins FBH, FBL.

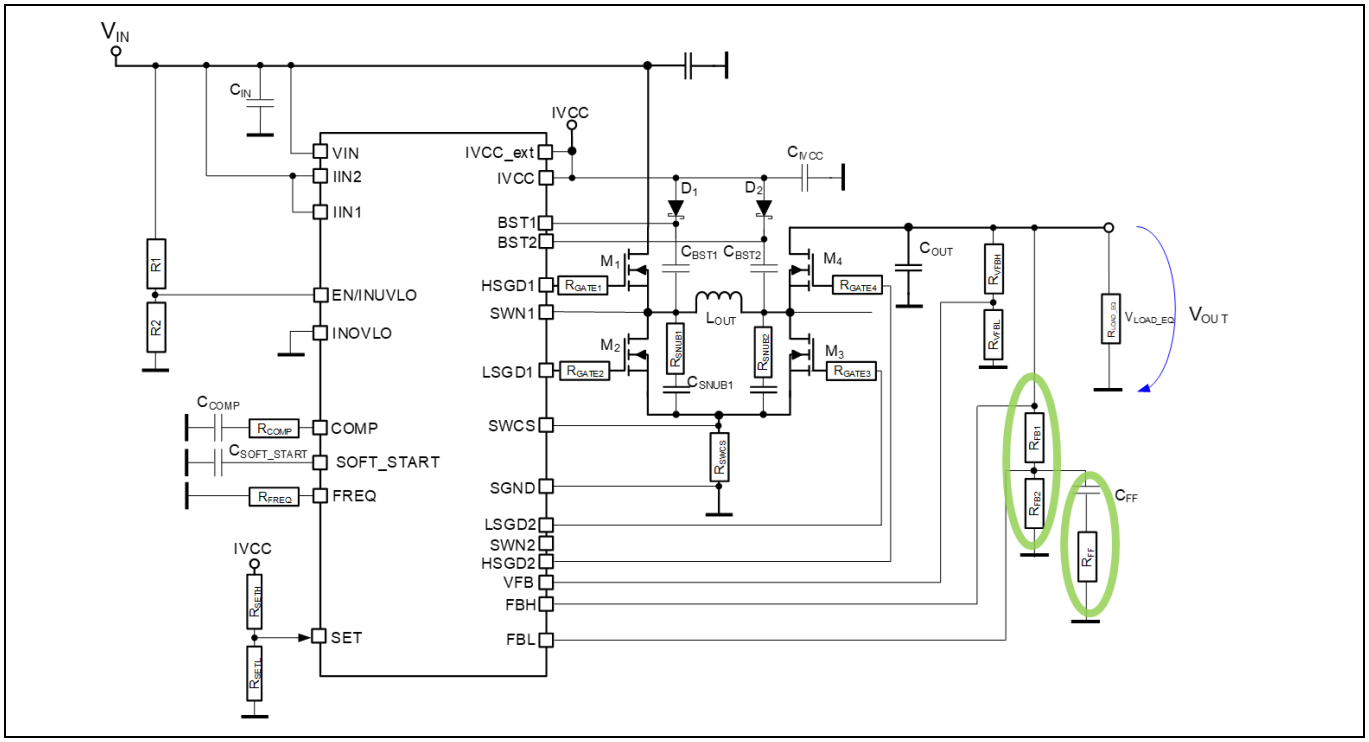

Figure 7 Output current sensing resistor

The first resistor R_{FB1} is chosen with 150 Ω in order to reduce the influence of the leakage current on FBL pin (I_{FBL_HSS}). Then R_{FB2} is calculated by:

$$R_{FB2} = \frac{V_{OUT} - V_{FBH-FBL}}{\frac{V_{FBH-FBL}}{R_{FB1}} - I_{FBL\_HSS}} = \frac{12\ V - 0.15\ V}{\frac{0.15\ V}{150\ \Omega} - 30\ \mu A} = 12.22\ k\Omega$$

The commercial value (E192 series) close to the calculated one is $\boldsymbol{R_{FB2}}$ **= 12.3 kΩ** which produces 12.08 V at V_{OUT}.

The feedback voltage divider resistors can also be calculated with the Excel component calculator.

The output voltage is calculated by

$$V_{OUT} = \left(\frac{V_{FBH-FBL}}{R_{FB1}} - I_{FBL_{HSS}}\right) * R_{FB2} + V_{FBH-FBL}$$

The output voltage can be reduced by applying analog dimming by the SET pin. The dimmed feedback reference value is calculated by:

$$V_{FBH-FBL} = \frac{V_{SET} - 200\ mV}{8}$$

This formula is valid for voltages at the SET pin (V_{SET}) between 0.2 V and 1.4 V.
If 100% analog dimming is needed, it is recommended to keep the SET pin above 1.5 V.

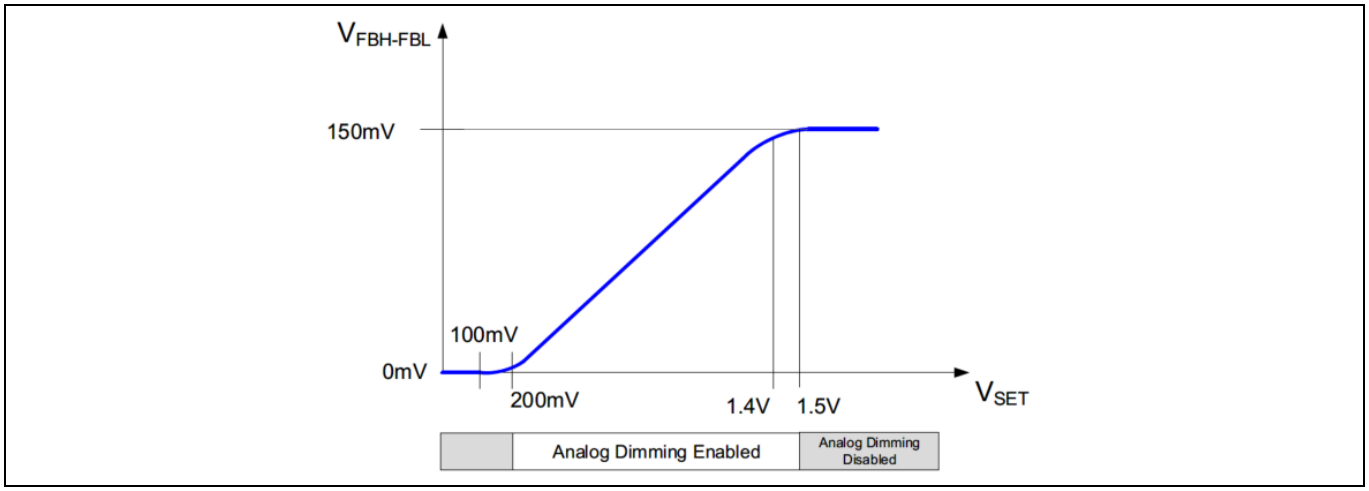

Figure 8 Analog dimming effect on $V_{FBH-FBL}$

To increase phase margin, PSRR, and bandwidth, it is suggested to apply a feed forward RC network C_{FF} and R_{FF} at the FBL pin. This network amplifies a possible variation in the output voltage at the sensing pins FBH and FBL. On the other hand the V_{OUT} ripple is amplified at FBH and FBL when C_{FF} is applied, therefore if the C_{FF} capacitor is too large this may cause to V_{OUT} to be regulated lower than expected.

As a starting point for the feed forward network ***R_{FF}=1.5 kΩ*** and ***C_{FF}= 10 nF*** are adopted (assuming RFB1 = 150 Ω). It is recommended to test the system reaction at startup and load variation.

2.6 Bootstrap diodes and capacitors

Bootstrap capacitors and diodes on TLD5190 follow the standard design rules for any gate driver using bootstrap circuitry.

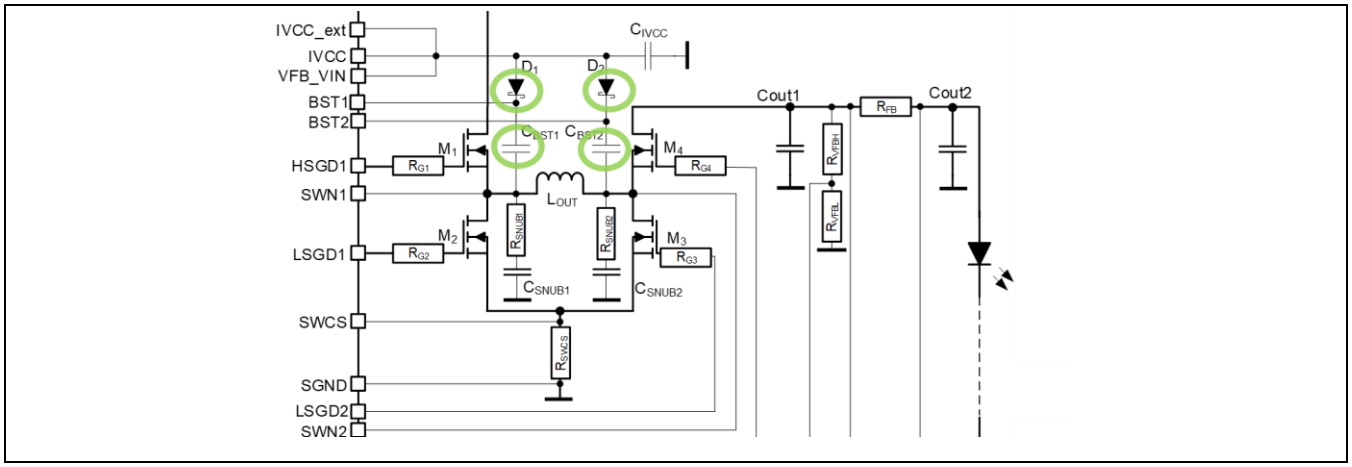

Figure 9 Bootstrap diodes and capacitors

The bootstrap capacitors must have enough energy to drive the gate of the high-side MOSFET without being depleted by more than 10%. Therefore, the bootstrap capacitor should be at least 10 times bigger than the equivalent gate capacitance of the high-side FET.

For this application a standard **100 nF 50 V** capacitor is chosen, which drives any modern generation MOSFET down to a few mΩ of $R_{DS(ON)}$ (for example, 40 V 2Ω IAUC100N04S6L020). This capacitor is only charged up to 5 V, so the voltage class can be as low as 10 V.

Bootstrap diodes generate the high-side gate driver bias by charging the bootstrap capacitor. In order to minimize charge losses associated with the reverse recovery, a Schottky diode with low forward voltage drop and low junction capacitance is recommended.

Another requirement is the diode reverse current at the highest working temperature. Reverse leakage current at high temperature may discharge the bootstrap capacitor and lead to the driver's undervoltage and to the shutdown of the gate driver. The reverse leakage current impact is higher for low switching frequency.

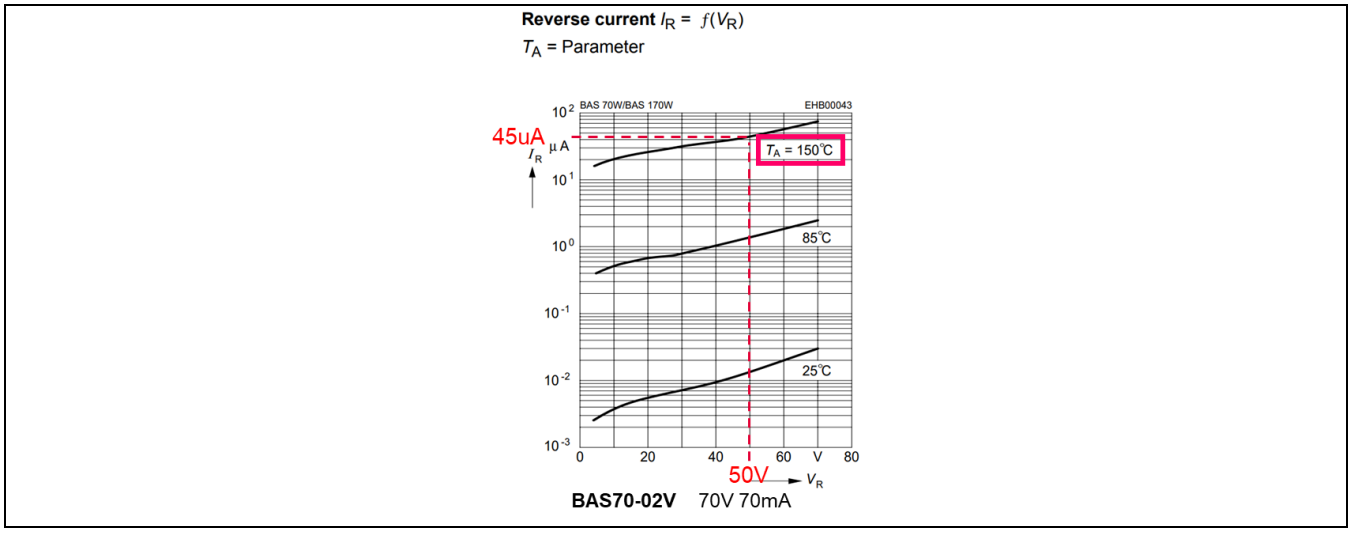

Figure 10 Bootstrap diodes reverse current of BAT 46WJ

For this application 70 V **Infineon BAS70-02V** with low reverse current is chosen.

As a rule of thumb, the reverse current on the bootstrap at the maximum application operating temperature and voltage shall be smaller than 1 mA assuming that the switching frequency is above 250 kHz.

3 Protections and spread spectrum

3.1 Output overvoltage and short to ground protection

The output overvoltage protection and the short to ground protection are set by a resistor divider on the VFB pin.

It is possible to set the overvoltage and short to ground threshold independently by using a 3 resistor divider on the VFB pin, connected to V_{OUT} and V_{IVCC} like explained in Figure 12

The overvoltage at the output (V_{OUT_OV}) has to be set higher than the nominal output voltage (12 V), with some margin, in order to avoid triggering the overvoltage in case of load step. For this application the overvoltage threshold of 15 V has been chosen.

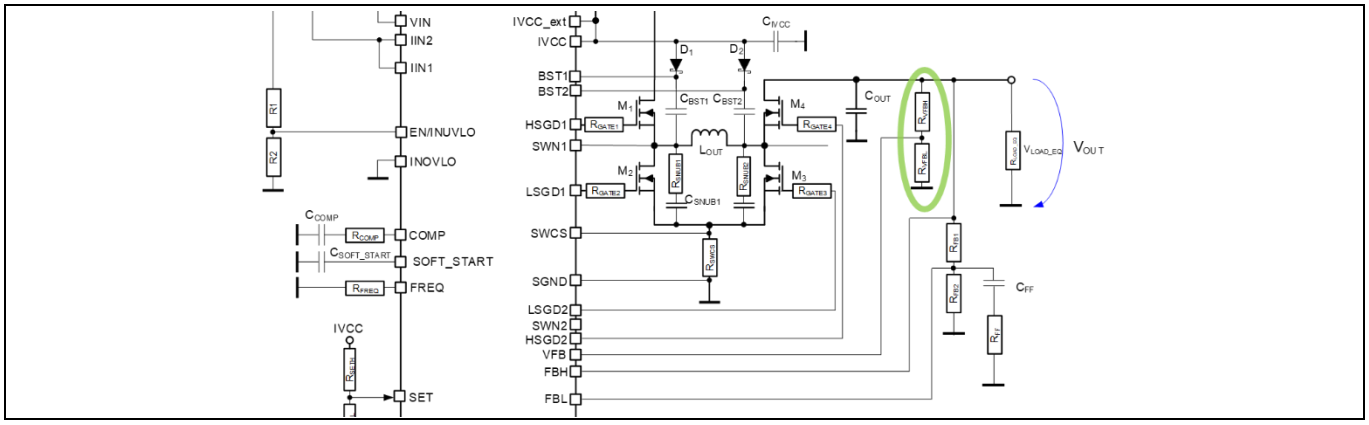

Figure 11 Overvoltage and short to ground voltage divider

The resistor divider has to be sized considering the overvoltage threshold. The short to ground as consequence will be approximately 1/3 of the overvoltage since $V_{VFB\_OVTH(typ)}$ = 1.45 V and $V_{VFB\_S2G(typ)}$ = 0.563 V.

In case the short to ground threshold has to be set independently from the overvoltage threshold, it is possible to adjust the 2 thresholds by adding a third resistor to the VFB pin as shown in Figure 12. The 3 resistors can be quickly calculated with the LED Excel component calculator.

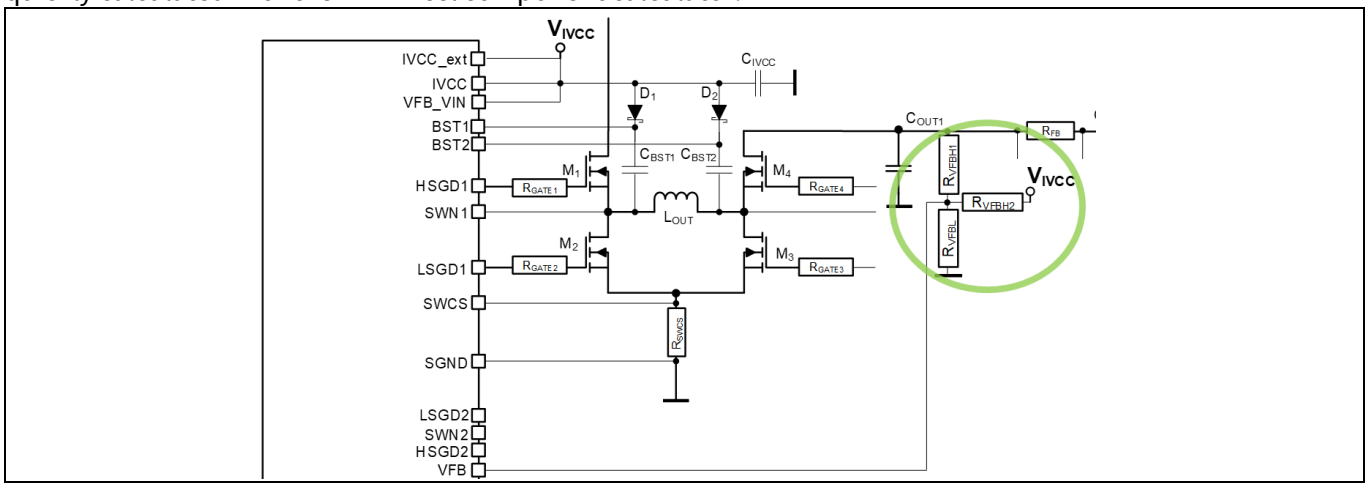

Figure 12 Overvoltage and short independent thresholds by means of 3 resistors

For this specific application note a resistors divider with 2 resistors is used. It is derived from the following formula:

$$V_{OUT\_OV} = V_{VFB\_OVTH} \cdot \frac{R_{VFBH} + R_{VFBL}}{R_{VFBL}}$$

In order to reduce the parasitic effects of moisture and leakage from the VFB pin, it is recommended to choose as starting point R_{VFBL} = 1.5 kΩ.

Setting on the Excel tool an output overvoltage of 15 V, the calculated R_{VFBH} is 13.91 kΩ. The commercial value (E96 series with 1% accuracy) is $\boldsymbol{R_{VFBH}}$ **= 14 kΩ**.

The following protection thresholds are produced:

V_{OUT_OV} = 15.09 V, V_{OUT_SHORT} = 5.82 V

With the TLD5190 component calculator it is also possible to check what is the effect of the overvoltage thresholds V_{OUT_OVTH} parameter deviations (Max, Min), by changing the value on V_{VFB_OV} cell.

3.2 Soft start capacitor

The soft start routine has 2 functionalities:

- Fault mask and wait-before-retry time
- Limit input inrush current and output overshoots at startup

Soft start duration is determined by the soft start capacitor C_{SST}. The inrush current limit is effective only when the soft start capacitor is larger than the C_{COMP} capacitor. Its effect is visible mainly in buck-boost and boost regulation modes.

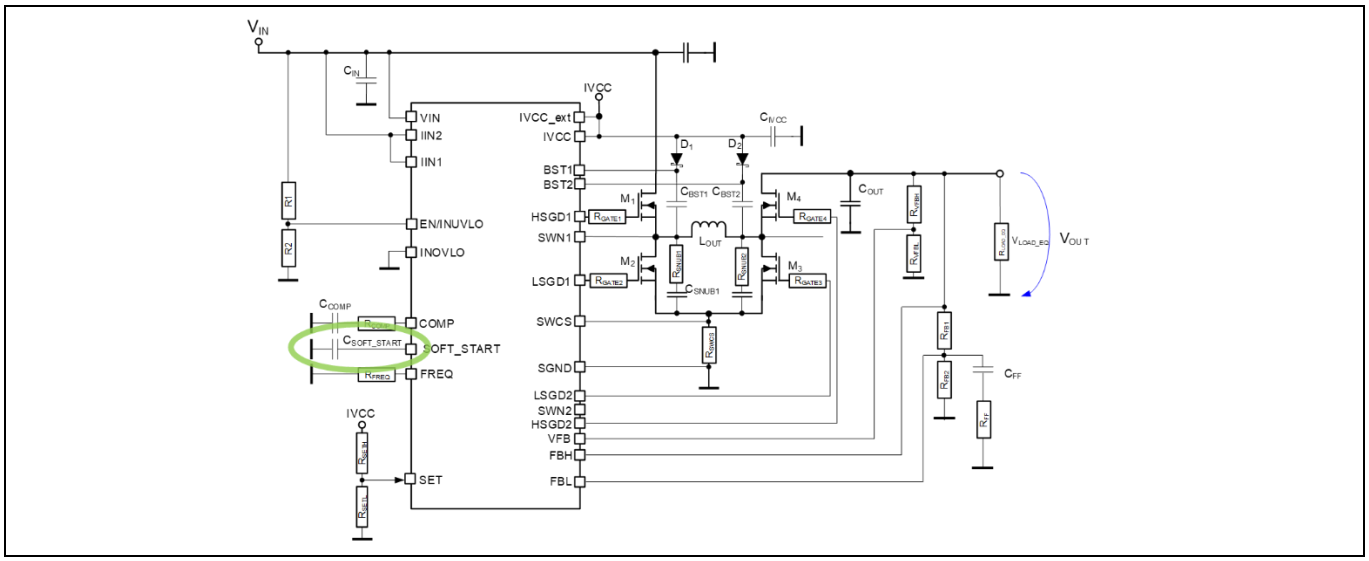

Figure 13 Soft start capacitor

The minimum value for the soft start capacitor is designed that, at startup, the output voltage exceeds the short to ground threshold (V_{OUT_SHORT}) before the soft start expires. The soft start expires when C_{SOFT_START} voltage reaches $V_{Soft\_Start\_LOFF}$. V_{OUT_SHORT} is set to 5.8 V in chapter 3.1.

During soft start, DCM (discontinuous conduction mode) is allowed. Therefore if the soft start is too long, the output voltage may build up above the target if no load is connected. The C_{COMP} discharges because the output voltage exceeds the target. Once the soft start expires, the discharged C_{COMP} may produce undershoot at the

output when CCM is applied. This undershoot can potentially trigger the short to ground protection. This sequence may repeat preventing the system from startup.

Figure 14 Output overshoot/undershoot at startup with no load due to excessively long soft start

Therefore, if no load condition occurs at startup, the soft start capacitor has to be carefully selected: not too small to avoid short to ground detection, not too big to avoid output overshoot. Under the assumption that V_{IN} > 6 V and I_{OUT} = 0 A at least until $V_{OUT} < V_{OUT\_SHORT}$, a good starting point for the selection of the soft start capacitor is given by the following approximate value:

$$C_{SST} \approx 0.6 \cdot C_{\mathrm{COMP}}$$

The effectiveness of the soft start should be tested in the real application. Soft start dimensioning should be verified in several operating conditions, for instance:

- At minimum temperature and minimum input voltage and full load as worst-case condition for the short to ground mask
- At maximum temperature and minimum output voltage (in case of adjustable output voltage) for eventual overshoot at no load condition

For this application **C_{SST} = 12 nF** has been verified to provide sufficient short to ground mask time and no overshoot at startup.

If a load is applied at startup, the overshoot due to DCM does not happen. Then a bigger soft start can be freely chosen.

3.1 Input undervoltage and overvoltage protections

The input voltage requirement for the power supply module is from 6 V up to 35 V (extended range). Therefore, the input undervoltage and overvoltage protections must be set based on those threshold on the EN/INUVLO and INOVLO pins. The 2 thresholds are $V_{INOVLOth}$ and $V_{EN/INUVLOth}$

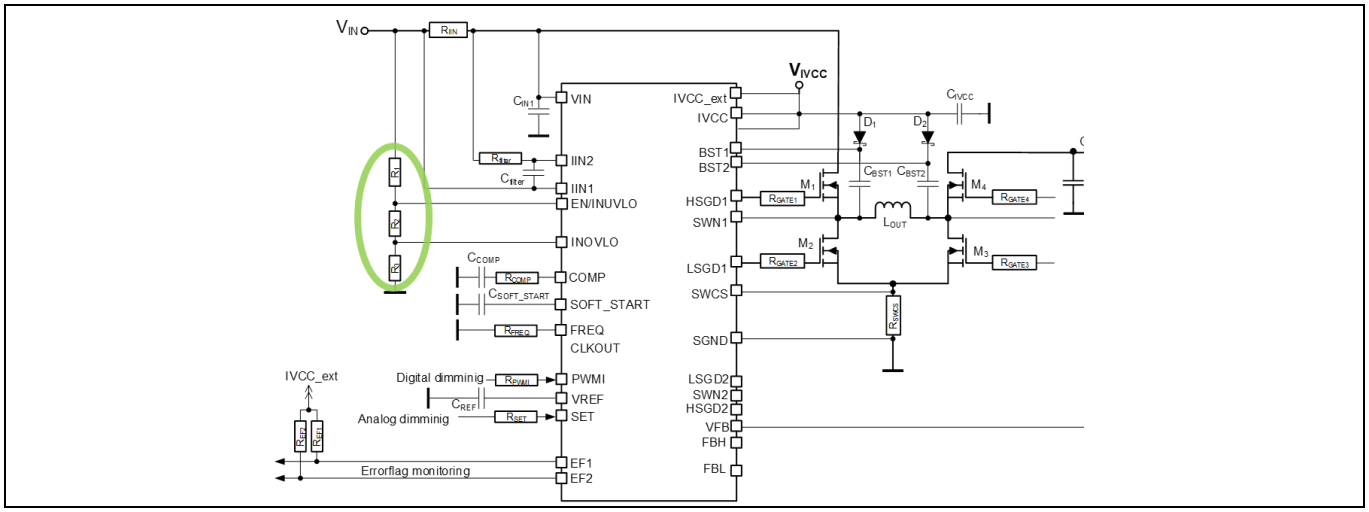

Figure 15 EN/INUVLO and INOVLO resistor divider

For this application an undervoltage threshold of 5.5 V is chosen (entry threshold, V_{IN} falling) while the input overvoltage threshold has been set to 37 V, above the 35 V maximum operating request for the module. The low-side resistor should be in the range from 2 kΩ up to 10 kΩ to avoid excessive leakage current and to provide an accurate threshold.

Choosing **R3 = 2.2 kΩ** as low-side voltage divider resistor, the high-side resistors (R1 and R2) are calculated by the TLD5190 LED Excel component calculator as:

R_2= 10750 Ω and R_1= 27750 Ω

The commercial values (E96 series with 1% accuracy) close to the calculated ones are:

$$R_2 = 10.7\ k\Omega \qquad R_1 = 27.4\ k\Omega$$

In case the input overvoltage protection is not desired, INOVLO pin can be shortened to ground leaving only 2 resistors at the EN/INUVLO pin, which are calculated by:

$$R2 = 2.2\ k\Omega \qquad R1 = R2 \cdot \frac{UV_{th} - EN/INUVLO_{th}}{EN/INUVLO_{th}} = 2.2k \cdot \frac{5.5V - 1.75V}{EN/INUVLO_{th}} = 4714\ \Omega$$

3.2 Input current sense and limiter resistor

The input current of the application can be measured and limited by the TLD5190 with a shunt resistor (R_{IIN}) via IIN1 and IIN2 pins. IIN1 is the positive sense terminal, IN2 is the negative sense terminal.

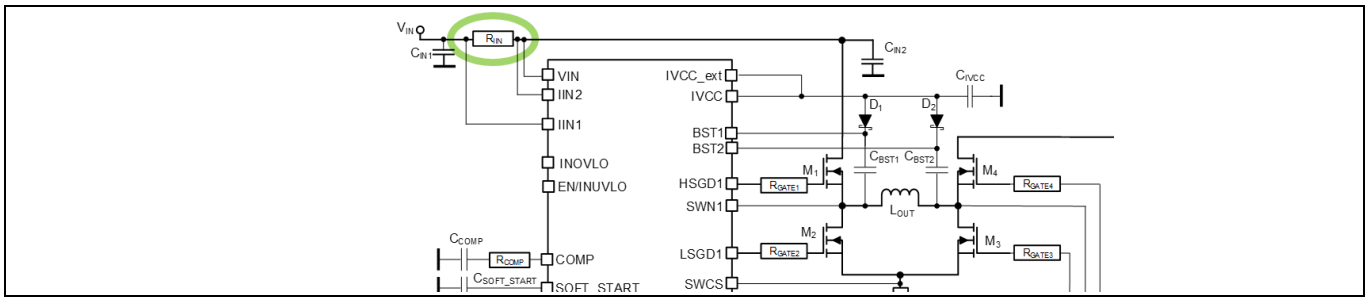

Figure 16 Input current monitor resistor

IINMON pin produces a voltage proportional to $V_{IIN1-IIN2}$ following this equation:

$$V_{IINMON(typ)} = I_{IN} \cdot R_{IIN} \cdot 20$$

The control loop reduces the C_{COMP} voltage when the voltage across the pins reaches the input current sense thresholds $V_{IIN1-IIN2}$ to keep the input current below a certain limit (I_{INMax}).

If the input current monitor is used only for monitoring the input current, then R_{IIN} should be dimensioned in order to be able to provide the maximum current needed by the application at the worst case (minimum $V_{IIN1-IIN2}$)

$$R_{IIN} \leq \frac{V_{IIN1-IIN2}(min)}{I_{IN(max)}} = \frac{46\ mV}{5.7\ A} = 8.1\ m\Omega$$

where:

$$I_{L\_AVG\_MAX} = I_{IN\_AVG\_MAX} = \frac{P_{OUT\_max}}{V_{IN\_min} \cdot \eta} = \frac{48\ W}{9 \cdot 93\%} = 5.7\ A$$

The efficiency at 9 V input voltage has been calculated with the TLD5190 Excel component calculator. A standard resistor value close to the calculated one is **R_{IIN} = 8 mΩ**.
The R_{IIN} has to be dimensioned differently if the application specifies a defined maximum input current. For example I_{IN_LIMIT} = 4 A. In that case, R_{IIN} is calculated as:

$$R_{IIN} = \frac{V_{IIN1-IIN2}(max)}{I_{IN\_LIMIT}} = \frac{54\ mV}{4\ A} = 13.5\ m\Omega$$

The current sensed by IIN1 and IIN2 can be monitored through IINMON pin. The IINMON pin output impedance is about 36 kΩ (typ). If IINMON is not used, it has to be left open. Then IIN1 and IIN2 pins should be connected to VIN pin.

4 EMC

4.1 Spread spectrum

The TLD5190 offers a spread spectrum modulation that significantly improves the EMC in the lower frequency range of the spectrum (f < 30 MHz). The spread spectrum is enabled by connecting the SPREAD_SPECTRUM pin to IVCC.

The effect of the spread spectrum is evident in Figure 17. In this EMC test report the conducted and radiated emission peaks are reduced by 10 dB and more. Therefore, class 5 limits pass.

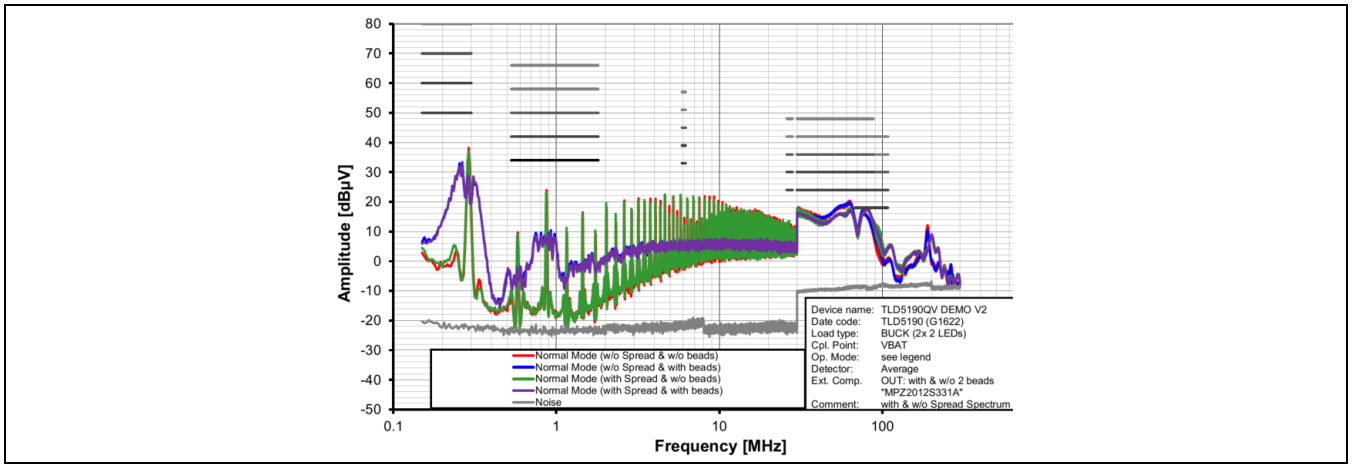

Figure 17 Spread spectrum effects on conducted emission (CISPR-25 conducted emission limits)

The spread spectrum may produce a small ripple at the output voltage.

4.2 Gate driver resistors

Gate driver resistors are placed at the gate driver output in order to improve the EMC performances. The same rules for the gate driver resistor dimensioning as for any standard DC-DC controller apply. These resistors reduce switching speed and ringing at the switching nodes. The gate driver resistors impact the efficiency of the DC-DC converter, and they should be increased only to pass the target EMC regulation (for example, CISPR25).

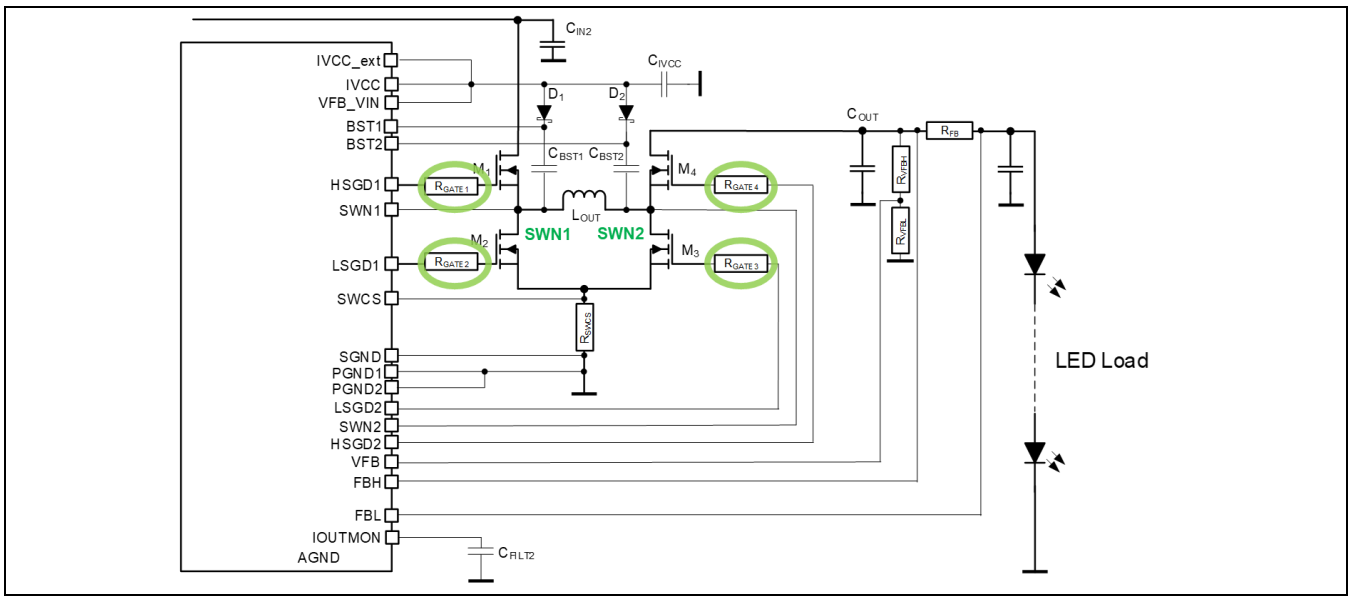

Figure 18 Gate resistors

The high-side gate driver resistor R_{GATE1} impacts the rise time of the buck switching node (SWN1). At the boost side, the low-side gate driver resistor R_{GATE3} impacts the falling time of the boost switching node (SWN2).

As a starting point for good EMC performance (Class 5 CISPR 25), the buck switching node rise-time and boost switching node fall-time, should be in the range of 10 ns to 50 ns. The final EMC result depends on output voltage, switching frequency, PCB layout, cable length, and other application parameters. Therefore, gate resistors should be tuned in the final application after an EMC measurement.

With the current MOSFET choice, a gate resistor $\boldsymbol{R_{GATEx} = 15\ \Omega}$ is selected as the starting point, with a measured rise time for the buck switching node of approximately 13 ns.

The impact on the efficiency is measured at the maximum output power 48 W (V_{IN} = 12 V, V_{OUT} = 12 V, I_{OUT} = 4 A):

- 94% with 15 Ω gate resistor
- 96% with 0 Ω gate resistor

This resistor value could be increased or decreased after EMC measurement.

4.3 Snubbers

As an additional measure to improve the EMC performance and to reduce switching node spikes add 2 RC damping circuits across the 2 switching nodes as shown in Figure 19. This snubber network provides damping and controls the switching node voltage rise speed.

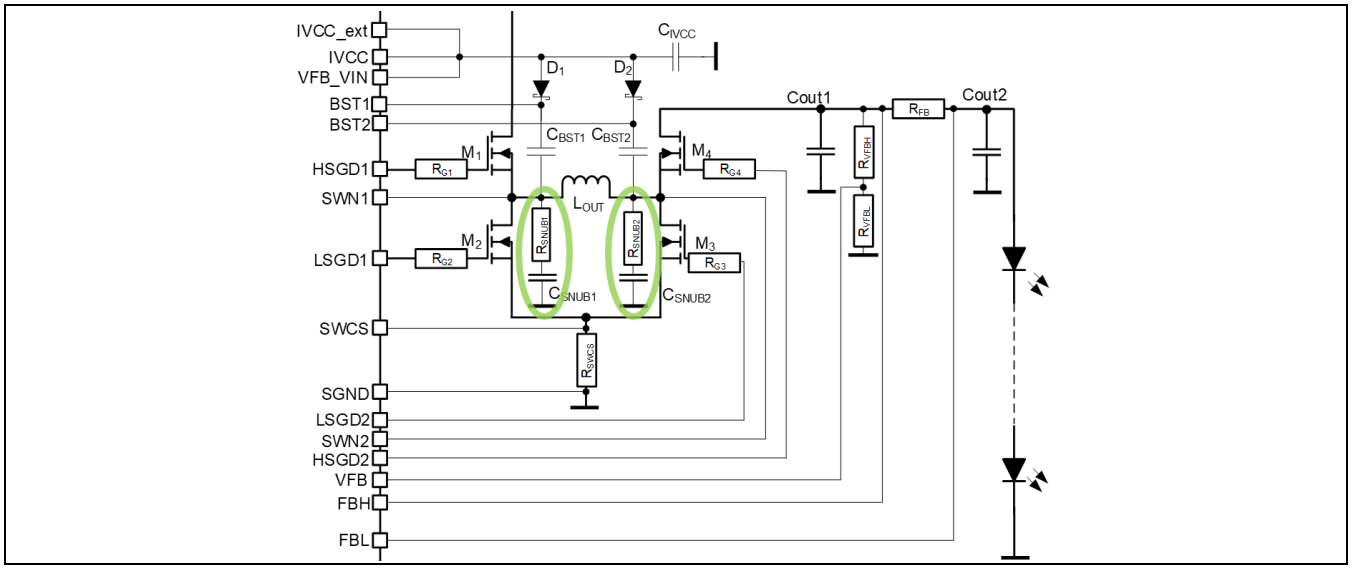

Figure 19 Snubbers

The snubber capacitance has to be big enough to dampen oscillations. At the same time, it has to be small enough to keep the power dissipation at a minimum. There is literature available on the WWW in order to carefully select the snubber resistor and capacitor values. It is common practice to leave the placeholder in the PCB board and then choose the RC value after the board is built up and running.

4.4 Layout considerations

For a DC-DC converter, the PCB design as well as component selection are critical tasks. Even if the circuit topology and the selected components are good, the performance of the whole system will be lower than expected, if the PCB layout is not good enough.

A proper layout is also the basis for good EMC performance. The most important PCB layout rules are explained in a dedicated application note, "*LITIX™ PCB design guideline document*" [5]. Figure 20 depicts a screenshot of this application.

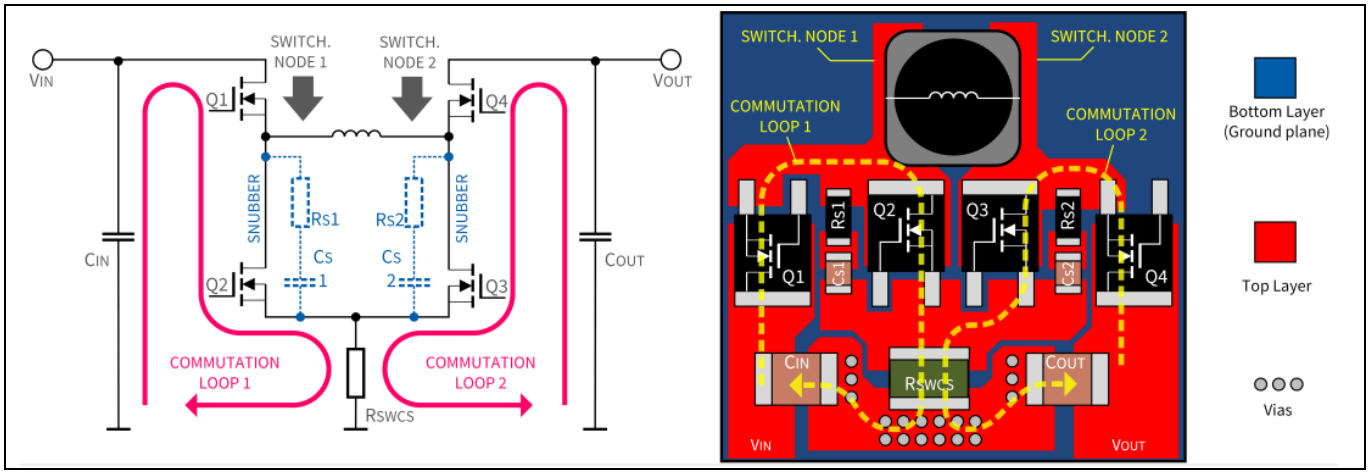

Figure 20 Hot loops and recommended layout for H-bridge topology

In the TLD5190 circuitry there are 3 differential amplifiers:

- FBH - FBL
- SGND – SWCS
- IIN1 – IIN2

The nets to these pins should be routed a differential pair. Special attention must be paid to the SGND pin. Since it is not a ground signal, it should not be tied to a ground plane. SGND is the negative input of a differential amplifier, so it should be connected directly at the R_{SWCS} resistance, which is then connected to a ground plane.

These nets work on small signals. They affect the regulation, so they should be routed far away from the switching nodes or the bootstrap nets.

5 List of references

[1] TLD5190 TLD5541-1 LED Component calculator

[2] Infineon LITIX™ Power TLD5190

[3] Ridley, R. B.; *A new Continuous Time Model for Current Mode Control*; IEEE Transaction on Power Electronics; Vol. 6; Issue 2; pp. 271-280; 1991

[4] Infineon TLD5190 DS Rev.1.20

[5] Infineon Z8F80033952 LITIX™ PCB design guidelines AN

Revision history

Major changes since the last revision

Page or Reference	Description of change
2021-08-13	Initial release

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