LITIX™ Power Flex TLD5190QU/QV

LED driver in buck-boost topology

About this document

Scope and purpose

This document explains how to design an LED driver using a TLD5190 for a powerful and efficient design. The application used as an example could be a typical automotive low beam or combined low beam + high beam driver ECU.

The TLD5190 is a 4-switch buck-boost controller designed to build high power and high efficiency LED drivers in automotive applications. It also includes built in diagnosis and protection features and spread spectrum modulator for simplified EMC design.

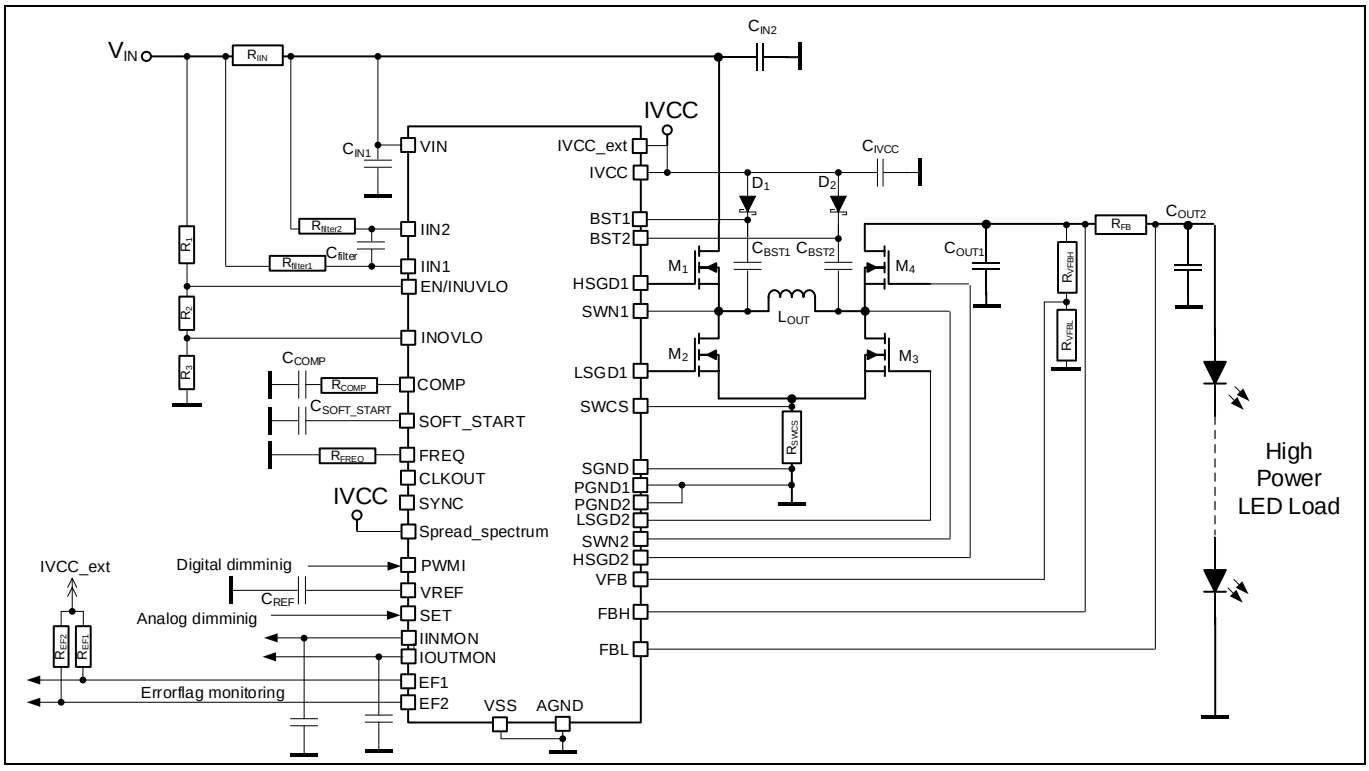

Figure 1 TLD5190 controller as LED driver

Intended audience

HW designers, LED system architects for LED lighting applications

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1 Introduction

This document explains how to correctly size all TLD5190 external components for a specific LED driver application.

It is possible to use the Infineon TLD5190 LED component calculator available on the TLD5190 Infineon webpage [1]. All TLD5190 external components, currents, efficiency and stability are calculated with minimum effort with this tool.

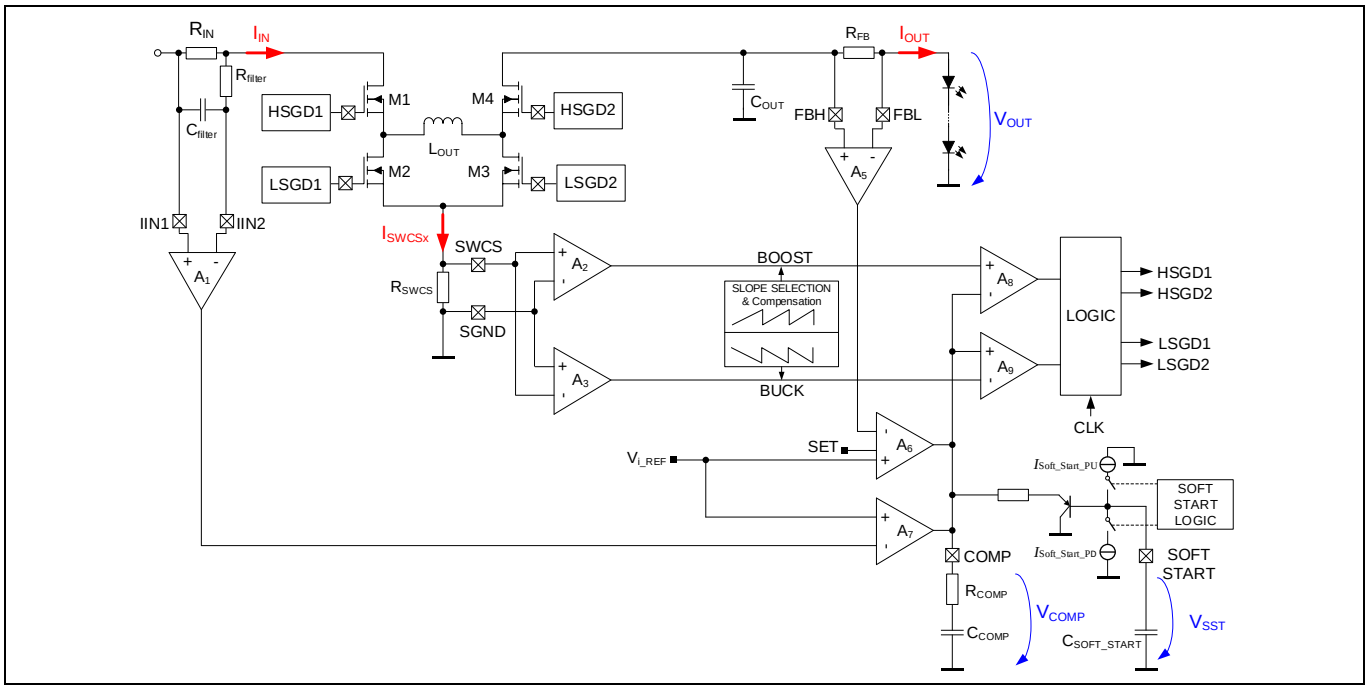


Figure 2 TLD5190 regulator block diagram

Even if the switching DC-DC output stage has a 4 switch, the core of the regulator is a current mode controller with compensation capacitor, similar to a standard boost controller.

Careful selection of external components has to provide the best compromise between efficiency, stability, EMC and cost of the application conditions.

1.1 Application example

The LED driver module (LDM) with TLD5190 designed in this application note will have the following specifications to drive a powerful automotive low beam function.

Table 1 LDM requirements

Parameter	Symbol	Value			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Input voltage	V_{IN}	6	13.5	35	V	Extended range
		9	13.5	16	V	Operating range
Output voltage	V_{OUT}	5	–	45	V	–
Output current	I_{OUT}	700	–	1500	mA	–
Output power	P_{OUT}	5	–	45	W	V_{IN} 9 V to 35 V, T_A = 25°C Power derating applies for V_{IN} < 9 V
Switching frequency	f_{SW}	–	385	–	kHz	–
System efficiency	η	–	95	–	%	V_{IN} = 13.5 V LED mode: 6 LED, I_{OUT} = 1500 mA,

2 External component design

2.1 Inductor

The inductor in a boost converter is designed based on the specified average and ripple current. Usually, the ripple current is in the range of 20% to 40% of the average value at the maximum rated power.

The inductor value depends on the switching frequency. Increasing the switching frequency allows smaller inductor and output capacitors, however increasing the switching frequency increases switching losses.

Increasing the inductor value results in:

- Reduced core losses (which depend on ripple value)
- Increased conduction losses on inductor (higher inductor DCR if same dimension is kept)
- Reduced conduction losses on MOSFET (smaller ripple current)
- Improved light load efficiency
- Reduced stability (more delay between regulation duty cycle change and effective current change)
- Reduced loop speed

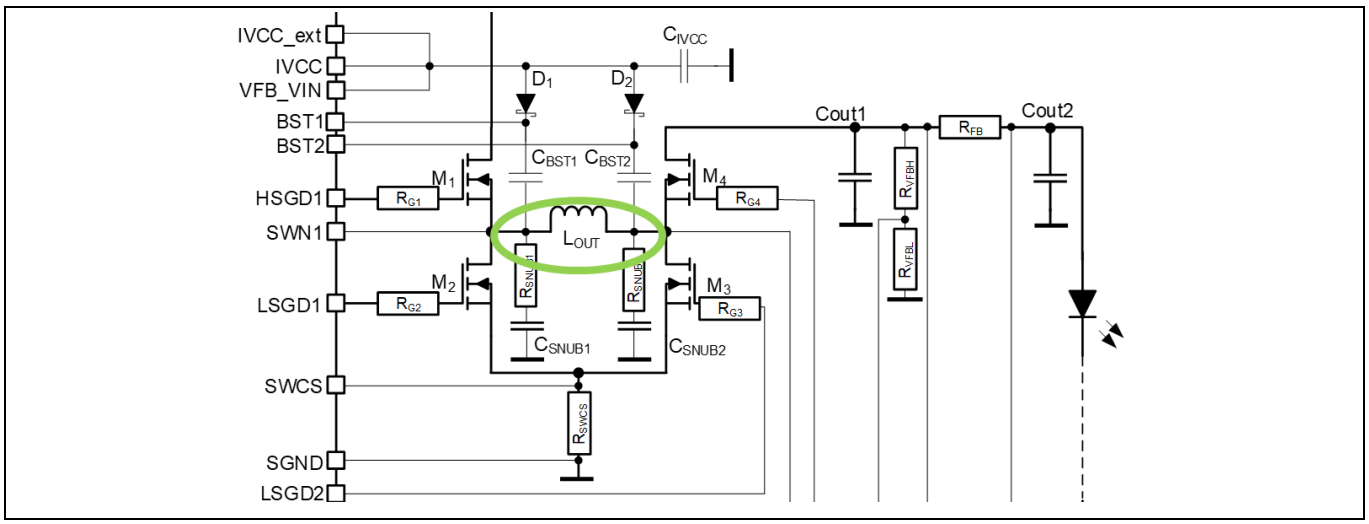


Figure 3 Main switching inductor

In this application 40% ripple current has been chosen, to minimize inductor size. An approximate efficiency of 95% is used in order to calculate the inductor current from the maximum output power.

The following equation determines the inductor value to obtain the required ripple current with typical input voltage and maximum output power (P_{OUT} = 45 W, $V_{OUT\_max,P}$ = 30 V, I_{OUT} =1.5 A).

$$L_{MIN} = D_{TYP} \cdot \frac{V_{IN_{TYP}}}{\Delta I_{L_{pkpk\_typ}} \cdot f_{sw}} = 0.55 \cdot \frac{13.5\ V}{1.4A \cdot 385\ kHz} = 13.7\ \mu H$$

where

$D_{TYP} = \frac{V_{OUT\_maxP} - V_{IN\_typ}}{V_{OUT}} = 0.55$

$$\Delta I_{L_{pkpk\_typ}} = 40\%\, I_L = \ 0.4 \cdot I_{IN} = 0.4 \cdot \frac{P_{OUT\_max}}{V_{IN} \cdot \eta} = 0.4 \cdot \frac{45W}{13.5V \cdot 0.95} = 1.4A$$

The actual peak current in worst case condition (when minimum input voltage and maximum output power is applied) can be calculated as:

$$I_{L\_peak} = \ I_{IL\_AVG\_MAX} \ + \frac{\Delta I_{Lpkpk_{vinmin}}}{2} = 5.4\ A + 0.545\ A = 5.95\ A$$

Where, in boost mode $I_L = I_{IN}$, assuming efficiency is a little lower (approximately 93%) for V_{IN} = 9 V

$$I_{L\_AVG\_MAX} = I_{IN\_AVG\_MAX} = \frac{P_{OUT\_max}}{V_{IN\_min} \cdot \eta} = \frac{45W}{9 \cdot 93\%} = 5.4\ A$$

$$\Delta I_{Lpkpk\_vinmin} = D_{MAX} \cdot \frac{V_{IN_{MIN}}}{L \cdot f_{sw}} = 0.7 \cdot \frac{9\ V}{15\ \mu H \cdot 385\ kHz} = 1.09\ A$$

$$D_{MAX} \approx \frac{V_{OUT_{maxP}} - V_{IN\_min}}{V_{OUT_{maxP}}} = 0.7$$

The important key parameters to select an inductor are then:

- Inductance > 13 µH
- Saturation current and RMS current > 6.49 A

An inductor that fulfills above requirements is the **15 µH** TDK SPM10065VT-150M-D.

Efficiency, minimum inductor value, inductor currents and ripples can be quickly calculated using the Infineon TLD5190 LED component calculator Excel [1].

2.2 Output capacitors

The output capacitor acts as an energy tank when M4 is off and for this reason it is subject to a high ripple current. This component affects the bandwidth of the system and also the output current ripple performance. Usually, for this kind of application, multilayer ceramic capacitors (X7R - MLCC) with low ESR are preferred over electrolytic capacitors.

Dimensioning of C_{OUT} is mainly driven by the output voltage ripple ΔV_{OUT}. Worst case condition for the output ripple is when the device is in boost mode (output current discontinuous), minimum input voltage, maximum output current and maximum output power.

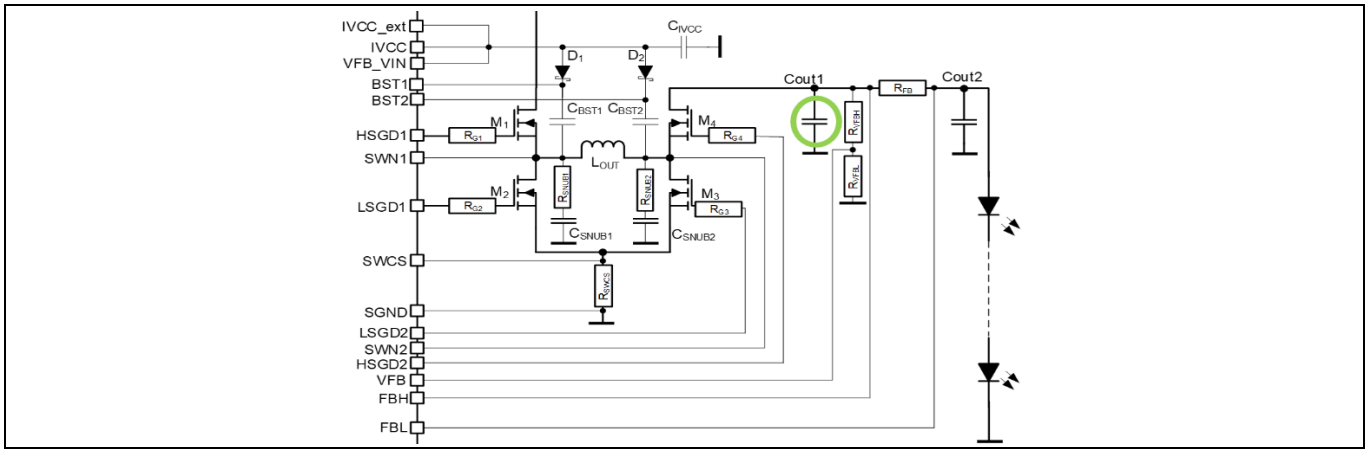


Figure 4 Output capacitors

In boost mode the capacitor is discharged by a constant current equal to average output current, for a time equal to $t_{ON} = D_{MAX}/f_{SW}$.

Assuming an ideal capacitor ($R_{ESR} = 0\ \Omega$) its value can be calculated from the desired output voltage ripple in worst case condition:

$$C \geq \frac{I_{OUT}}{\Delta V_{OUT}} \cdot \frac{D_{MAX}}{f_{sw}} = \frac{1.5A}{0.2\ V} \cdot \frac{0.7}{385\ kHz} = 13.6\ \mu F$$

The ESR of the output capacitor adds more ripple, given with the equation:

$$\Delta V_{OUT_{ESR}} = ESR \cdot ILpeak = ESR \cdot \left(\frac{I_{OUT}}{1 - \mathrm{Dmax}} + \frac{\Delta I_{Lpkpk_{vinmin}}}{2}\right)$$

From the equations above, it is possible to calculate the maximum ESR so that ESR contributes 20%; as a rule of thumb, of C_{OUT} ripple.

$$R_{ESR} \leq \frac{\Delta V_{ESR}}{I_{L_{peak}}} = \frac{0.2 \cdot \Delta V_{OUT}}{5.95A} = \frac{0.2 \cdot 0.2\ V}{5.95A} = 6.7\ m\Omega$$

A parallel 3 x 4.7 µF X7R capacitor would be sufficient to fulfill required capacitance and series impedance, but during the stability calculations, it has been increased to **5 x 4.7 µF X7R** to improve phase margin in boost mode.

Note: MLCC capacitors show a strong variation of the capacitance as a function of the applied voltage. An X7R 50 V capacitor may show 30% drop at 25 V bias voltage.

2.3 MOSFETs

Switching MOSFETs must be logic level they must withstand at least the maximum current calculated for the inductor sizing in Chapter 2.1:

$$I_{SW\_peak} = I_{L\_peak} = 5.95\ A$$

Voltage class on the buck (input) side must be higher than the maximum input voltage (35 V). At the boost (output) side, voltage class must be higher than the maximum output voltage (50 V).

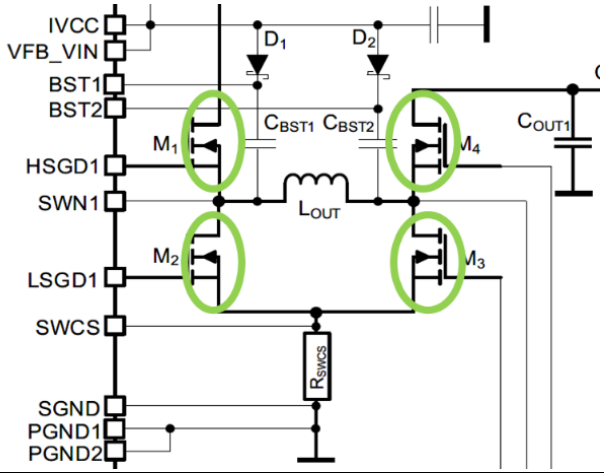


Figure 5 Switching MOSFETs

Note: Choosing a very low $R_{DS(ON)}$, MOS it is not always the best choice. The optimum $R_{DS(ON)}$ shall balance switching losses and conduction losses, improving the efficiency.

In this design focus is on the highest efficiency, so a **7 mΩ 40 V MOSFET** has been chosen for the buck side (Infineon IPZ40N04S5L-7R4) and a **14 mΩ 60 V MOSFET** has been chosen for the boost side (Infineon IAUZ30N06S5L140). These MOSFETs have low parasitic capacitances with low reverse recovery charge (Q_{rr}) providing a 96% efficiency at V_{IN} = 13.5 V V_{OUT} = 30 V 1 A.

Efficiency on several MOSFETs can be easily compared in MOSFET selection process using the TLD5190 component calculator [1].

Note: For EMI reasons, it is common practice to place a resistor (R_{GATE}) of approximately 5 Ω to 15 Ω in series depending on the gate charge and EMI performance of the circuit. On the other hand, this lowers the overall efficiency of the converter.

2.4 Switch current limiter R_{SWCS}

The TLD5190 offers a switch current limit protection with the R_{SWCS} resistor.

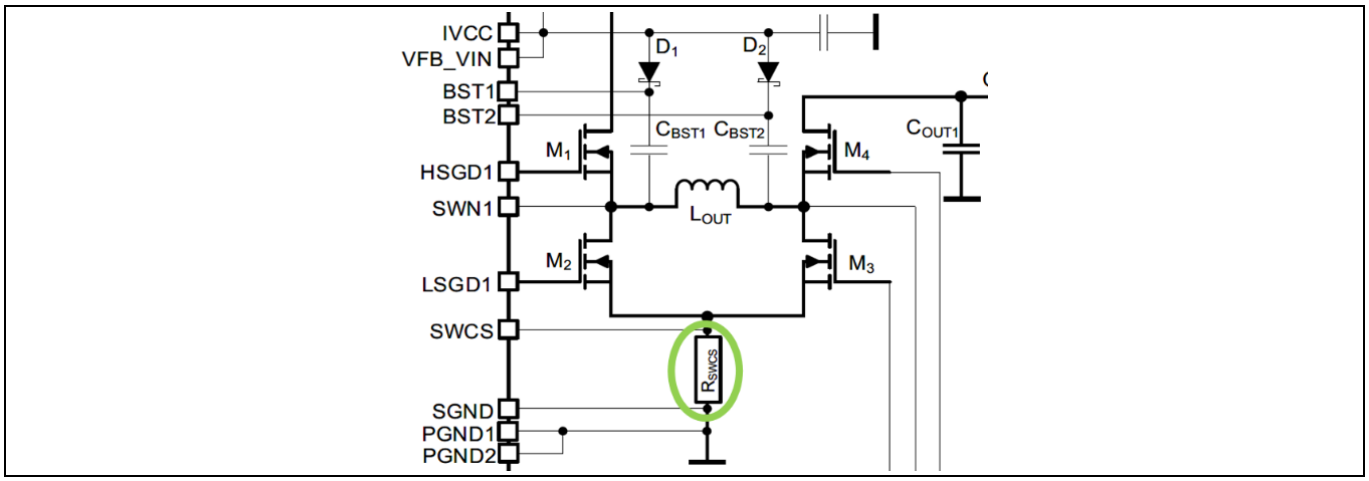


Figure 6 Switch current limiter R_{SWCS}

Please note that the SGND pin it is not a ground signal, but it is a differential input for the R_{SWCS} sense amplifier, so it has to be routed in the PCB as differential couple with the SWCS net.

The current limit shall be set higher than the previously calculated maximum switch current I_{SW_peak} (5.95 A), with the following formula:

$$R_{SWCS} < \frac{V_{SWCS\_boost(min)}}{I_{L\_peak}} = \frac{40mV}{5.95A} = 6.7m\Omega$$

R_{SWCS} is also the current mode controller inductor sensing resistor and impacts stability. The larger R_{SWCS}, the higher the phase margin and PSRR.

Choose the resistor slightly smaller than the required value to fulfill the minimum switch current limit for example, low ESL **6 mΩ** Susumu PRL1632-R006-F-T1, which provides a switch current limit in boost mode of:

$$I_{SW_{LIMIT(typ)}} = \frac{V_{SWCS_{boost}(typ)}}{R_{SWCS}} = \frac{50mV}{6mOhm} = 8.3A$$

Note: Use low inductive resistor on R_{SWCS}, in order to reduce fast transients switching activity noise.

2.5 Output current sense resistor

The output current sensor can easily be calculated by imposing the feedback voltage $V_{FBH\text{-}FBL\_REF}$ regulated by the device with the required output current.

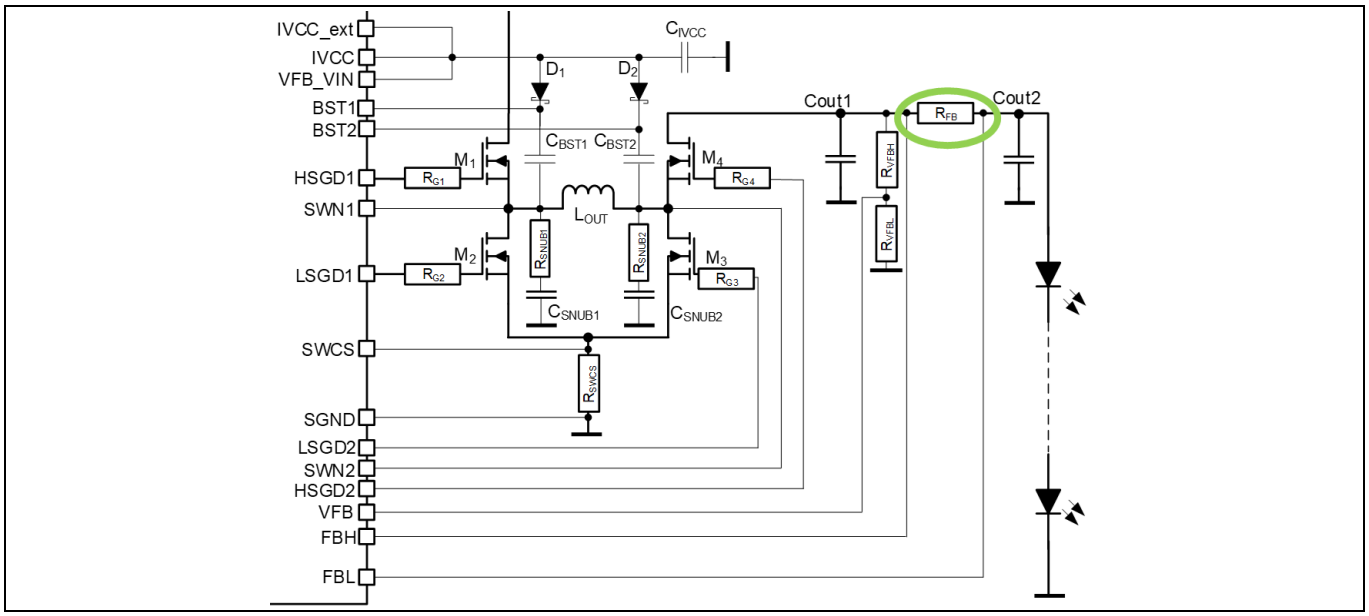


Figure 7 Output current sensing resistor

For this application, the resistor can be calculated as:

$$R_{FB} = \frac{V_{\text{VFBH}-\text{FBL\_REF}}}{I_{OUT}} = \frac{0.15\ V}{1500\ mA} = 100\ m\Omega$$

The power rating of this device can be calculated as

$P = R_{FB} \cdot I_{OUT}^2 = 0.1\ \Omega \cdot (1.5A)^2 = 0.225\ W$

For this application PRL1632-R100-F-T1 from Susumu, satisfies the requirements.

2.6 Bootstrap diodes and capacitor

Bootstrap diodes and capacitors on TLD5190 follow the standard design rules for any gate driver that uses bootstrap circuitry.

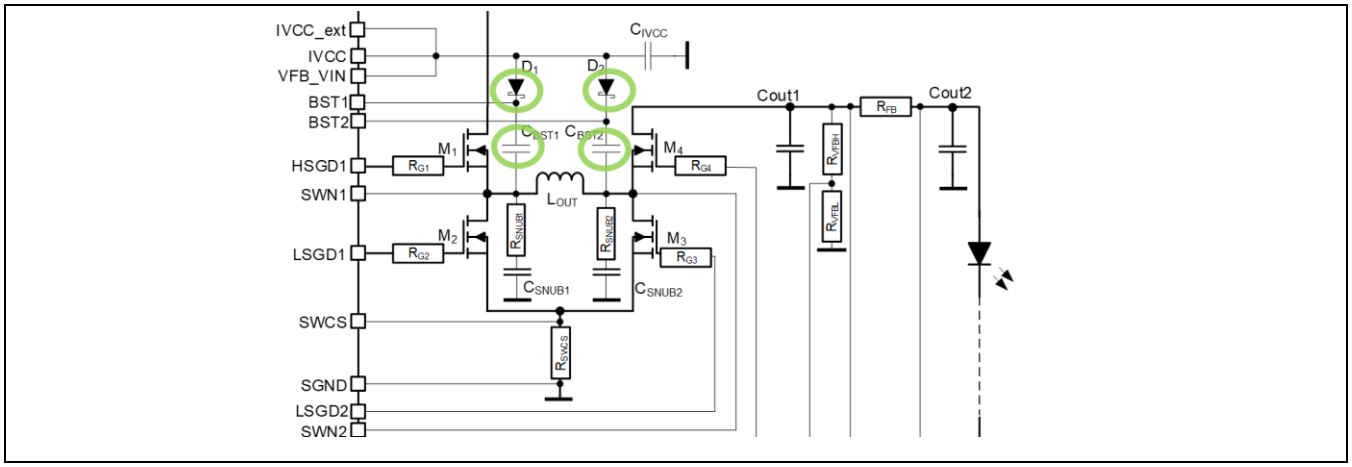


Figure 8 Bootstrap diodes and capacitors

The bootstrap capacitors must have enough energy to drive the gate of the high-side MOSFET without being depleted by more than 10%. Therefore, the bootstrap capacitor should be at least 10 times greater than the equivalent gate capacitance of the high-side FET.

For this application a standard **100 nF 50 V** capacitor is chosen, which could drive about any modern generation MOSFET down to few mΩ of $R_{DS(ON)}$ for example, 40 V 2Ω IAUC100N04S6L020. This capacitor will be charged to 5 V only.

Bootstrap diodes generate the high-side gate driver bias by charging the bootstrap capacitor. In order to minimize losses associated with the reverse recovery, a Schottky diode with low forward voltage drop and low junction capacitance is recommended.

Another requirement that is often overlooked is the diode reverse current at the highest working temperature. Reverse leakage current at high temperature may discharge the bootstrap capacitor and lead to driver's undervoltage and shutdown the gate driver. Reverse leakage current impact is high for low switching frequency.

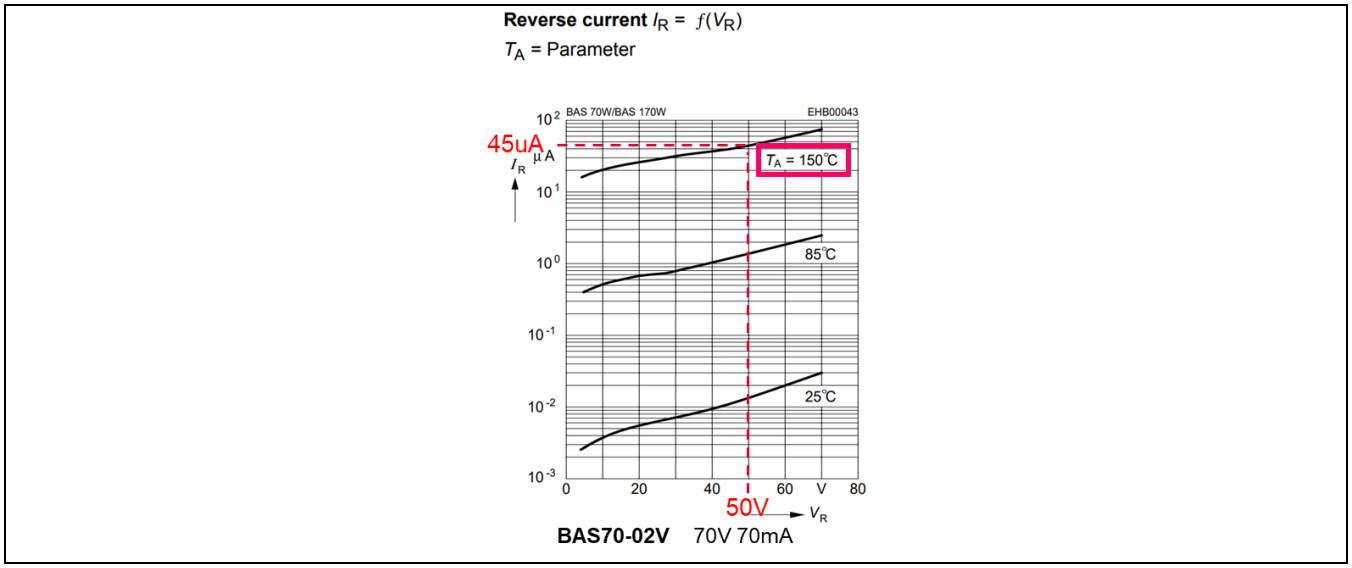


Figure 9 Bootstrap diodes reverse current of the BAT 46WJ

For this application with a 70 V **Infineon BAS70-02V** with low reverse current is chosen.

As a rule of thumb, the reverse current on the bootstrap at maximum application operating temperature and voltage shall be smaller than 1 mA assuming switching frequency is above 250 kHz.

2.7 Analog dimming - SET resistor divider

The LED driver module has 1500 mA maximum current, but the output current can be reduced with the analog dimming.

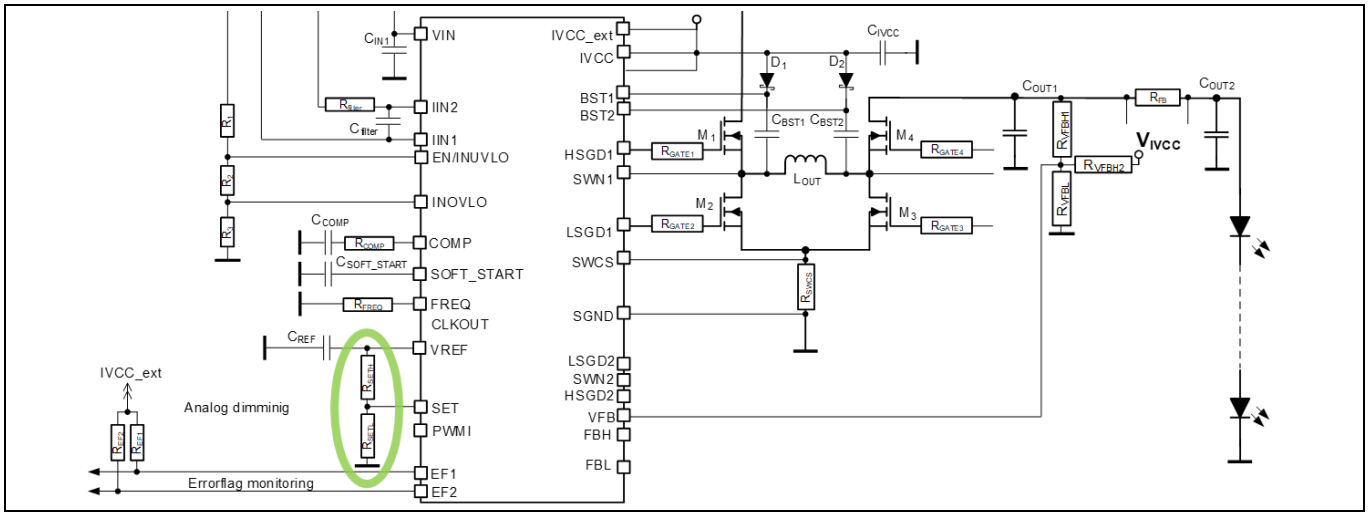


Figure 10 SET resistor divider

A resistor divider can be applied to a reference voltage (example to the 5 V IVCC) in order to reduce the output current $I_{OUT(AD)}$ below the maximum value (given by R_{FB}) by means of the SET pin.

In order to reduce the parasitic effects of moisture and leakage from the SET pin, it is recommended to choose R_{SETL} equal to 15 kΩ.

Supposing that the requested output current, set by the SET pin, is $I_{OUT(AD)}$= 0.9 A, then R_{SETH} is calculated using the following formula:

$$R_{SETH} = R_{SETL} \cdot \frac{V_{REF} - \left(I_{OUT(AD)} \cdot RFB \cdot 8 + 0.2\right)}{\left(I_{OUT(AD)} \cdot RFB \cdot 8 + 0.2\right)} = 15\text{k}\Omega \cdot \frac{2V - (0.9A \cdot 0.1\Omega \cdot 8 + 0.2V)}{(0.9A \cdot 0.1\Omega \cdot 8 + 0.2)} = 17{,}60\ \text{k}\Omega$$

Choosing 18 kΩ as closest commercial value, the effective output current will be:

$$I_{OUT(AD)} = \frac{V_{SET} - 200mV}{R_{FB} \cdot 8} = \frac{V_{REF} \cdot \frac{R_{SETL}}{R_{SETH} + R_{SETL}} - 200mV}{R_{FB} \cdot 8} = \frac{2V \cdot \frac{15\text{k}\Omega}{18\text{k}\Omega + 15\text{k}\Omega} - 200mV}{0.1\Omega \cdot 8} = 0.89\ A$$

3 Protections and spread spectrum

3.1 Output overvoltage, open load and short to ground protection

The output overvoltage, open load and short to ground protections are all set by a resistor divider on the VFB pin.

The open load is detected if the VFB pin is above the open load threshold (parameter $V_{VFB\_OL,rise}$ =1.34 V typ) and the output current is still below 10% of the maximum value (parameter $V_{FBH\_FBL\_OL}$ = 15 mV typ). To avoid undesired tripping of the open load protection, it is better to set the open load detection (V_{FB_OL} threshold) above the maximum application voltage (45 V in this application).

If this is not possible, because the maximum output voltage of the TLD5190 is needed, then the output overvoltage is intended to be the maximum application voltage. In this case, the user should check the application when VFB is at the $V_{VFB\_OL,rise}$ threshold. In case the open load condition occurs only at startup, while V_{OUT} rises to the target voltage, the open load could be masked by an adequate soft start timing.

It is possible to set the overvoltage and short to ground threshold independently by using a 3-resistor divider on the VFB pin, connected to V_{OUT} and V_{IVCC}. The open load threshold will fall as a consequence of the other 2 thresholds.

The overvoltage at the output (V_{OUT_MAX}) has to be set:

- Higher than the maximum load voltage
- Lower than the absolute maximum voltage of the TLD5190 FBL pin (60 V) and switching MOSFET M3-M4
- Possibly above the maximum expected battery voltage (see TLD5190 datasheet for details)

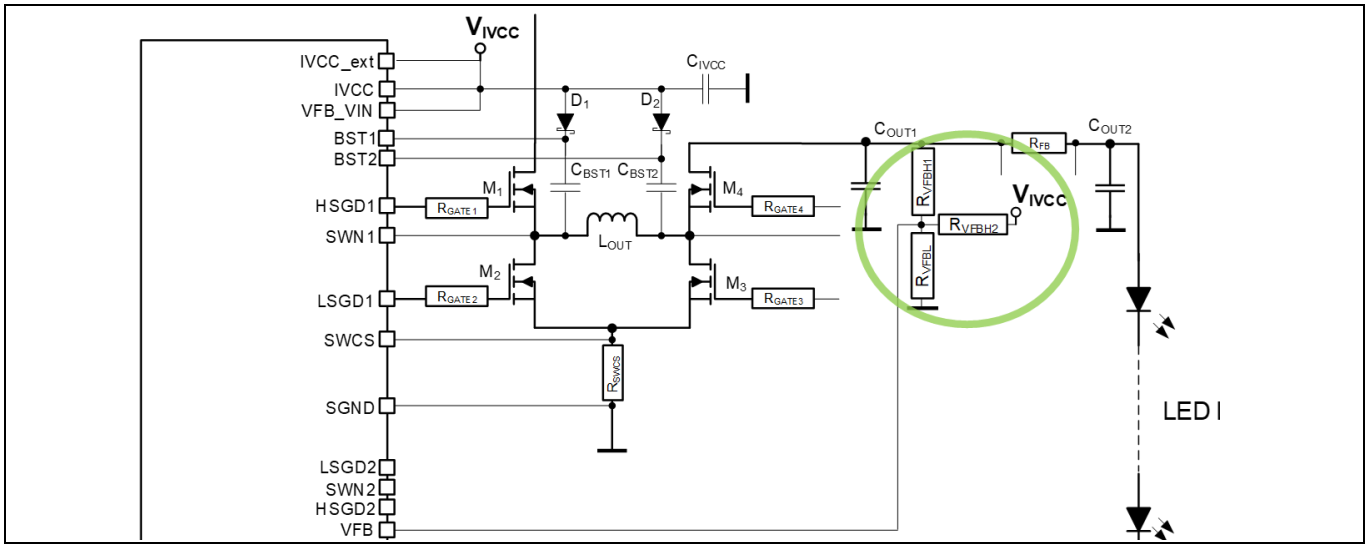


Figure 11 Overvoltage and short to ground voltage divider

The 3 resistors can be calculated manually resolving a system composed of the superposition principle on the VFB pin, summing the effect of V_{IVCC} and V_{OUT}. It is faster to calculate the resistors on the TLD5190 tool, by setting the desired overvoltage and short to ground thresholds.

In order to reduce the parasitic effects of moisture and leakage from the VFB pin, it is recommended to choose R_{VFBL} as the starting point equal to 1.5 kΩ 1%.

Setting on the Excel tool an output overvoltage of 52 V and a short to ground level of 5 V, the derived open load is 45.5 V (which fulfills the 45 V maximum voltage for this application). The calculated resistors for these thresholds are:

R_{VFBH1}= 69714 Ω and R_{VFBH2}= 14253 Ω

The commercial values (E96 series with 1% accuracy) close to the calculated ones are:

$$R_{VFBL} = 1.5\ k\Omega \quad R_{VFBH1} = 69.8\ k\Omega \quad R_{VFH2} = 14\ k\Omega$$

Producing an effective protections thresholds of (calculated by the Excel tool):

V_{OUT_MAX} = 51.75 V, V_{OUT_SHORT} = 4.61 V, V_{OUT_OL}= 45.45 V

With the Excel calculator it is also possible to check the effect of the overvoltage thresholds V_{OUT_OVTH} parameter deviations (Max, Min), by changing the value on V_{VFB_OV} cell.

3.2 Soft start capacitor

The soft start routine has 2 functionalities:

- Fault mask and wait-before-retry time
- Limit input inrush current and output overshoots at startup

The most relevant function of the soft start routine for LED drivers is only the fault (short to ground) mask at startup. At startup the output voltage is very likely 0 V therefore, without the fault mask, a short to ground would be detected.

Soft start duration is determined by the soft start capacitor C_{SST}. Minimum value for soft start capacitor shall be designed to grant short circuit mask at startup. Therefore the output voltage must exceed the short to ground threshold (V_{OUT_SHORT} will be set to 5 V in Chapter 3.1), before the soft start expires meaning that V_{SST} voltage reaches $V_{Soft\_Start\_LOFF}$.

The only side effect on a LED driver for a long soft start time, is a longer fault retry time, therefore, to be on the safe side it is suggested to choose a soft start capacitor larger than the minimum necessary. A simplified formula which provides a sufficient startup fault mask is:

$$C_{\mathrm{SST}} \geq 2\ C_{\mathrm{COMP}}$$

If the soft start time is higher than the minimum needed for S2G mask, it also limits inrush current. In addition this masks possible open load detection at startup, in case of load close to the overvoltage protection. In this application **C_{SST} = 47 nF** has been chosen.

If a shorter retry time is needed C_{SST} could be reduced to $C_{\mathrm{SST}} = C_{\mathrm{COMP}}$ but the effectiveness of soft start should then be tested in the real application. Minimum application temperature and input voltage shall be considered as worst-case condition for previously mentioned dimensioning.

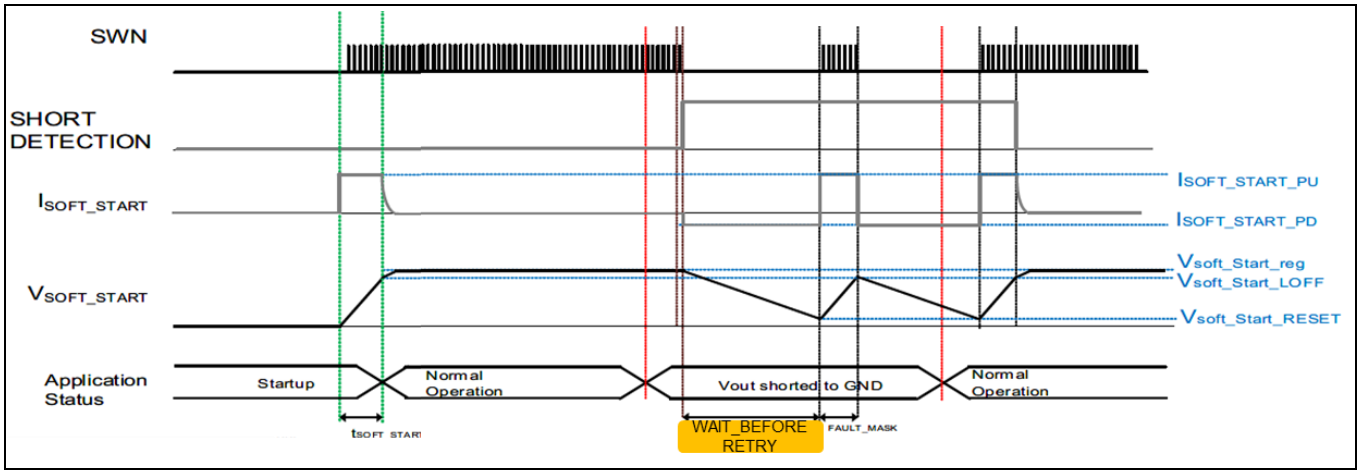


Figure 12 Wait before retry time

Wait time before retry (t_{retry}) in case of a fault will be:

$$t_{retry} = (V_{Soft_{Start_{LOFF}}} - V_{Soft_{Start_{RESET}}}) \frac{C_{SST}}{I_{Soft_{Start_{PD}}}} = (1.75\,V - 0.2V)\,\frac{47nF}{2.6uA} = 29\,ms$$

The first retry time after a fault is slightly longer than the following times, because the soft start capacitor during regulation stays at $V_{Soft\_Start\_REG}$ instead of $V_{Soft\_Start\_LOFF}$. In addition, the first rise time of the soft start after power on is different from the successive retry rise time, because the soft start capacitor voltage starts from 0 V instead of $V_{Soft\_Start\_RESET}$.

3.1 Input undervoltage and overvoltage protections

The input voltage requirement for the LED driver module is 6 V to 35 V (extended range) therefore, the input undervoltage and overvoltage protections must be set based on these thresholds on the EN/INUVLO and INOVLO pins. The 2 relevant thresholds are $V_{INOVLOth}$ and $V_{EN/INUVLOth}$.

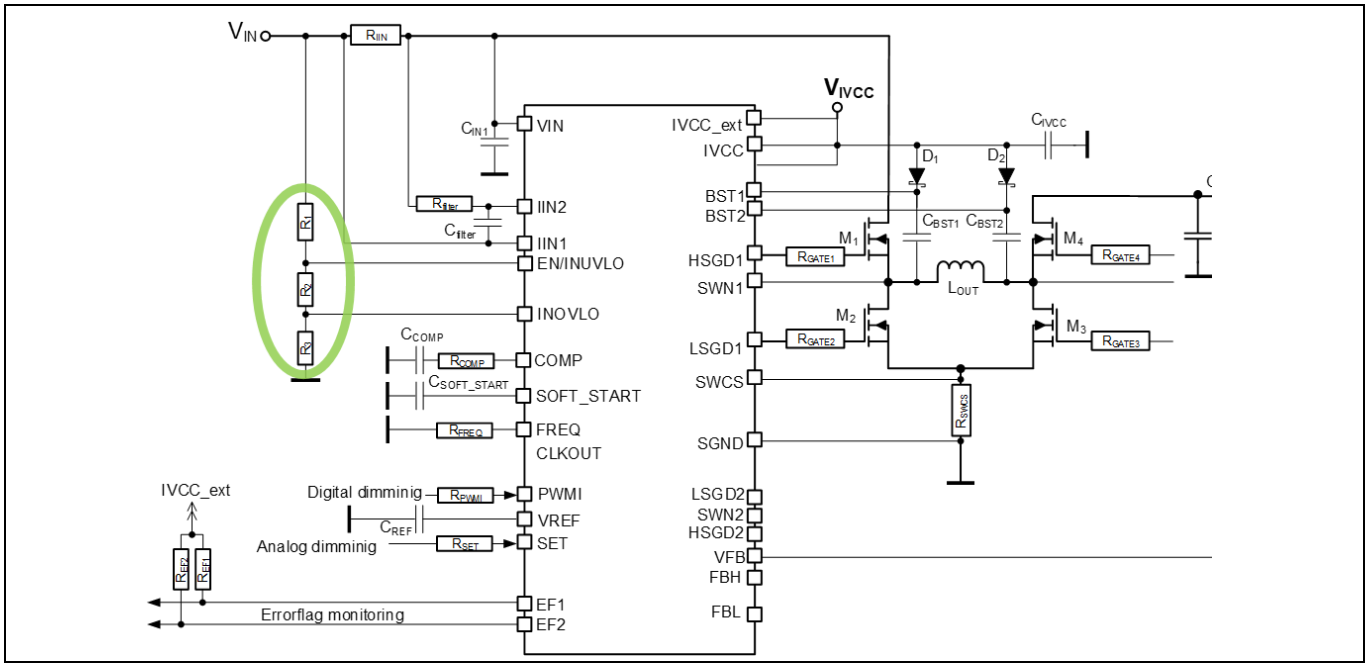


Figure 13 EN/INUVLO and INOVLO resistor divider

For this application, an undervoltage threshold of 5.5 V (entry threshold, V_{IN} falling) while the input overvoltage threshold has been set to 37 V, above the 35 V maximum operating request for the module. The low-side resistor should be in the range of 2 kΩ to 10 kΩ to avoid excessive leakage current and to provide an accurate threshold.

Choosing **R3 = 2.2 kΩ** as low-side voltage divider resistor, the high-side resistors (R1 and R2) are calculated by the Excel component calculator as

R_2= 10750 Ω and R_1= 27750 Ω

The commercial values (E96 series with 1% accuracy) close to the calculated values are:

$$R_2 = 10.7\ k\Omega \qquad R_1 = 27.4\ k\Omega$$

In case the input overvoltage protection is not needed, INOVLO pin can be shorted to ground leaving only 2 resistors at the EN/INUVLO pin, which are calculated as:

$$R2 = 2.2\ k\Omega \qquad R1 = R2 \cdot \frac{UV_{th} - EN/INUVLO_{th}}{EN/INUVLO_{th}} = 2.2k \cdot \frac{5.5V - 1.75V}{EN/INUVLO_{th}} = 4714\ \Omega$$

3.2 Input current sense and limiter resistor

The input current of the application can be measured and limited by the TLD5190 with a shunt resistor (R_{IIN}) via IIN1 and IIN2 pins. IIN1 is the positive sense terminal, IN2 is the negative sense terminal.

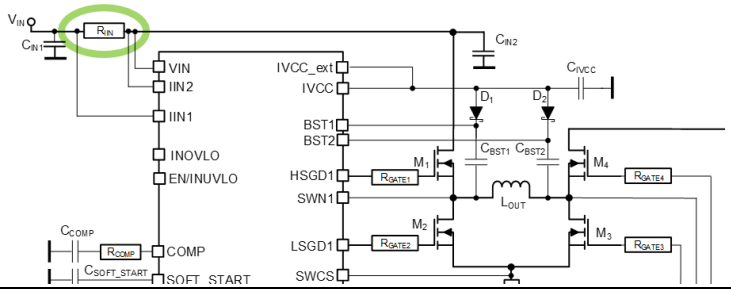


Figure 14 Input current monitor resistor

IINMON pin produces a voltage proportional to $V_{IIN1\text{-}IIN2}$ following this equation:

$$V_{IINMON(typ)} = I_{IN} \cdot R_{IIN} \cdot 20$$

The control loop reduces the V_{COMP} when the voltage $V_{IIN1\text{-}IIN2}$ reaches input current sense threshold $V_{IIN1\text{-}IIN2}$ to keep the input current below a certain limit (I_{INMax}).

If the input current monitor is used only for monitoring the input current, then R_{IIN} should be dimensioned so that the maximum current needed by the application is provided, at the worst case (minimum $V_{IIN1\text{-}IIN2}$).

$$R_{IIN} <= \frac{V_{IIN1-IIN2}(min)}{I_{IN(max)}} = \frac{46mV}{5.4\ A} = 8{,}5\ m\Omega$$

Where:

$$I_{IN(max)} = \frac{P_{OUT\_max}}{V_{IN\_min} \cdot eff} = \frac{45W}{9 \cdot 93\%} = 5.4\ A$$

Efficiency at 9 V input voltage has been calculated with the TLD5190 Excel component calculator. A standard resistor value close to the calculated one could be R_{IIN} **= 8 mΩ**.
The R_{IIN} has to be dimensioned differently if the application specifies a defined maximum input current for example, $I_{IN\_LIMIT} = 4$ A, in this case, R_{IIN} should be calculated as:

$$R_{IIN} = \frac{V_{IIN1-IIN2}(typ)}{I_{IN\_LIMIT}} = \frac{50mV}{4\ A} = 12.5\ m\Omega$$

The current sensed by IIN1, IIN2 can be monitored through IINMON pin. The IINMON pin output impedance is about 36 kΩ (typ). If IINMON is not used, leave it open, while IIN1, IIN2 pins should be connected to VIN.

4 Compensation network

In this chapter the TLD5190 Excel component calculator is used to quickly calculate the compensation network. With this tool several operating conditions and compensation networks can be quickly verified.

In the next chapter the main stability equations are provided for an analytical approach.

SIMETRIX average model of the TLD5190 it is available on the TLD5190 webpage, and it can be used to verify the behavior of the device for the application circuit.

Good practice is to dimension the external components and check stability in the corner cases, for example at minimum V_{IN} and maximum V_{OUT}, and maximum V_{OUT} and minimum V_{IN}.

The RC compensation network is applied to the COMP pin (proportional and integral compensation).

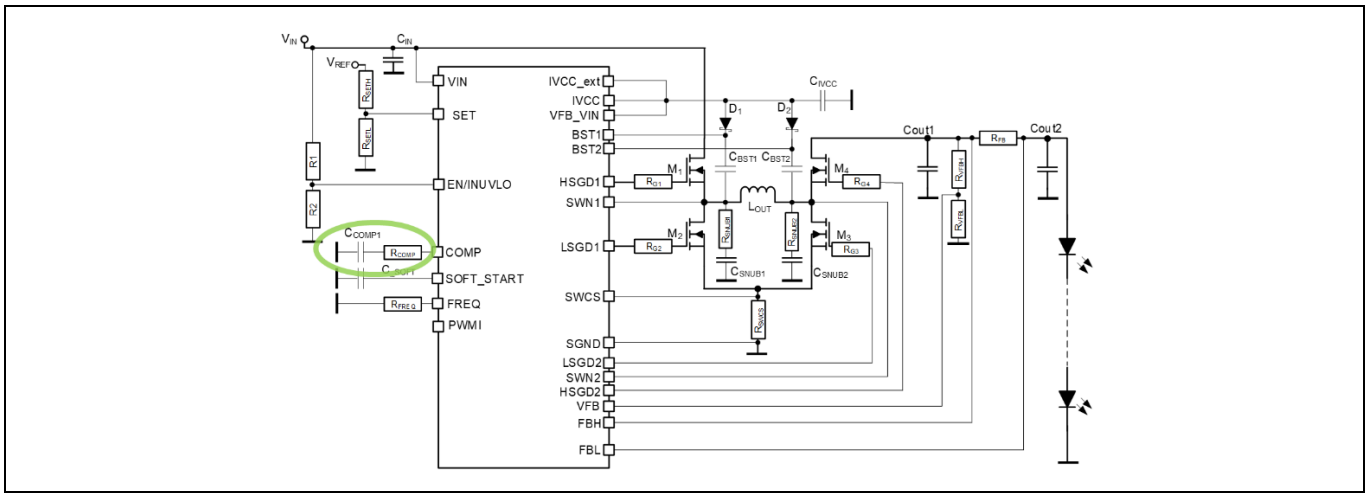


Figure 15 Compensation network

Inside the device, at the COMP pin, there is approximately 1.7 kΩ built in series resistor. For this application, with the given inductor and output capacitor, a good compromise for stability and transient response has been found with **22 nF C_{COMP}** and **0 Ω R_{COMP}** at the external compensation network. To further improve the phase margin and PSRR, it is suggested to apply a small capacitor C_{OUT2} after the sensing resistor. This capacitor amplifies a possible variation in the output voltage at the sensing pins FBH and FBL, and it improves the phase margin. On the other hand, also the V_{OUT} ripple is amplified at FBH and FBL when C_{OUT2} is applied, this may lead to erroneous output current regulation if the capacitor is too big and the output ripple is high. As a rule of thumb C_{OUT2}=1/20 to 1/10 of C_{OUT1}. For this application **C_{OUT2} = 1 µF** has been chosen, the effect is immediately visible using the Excel component calculator.

Stability section	SYMBOLS	VALUES	UNITS
Analog dimming SPI word (decimal value 0 -- 255)		240	
SET Voltage (used on Efficiency and stability)	V_{SET} =	1,40	V
Analog dimming current stability & efficiency	$I_{OUT(AD)}$ =	1,50	A
Output voltage Vout analog dimming	$V_{OUT(AD)}$ =	23,75	V
DC-Gain	T_0 =	77,13	dB
Cut frequency	f_C =	13,0	kHz
Phase-Margin	PM =	62,56	deg
Gain-Margin	GM =	10,17	dB

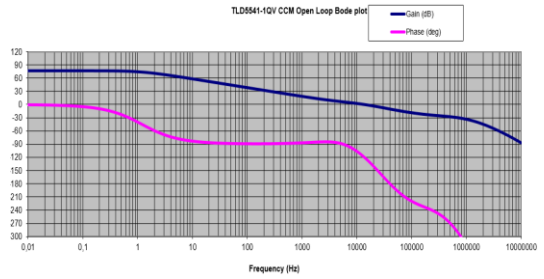


Figure 16 Example bode plot and stability section from the TLD5190 Excel component calculator [1]

For illustration purposes, Figure 16 shows a screenshot of the Excel component calculator bode plots and stability section with 8 white LED (modeled with V_{LED_th} = 2.8 V and R_{LED} = 0.1 Ω) and 12 V input voltage.

For applications with wide output voltage span, it is recommended to verify the stability in several load conditions and input voltages. It is common practice to consider a system stable when the phase margin is above 40°.

4.1 Stability tips

Phase margin could be improved by tuning some key components shown in Figure 17.

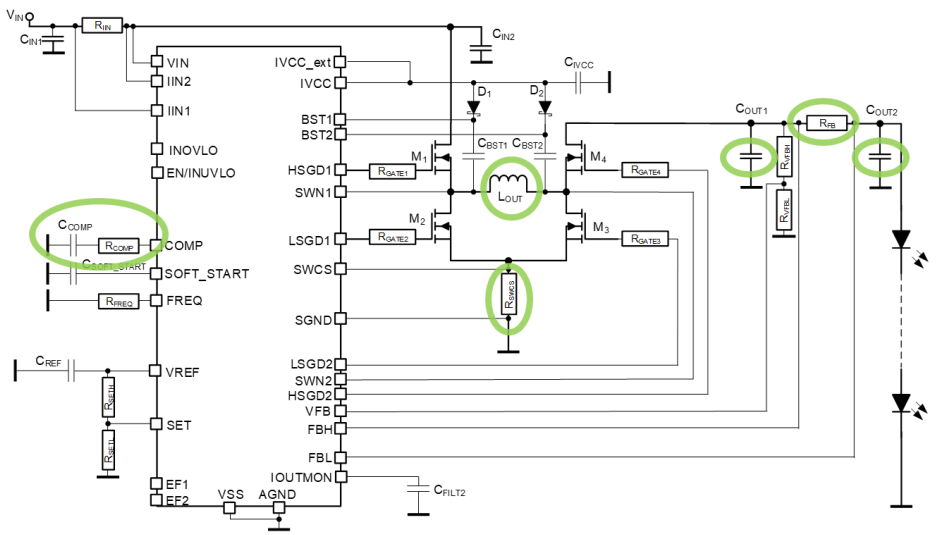


Figure 17 Components that can be tuned to improve stability

Each component may have some benefit, however there are also drawbacks in other aspects. The effect can be checked with the Excel component calculator for the specific operating point.

Table 2 Effect of tuning key components

Component	Improvement	Drawback
Increasing R_{SWCS}	Phase margin and enhance response to battery variation	Reduced maximum output power
Increasing C_{COMP}	Phase margin	Slower response to battery variations
Decreasing R_{COMP}	Possible improvement of margin in buck region	Possible reduced stability in boost mode, enhanced response to battery variation
Increasing R_{COMP}	Possible improvement of margin in boost region	Possible reduced stability in buck mode, enhanced response to battery variation
Increasing C_{OUT2} capacitor (cap. placed after sensing resistor)	Increases phase margin in both buck and boost mode	Lowers cut frequency
Increasing C_{OUT1} capacitor		It has different and sometime opposite impact in buck mode or in boost mode

4.2 Stability equations

Below, the stability equation for the TLD5190 regulation loop are provided. The modulator transfer function can be expressed as the product of two main parts: the gain of the error amplifier and the gain of the current mode modulator:

$$T(s) = (A_{EA}(s) \cdot A_{CM}(s) \cdot \beta)$$

The equations are different if the device operates in boost mode or in buck mode.

Error amplifier frequency response:

The gain of the error amplifier is described with the following formula:

$$A_{EA}(s) = g_{m\_EA} \cdot R_{EA} \cdot \frac{(1 + s \cdot \tau_{z1})}{(1 + s \cdot \tau_{p1})}$$

Where

- g_{m_EA} is the trans-conductance of the error amp. (A5, A6 with comprehensive gain $IFBx_{gm}$ = 890 µS typ)
- R_{EA} is the output resistance of the error amplifier (TLD5190 R_{EA} = 6 MΩ typ)
- $\tau_{z1} = C_{\mathrm{COMP}} \cdot (R_{\mathrm{COMP\_INT}} + R_{\mathrm{COMP}})$ is the zero of compensation network
- $R_{\mathrm{COMP\_INT}}$ is the internal compensation network resistance (1.7 kΩ typ)
- $\tau_{p1} = (C_{\mathrm{COMP}}) \cdot R_{EA}$ is the pole associated to compensation network and the resistor of error amplifier

Boost operating mode stability equations:

The gain of the current mode modulator can be described following the model presented by R.B Ridley [2].

Mathematically, it is described as:

$$A_{CM\_boost}(s) = \frac{0.17 \cdot (1 - D) \cdot R_{LOAD}}{\left(1 + \frac{I_L \cdot (1 - D) \cdot R_{LOAD}}{V_{OUT}}\right) \cdot R_{swcs}} \cdot \frac{(1 + s \cdot \tau_{z2})}{(1 + s \cdot \tau_{p3}) \cdot \left(1 + \frac{s}{\omega_n \cdot Q} + \frac{s^2}{\omega_n^2}\right)}$$

$$A_{CM\_boost}(s) = \frac{0.17 \cdot (1-D) \cdot R_{LOAD}}{\left(1 + \frac{V_{REF} \cdot R_{loadLOAD}}{V_{OUT} \cdot R_{FB}}\right) \cdot R_{swcs}} \cdot \frac{(1 + s \cdot \tau_{z2})}{(1 + s \cdot \tau_{p3}) \cdot \left(1 + \frac{s}{\omega_n \cdot Q} + \frac{s^2}{\omega_n^2}\right)}$$

$$I_L = \frac{V_{REF}}{R_{FB}(1-D)}$$

Where:

- R_{LOAD} is the total resistor at the output of DC-DC and it is the sum of R_{FB} and R_{LED_string}
- V_{REF} is the voltage reference across FBH and FBL (typical 150 mV)
- V_{OUT} is the voltage on LED string V_{LED} plus input voltage V_{IN} (Voltage across PMOS has been neglected)
- $\tau_{z2} = -\frac{L_{BO}}{(1-D)^2} \cdot \frac{(I_{OUT})}{(V_{OUT})}$ is the zero (RHP) of the boost DC-DC with the return to battery
- $\tau_{p3} = C_{OUT} \cdot R_{LOAD} \cdot \frac{V_{OUT}}{I_{OUT} \cdot R_{LOAD} + V_{OUT}}$ is the pole associated with boost converter with the return to battery
- $\omega_n = \pi \cdot \frac{f_s}{2}$ is the natural pulsation of the system
- $Q = \frac{1}{\pi \cdot \left(\left(1 + \frac{S_e}{S_n}\right) \cdot (1-D) - 0.5\right)}$ is the quality factor of a second order system, where S_e is the slope of current compensation circuit (coefficient fixed by internal references) and S_n is the slope of the current sensed by R_{swcs}.

$$S_e = 60 \cdot 10^{-3} \cdot f_{sw}$$

$$S_n = \frac{V_{IN} \cdot R_{SWCS}}{L_{BO}}$$

The transfer function of the feedback network is the ratio between R_{FB} and the R_{LED}

$$\beta = \frac{R_{FB}}{R_{FB} + R_{LED_{string}}}$$

Buck operating mode stability equations:

In buck mode, the gain of the error amplifier remains the same of the boost mode described above.

the current mode gain can be mathematically approximated as:

$$A_{CM\_buck}(s) = \frac{0.17 \cdot R_{LOAD}}{R_{swcs}} \cdot \frac{1}{(1 + s \cdot \tau_{p3}) \cdot \left(1 + \frac{s}{\omega_n \cdot Q} + \frac{s^2}{\omega_n^2}\right)}$$

Where:

- R_{LOAD} is the total resistor at the output of DC-DC and it is the sum of R_{FB} and R_{LED_string}
- V_{REF} is the voltage reference across FBH and FBL (typical 150 mV)

- V_{OUT} is the voltage on LED string V_{LED} plus input voltage V_{IN} (Voltage across PMOS has been neglected)
- $\tau_{p3} = C_{OUT} \cdot R_{LED}$ is the pole associated to buck converter with the return to battery
- $\omega_n = \pi \cdot \frac{f_s}{2}$ is the natural pulsation of the system
- $Q = \frac{1}{\pi \cdot \left(\left(1+\frac{S_e}{S_n}\right) \cdot D - 0.5\right)}$ is the quality factor of a second order system, where S_e is the slope of current

Compensation circuit (coefficient fixed by internal references) and S_n is the slope of the current sensed by R_{SWCS}.

$$S_e = 60 \cdot 10^{-3} \cdot f_{sw}$$

$$S_n = \frac{V_{OUT} \cdot R_{SWCS}}{L_{BO}}$$

Using the data previously calculated, it is possible to calculate the gain in DC and cross-over frequency f_c and the phase margin.

The transfer function of the feedback network is the ratio between R_{FB} and the R_{LED}

$$\beta = \frac{R_{FB}}{R_{LED\_string}}$$

5 EMC

5.1 Spread spectrum

The TLD5190 offers a spread spectrum modulation that significantly improves the EMC in the lower frequency range of the spectrum (f < 30 MHz). Spread spectrum is disabled by default and can be enabled by setting the register, ENSPREAD to 1, via SPI. Deviation frequency is set by FDEVSPREAD and modulation frequency is set by FMSPREAD via SPI, see TLD5190 datasheet [3] for details.

The effect of the spread spectrum and the FDEVSPREAD register is evident in Figure 18. In this EMC test report the emission peaks are reduced by 10 dB and more. Hereby, class 5 limits pass.

Larger deviations; in percent, and modulation frequency, lower but widen the emissions peaks. Depending on the switching frequency and regulator limits the shape of the emission can be modified for best convenience.

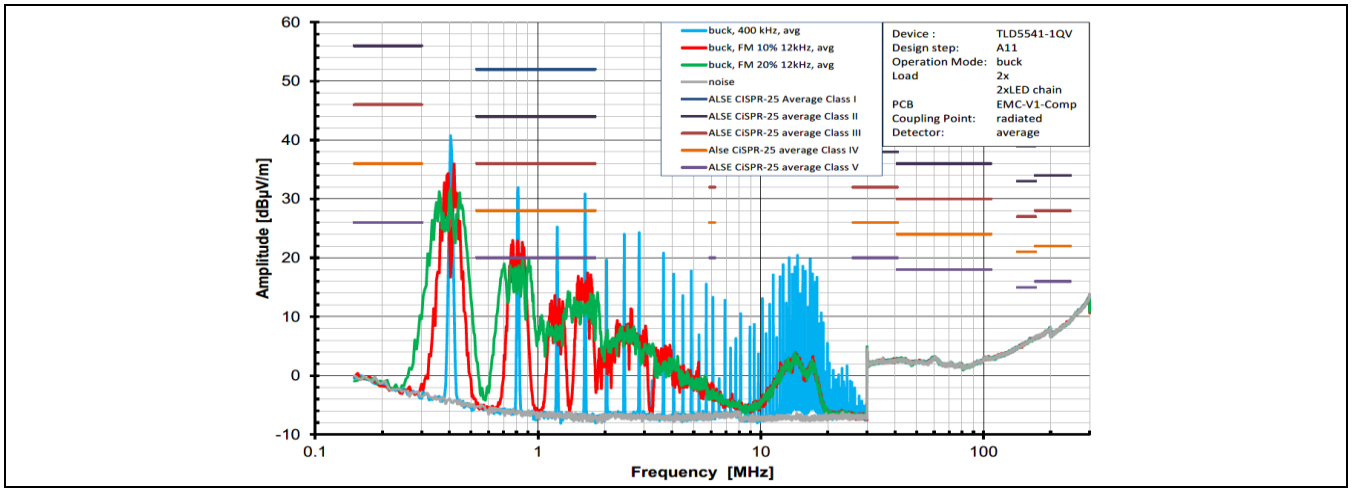
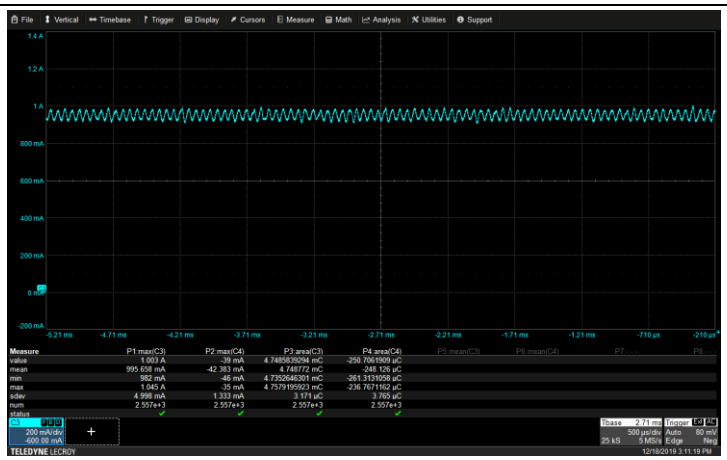


Figure 18 Spread spectrum effects on radiated emission

The effect of the spread spectrum on the output current is a ripple with the deviation frequency, which does not produce any visible flicker.



Condition	Value
LOAD	2 LED
CURRENT	1A
REGISTER: FDEVSPREAD	1 (8% deviation)
REGISTER: FMSPREAD	1 (18kHz modulation)
f_{SW}	400kHz
V_{IN}	18V

Figure 19 Spread spectrum I_{OUT} ripple

A widely adopted setting for the 2 spread spectrum configuration bit, which is a good compromise of ripple and EMC attenuation is:

- FDEVSPREAD = 1 (8% of f_{sw})
- FMSPREAD = 1 (18 kHz)

5.2 Gate driver resistors

Gate driver resistors are placed at the gate driver output in order to improve EMC performances. Rules for the gate driver resistor dimensioning are as for any standard DC-DC controller. The effect of these resistors is to reduce switching speed and ringing at the switching nodes. Gate driver resistors impact the efficiency of the DC-DC converter, and they should be increased only to pass the target EMC regulation (for example, CISPR25).

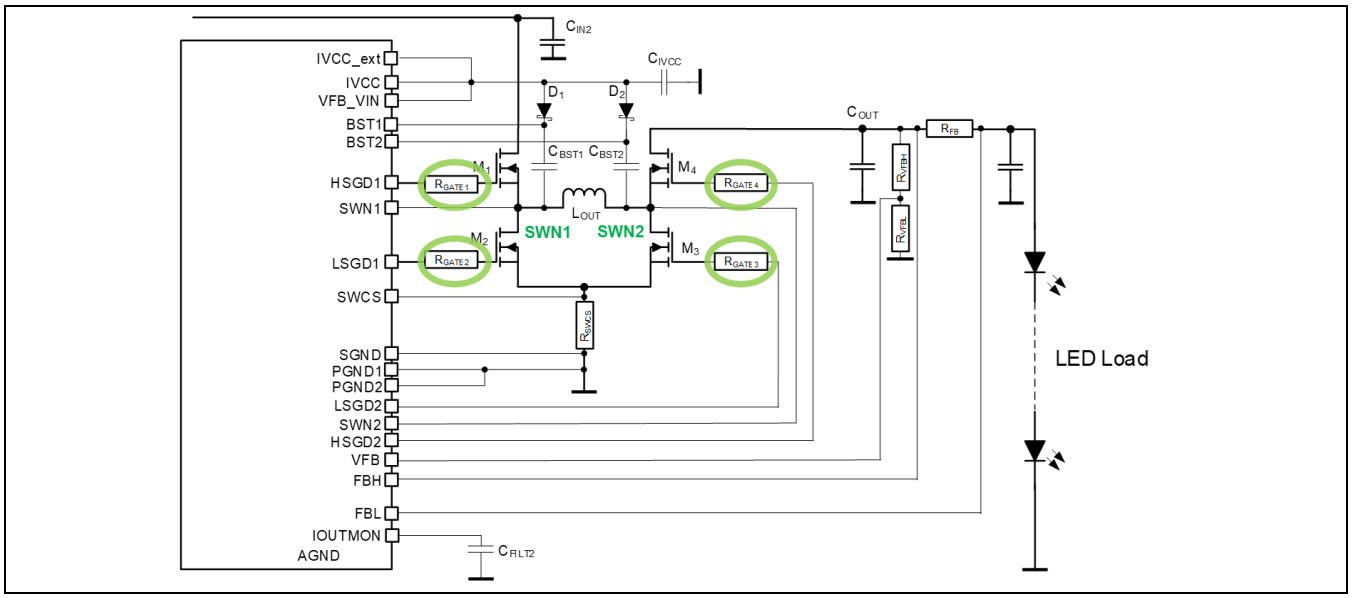


Figure 20 Gate driver resistors

The high-side gate driver resistor R_{GATE1} impacts only the rise time of the buck switching node (SWN1). At the boost side, the low-side gate driver resistor R_{GATE3} impacts the falling time of the boost switching node (SWN2).

As starting point for good EMC performance (Class 5 CISPR 25), the buck switching node rise-time and boost switching node fall-time, should be in the 10 ns to 50 ns range. The final EMC result depends on output voltage, switching frequency, PCB layout, cable length and other application parameters. Therefore, gate resistors should be tuned in the final application, after an EMC measurement.

With the current MOSFET choice, a 22 Ω gate resistor has been selected as starting point, with a measured rise time for the buck switching node of approximately 18 ns with a 4 LED load.

The impact of the efficiency is calculated with the TLD5190 Excel component calculator, at the maximum output power 45 W (30 V 1.5 A):

- 93.4% with 22 Ω gate resistor
- 95.65% with 0 Ω gate resistor

This resistor value could be increased or decreased after EMC measurement.

5.3 Layout considerations

For a DC-DC converter, the PCB design is a critical task as well as the component selection. Even if the circuit topology and components selection are good, if the PCB layout is not good enough, the performances of the whole system will be lower than expected.

A proper layout is also the basis for good EMC performances. The most important PCB layout rules are explained in a dedicated application note, "*LITIX™ PCB design guideline document*" [4]. Figure 21 depicts a screenshot of this application.

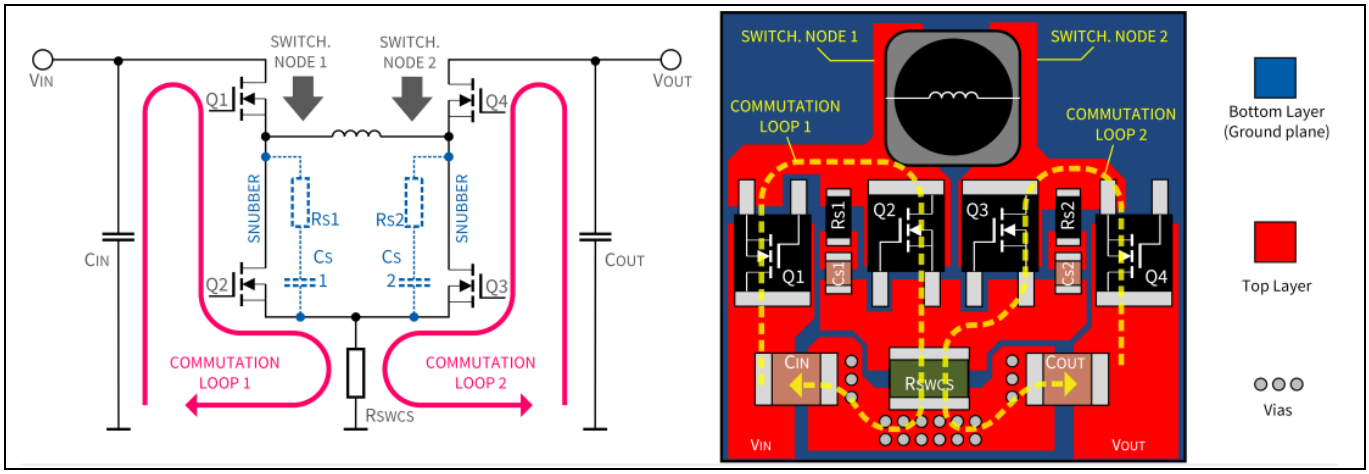


Figure 21 Hot loops and recommended layout for H-bridge topology

Differential net, in the TLD5190 circuitry 3 differential amplifiers are present

- FBH - FBL
- SGND – SWCS
- IIN1 – IIN2

The nets to these pins should be routed as differential net. Special attention to the SGND pin, it is not a ground signal, so it should not be tied to a ground plane, but the negative input of a differential amplifier, so it should be connected directly at the RSWCS resistance, which is then connected to a ground plane.

These nets work on small signals and affect the regulation, so they should be routed far from the switching nodes or the bootstrap nets.

6 List of references

[1] Infineon LITIX™ Power Flex

[2] Ridley, R. B.; *A new Continuous Time Model for Current Mode Control*; IEEE Transaction on Power Electronics; Vol. 6; Issue 2; pp. 271-280; 1991

[3] Infineon TLD5190 DS Rev.1.10

[4] Infineon Z8F80033952 LITIX™ PCB design guidelines AN Rev.1.00

Revision history

Major changes since the last revision

Page or Reference	Description of change
2021-05-31	Initial release

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