TLD5542-1

LED driver in buck-boost topology

About this document

Scope and purpose

This document explains how to design an LED driver using a TLD5542-1 for a powerful and efficient design. The application requirements, used as an example, could be for a typical automotive low beam LED driver ECU.

The TLD5542-1 is an H-bridge buck-boost controller designed to build high power and high efficiency LED drivers in automotive applications. It also includes built in diagnosis and protection features and spread spectrum modulator.

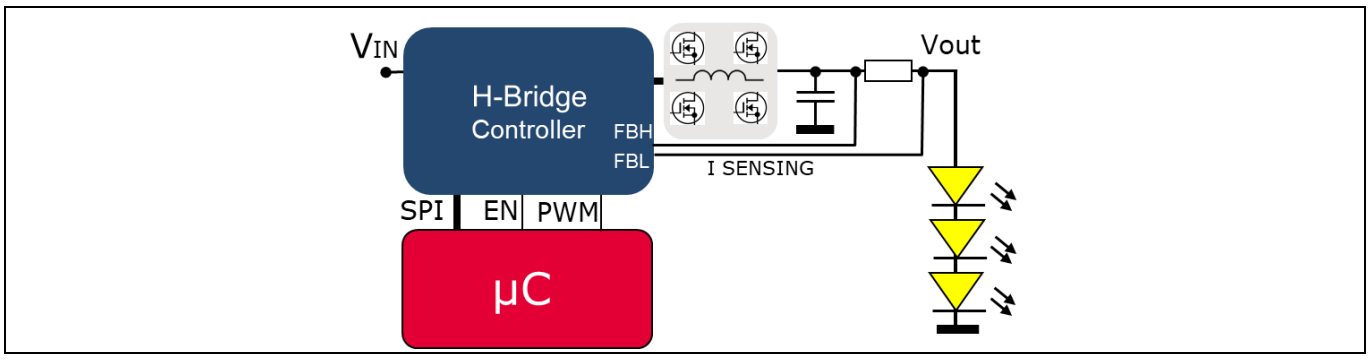

Figure 1 TLD5542-1 controller as LED driver

Intended audience

HW designers, LED system architects for LED lighting applications

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1 Introduction

An explanation for how to derive external components for a specific TLD5542-1 application will be given. All DC-DC equations, for a deeper understanding of the circuit, are included.

For fast calculation it is possible to use the Infineon TLD5542-1 LED component calculator excel [1] available on the TLD5542-1 Infineon website [2]. All TLD5542-1 external components, currents, efficiency, maximum power and stability are calculated with minimum effort.

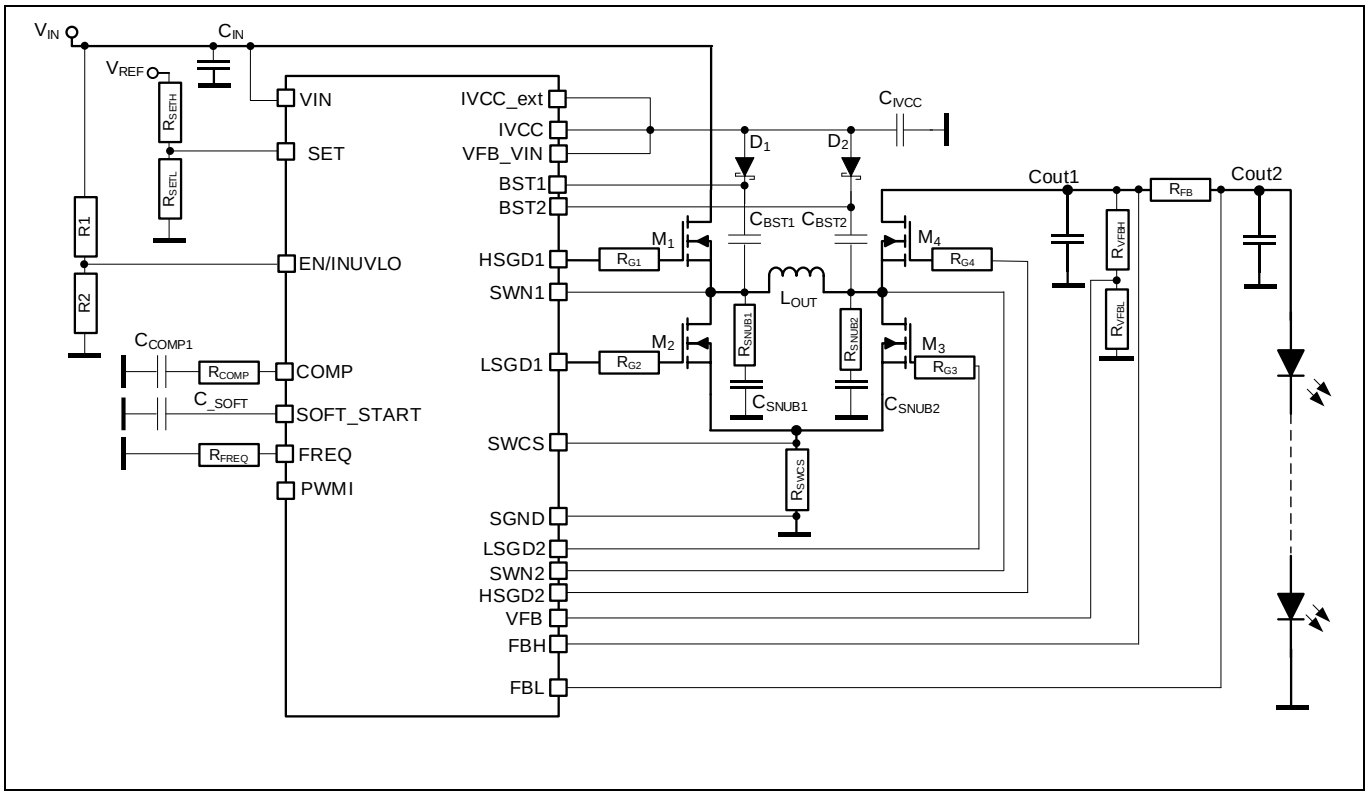


Figure 2 Application diagram - TLD5542-1 as LED driver

The core of the DC-DC is a current mode controller with compensation capacitor. Therefore, the dimensioning of external components is similar to a standard boost converter.

Careful selection of external components has to provide the best compromise between efficiency, stability, EMC and cost in all operating conditions.

1.1 Application example

The LED driver module (LDM) with TLD5542-1 designed in this application note will have the following specifications to drive a powerful automotive low beam function.

Table 1 LDM requirements

Parameter	Symbol	Value			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Input voltage	V_{IN}	6	13.5	35	VV	Extended range
		9	13.5	16	V	Operating range
Output voltage	V_{OUT}	5	–	50	V	–
Output current	I_{OUT}	700	–	1500	mA	–
Output power	P_{OUT}	5	–	45	W	V_{IN} 9 V to 35 V, T_A = 25°C Power derating applies for V_{IN} < 9 V
Switching frequency	f_{SW}	–	385	–	kHz	–
System efficiency	η	–	95	–	%	V_{IN} = 13.5 V LED mode: 6 LED, I_{OUT} = 1500 mA,

2 External component design

2.1 Inductor

The inductor in a boost converter is designed based on the specified average and ripple current. Usually, the ripple current is in the range of 20% to 40% of the average value at the maximum rated power.

The inductor value depends on the switching frequency. Increasing the switching frequency allows smaller inductor and output capacitors, however increasing the switching frequency increases switching losses.

A high inductor value results in:

- Reduced core losses (which depend on ripple value)
- Reduced conduction losses on MOSFET (smaller ripple current)
- Improved light load efficiency
- Increased conduction losses on inductor (higher inductor DCR if same dimension is kept)
- Reduced stability (more delay between regulation duty cycle change and effective current change)
- Reduced loop speed

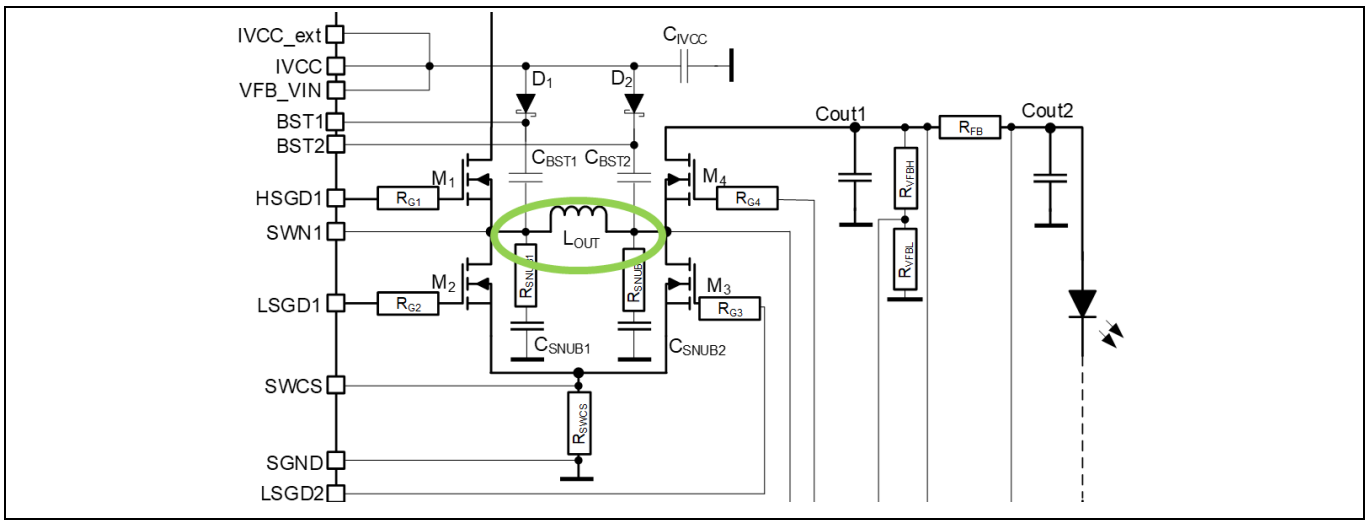


Figure 3 Main switching inductor

In this application 40% ripple current has been chosen, to minimize inductor size. An approximate efficiency of 95% is used in order to calculate the inductor current.

The following equation determines the inductor value to obtain the required ripple current with typical input voltage and maximum output power (P_{OUT} = 45 W, $V_{OUT\_max,P}$ = 30 V, I_{OUT} =1.5 A).

$$L_{MIN} = D_{TYP} \cdot \frac{V_{IN_{TYP}}}{\Delta I_{L_{pkpk\_typ}} \cdot f_{sw}} = 0.55 \cdot \frac{13.5\ V}{1.4A \cdot 385\ kHz} = 13.2\ \mu H$$

where

$D_{TYP} = \frac{V_{OUT\_maxP} - V_{IN\_typ}}{V_{OUT}} = 0.55$

$$\Delta I_{L_{pkpk\_typ}} = 40\%\, I_L = 0.4 \cdot I_{IN} = 0.4 \cdot \frac{P_{OUT\_max}}{V_{IN} \cdot \eta} = 0.4 \cdot \frac{45W}{13.5V \cdot 0.95} = 1.4A$$

The actual peak current in worst case condition (when minimum input voltage and maximum output power is applied) can be calculated as:

$$I_{L_{peak}} = I_{IL\_AVG\_MAX} + \frac{\Delta I_{Lpkpk_{vinmin}}}{2} = 5.4\ A + 1.09\ A = 6.49\ A$$

Where, in boost mode $I_L = I_{IN}$, assuming efficiency is a little lower (approximately 93%) for V_{IN} = 9 V

$$I_{L\_AVG\_MAX} = I_{IN\_AVG\_MAX} = \frac{P_{OUT\_max}}{V_{IN\_min} \cdot \eta} = \frac{45W}{9 \cdot 93\%} = 5.4\ A$$

$$\Delta I_{Lpkpk\_vinmin} = D_{MAX} \cdot \frac{V_{IN_{MIN}}}{L \cdot f_{sw}} = 0.7 \cdot \frac{9\ V}{15\ \mu H \cdot 385\ kHz} = 1.09\ A$$

$$D_{MAX} \approx \frac{V_{OUT_{maxP}} - V_{IN\_min}}{V_{OUT_{maxP}}} = 0.7$$

The important key parameters to select an inductor are then:

- Inductance > 13 µH
- Saturation current and RMS current > 6.49 A

An inductor that fulfills above requirements is the **15 µH** TDK SPM10065VT-150M-D.

Efficiency, minimum inductor value, inductor currents and ripples can be quickly calculated using the Infineon TLD5542-1 LED component calculator excel [1].

2.2 Output capacitors

The output capacitor acts as an energy tank when M4 is off and for this reason it is subject to a high ripple current. This component affects the bandwidth of the system and also the output current ripple performance. Usually, for this kind of application, multilayers ceramic capacitors (X7R - MLCC) with low ESR are preferred over electrolytic capacitors.

Dimensioning of C_{OUT} is mainly driven by the output voltage ripple ΔV_{OUT}. Worst case condition for the output ripple is when the device is in boost mode (output current discontinuous), minimum input voltage, maximum output current and maximum output power.

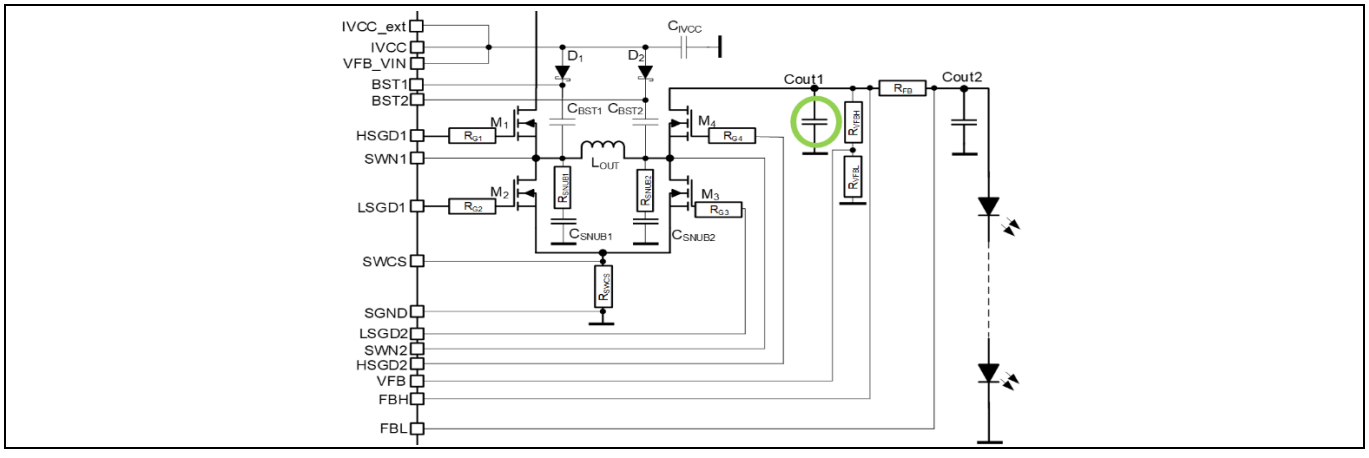


Figure 4 Output capacitors

In boost mode the capacitor is discharged by a constant current equal to average output current, for a time equal to $t_{ON} = D_{MAX}/f_{SW}$.

Assuming an ideal capacitor ($R_{ESR} = 0\ \Omega$) its value can be calculated from the desired output voltage ripple in worst case condition:

$$C \geq \frac{I_{OUT}}{\Delta V_{OUT}} \cdot \frac{D_{MAX}}{f_{sw}} = \frac{1.5A}{0.2\ V} \cdot \frac{0.7}{400\ kHz} = 13.0\ \mu F$$

The ESR of the output capacitor adds more ripple, given with the equation:

$$\Delta V_{OUT_{ESR}} = ESR \cdot I_{L_{peak}} = ESR \cdot \left(\frac{I_{OUT}}{1 - D_{MAX}} + \frac{\Delta I_{Lpkpk_{vinmin}}}{2}\right)$$

From the equations above, it is possible to calculate the maximum ESR so that ESR contributes 20%; as a rule of thumb, of C_{OUT} ripple.

$$R_{ESR} \leq \frac{\Delta V_{ESR}}{I_{L_{peak}}} = \frac{0.2 \cdot \Delta V_{OUT}}{6.25A} = \frac{0.1 \cdot 0.2\ V}{6.25A} = 6\ m\Omega$$

A parallel **3 x 4.7 µF X7R** capacitor can fulfill required capacitance and series impedance.

Note: MLCC capacitors show a strong variation of the capacitance as a function of the applied voltage. A X7R 100 V capacitor shows up to 30% drop at 30 V bias.

2.3 MOSFETs

Switching MOSFETs must be logic level, and must withstand at least the maximum current calculated for the inductor sizing in Chapter 2.1:

$$I_{SW\_peak} = I_{L_{peak}} = I_{IL\_AVG} + \frac{\Delta I_{Lpkpk_{vinmin}}}{2} = 5.2\ A + 1.05\ A = 6.25\ A$$

Voltage class on the buck (input) side must be higher than the maximum input voltage (35 V). At the boost (output) side, voltage class must be higher than the maximum output voltage (50 V).

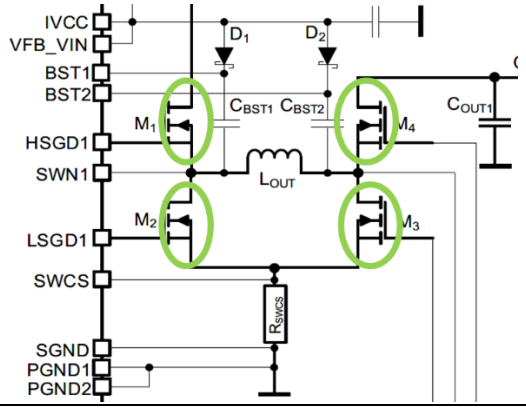


Figure 5 Switching MOSFETs

Note: Choosing a very low $R_{DS(ON)}$ MOS it is not always the best choice. The optimum $R_{DS(ON)}$ shall balance switching losses and conduction losses, improving the efficiency. Efficiency on several MOSFETs can be easily compared during MOSFET selection process using the excel component calculator [1].

In this design focus is on the highest efficiency, so a **7 mΩ 40 V MOSFET** has been chosen for the buck side (Infineon IPZ40N04S5L-7R4) and a **14 mΩ 60 V MOSFET** has been chosen for the boost side (Infineon IAUZ30N06S5L140). These MOSFETs have low parasitic capacitances with low reverse recovery charge (Q_{rr}) providing a 96% efficiency at V_{IN} = 13.5 V V_{OUT} = 30 V 1.5 A.

Note: For EMI reasons, it is common practice to place a resistor (R_{GATE}) of approximately 5 Ω to 15 Ω in series depending on the gate charge and EMI performance of the circuit. This helps to reduce the current spikes into the gate and also to have a smooth transition from OFF state to ON state. On the other hand, this lowers the overall efficiency of the converter.

2.4 Switch current limiter R_{SWCS}

The TLD5542-1 offers a switch current limit protection with the R_{SWCS} resistor.

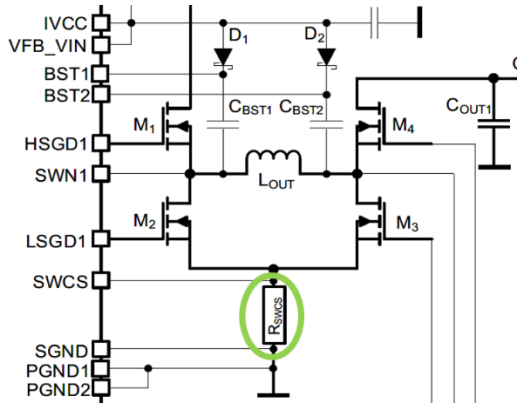


Figure 6 Switch current limiter R_{SWCS}

The current limit shall be set higher than the previously calculated maximum switch current I_{SW_peak} (6.25 A), with the following formula:

$$R_{SWCS} < \frac{V_{SWCS\_boost(min)}}{I_{L_{peak}}} = \frac{70mV}{6.25A} = 11.2m\Omega$$

R_{SWCS} is also the current mode controller inductor sensing resistor and impacts stability. The larger R_{SWCS}, the higher the phase margin and PSRR. Choose the resistor slightly smaller than the required value to fulfill the minimum switch current limit for example, low ESL **10 mΩ** Susumu PRL1632-R010-F-T1, which provides a switch current limit in boost mode of:

$$I_{SW_{LIMIT(typ)}} = \frac{V_{SWCS_{boost}(typ)}}{R_{SWCS}} = \frac{75mV}{10m\Omega} = 7.5A$$

Note: In buck and buck-boost mode, the switch current limit threshold is decreased to $V_{SWCS_{buck}(typ)}$ *= 50 mV, so if the maximum power load it is in the buck boost region, use 50 mV in the* $I_{SW_{LIMIT(typ)}}$ *to calculate* R_{SWCS} *properly*

Note: Use low inductive resistor on R_{SWCS}*, in order to reduce fast transients switching activity noise.*

2.5 Output current sense resistor

The output current sensor can be easily calculated by imposing the feedback voltage $V_{FBH\text{-}FBL\_REF}$ regulated by the device with the required output current.

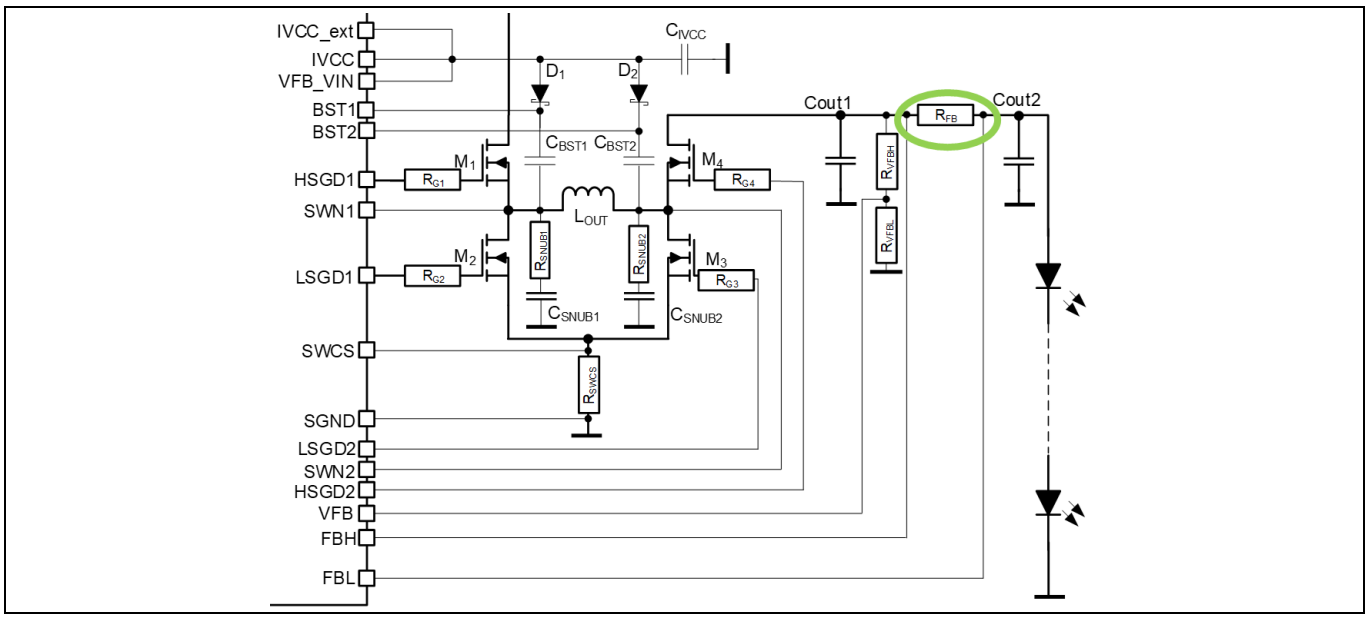


Figure 7 Output current sensing resistor

For this application, the resistor can be calculated as:

$$R_{FB} = \frac{V_{\text{VFBH}-\text{FBL\_REF}}}{I_{OUT}} = \frac{0.15\ V}{1500\ mA} = 100\ m\Omega$$

The power rating of this device can be calculated as

$P = R_{FB} \cdot I_{OUT}^2 = 0.15\ \Omega\ \cdot (1.5A)^2 = 0.33\ W$

For this application PRL1632-R100-F-T1 from Susumu, satisfies the requirements.

2.6 Bootstrap diodes and capacitor

Bootstrap capacitors and diodes on TLD5542-1 follow the standard design rules for any gate driver which uses bootstrap circuitry.

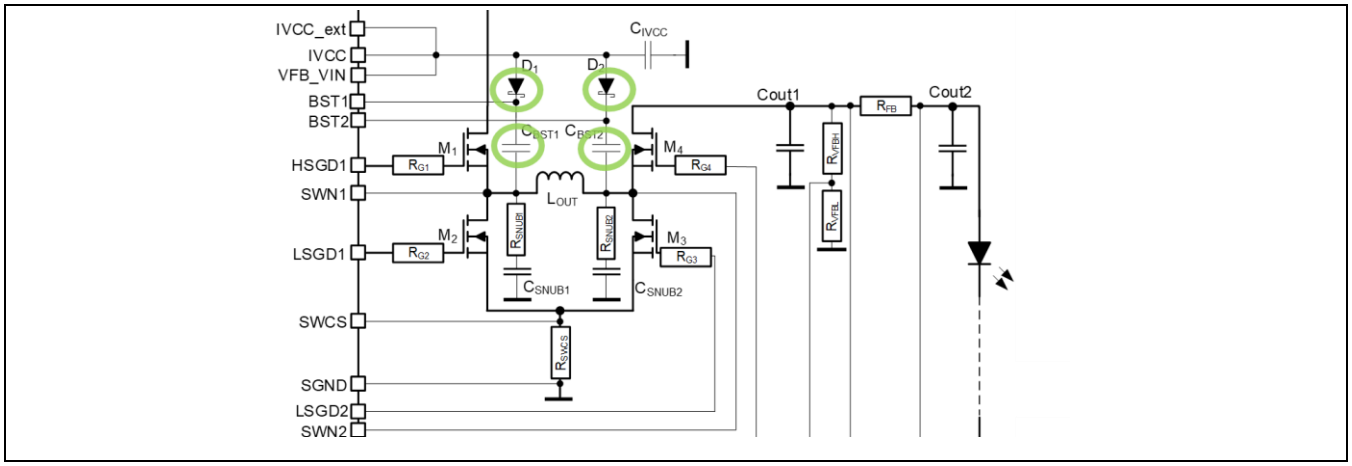


Figure 8 Bootstrap diodes and capacitors

The bootstrap capacitors must have enough energy to drive the gate of the high-side MOSFET without being depleted by more than 10%. Therefore, the bootstrap capacitor should be at least 10 times greater than the equivalent gate capacitance of the high-side FET.

For this application a standard **100 nF 50 V** capacitor is chosen, which could drive about any modern generation MOSFET down to few mΩ $R_{DS(ON)}$ for example, 40 V 2Ω IAUC100N04S6L020. This capacitor only will be charged to 5 V.

Bootstrap diodes generate the high-side gate driver bias by charging the bootstrap capacitor. In order to minimize losses associated with the reverse recovery, a Schottky diode with low forward voltage drop and low junction capacitance is recommended.

Another requirement that is often overlooked is the diode reverse current at the highest working temperature. Reverse leakage current at high temperature may discharge the bootstrap capacitor and lead to driver's undervoltage and shutdown the gate driver. Reverse leakage current impact is high for low switiching frequency.

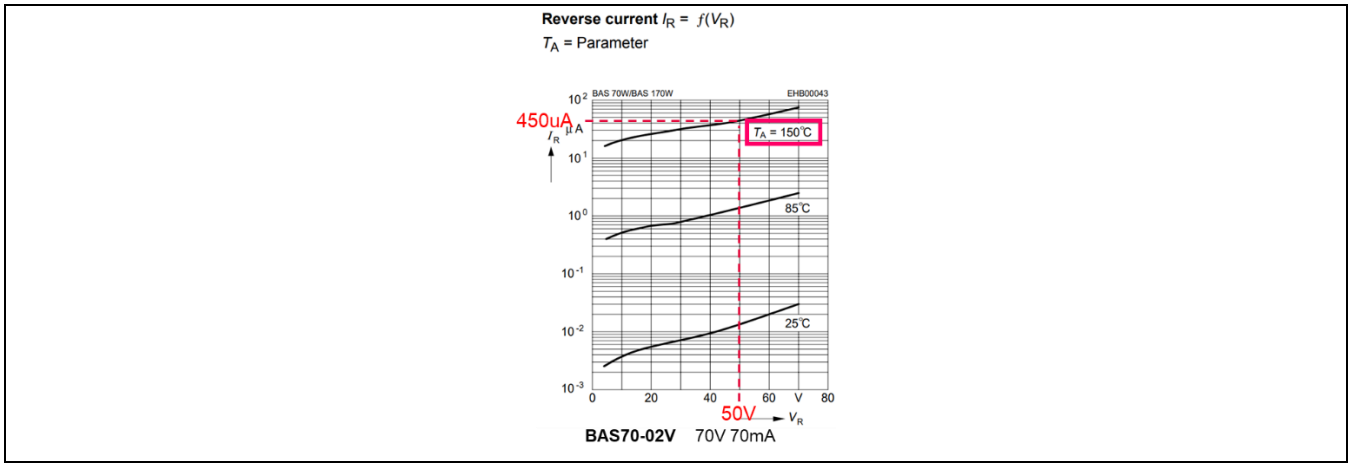


Figure 9 Bootstrap diodes reverse current of the BAT 46WJ

For this application with a 70 V **Infineon BAS70-02V** with low reverse current is chosen.

As a rule of thumb, the reverse current on the bootstrap at maximum application operating temperature and voltage shall be smaller than 1 mA assuming switching frequency is above 250 kHz.

2.7 Soft start capacitor

The soft start routine has 2 functionalities:

- Fault mask and wait-before-retry time
- Limit input inrush current and output overshoots at startup

The most relevant function of the soft start routine for LED drivers is only the fault (short to ground) mask at startup. At startup the output voltage is very likely 0 V therefore, without the fault mask, a short to ground would be detected.

Soft start duration is determined by the soft start capacitor C_{SST}. Minimum value for soft start capacitor shall be designed such that, at startup, the output voltage exceeds the short to ground threshold ($V_{FBH\_S2G\_inc}$), before the soft start expires (voltage reaches $V_{Soft\_Start\_LOFF}$).

Under the assumption of V_{IN} > 6 V and I_{OUT} = 0 A at least until V_{OUT} < $V_{FBH\_S2G\_inc}$, if the soft start capacitor follows the formula below, then a sufficient fault mask is achieved.

$$C_{SST} > 0.6 \cdot C_{\mathrm{COMP}}$$

If the soft start time is higher than the minimum needed for S2G mask, then the only side effect on a LED driver is a longer fault retry time. Therefore, for this application it is simple and safe to choose $\boldsymbol{C_{SST} = C_{COMP} = 22\ nF}$.

Note: The above formula has been tested for output capacitor below 100 µF, effectiveness of soft start should be tested in the real application. Soft start network validation: Minimum temperature and minimum input voltage shall be considered as worst-case condition for previously mentioned dimensioning.

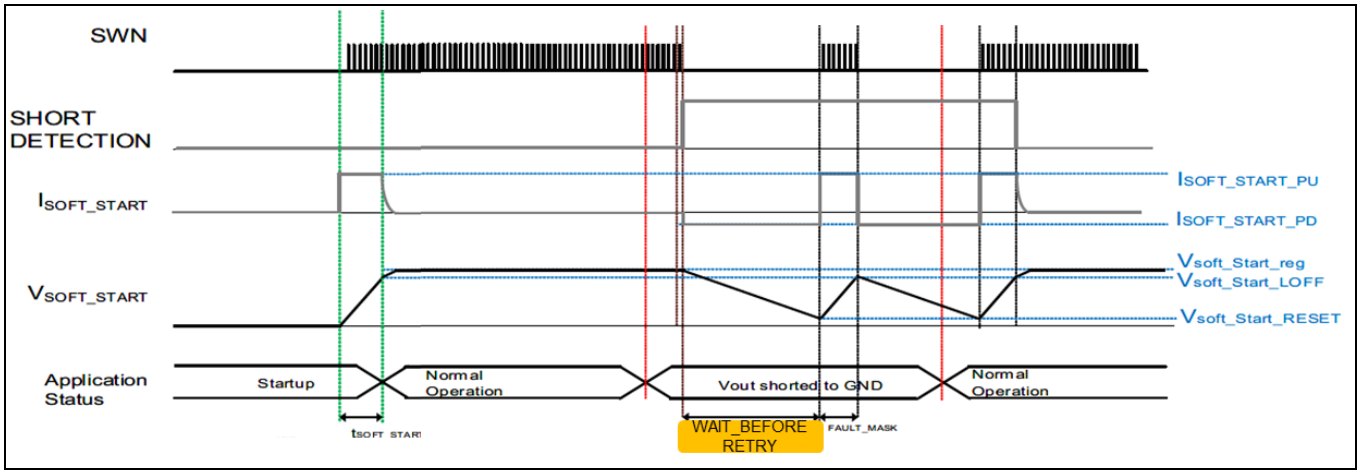


Figure 10 Wait before retry time

Wait time before retry (t_{retry}) in case of a fault will be:

$$t_{retry} = (V_{Soft_{Start_{LOFF}}} - V_{Soft_{Start_{RESET}}}) \frac{C_{SST}}{I_{Soft_{Start_{PD}}}} = (1\,V - 0.2V)\,\frac{22nF}{2.6uA} = 13\,ms$$

The first retry time after a fault is slightly longer than the following times, because the soft start capacitor during regulation stays at $V_{Soft\_Start\_REG}$ instead of $V_{Soft\_Start\_LOFF}$. In addition, the first rise time of the soft start after power on is different from the successive retry rise time, because the soft start capacitor starts from 0 V instead of $V_{Soft\_Start\_RESET}$.

Note: To ensure PWM extension in case a low duty PWM is applied at startup place a capacitor on IOUTMON pin

2.8 Analog dimming - SET resistor divider

Analog dimming can be applied by the SET pin (TLD5542-1 only during limp home mode).

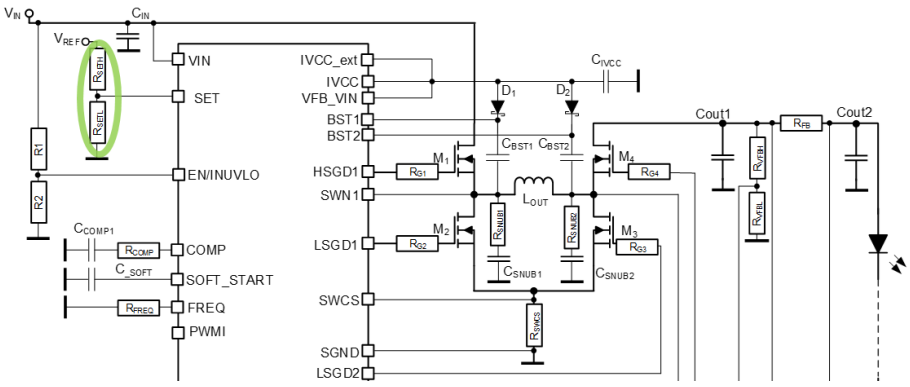


Figure 11 SET resistor divider

A resistor divider can be applied to a reference voltage (example to the 5 V IVCC) in order to set the desired output current $I_{OUT(AD)}$ by means of the SET pin.

In order to reduce the parasitic effects of moisture and leakage from the SET pin, it is recommended to choose R_{SETL} equal to 15 kΩ.

Supposing that the requested output current, set by the SET pin, is $I_{OUT(AD)}$= 0.9 A, then R_{SETH} is calculated using the following formula:

$$R_{SETH} = R_{SETL} \cdot \frac{V_{REF} - (I_{OUT(AD)} \cdot RFB \cdot 8 + 0.2)}{(I_{OUT(AD)} \cdot RFB \cdot 8 + 0.2)} = 15\text{k}\Omega \cdot \frac{5V - (0.9A \cdot 0.1\Omega \cdot 8 + 0.2V)}{(0.9A \cdot 0.1\Omega \cdot 8 + 0.2)} = 66.5\ \text{k}\Omega$$

Choosing 68 kΩ as closest commercial value, the effective output current will be:

$$I_{OUT(AD)} = \frac{V_{SET} - 200mV}{R_{FB} \cdot 8} = \frac{V_{REF} \cdot \frac{R_{SETL}}{R_{SETH} + R_{SETL}} - 200mV}{R_{FB} \cdot 8} = \frac{5V \cdot \frac{15\text{k}\Omega}{68\text{k}\Omega + 15\text{k}\Omega} - 200mV}{0.1\Omega \cdot 8} = 0.88\,A$$

3 Protections and spread spectrum

3.1 Overvoltage protection at the output

This feature protects the LED driver module if the load gets disconnected.

The overvoltage at the output (V_{OUT_MAX}) has to be set:

- higher than the maximum voltage
- lower than the absolute maximum voltage of the TLD5542-1 FBL pin (60 V)
- above the maximum expected battery voltage (see TLD5542-1 datasheet)

To avoid unwanted tripping, it is good practice to calculate V_{OUT_MAX} at the minimum overvoltage threshold (V_{VFB_OVTH}) of the device (see datasheet).

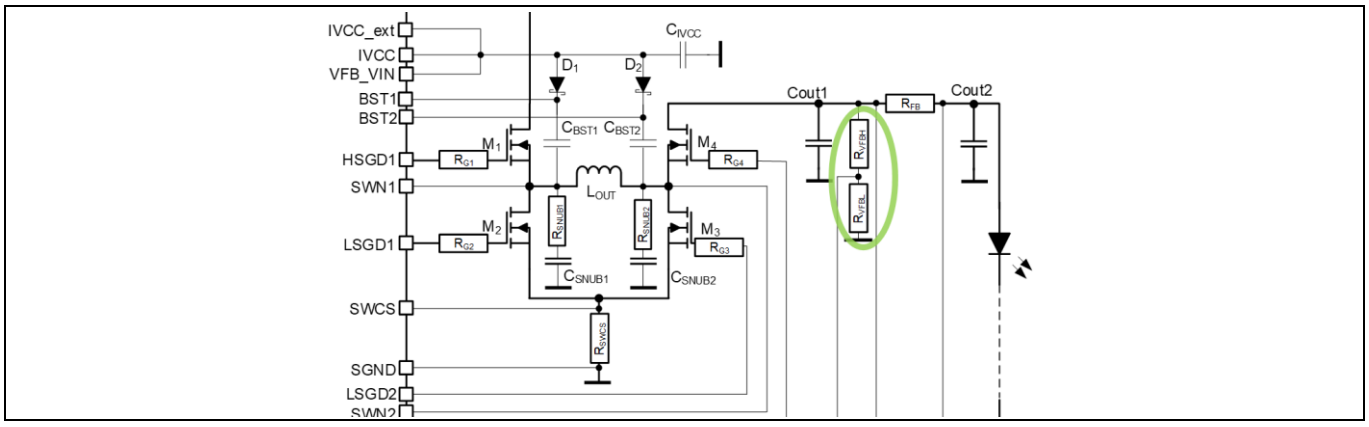


Figure 12 Overvoltage protection schematic

Overvoltage is triggered when the voltage on VFB pin reaches 1.46 V (typ). Overvoltage detection is enabled by a resistor divider as shown in Figure 12.

In order to reduce the parasitic effects of moisture and leakage from the VFB pin, it is recommended to choose R_{VFBL} equal to 1.5 kΩ.

The second resistor of the voltage divider is calculated as:

$$R_{VFBH} = R_{VFBL} \cdot \frac{V_{OUT\_MAX}}{V_{OUT\_OVTH(typ)}} - R_{VFBL} = 1.5\ \text{k}\Omega \frac{50\ V}{1.46\ V} - 1.5\ \text{k}\Omega = 49.86\ k\Omega$$

The closest value as off-the-shelf component on E96 series is 49.9 kΩ.

The real output overvoltage value is calculated using the real component value with the following formula:

$$V_{OUT\_MAX} = V_{OUT\_OVTH} \cdot \frac{R_{VFBL} + R_{VFBH}}{R_{VFBL}}$$

With the above formula it is also possible to check what the effect of V_{OUT_OVTH} deviations (min-max) would be.

The excel calculator also help to calculate the overvoltage protection.

3.1 Input undervoltage protection

The input voltage requirement for the LED driver module is 6 V (extended range) therefore, the input undervoltage protection must be set below this threshold.

Even if the TLD5542-1 has switch current limiter (R_{SWCS}) and gate driver undervoltage protection, it is better to set the undervoltage threshold above 5 V. This is to avoid stress on switching MOSFETs, due to increased input current and reduced gate driver voltage.

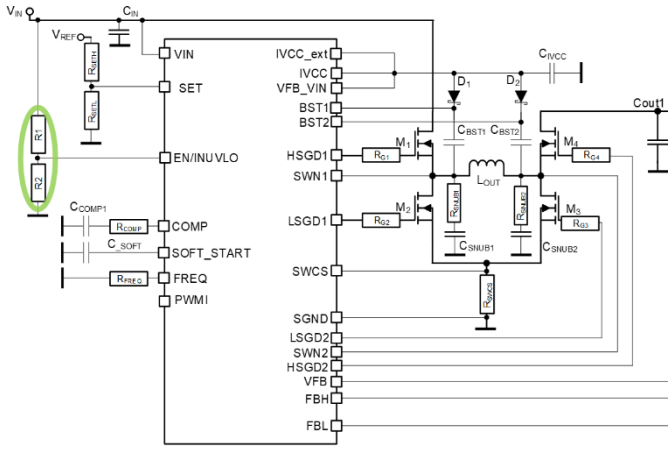


Figure 13 EN/INUVLO resistor divider

For this application an undervoltage threshold of 5.5 V (entry threshold, V_{IN} falling) has been chosen. The low-side resistor should be in the range of 2 kΩ to 10 kΩ to avoid excessive leakage current and to provide an accurate threshold.

Choosing **R2 = 2.2 kΩ** as low-side voltage divider resistor, the high-side resistor (R1) is calculated as

$$R1 = R2 \cdot \frac{UV_{th} - EN/INUVLO_{th}}{EN/INUVLO_{th}} = 2.2k \cdot \frac{5.5V - 1.75V}{EN/INUVLO_{th}} = 4714\ \Omega$$

Standard value is **R1 = 4.7 kΩ**. The same value can be calculated with the excel component calculator.

3.2 Input current sense resistor

The input current of the application can be measured by the TLD5542-1 and a shunt resistor (R_{IIN}) via IIN1 and IIN2 pins. The sensed current can be monitored through an analog output pin (IINMON) and an SPI register. IIN1 is the positive sense terminal, IN2 is the negative sense terminal.

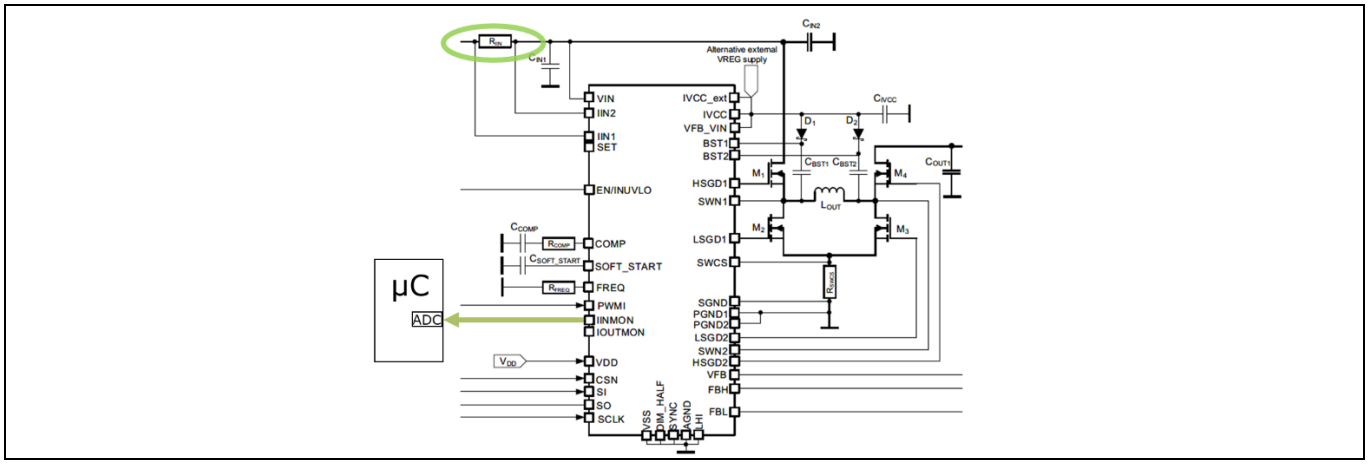


Figure 14 Input current monitor resistor and IINMON output

IINMON pin produces a voltage proportional to $V_{IIN1\text{-}IIN2}$ following this equation:

$$V_{IINMON(typ)} = I_{IN} \cdot R_{IIN} \cdot 20$$

IINMON pin voltage produces 1 V (typ.) when $V_{IIN1\text{-}IIN2}$ = 50 mV. The sensing resistor shall be dimensioned in order to have maximum 60 mV at IIN1-IIN2 when the current is at the maximum value, otherwise IINMON will saturate the above this value.

$$R_{IIN} \leq \frac{V_{IINMON(max)}}{I_{IN(max)}} = \frac{60mV}{5.4\ A} = 11\ m\Omega$$

where:

$$I_{IN(max)} = \frac{P_{OUT\_max}}{V_{IN\_min} \cdot \eta} = \frac{45W}{9 \cdot 93\%} = 5.4\ A$$

- Efficiency of 9 V has been calculated with the TLD5542-1 excel component calculator.
- A standard resistor value close to the calculated one could be $\boldsymbol{R_{SWCS}}$ **= 10 mΩ**. If the component selected is smaller than this value, less accurate input current reading will occur, especially at low input currents.
- When IINMON goes above 1.2 V, then linearity decreases and will tend to saturate at approximately 1.4 V. IINMON pin could present typically 2 mV and maximum 15 mV offset.
- The IINMON pin output impedance is typically about 36 kΩ.
- If IINMON is not used, it has to be left open, while IIN1, IIN2 pins should be connected to VIN.

4 Compensation network

In this chapter the main stability equations are provided and an analytical approach can be completed in all the operating conditions.

A faster approach is to use the TLD5542-1 excel component calculator, where several operating conditions and compensation networks can be quickly verified.

Good practice is to dimension the external components and check stability in the corner cases, for example at minimum V_{IN} and maximum V_{OUT}, and maximum V_{OUT} and minimum V_{IN}.

The RC compensation network is applied to the COMP pin (proportional and integral compensation). In small signal approximation, the open loop transfer function of a DC-DC is the product of modulator transfer function and the feedback network transfer function.

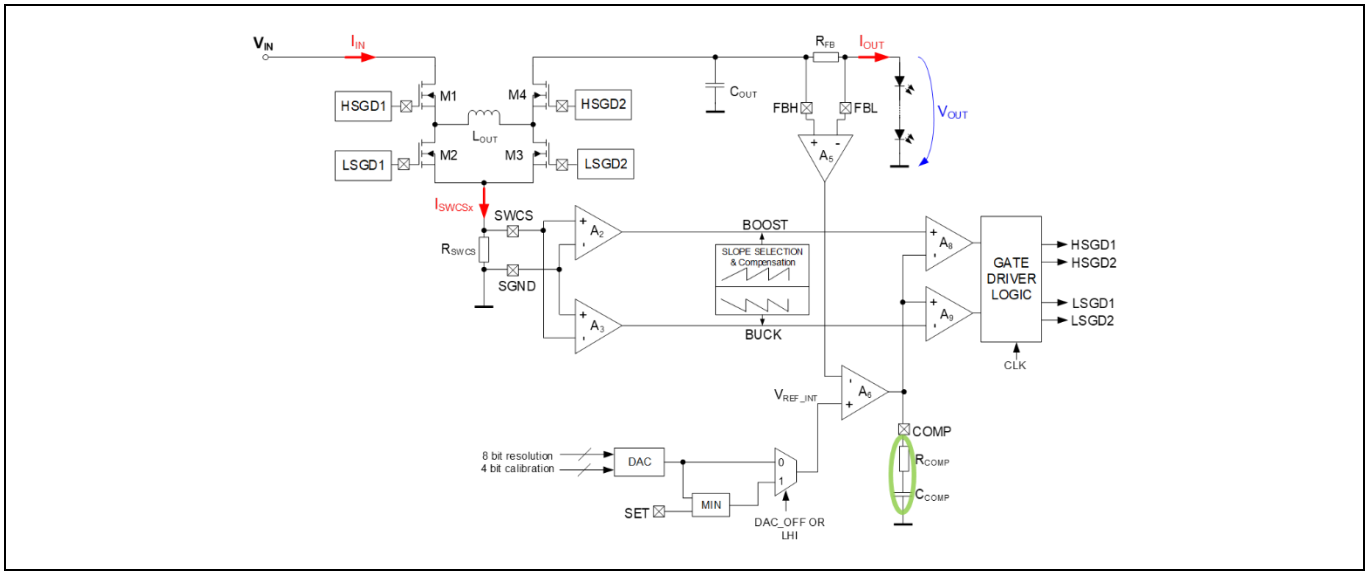


Figure 15 Compensation network schematic

The modulator transfer function can be expressed as product of two main parts: the gain of the error amplifier and the gain of the current mode modulator. The equations are different if the device operates in boost mode or in buck mode.

Buck operating mode stability equations:

In buck mode, the gain of the error amplifier is described with the following formula:

$$A_{EA\_buck}(s) = g_{m\_EA} \cdot R_{EA} \cdot \frac{(1 + s \cdot \tau_{z1})}{(1 + s \cdot \tau_{p1})}$$

Where

- g_{m_EA} is the trans-conductance of the error amp. (A5, A6 with comprehensive gain $IFBx_{gm(typ)}$ = 890 µS)
- R_{EA} is the output resistance of the error amplifier (TLD5542-1 R_{EA_typ} = 6 MΩ)
- $\tau_{z1} = C_{COMP} \cdot R_{COMP}$ is the zero of compensation network
- $\tau_{p1} = (C_{COMP}) \cdot R_{EA}$ is the pole associated to compensation network and the resistor of error amplifier

Boost operating mode stability equations:

The gain of the current mode modulator can be described following the model presented by R.B Ridley [3].

Mathematically, it is described as:

$$A_{CM\_boost}(s) = \frac{0.17 \cdot (1-D) \cdot R_{LOAD}}{\left(1 + \frac{I_L \cdot (1-D) \cdot R_{LOAD}}{V_{OUT}}\right) \cdot R_{swcs}} \cdot \frac{(1 + s \cdot \tau_{z2})}{(1 + s \cdot \tau_{p3}) \cdot \left(1 + \frac{s}{\omega_n \cdot Q} + \frac{s^2}{\omega_n^2}\right)}$$

$$A_{CM\_boost}(s) = \frac{0.17 \cdot (1-D) \cdot R_{LOAD}}{\left(1 + \frac{V_{REF} \cdot R_{LOAD}}{V_{OUT} \cdot R_{FB}}\right) \cdot R_{swcs}} \cdot \frac{(1 + s \cdot \tau_{z2})}{(1 + s \cdot \tau_{p3}) \cdot \left(1 + \frac{s}{\omega_n \cdot Q} + \frac{s^2}{\omega_n^2}\right)}$$

$$I_L = \frac{V_{REF}}{R_{FB}(1-D)}$$

Where:

- R_{LOAD} is the total resistor at the output of DC-DC and it is the sum of R_{FB} and R_{LED_string}
- V_{REF} is the voltage reference across FBH and FBL (typical 150 mV)
- V_{OUT} is the voltage on LED string V_{LED} plus input voltage V_{IN} (Voltage across PMOS has been neglected)
- $\tau_{z2} = -\frac{L_{BO}}{(1-D)^2} \cdot \frac{(I_{OUT})}{(V_{OUT})}$ is the zero (RHP) of the boost DC-DC with the return to battery
- $\tau_{p3} = C_{OUT} \cdot R_{LOAD} \cdot \frac{V_{OUT}}{I_{OUT} \cdot R_{LOAD} + V_{OUT}}$ is the pole associated with boost converter with the return to battery
- $\omega_n = \pi \cdot \frac{f_s}{2}$ is the natural pulsation of the system
- $Q = \frac{1}{\pi \cdot \left(\left(1 + \frac{S_e}{S_n}\right) \cdot (1-D) - 0.5\right)}$ is the quality factor of a second order system, where S_e is the slope of current compensation circuit (coefficient fixed by internal references) and S_n is the slope of the current sensed by R_{swcs}.

$$S_e = 60 \cdot 10^{-3} \cdot f_{sw}$$

$$S_n = \frac{V_{IN} \cdot R_{SWCS}}{L_{BO}}$$

Using the data previously calculated, it is possible calculate the gain in DC and cross over frequency f_c and the phase margin.

The transfer function of the feedback network is the ratio between R_{FB} and the R_{LED}

$$\beta = \frac{R_{FB}}{R_{FB} + R_{LED_{string}}}$$

For the gain calculation in typical conditions, the three parts $(A_{EA}(0)\ , A_{CM}(0), \beta)$ to be calculated are shown below, calculated in an exemplary boost duty cycle of 50%:

$$A_{EA\_boost}(0) = g_{m\_EA} \cdot R_{EA} = 0.00089\ S \cdot 6\ M\Omega = 5340$$

$$A_{CM\_boost}(0) = \frac{0.17 \cdot (1-D) \cdot R_{LOAD}}{\left(1 + \frac{V_{REF} \cdot R_{LOAD}}{V_{OUT} \cdot R_{FB}}\right) \cdot R_{swcs}} = \frac{0.17 \cdot (1-0.5) \cdot 2.1\ \Omega}{\left(1 + \frac{0.15\ V \cdot 2.1}{27.9\ V \cdot 0.1\Omega}\right) \cdot 0.010\ \Omega} = 16.04$$

$$\beta = \frac{R_{FB}}{R_{FB} + R_{LED\_string}} = \frac{0.1\ \Omega}{2.1\ \Omega} = 0.0476$$

And then the gain in DC can be calculated as:

$$T(0)|_{dB} = 20 \cdot \log(A_{EA}(0) \cdot A_{CM}(0) \cdot \beta) = 20 \cdot \log(5340 \cdot 16.04 \cdot 0.0476) = 72.2\ dB$$

Poles and zeroes can be calculated with the above formulas.

For this application, with the given inductor and output capacitor, a good compromise for stability and transient response has been found with **22 nF C_{COMP}** and **1 kΩ R_{COMP}** at the compensation network.

For illustration purposes, Figure 16 shows a screenshot of the excel component calculator bode plots.

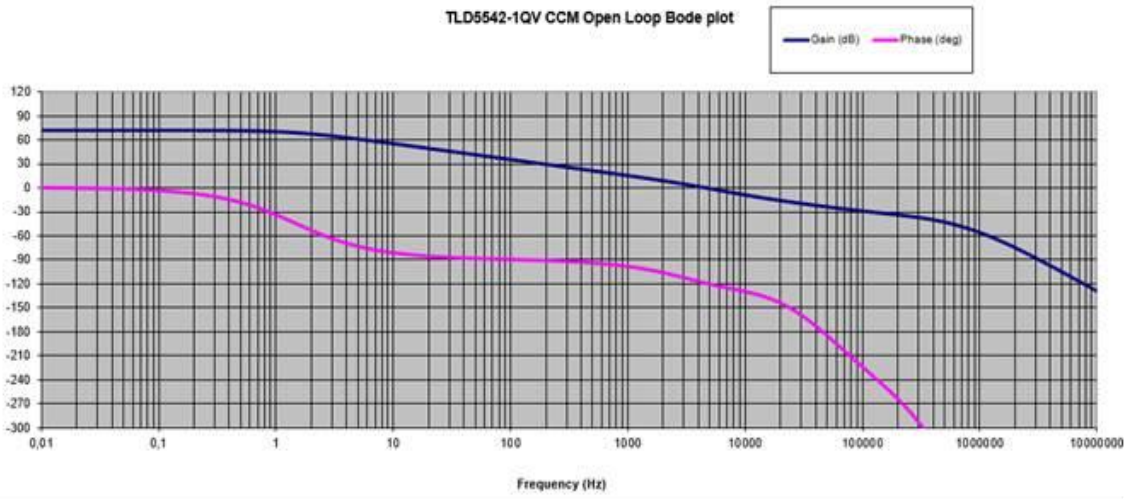


Figure 16 Example bode plot screenshot from Infineon TLD5542-1 LED component calculator excel [1]

It is common practice to consider a system stable when the phase margin is above 45° (better if closer to 60°).

Buck operating mode stability equations:

In buck mode, the gain of the error amplifier remains the same of the boost mode described above.

the current mode gain can be mathematically approximated as:

$$A_{CM\_buck}(s) = \frac{0.17 \cdot R_{LOAD}}{R_{swcs}} \cdot \frac{1}{(1 + s \cdot \tau_{p3}) \cdot \left(1 + \frac{s}{\omega_n \cdot Q} + \frac{s^2}{\omega_n^2}\right)}$$

Where:

- R_{LOAD} is the total resistor at the output of DC-DC and it is the sum of R_{FB} and R_{LED_string}
- V_{REF} is the voltage reference across FBH and FBL (typical 150 mV)

- V_{OUT} is the voltage on LED string V_{LED} plus input voltage V_{IN} (Voltage across PMOS has been neglected)
- $\tau_{p3} = C_{OUT} \cdot R_{LED}$ is the pole associated to buck converter with the return to battery
- $\omega_n = \pi \cdot \frac{f_s}{2}$ is the natural pulsation of the system
- $Q = \frac{1}{\pi \cdot \left(\left(1+\frac{S_e}{S_n}\right) \cdot D - 0.5\right)}$ is the quality factor of a second order system, where S_e is the slope of current

Compensation circuit (coefficient fixed by internal references) and S_n is the slope of the current sensed by R_{SWCS}.

$$S_e = 60 \cdot 10^{-3} \cdot f_{sw}$$

$$S_n = \frac{V_{OUT} \cdot R_{SWCS}}{L_{BO}}$$

Using the data previously calculated, it is possible to calculate the gain in DC and cross-over frequency f_c and the phase margin.

The transfer function of the feedback network is the ratio between R_{FB} and the R_{LED}

$$\beta = \frac{R_{FB}}{R_{LED\_string}}$$

For the gain calculation in typical conditions, the three parts for buck mode $(A_{EA}(0), A_{CM}(0), \beta)$ can be calculated as shown in the boost mode.

4.1 Stability tips

Phase margin could be improved by tuning some key components shown in Figure 17. Each component may have some benefit, however there are also drawbacks in other aspects:

Table 2 Effect of tuning key components

Component	Improvement	Drawback
Increasing R_{SWCS}	Phase margin and enhance response to battery variation	reduced maximum output power:
Increasing C_{COMP}	Phase margin	slower response to battery variations
Decreasing R_{COMP}	could improve margin in buck region	possible reduced stability in boost mode, enhanced response to battery variation
Increasing R_{COMP}	could improve margin in boost region	possible reduced stability in buck mode, enhanced response to battery variation
Increasing C_{OUT2} capacitor (capacitor placed after sensing resistor)	phase margin in both buck and boost mode	lowers cut frequency

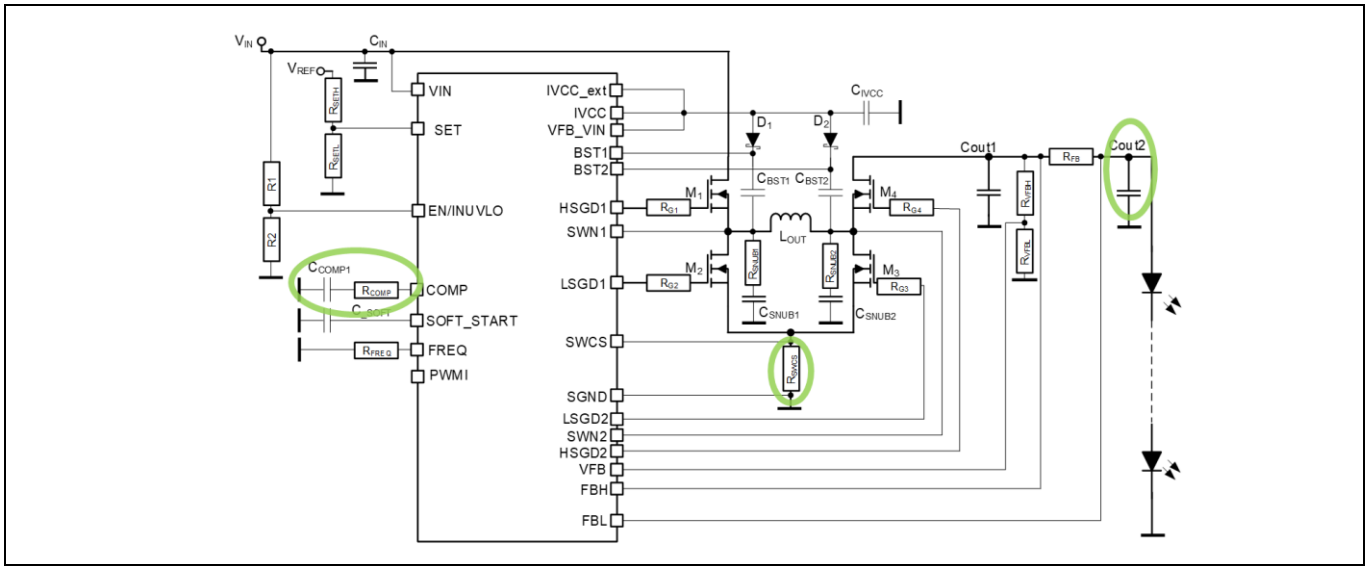


Figure 17 Components that can be tuned to improve stability

Infineon is producing a SIMETRIX average model of the device for electrical simulations, which can be used to verify the behavior of the device for any application circuits.

5 EMC

5.1 Spread spectrum

The TLD5542-1 offers a spread spectrum modulation that significantly improves the EMC in the lower frequency range of the spectrum (f < 30 MHz). Spread spectrum is disabled by default and can be enabled by setting the register, ENSPREAD to 1, via SPI. Deviation frequency is set by FDEVSPREAD and modulation frequency is set by FMSPREAD via SPI, see TLD5542-1 datasheet [4] for details.

The effect of the spread spectrum and the FDEVSPREAD register is evident in Figure 18. In this EMC test report the emission peaks are reduced by 10 dB and more. Hereby, class 5 limits pass.

Larger deviations, in percent, and modulation frequency are lowering but widening the emissions peaks. Depending on the switching frequency and regulator limits the shape of the emission can be modified for best convenience.

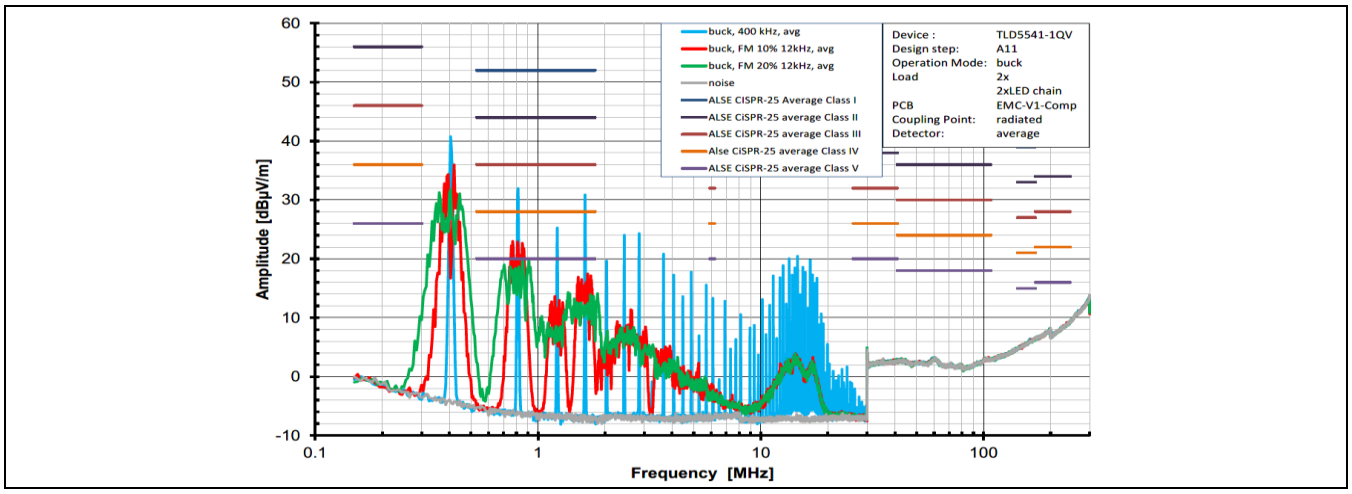
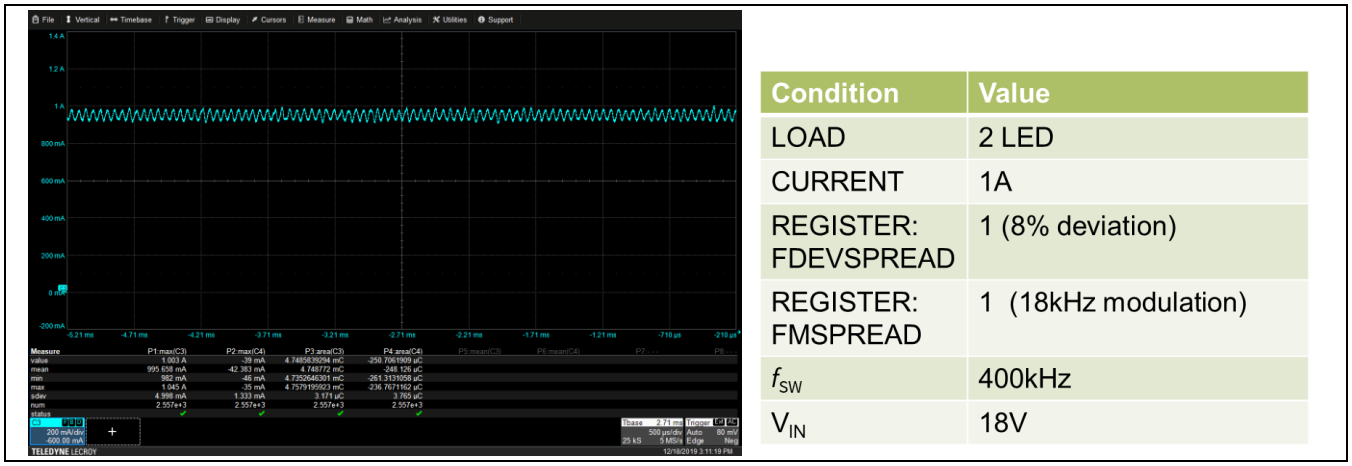


Figure 18 Spread spectrum effects on radiated emission

The effect of the spread spectrum on the output current is a ripple with the deviation frequency, which does not produce any visible flicker.



Condition	Value
LOAD	2 LED
CURRENT	1A
REGISTER: FDEVSPREAD	1 (8% deviation)
REGISTER: FMSPREAD	1 (18kHz modulation)
f_{SW}	400kHz
V_{IN}	18V

Figure 19 Spread spectrum I_{OUT} ripple

A widely adopted setting for the 2 spread spectrum configuration bit, which is a good compromise of ripple and EMC attenuation is:

- FDEVSPREAD = 1 (8% of f_{sw})
- FMSPREAD = 1 (18 kHz)

5.2 Gate driver resistors

Gate driver resistors are placed at the gate driver output in order to improve EMC performances. Rules for the gate driver resistor dimensioning are as for any standard DC-DC controller. The effect of these resistors is to reduce switching speed and ringing at the switching nodes. Gate driver resistors impact the efficiency of the DC-DC converter, and they should be increased only to pass the target EMC regulation (for example, CISPR25).

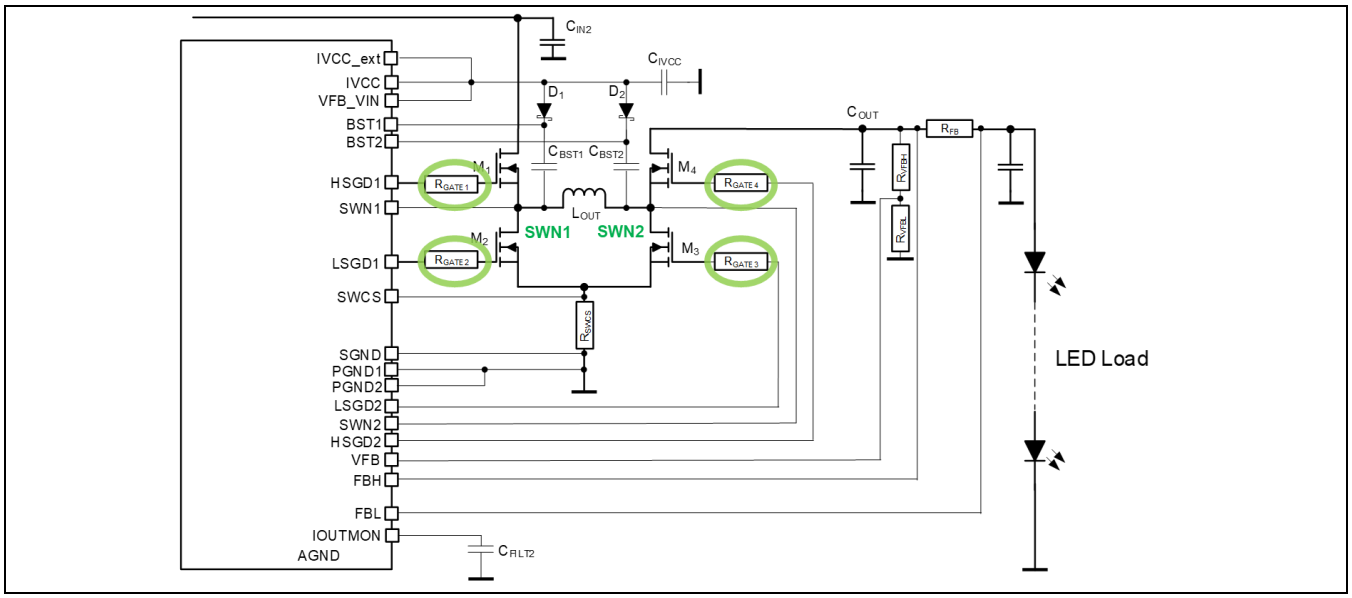


Figure 20 Gate driver resistors

The high-side gate driver resistor R_{GATE1} impacts only the rise time of the buck switching node (SWN1).At the boost side, the low-side gate driver resistor R_{GATE3} impacts the falling time of the boost switching node (SWN2).

As starting point for good EMC performance (Class 5 CISPR 25), the buck switching node rise-time and boost switching node fall-time, should be in the 10 ns to 50 ns range. The final EMC result depends on output voltage, switching frequency, PCB layout, cable length and other application parameters. Therefore, gate resistors should be tuned in the final application, after an EMC measurement.

With the current MOSFET choice, a 22 Ω gate resistor has been selected as starting point, with a measured rise time for the buck switching node of approximately 18 ns with a 4 LED load.

The impact of the efficiency is calculated with the TLD5542-1 excel component calculator, at the maximum output power 45 W (30 V 1.5 A):

- 93.4% with 22 Ω gate resistor
- 95.65% with 0 Ω gate resistor

This resistor value could be increased or decreased after EMC measurement.

5.3 Layout considerations

For a DC-DC converter, the PCB design is a critical task as well as the component selection. Even if the circuit topology and components selection are good, if the PCB layout is not good enough, the performances of the whole system will be lower than expected. A proper layout is also the basis for good EMC performances. The most important PCB layout rules are explained in a dedicated application note, "*LITIX™ PCB design guideline document*" [5]. Figure 21 depicts a screenshot of this application.

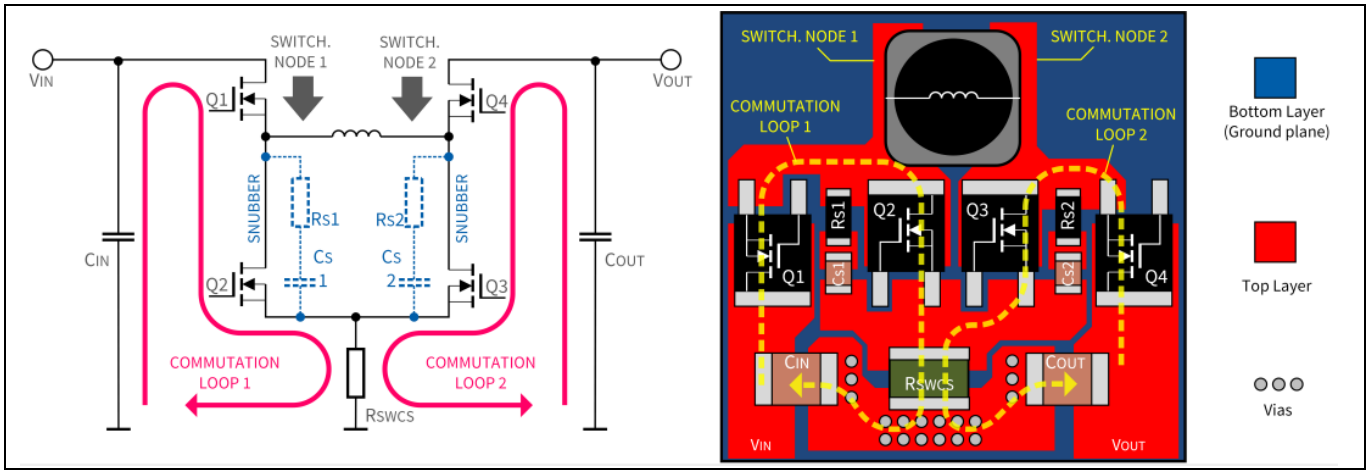


Figure 21 Hot loops and recommended layout for H-bridge topology

6 List of references

[1] Infineon LITIX™ Power Flex/TLD5542-1QV/Development_Tools/TLD5542-1 LED Component calculator/ TLD5542_1_LED_Comp_calc-DevelopmentTools excel component calculator

[2] Infineon LITIX™ Power Flex website

[3] Ridley, R. B.; *A new Continuous Time Model for Current Mode Control*; IEEE Transaction on Power Electronics; Vol. 6; Issue 2; pp. 271-280; 1991

[4] Infineon TLD5542-1 DS Rev.1.10 (2019-12-11)

[5] Infineon Z8F80033952 LITIX™ PCB design guidelines AN Rev.1.00

Revision history

Major changes since the last revision

Page or Reference	Description of change
2021-01-15	Initial release

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