LITIX™ Power TLD5097EP/TLD5098EP/TLD5099EP

Voltage regulator in boost configuration for automotive applications

About this document

Scope and purpose

This document covers the design steps for a voltage regulator with a DC-DC converter in boost configuration with products provided by Infineon Technologies such as the TLD5099EP. Equations and results can also be applied to TLD5098EP and TLD5097EP. The solution described in the document covers a typical automotive application. However, the system proposed can also be used in all applications where a low voltage power source (such as battery stack or 5 V USB output) has to be boosted to a higher value.

Intended audience

Hardware designer engineers

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1 Introduction

Automotive environment loads directly connected to the battery line are perturbed by a non-stable voltage due to engine starting/stopping and load jumps. Voltage regulators are frequently used in order to stabilize the load voltage.

Boost converters are used if the desired voltage level for a load is above the maximum battery voltage (e.g. to stabilize the voltage of a linear current source with long LED strings).

TLD5099EP is a multi-topology controller that can easily address DC-DC converters for this purpose. Boost topology is one of the possible configurations and it is schematized in Figure 1.

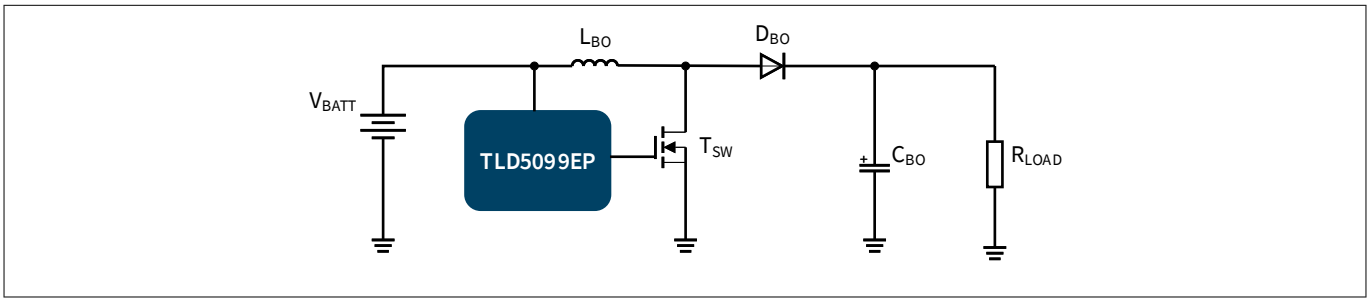

Figure 1 Boost to ground topology simplified

In this application note the regulator is used to adjust the input voltage of multiple constant current sources (linear current sources such as BASIC+ as in TLD2132-1EP or buck DC-DC converter such as TLD5045EJ) in a rear lamp. In Figure 2 an application diagram is presented. By boosting the battery voltage, it is possible to generate a differential voltage to insert the constant current sources with long LED string.

In this example the TLD5099EP is used to boost the voltage up to 36 V, while the TLD5045EJ, TLD2131-3EP and TLD2132-1EP power the LED strings with constant current. Assuming that the maximum red LED forward voltage is 2.5 V the proposed configuration can supply up to 15 LEDs in series.

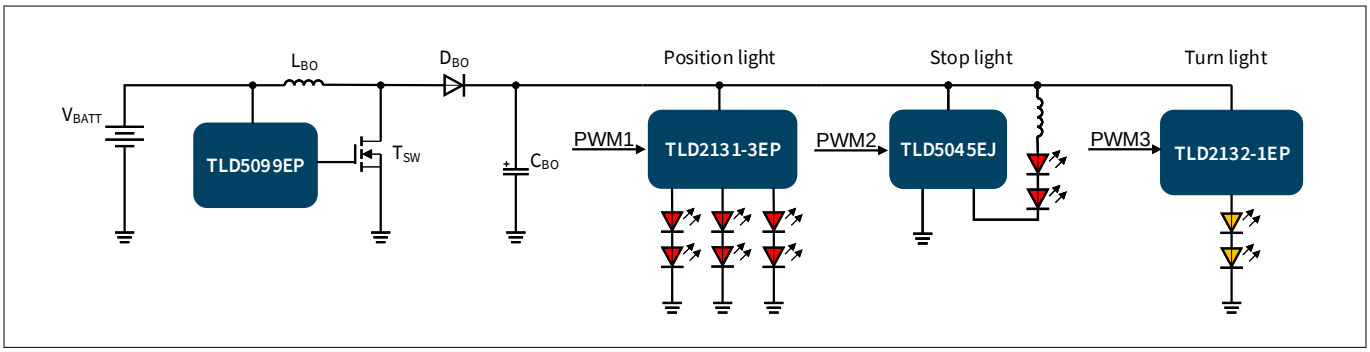

Figure 2 Rear lamp application with linear current sources and DC-DC

1.1 Application assumptions

How to use the TLD5099EP as a voltage regulator is shown exemplary for the following converter specification:

Table 1 DC-DC specifications

Function	Pre-regulator for multiple output current sources
Input voltage	8 to 26 V (typ. 13.5 V)
Output voltage	36 V
Voltage ripple	± 1%
Maximum output power	24 W (54 Ω equivalent resistor at 36 V output voltage)
Switching frequency	400 kHz
EMC requirements	CISPR class V

In the following pages, the load is considered as an equivalent resistor of 54 Ω.

2 Main regulator design

During the design of DC-DC converter there are few parameters that are needed to define and select electronic components and devices. The duty cycle (D) of the switching regulator is such a parameter and it is derived by the minimum and maximum voltage of the input and output. The formula for a voltage mode boost converter is:

$$D = 1 - \frac{V_{IN}}{V_{OUT}} \tag{1}$$

Table 2 represents an example of duty cycle range:

Table 2 Duty cycle range

Input voltage (V_{IN})	Duty cycle (D)
8 V (jump start)	0.778
13.5 V (typical)	0.625
26 V (load dump)	0.278

The average input current is a function of battery voltage and its value is used to define the ratings of the switching elements (maximum current) and to check if the converter works in continuous conduction mode (minimum current).

The average current (maximum, typical and minimum) is calculated by the formulas below assuming 90% of overall efficiency.

$$< I_{IN\_MAX} > = \frac{P_{OUT}}{V_{IN\_MIN} \cdot \eta} = \frac{24\ W}{8\ V \cdot 0.9} = 3.33\ A \tag{2}$$

$$< I_{IN\_TYP} > = \frac{P_{OUT}}{V_{IN\_TYP} \cdot \eta} = \frac{24\ W}{13.5\ V \cdot 0.9} = 1.97 A \tag{3}$$

$$< I_{IN\_MIN} > = \frac{P_{OUT}}{V_{IN\_MAX} \cdot \eta} = \frac{24\ W}{26\ V \cdot 0.9} = 1.02\ A \tag{4}$$

2.1 Inductor

The inductor of the boost converter is selected by fixing a certain ratio between average current and ripple current $\Delta I_{L\_TYP(P\text{-}P)}$ (as peak to peak measurement) in typical condition. Usually the peak current is in the range of 20% to 40% of the average ripple current; the lower the ripple current, the lower the electromagnetic emission. For this application 30% ripple current has been chosen.

Two equations are needed to calculate the correct value of the inductor for the DC-DC. The first equation determines the value to keep the required ripple current with typical voltage at input.

$$L_{MIN} \geq D_{TYP} \cdot \frac{V_{IN_{TYP}}}{\Delta I_{L\_TYP(P-P)} \cdot f_{SW}} = 0.625 \cdot \frac{13.5\ V}{2 \cdot 0.3 \cdot 1.97\ A \cdot 400\ \text{kHz}} = 17.8\ \ \mu\text{H} \tag{5}$$

2 Main regulator design

The second equation determines the minimum inductor to prevent discontinuous conduction mode when the current is at minimum (i.e. with maximum input voltage as worst case condition)

$$L_{\mathrm{MIN}} \geq D_{\mathrm{MIN}} \cdot \frac{V_{\mathrm{IN_{MAX}}}}{2 \cdot < I_{\mathrm{IN_{MIN}}} > \cdot f_{\mathrm{SW}}} = 0.27 \cdot \frac{26\ V}{2 \cdot 1.02\ A \cdot 400\ \mathrm{kHz}} = 8.6\ \mu\mathrm{H} \quad (6)$$

The closest commercial value that satisfies both equations is 22 µH (to include the tolerance of the component). With this value, the actual ripple current in worst condition (i.e. when input voltage is at minimum) is:

$$\Delta I_{L(P-P)} = D_{\mathrm{MAX}} \cdot \frac{V_{\mathrm{IN_{MIN}}}}{L \cdot f_{\mathrm{SW}}} = 0.778 \cdot \frac{8\ V}{22\ \mu\mathrm{H} \cdot 400\ \mathrm{kHz}} = 0.71\ \ A \quad (7)$$

Then the maximum peak current into inductor is calculated as:

$$I_{L\_\mathrm{MAX}} = < I_{\mathrm{IN\_MAX}} > + \frac{\Delta I_{L(P-P)}}{2} = 3.33\ A + 0.35\ A = 3.68\ \ A \quad (8)$$

The important key parameters to select an inductor are then:

- Inductance > 17.8 µH
- Saturation current > 3.68 A

An inductor that fulfills the above requirements (nominal inductor value and saturation current) is the TDK B82477P4223M000.

2.2 Output capacitor

The output capacitor acts as an energy tank when the rectifier diode D_{BO} is in reverse polarity and for this reason it has to stand a high ripple current. This component affects the bandwidth of the system and also the voltage ripple performance at the output.

Figure 3 depicts how the system manages the current in reactive components.

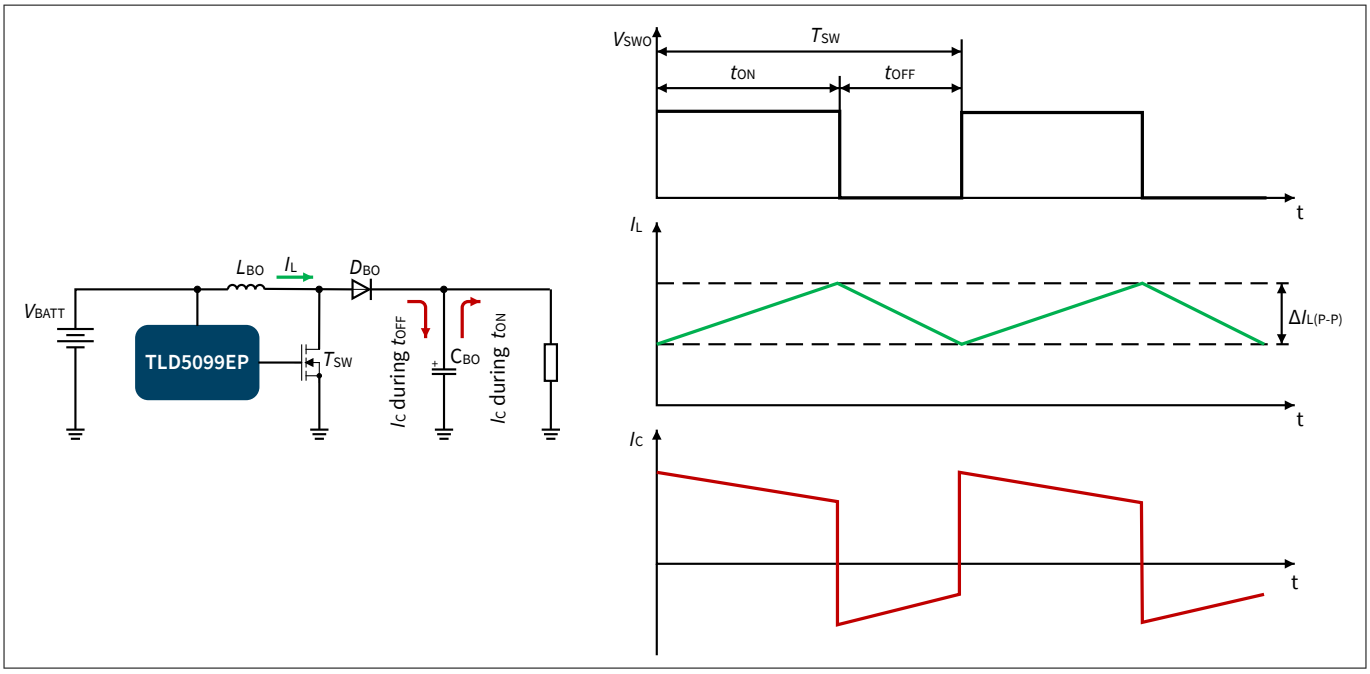

Figure 3 Current waveforms in reactive components and LED string

Assuming that the capacitor is discharged by a constant current (equal to average output current) for a time equal to t_{ON} and knowing the maximum ripple, the capacitor value can be calculated in worst condition when duty cycle is maximum by:

$$C \geq \frac{I_{OUT}}{\Delta V_{OUT}} \cdot \frac{D_{MAX}}{f_{SW}} = \frac{1.5\ A}{0.36\ V} \cdot \frac{0.778}{400\ \text{kHz}} = 8.1\ \mu\text{F} \quad (9)$$

This value has to be increased to consider also the equivalent series resistor (ESR) contribution to the output ripple.

Selecting for example 20 µF, the output ripple caused by ideal capacitor is:

$$\Delta V_{OUT} = \frac{I_{OUT}}{C_{OUT}} \cdot \frac{D_{MAX}}{f_{SW}} = \frac{1.5\ A}{20\ \mu\text{F}} \cdot \frac{0.778}{400\ \text{kHz}} = 145.9\ \text{mV} \quad (10)$$

Then the range for the ESR contribution to the ripple can be up to 214.1 mV (calculated as 360 mV to 145.9 mV)

The higher the output capacitance, the higher the ESR contribution can be.

The ripple associated to the ESR is calculated during two phases:

- During capacitor discharging it can be described by:
  $\Delta V_{ESR} = R_{ESR} \cdot I_{OUT}$
- During the charging phase it can be described by:
  $\Delta V_{ESR} = R_{ESR} \cdot (I_L - I_{OUT})$

$$R_{ESR} \leq \frac{\Delta V_{ESR}}{I_{OUT}} = \frac{214.1\ mV}{1.5\ A} = 142\ m\Omega \quad (11)$$

$$R_{ESR} \leq \frac{\Delta V_{ESR}}{I_{L\_MAX} - I_{OUT}} = \frac{214.1\ mV}{3.33\ A - 1.5\ A} = 117\ m\Omega \quad (12)$$

The calculation above is valid only if the load draws a constant average current from the output capacitor. In case of pulsed load a proper sizing of output capacitors and other workarounds are presented in Chapter 2.5.

2.3 Input PI filter

A PI input filter is a common choice to filter out the undesired frequency components that affect the emission spectrum in the standardized bands.

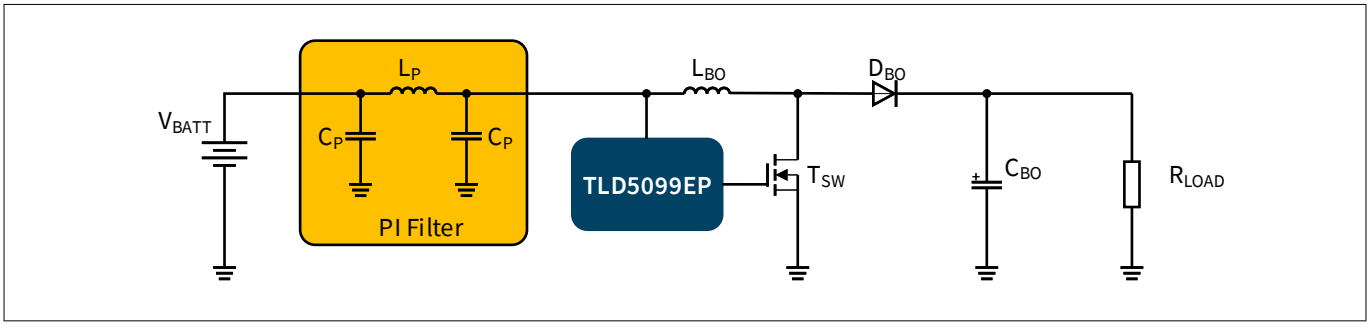

Figure 4 PI filter simplified schematic

Parasitic effects on capacitors and inductor shape the frequency response of PI filter and for this reason it works fine between 5 to 10 MHz. At higher frequency, special care has to be taken for a PCB layout with minimized parasitic elements in order to ensure low EMI emissions.

The real frequency response of the filter is shown in Figure 5. The filter has a maximum attenuation factor inside the damp zone.

2 Main regulator design

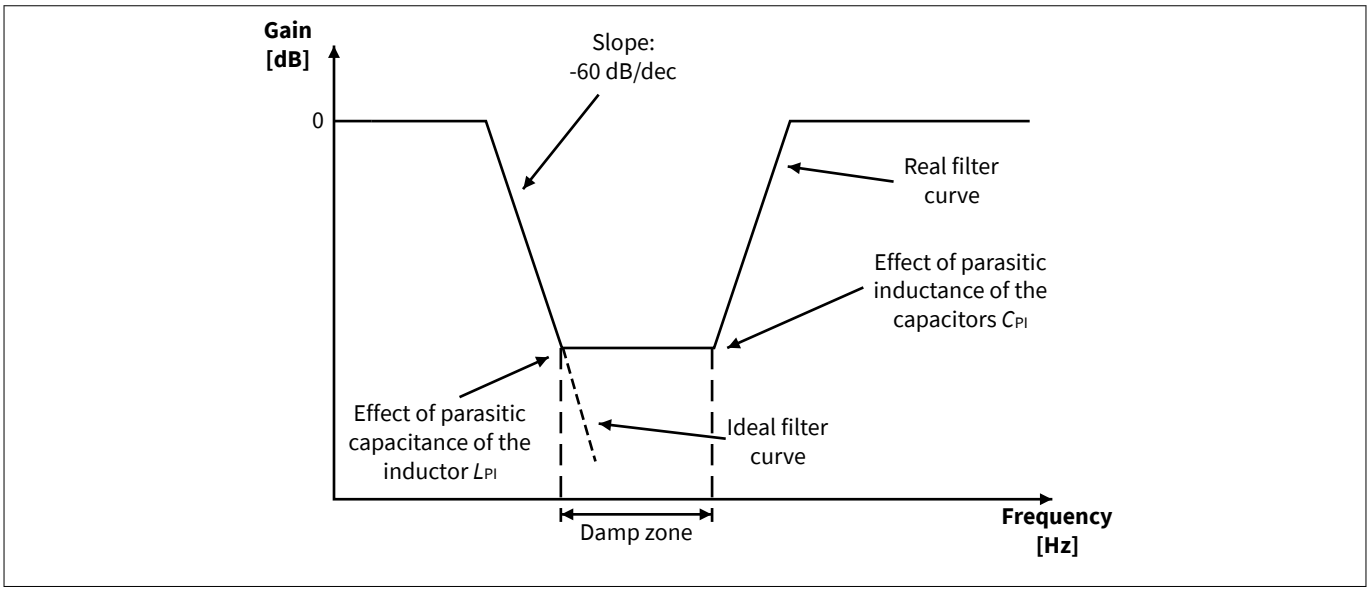

Figure 5 Frequency characteristic of PI filter

To achieve good results, the damp zone of the filter has to be placed where harmonics of the switching frequency may exceed the limits related to the standard. Usually, harmonics of the switching frequency cause problems in the AM band (525 kHz to 1.7 MHz).

To design the PI filter, the following rules of thumb can be used:

- Select L_{PI} equal 1/10 * L_{BO} = 2.2 µH
- Put the corner frequency of PI filter 1/10 of the switching frequency of DC-DC then, f_{PI} = 0.1 * f_{SW} = 40 kHz
- Have equal capacitance distribution on both sides of PI-Filter and value

$$C_{PI} = \frac{1}{4 \cdot \pi^2 \cdot L_{PI} \cdot f_{PI}^2} = \frac{1}{4 \cdot \pi^2 \cdot 2.2\,\mu\text{H} \cdot (40\ \text{kHz})^2} = 7.2\,\mu\text{F} \quad (13)$$

Then, for each side of PI filter at least 7.2 µF is needed; a possible choice is to have 2 capacitors of 4.7 µF that minimize parasitic effects.

For this purpose, CGA5L3X7R1V475K160AB is a good candidate for the capacitors while the inductor could be SPM4015T-2R2M-LR.

2.4 Switching transistor

NMOS type device is used as switching element of the proposed DC-DC. The switching behavior is illustrated in Figure 6.

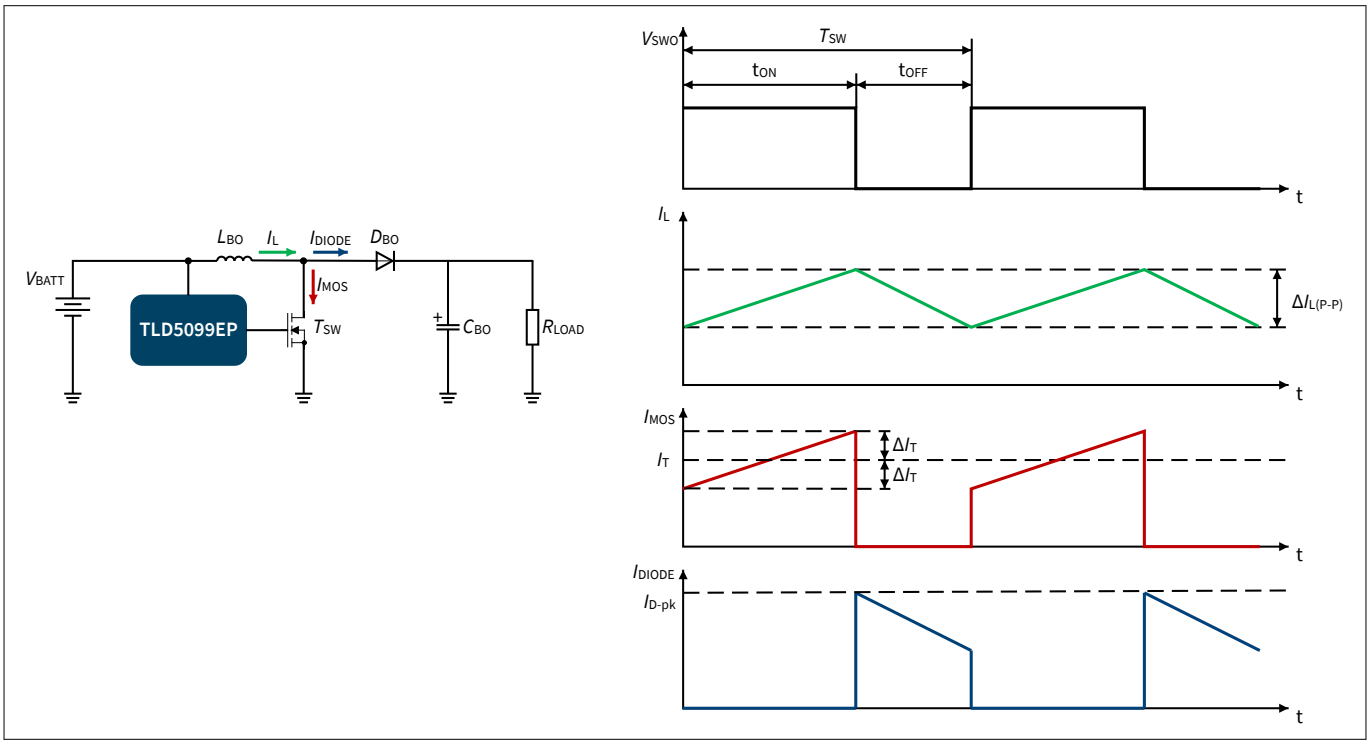

Figure 6 Current waveforms in power devices and inductor

The RMS value of the current that flows into the transistor can be calculated as:

$$I_{T\_RMS} = \sqrt[2]{\frac{1}{T}\int_0^T I_{MOS}(t)^2 dt} = \sqrt[2]{\frac{1}{T}\int_0^T \left(\frac{(I_T + \Delta I_T - I_T + \Delta I_T)\cdot t}{t_{ON}} + (I_T - \Delta I_T)\right)^2 dt}$$
$$= \sqrt{\frac{t_{ON}}{3T}\left(I_{MOS\_MIN}^2 + I_{MOS\_MIN}\cdot I_{MOS\_MAX} + I_{MOS\_MAX}^2\right)} \quad (14)$$
$$= \sqrt{\frac{D}{3}\left(I_{MOS\_MIN}^2 + I_{MOS\_MIN}\cdot I_{MOS\_MAX} + I_{MOS\_MAX}^2\right)}$$

Considering the MOSFET current during the ON state is the same as the inductor current. The equation above, Equation (14) has a maximum when V_{IN} is minimal (duty cycle is also at maximum) and it can be calculated as:

$$I_{T\_RMS,MAX} = \sqrt{\frac{D_{MAX}}{3}\left(I_{L\_MIN\_VIN,MIN}^2 + I_{L\_MIN\_VIN,MIN}\cdot I_{L\_MAX\_VIN,MIN} + I_{L\_MAX\_VIN,MIN}^2\right)}$$
$$= \sqrt{\frac{0.778}{3}\left((3.33\ A - 0.35\ A)^2 + (3.33\ A - 0.35\ A)\cdot(3.33\ A + 0.35\ A) + (3.33A - 0.35A)^2\right)} \quad (15)$$
$$= 2.94\ A$$

When the MOSFET is in off state it is stressed by the voltage equal to output voltage (voltage drop on diode is not taken into account). A device with a 60 V_{DS} capability fits this application.

For EMI reasons, it is common practice to place a R_{GATE} resistor of approximately 4.7 Ω to 15 Ω in series to the gate. This facilitates a smooth transition from the OFF state to ON state of the MOSFET. On the other hand, this lowers the overall efficiency of the converter.

To avoid excess of power losses, switching transistors for DC-DC applications have to be fast in transition and low resistive during the conduction time. The two relevant datasheet parameters are Q_g (affects the switching time and the switching losses) and $R_{DS(ON)}$ (affects the static losses). Infineon offers a wide variety of MOSFETs covering the needs of many applications. In this case IPD15N06S2L-64 is a good compromise of gate charge Q_g and $R_{DS(ON)}$.

2.5 Rectifier diode

The diode D_{BO} is the rectification device of the DC-DC. The current that flows into the device is depicted in blue in Figure 6 and it can be described by the following equation:

$$I_{D\_RMS_{MAX}} = \sqrt{\frac{t_{OFF}}{3T}\left(I_{L_{MIN}}^2 + I_{L_{MIN}} \cdot I_{L_{MAX}} + I_{L_{MAX}}^2\right)}$$
$$= \sqrt{\frac{1-D}{3}\left((3.33A - 0.35A)^2 + \left(3.33A - 0.35A\right) \cdot \left(3.33A + 0.35A\right) + (3.33A - 0.35A)^2\right)} \quad (16)$$
$$= 1.56\ A$$

During the ON state of the transistor, the voltage across the diode is V_{OUT} = 41.4 V (voltage drop on the transistor and sensing resistor is not take into account). To provide for a margin of tolerance, a 60 V Schottky diode has to be selected.

A good choice for this kind application could be the Vishay VSS8D3M6 that provides 0.47 V forward voltage during the ON state.

2.6 Current sense resistor

The current control loop embedded inside TLD5099EP helps the system to increase stability. The feature is enabled by the sensing resistor R_{SWCS}. The resistor is placed below the transistor (refer to Figure 7) and senses the current into the switching NMOS and inductor. It converts the current flowing into the transistor into a voltage sensed by SWCS pin. The maximum voltage across the resistor must not reach the switch peak overcurrent threshold V_{SWCS} of 150 mV under typical conditions. This has to be true not only during the steady state but also during the transition phase.

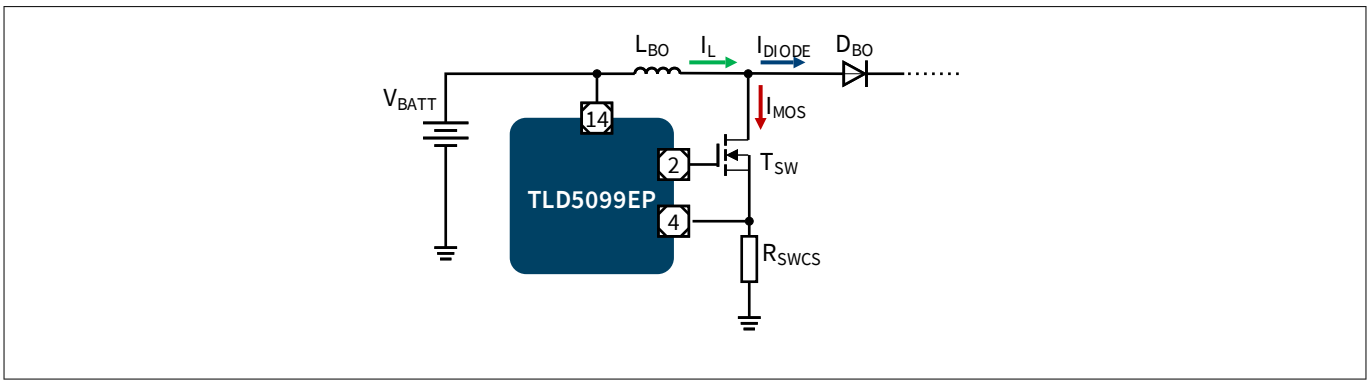

Figure 7 Peak current sensing resistor

For example if the system has a phase margin of 45° (the minimum bandwidth for a stable system), the output has an overshoot of about 50%. This is also reflected at the input side then the inductor current and switching

current have the same overshoot. Taking into account the corner case with lower V_{IN}, the maximum current in the R_{SWCS} can be calculated as:

$$R_{SWCS} < \frac{V_{SWCS}}{1.5 \cdot I_{L\_MAX}} = \frac{150\,mV}{1.5 \cdot 3.65A} = 27\,m\Omega \quad (17)$$

The impact on stability of current control loop is evaluated in Chapter 3.

To provide for a margin of tolerance, 18 mΩ is a good choice. The RMS current that flows into the resistor is equal to the current flowing into power NMOS, then the power dissipated by the resistor is:

$$P = R_{SWCS} \cdot I_{NMOS}^2 = 18\ m\Omega \cdot (2.94\ A)^2 = 155.6\,mW \quad (18)$$

To avoid overheating of the resistor it is a common practice to use resistors with 4 to 5 times higher power rating. For this application RCWL1218R018JQ from Vishay satisfies the requirements.

2.7 Output resistor divider

The output voltage is fixed by means of a resistor divider on feedback loop (refer to Figure 8). With the given reference voltage and biasing currents, the output voltage can be calculated as:

$$V_{OUT} = \frac{V_{REF}}{R_{FB2}} \cdot \left(R_{FB1} + R_{FB2} + R_{FB3}\right) + R_{FB1} \cdot I_{FBH} - R_{FB3} \cdot I_{FBL} \quad (19)$$

Where I_{FBH} and I_{FBL} are the currents flowing into FBH and FBL pins.

The device regulates V_{REF} across R_{FB2}. To reduce the power losses and to reduce the noise susceptibility, the current into the resistor divider should be in the range of 1 mA to 5 mA. Assuming 2 mA, this leads to:

$$R_{FB2} = \frac{V_{REF}}{I_{RFB2}} = \frac{300\,mV}{2\,mA} = 150\,\Omega \quad (20)$$

The remaining two resistors are selected to meet the target voltage

Selecting

- R_{FB1} = 7500 Ω
- R_{FB2} = 150 Ω
- R_{FB3} = 11000 Ω

The output voltage is adjusted up to 36.44 V

If a more precise voltage is needed, SET pin can be used to adjust V_{REF} and then, in turn, also adjusts the final output voltage.

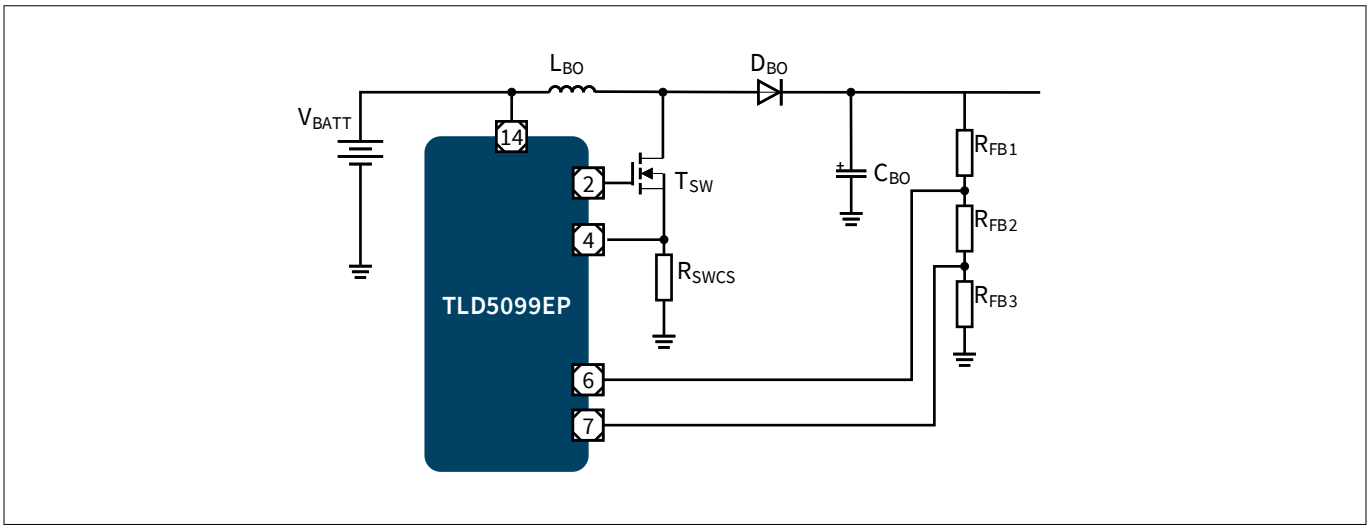

Figure 8 Feedback network

2.8 Spread spectrum

The spread spectrum modulator reduces the peak values of the EMI spectrum and flattens the power from the narrow peaks of the spectrum into a broad band signal by modulating the switching frequency.. It is activated by selecting the low resistor set for R_{FREQ} highlighted in Figure 9

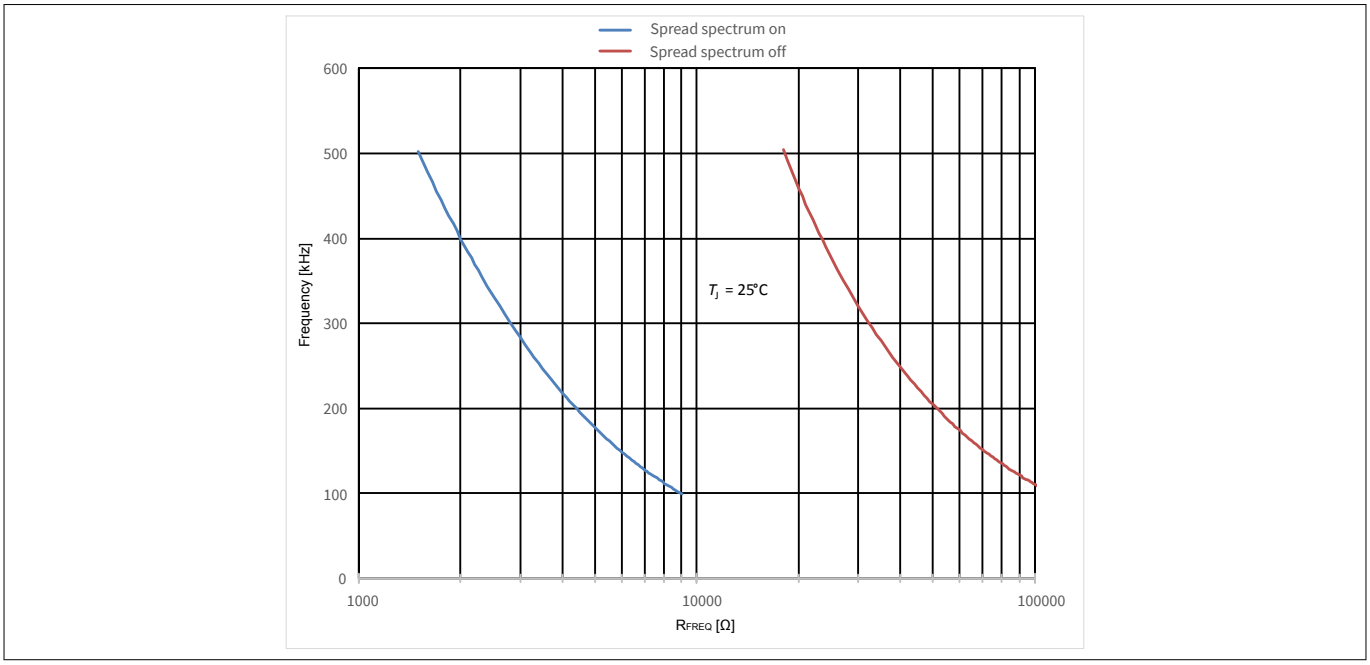

Figure 9 Switching frequency f_{SW} versus frequency select resistor to GND R_{FREQ}

To switch at 400 kHz with spread spectrum activated, a resistor can be selected by equation:

$$R_{\mathrm{FREQ-SSMon}} = \frac{1}{\left(600 \cdot 10^{-12} \cdot f_{\mathrm{FREQ}}\right)^{0.943}} - 600 = \frac{1}{\left(600 \cdot 10^{-12} \cdot 400\,\mathrm{kHz}\right)^{0.943}} - 600 = 1.99\,\mathrm{k\Omega} \quad (21)$$

Then 2.0 kΩ (E96 series) has to be selected and connected between pin 11 and ground.

This feature is available only with TLD5099EP [1]. If TLD5098EP [2] or TLD5097EP [3] is used, the equation to calculate the R_{FREQ} is described in the respective datasheet.

2.9 Overvoltage protection

When the load changes abruptly, the device takes a number of clock cycles to achieve the new steady state. During this time all the energy stored in the inductor is moved to the output capacitor, causing an output voltage higher than expected. This output voltage could become even higher than the voltage rating of the output capacitor.

When the overvoltage protection is triggered, TLD5099EP disables the internal gate driver connected to SWO pin. For a voltage regulator the threshold can be set 10% higher than typical output voltage.

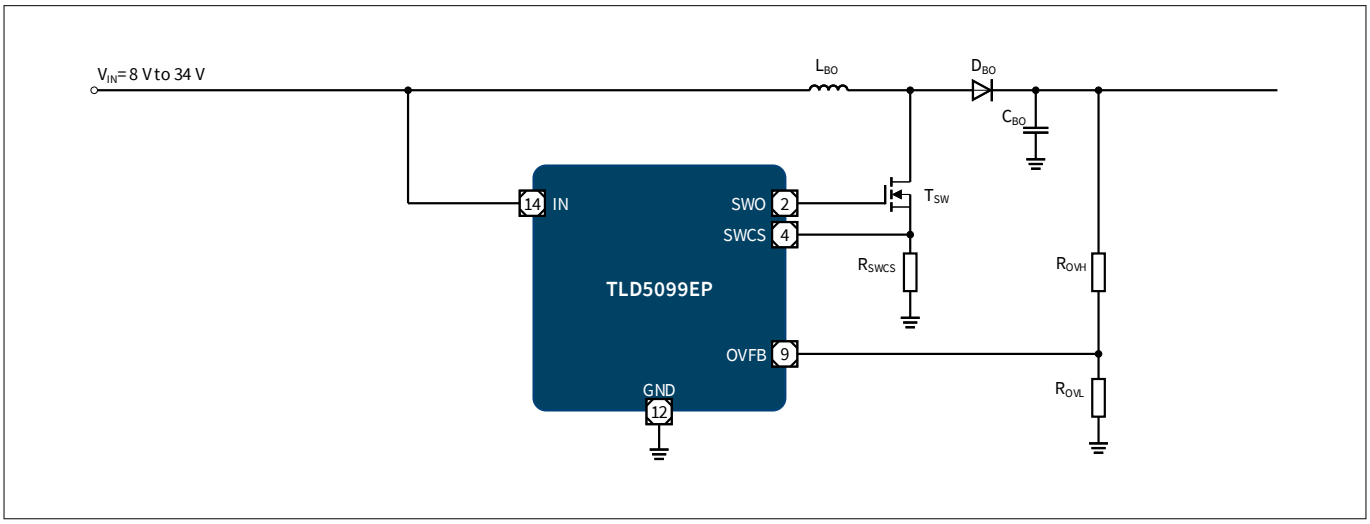

Figure 10 Overvoltage protection schematic

Overvoltage is triggered when the voltage on OVFB pin reaches 1.25 V.

A resistor divider is used to scale the output voltage to a suitable range for TLD5099EP. In this case, a current in range of 1 mA to 5 mA helps to avoid excess power losses and to have good noise immunity. Fixing the current to 1.25 mA, the two resistors can be calculated as

$$R_{OVH} = \frac{V_{OUT\_MAX} - V_{OVFB,TH}}{I_{R-OVFB}} = \frac{40\,V - 1.25\,V}{1.25\,mA} = 31\,k\Omega \quad (22)$$

$$R_{OVL} = \frac{V_{OUT\_MAX}}{I_{R-OVFB}} = \frac{1.25\,V}{1.25\,mA} = 1\,k\Omega \quad (23)$$

3 Compensation network

The TLD5099EP has a dedicated pin where the compensation network can be applied. An added RC network on this pin generates poles and zeros that shape the system transfer function.

In small signal approximation, the open loop transfer function of a DC-DC is the product of the modulator transfer function and the feedback network transfer function.

The modulator transfer function can be expressed as product of two main parts: the gain of the error amplifier (voltage loop) and the gain of the current mode modulator (current loop).

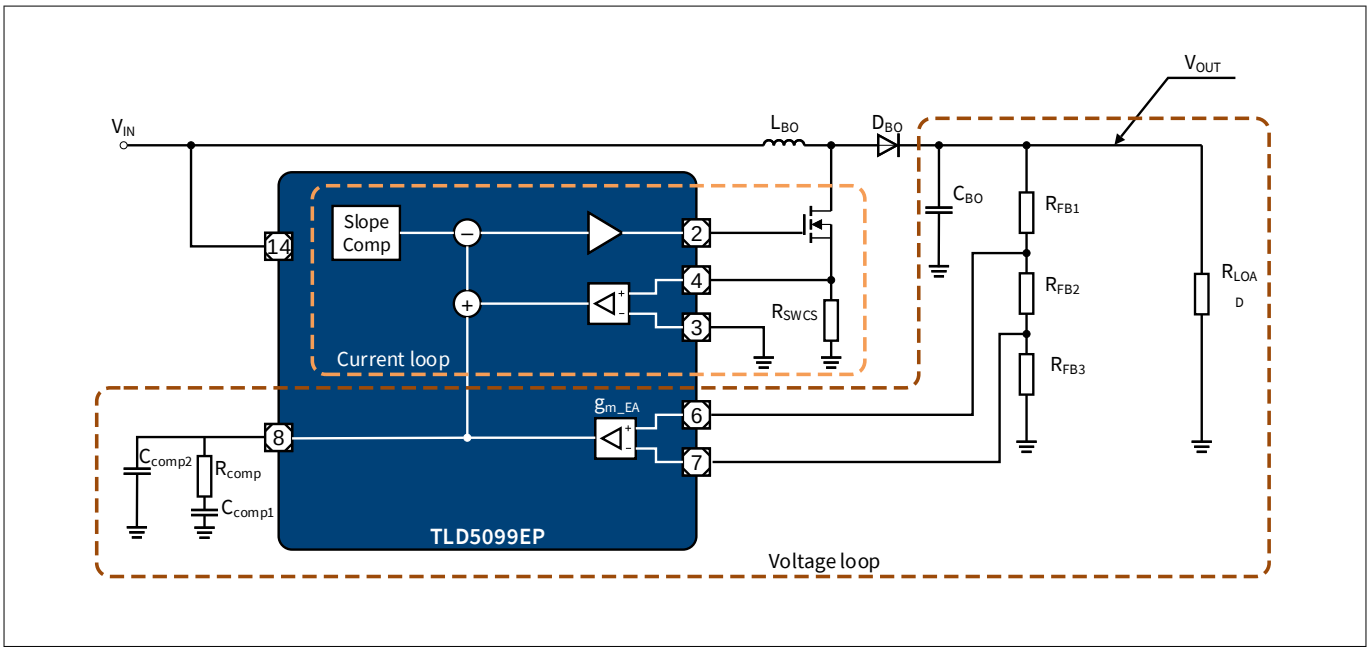

Figure 11 Compensation network schematic

The gain of the error amplifier can de described with:

$$\tau_{p3} = C_{\mathrm{OUT}} \cdot R_{\mathrm{LOAD}} \tag{24}$$

Where:

- $g_{\mathrm{m\_EA}}$ is the trans-conductance of the error amplifier (typical 600 µS)
- R_{EA} is the output resistance of the error amplifier (typical 2.5 MΩ)
- $\tau_{z1} = C_{\mathrm{COMP1}} \cdot R_{\mathrm{COMP}}$ is the zero of compensation network
- $\tau_{p1} = (C_{\mathrm{COMP1}} + C_{\mathrm{COMP2}}) \cdot R_{\mathrm{EA}}$ is the pole associated to compensation network and the resistor of error amplifier
- $\tau_{p2} = C_{\mathrm{COMP2}} + R_{\mathrm{COMP}}$ is a pole associated to compensation network

The gain of the current mode modulator can be described following the model presented by R.B Ridley [4]. It can be mathematically described as:

$$A_{\mathrm{CM}}(s) = \frac{0.2 \cdot (1-D) \cdot R_{LOAD}}{2 \cdot R_{\mathrm{SWCS}}} \cdot \frac{(1 + s \cdot \tau_{z2})}{(1 + s \cdot \tau_{p3}) \cdot \left(1 + \frac{s}{\omega_n \cdot Q} + \frac{s^2}{\omega_n^2}\right)} \tag{25}$$

Where:

- R_{LOAD} is the total resistor at the output of DC-DC

3 Compensation network

- V_{LOAD} is the output voltage
- $\tau_{z2} = \frac{L_{BO}}{(1-D)^2} \cdot \frac{I_{OUT}}{V_{OUT}}$ is the zero of the boost DC-DC

- $\tau_{p3} = C_{OUT} \cdot R_{LOAD}$ is the pole associated to boost converter
- ω_n is the natural pulsation of the system
- $Q = \frac{1}{\pi \cdot \left(\left(1 + \frac{S_e}{S_n}\right) \cdot \left(1 - D\right) - 0.5\right)}$ is the quality factor of a second order system, where:
  - $S_e = 50 \cdot 10^{-6} \cdot f_{sw}$ is the slope of current compensation circuit (coefficient fixed by internal references)
  - $S_n = \frac{V_{IN} \cdot R_{SWCS}}{L_{BO}} \cdot 10^{-3}$ where S_n is the slope of the current sensed by R_{SWCS}

Using the data previously calculated, it is possible to calculate the gain in DC, cross over frequency f_c and the phase margin.

The transfer function of the feedback network is the ratio between R_{FB} and the R_{LED}

$$\beta = \frac{R_{FB2}}{R_{FB1} + R_{FB2} + R_{FB3}} \tag{26}$$

For the gain calculation in typical conditions, the three parts to be calculated are:

$$\begin{aligned} A_{EA}(0) &= g_{m_{EA}} \cdot R_{EA} = 0.0006\ s \cdot 2.5\ M\Omega = 1500 \\ A_{CM}(0) &= \frac{0.2(1-D) \cdot R_{LOAD}}{2 \cdot R_{SWCS}} = \frac{0.2 \cdot (1 - 0.625) \cdot 54\ \Omega}{2 \cdot 0.018\ \Omega} = 112.5 \\ \beta &= \frac{R_{FB2}}{R_{FB1} + R_{FB2} + R_{FB3}} = \frac{160\ \Omega}{7.5k\Omega + 160\ k\Omega + 11\ \ k\Omega} = 0.0086 \end{aligned} \tag{27}$$

And then the gain in DC can be calculated as:

$$T(0)|_{dB} = 20 \cdot \log(A_{EA}(0) \cdot A_{CM}(0) \cdot \beta) = 20 \cdot \log(1500 \cdot 112.5 \cdot 0.0086) = 63.2dB \tag{28}$$

Using just a proportional and integrative compensation with R_{COMP} = 2200 kΩ and C_{COMP} = 22 nF, the constant time elements are:

$$\tau_{p1} = (C_{COMP1} + C_{COMP2}) \cdot R_{EA} = (22\ nF + 0) \cdot 2.5\ M\Omega = 0.055\ s \tag{29}$$

$$\tau_{p2} = C_{COMP2} \cdot R_{COMP} = 0\ F \cdot 2200\ \Omega = 0\ \ s \tag{30}$$

$$\tau_{p3} = C_{OUT} \cdot R_{LOAD} = 20\ \mu F \cdot 54\ \Omega = 1.08 \cdot 10^{-3} s \tag{31}$$

$$\tau_{z1} = C_{COMP2} \cdot R_{COMP} = 220\ nF \cdot 4700\ \Omega = 1.0310^{-3} s \tag{32}$$

3 Compensation network

$$\tau_{z2} = -\frac{L_{BO}}{(1-D)^2} \cdot \frac{(I_{OUT})}{V_{OUT}} = \frac{22\mu H}{(1-0.625)^2} \cdot \frac{0.66\,A}{36\,V} = -4.44 \cdot 10^{-6} s \tag{33}$$

$$\omega_n = \pi \cdot \frac{f_{SW}}{2} = 628 \cdot 10^3 \,\mathrm{rad}/s \tag{34}$$

$$Q = \frac{1}{\pi \cdot \left(\left(1 + \frac{S_e}{S_n}\right) \cdot \left(1 - D\right) - 0.5\right)} = \frac{1}{\left(\left(1 + \frac{50\,\mu \cdot 400\,kHz}{0.001 \cdot \frac{13.2V}{22\,\mu H} \cdot 0.018\Omega}\right) \cdot (1 - 0.625) - 0.5\right)} = 0.25 \tag{35}$$

For stability reasons, it is common practice to have Q below 1. In case Q is too high, it is necessary to lower it by increasing the value of inductor or/and increasing the switching frequency and/or reducing R_{SWCS}.

By using a mathematical analysis tool, it is possible to extract the cutoff frequency and phase margin of the system.

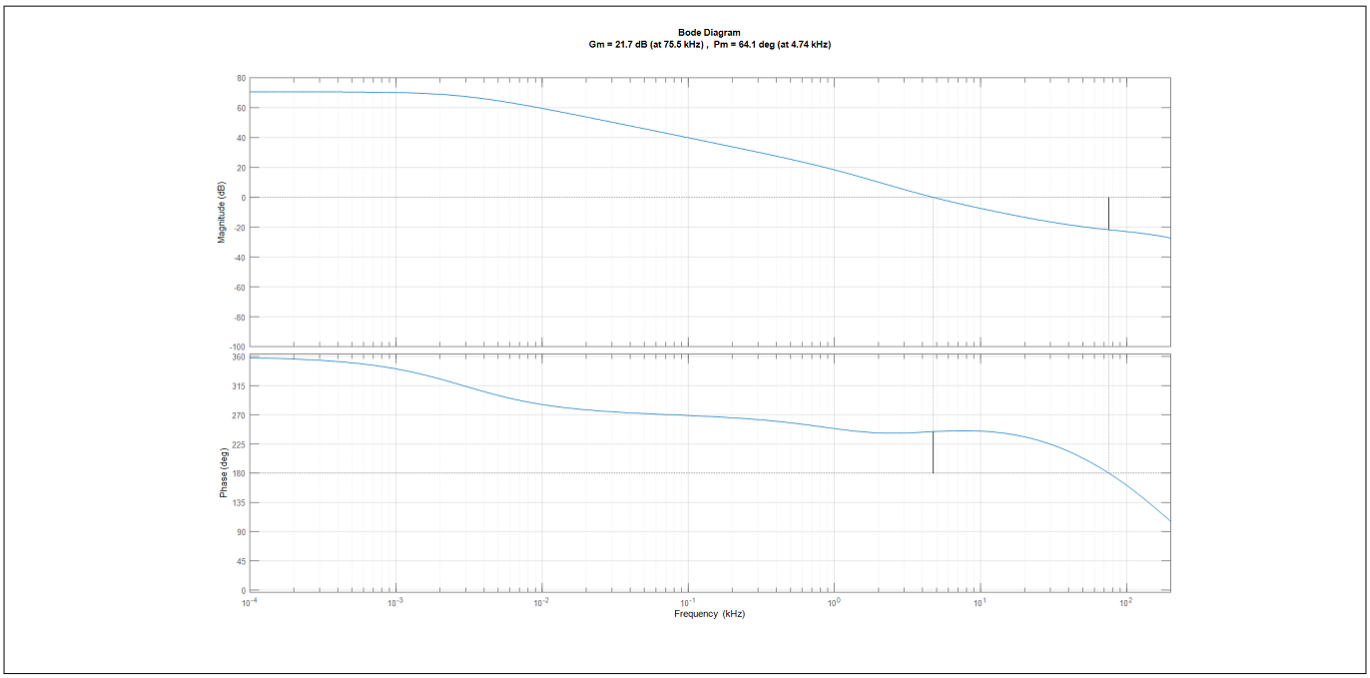

Figure 12 Cutoff frequency and phase margin calculated

As a rule of thumb, τ_{P1} is the dominant pole. By changing the value of C_{COMP1} it is possible to tailor the bandwidth of the system. The zero produced by C_{COMP1} and R_{COMP} is needed to compensate the pole τ_{P3}. If needed, C_{COMP2} can be used to reduce the secondary order effects.

Infineon can also provide SPICE models of the device to perform electrical simulation to double check performances.

4 Circuit revision in case of pulsed load

4.1 Increased output capacitor

As mentioned in Chapter 2.2, when a pulsed load is applied the output capacitor has to be carefully selected. This is the case when part of the load or even the full load is turned on without any synchronization with the DC-DC as illustrated in Figure 13.

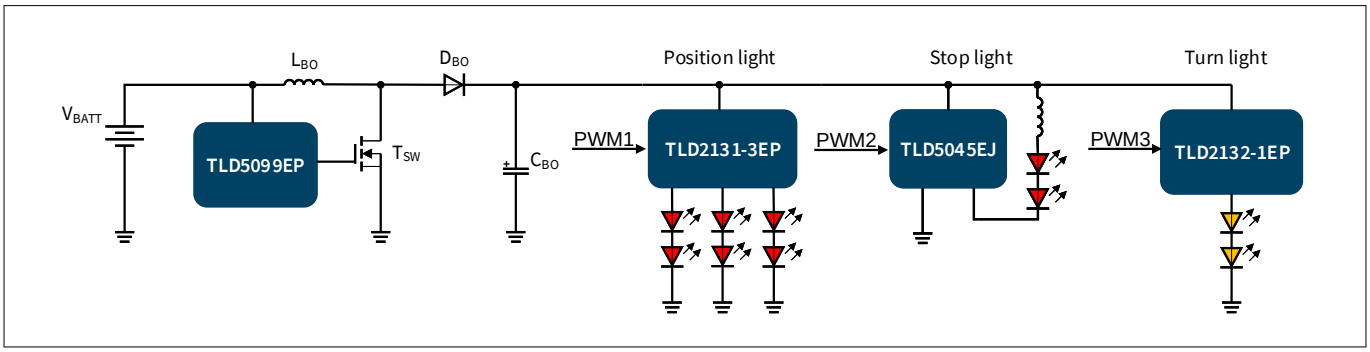

Figure 13 Application example with independent PWM for each current sources

When a load step is applied, the DC-DC controller takes several clock cycles to restore its steady state condition. The time elapsed is a function of the bandwidth of the system and the voltage step generated by the load pulse and can be quantified by:

$$\Delta V_{OUT} = \frac{\Delta I_{LOAD}}{C_{OUT}} \cdot \frac{2}{f_c} \tag{36}$$

Where f_c is the corner frequency (frequency where the gain curve intercepts the 0 dB axes) of the closed loop transfer function.

A reasonable value for the under voltage produced by a load step is in the order of 5% of the rated output voltage. With this assumption the output capacitor has to be increased to:

$$C_{OUT} \geq \frac{\Delta I_{LOAD}}{\Delta V_{OUT}} \cdot \frac{2}{f_c} = \frac{666.7\,mA}{0.05 \cdot 36\,V} \cdot \frac{2}{4.74\,kHz} = 156\,\mu F \tag{37}$$

This new output capacitor affects the stability and the new phase margin of the system and has to be re-calculated.

4.2 Feedforward compensation

Increasing the output capacitor also impacts the transfer function, lowering the bandwidth of the system and then increasing the time to return to the steady state. In order to boost the frequency response of the system, a feedforward capacitor can be used. To do this, a capacitor on the top of the resistor divider is added. This capacitor introduces an extra zero and one extra pole into the control loop transfer function.

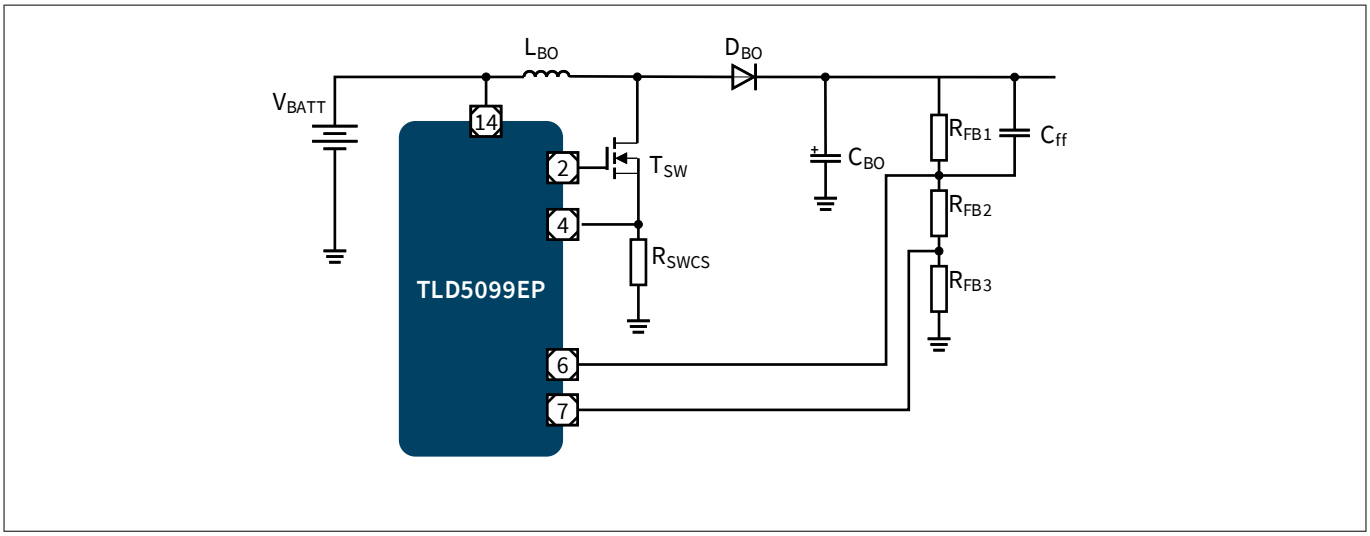

Figure 14 Feedforward feedback network

The pole introduced is located at

$$f_{POLE} = \frac{1}{2\pi \cdot C_{FF}} \left(\frac{1}{R_{\mathrm{FB1}}} + \frac{1}{R_{\mathrm{FB2}} + R_{\mathrm{FB3}}} \right) \tag{38}$$

While the zero is located at:

$$f_{ZERO} = \frac{1}{2\pi \cdot C_{FF} \cdot R_{\mathrm{FB1}}} \tag{39}$$

These two new parameters change the transfer function. To take them into account, the transfer function presented in Chapter 4.3 has to change as follows:

$$T(s) = A_{\mathrm{EA}}(s) \cdot A_{\mathrm{CM}}(s) \cdot \beta \cdot \frac{(1 + s/f_{ZERO})}{(1 + s/f_{POLE})} \tag{40}$$

4.3 PWM dimming

In rear light modules the PWM modulation is often used to dim the light of stop light (high brightness) down to position light (low brightness). The PWM modulation is applied to the LED driver (DC-DC or linear current sources). An example of this partitioning is illustrated in Figure 15.

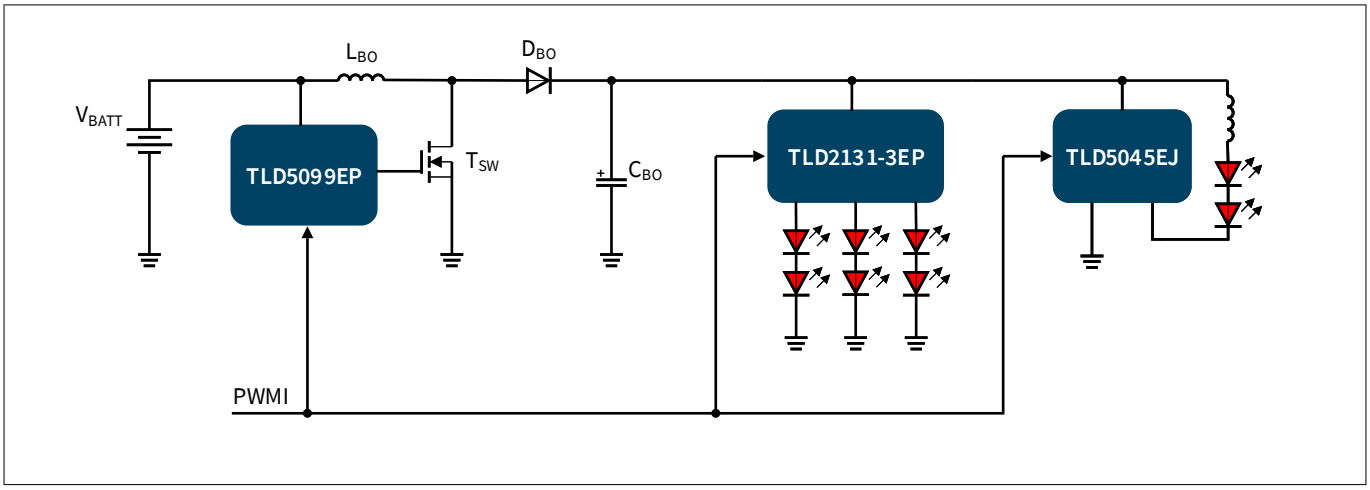

Figure 15 Application example with common PWM signal

Using PWM dimming the output capacitor can be left to the value calculated for steady state condition without any resizing proposed in Chapter 4.2.

The device reacts to different states of the PWM signal as follows:

- When the PWM signal is at high level the TLD5099EP operates normally, adjusting the output voltage according to input voltage and feedback voltage.
- When the PWM signal goes to low level, the device disables the gate driver connected to SWO and freezes the voltage on COMP pin. The output voltage does not evolve because there is no current absorbed by the load.

Therefore, when the PWM signal goes low, the device stops and does not supply power to the output, while when the PWM signal goes to high the device is biased to provide the exact amount of energy needed by the load and undershoots are avoided.

5 Conclusions

In this application note a voltage regulator based on TLD5099EP has been described. The application covers a typical automotive application where the regulator is used to supply multiple current sources with a constant voltage. The topology presented boosts the battery line to higher output voltage. This enables the second stage (buck converter or linear current regulators) to accommodate longer LED strings than when used connected directly to the battery.

Boost converters with TLD5099EP are also useful in other applications and not only related to the automotive environment. Applications supplied by battery strings or from USB ports can be addressed. All the formulas presented in the document can be applied to the target application.

If the spread spectrum feature is not needed for the target application, the TLD5099EP can be substituted with TLD5098EP or TLD5097EP without any degradation.

6 List of references

1. Infineon *TLD5099EP LITIX™ Power* Data Sheet Rev.1.00, 2019
2. Infineon *TLD5098EP LITIX™ Power Data Sheet* Rev.1.00, 2018
3. Infineon *TLD5097EP LITIX™ Power Data Sheet* Rev.1.00, 2018
4. Ridley, R. B.; *A new Continuous Time Model for Current Mode Control*; IEEE Transaction on Power Electronics; Vol. 6; Issue 2; pp. 271-280; 1991

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