LITIX™ Power PCB design guidelines

TLD5097EP, TLD5098EP, TLD5099EP

About this document

Scope and purpose

This application note is intended to provide guidance on how to design an optimized PCB with Infineon LITIX™ Power TLD5097EP, TLD5098EP and TLD5099EP DC-DC controllers.

This application note shall be used in conjunction with the Infineon application note **Z8F80033952 - LITIX™ PCB design guideline** *[1]* and the latest Infineon LITIX™ Power TLD5097EP, TLD5098EP and TLD5099EP datasheets *[2]*, *[3]*, *[4]* for a detailed component description. It is meant as an add-on to the datasheets and not as a document explaining the devices in detail. It is also not a replacement for the datasheets.

Note: *The following information is given as a hint for the implementation of the LITIX™ Power TLD5097EP, TLD5098EP and TLD5099EP devices only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.*

Intended audience

Hardware engineers in the design of PCB layout with a LITIX™ Power TLD5097EP, TLD5098EP and TLD5099EP controller.

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1 Abstract

Before reading this application note, it is recommended to read the Infineon application note **Z8F80033952 - LITIX™ PCB design guideline** *[1]*, where all the points in this document have been explained in detail.

In order to explain as clearly as possible all the critical points that should be considered while drawing a DC-DC PCB layout, a medium power DC-DC converter has been used as an example.

The following basic parameters should be obtained from the circuit designer before starting the PCB layout.

Table 1 Basic parameters to know before starting a DC-DC PCB layout

Symbol	Parameter	Purpose
P_{OUT}	Output power	Used to get power losses
η	Efficiency	
I_{IN}	Input current	Used to determine the width of power traces
I_{OUT}	Output current	
T_{J_MAX}	Maximum junction temperature of the MOSFET	Used to size the heatsink and the heat conduction path
T_A	Ambient temperature	
$P_{LOSS,MOS}$	Power loss on MOSFET	
R_{thJC}	Thermal resistance junction-case of the MOSFET	

In the following example all of these parameters will be used to design the PCB layout.

2 Example description

An example of a DC-DC as a boost to ground current source, typically used to light up power LEDs in the daytime running light (DRL) application is depicted in these chapters. It uses a TLD5098EP as PWM controller.

Note: The following example is given as a rough PCB design exercise for the implementation of the Infineon LITIX™ Power TLD509x family only. It shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.

This converter features the following characteristics that are useful in sizing traces, copper thickness and the heatsink:

- Output power, P_{OUT} = 15 W
- Efficiency, η = 0.85
- Input current, I_{IN} = 2.5 A
- Output current, I_{OUT} = 1.0 A
- Maximum junction temperature of the MOSFET, T_{J_MAX} = 160°C
- Ambient temperature, T_A = 105°C
- Power loss on MOSFET, $P_{LOSS,MOS}$ = 0.8 W
- Thermal resistance junction-case of the MOSFET, R_{thJC} = 5.1 K/W

2.1 Schematic

Figure 1 depicts the schematic of the DC-DC as a boost to ground current source, typically used to light up power LEDs in daytime running light (DRL). In this example it is supposed that the PCB is a four-layer stack in order to get the lowest EME. Verify if a different layer stack is needed, by consulting Chapters 1.1 and 3 of Infineon application note **Z8F80033952 - LITIX™ PCB design guideline** ***[1]***.

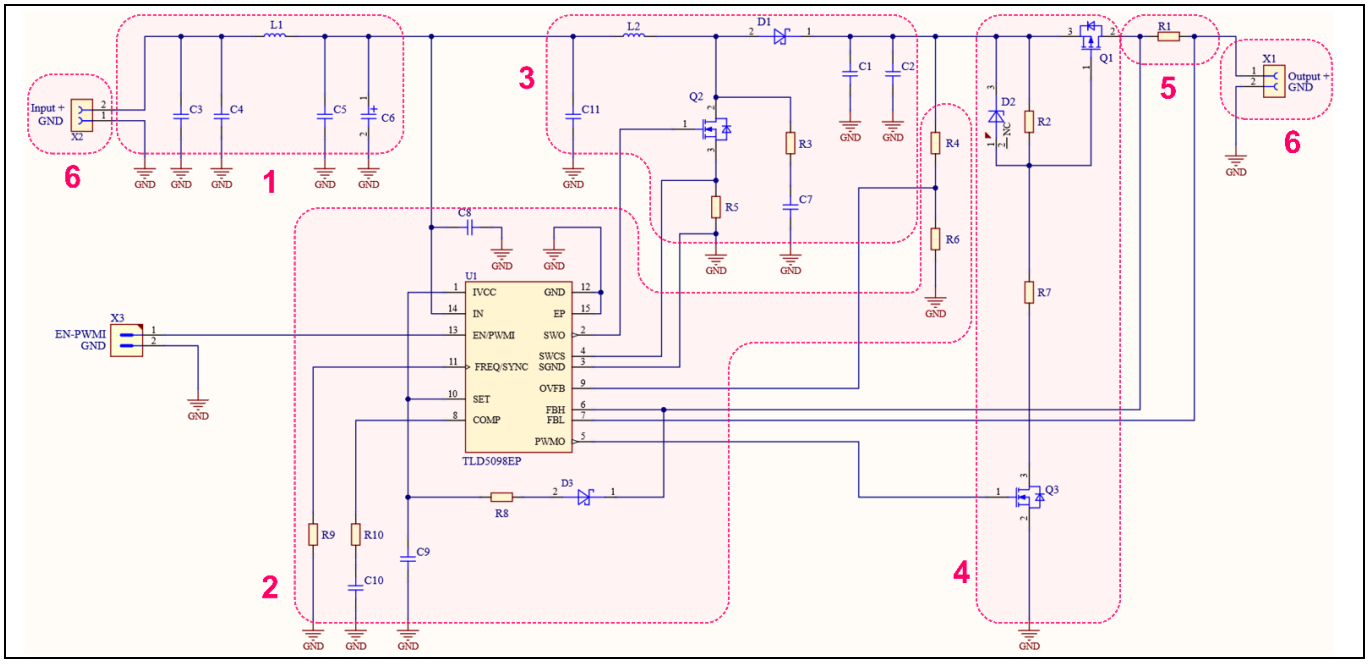

Figure 1 Schematic of application example

Example description

Six function groups can be easily recognized here on the schematic and also on the PCB in Figure 3:

1. Input filter stage
2. Controller
3. Power stage
4. Dimming circuit
5. Current sense shunt
6. Power connectors

2.2 PCB Layout

The layout designed for this example is depicted in ***Figure 2***.

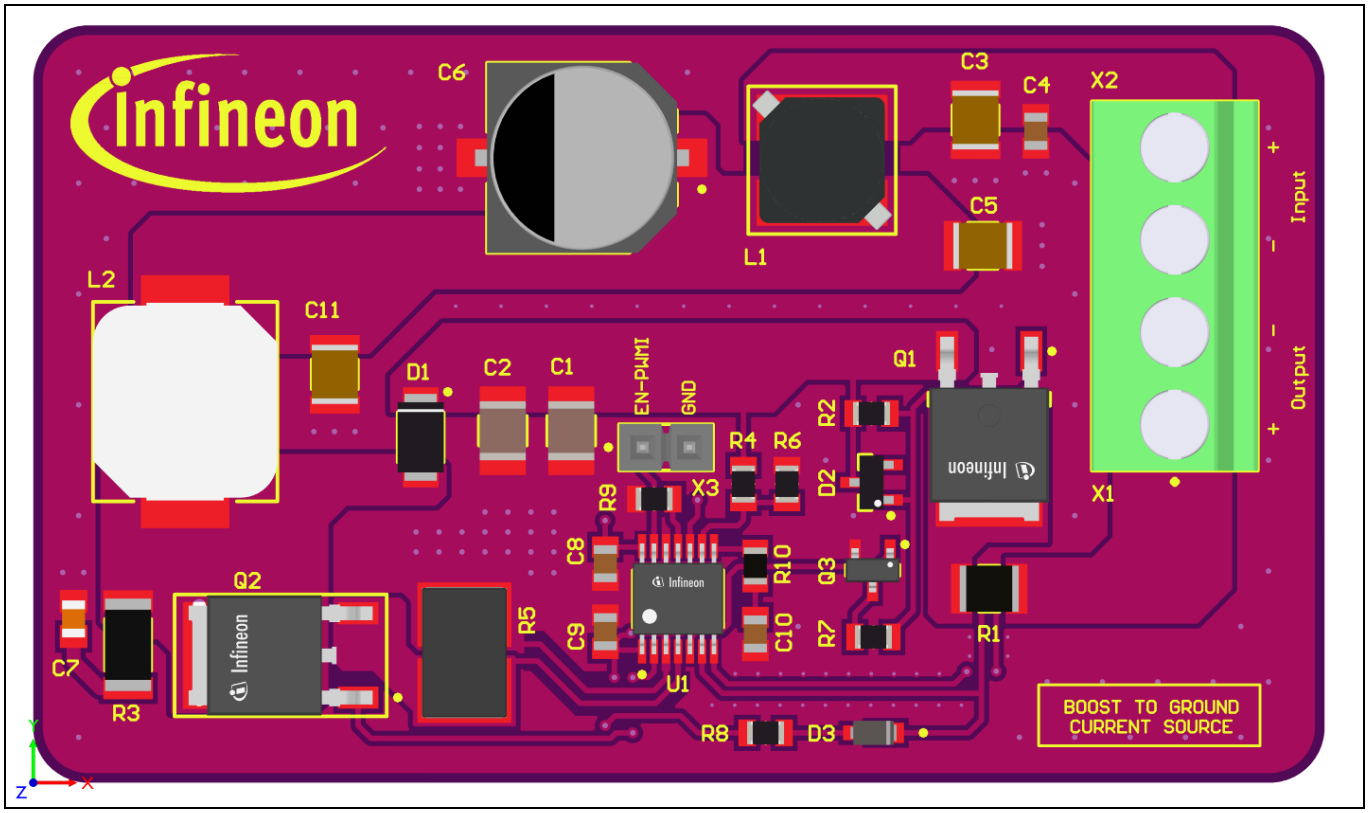

Figure 2 Placement of components

One of the most common rules is try to keep all the components that belong to the same group closely together in the same area. Referring to the schematic in ***Figure 1***, these groups can be identified in the layout depicted in ***Figure 3***.

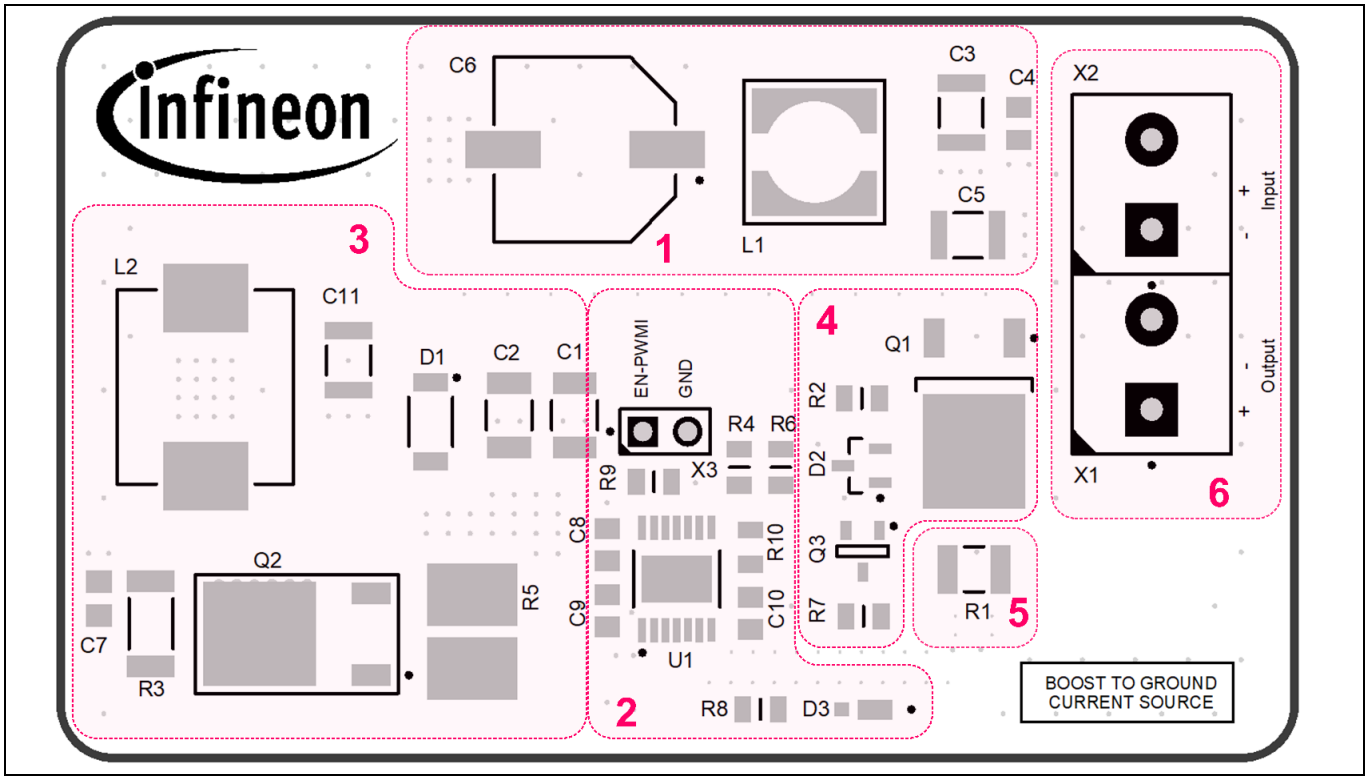

Figure 3 Component groups

2.3 Layers

A complete view of all four copper layers stacked in the example PCB is depicted in the following figures.

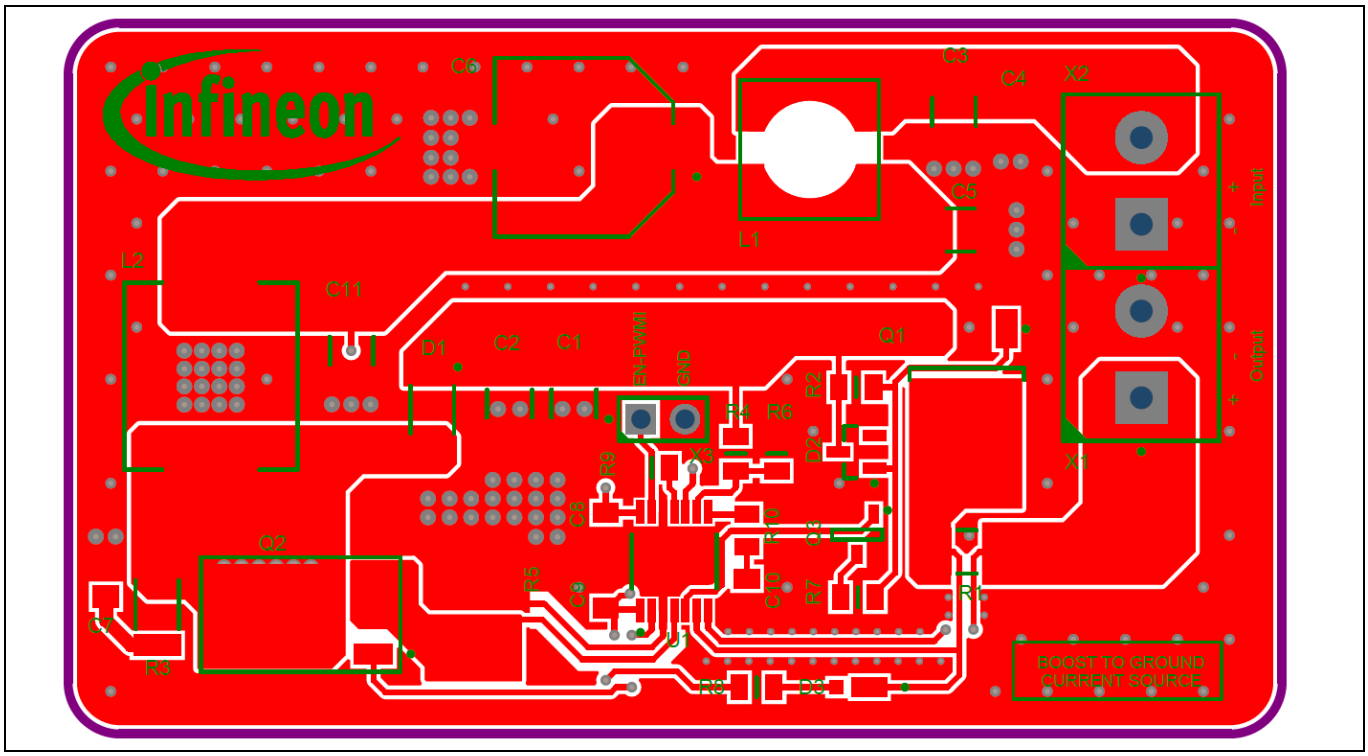

Figure 4 Top overlay

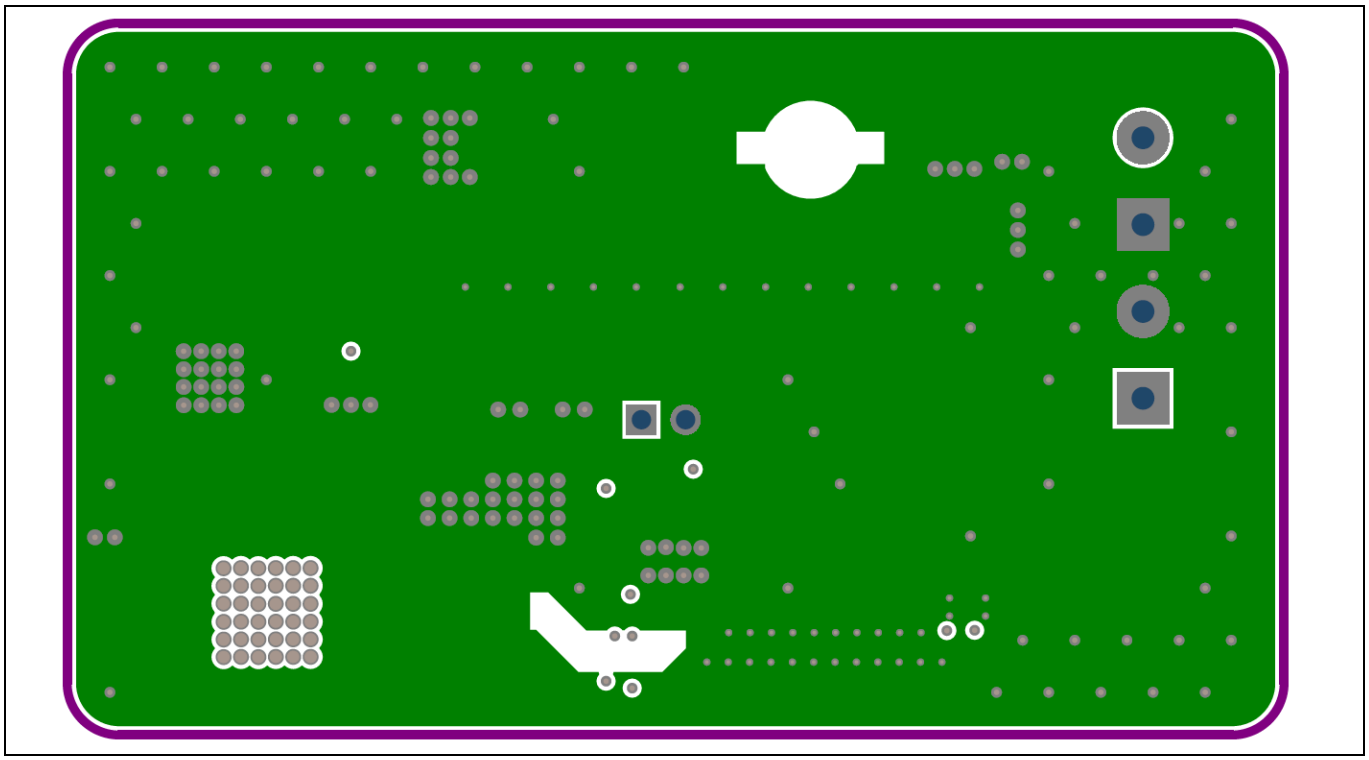

Figure 5 Internal overlay 1 (ground plane)

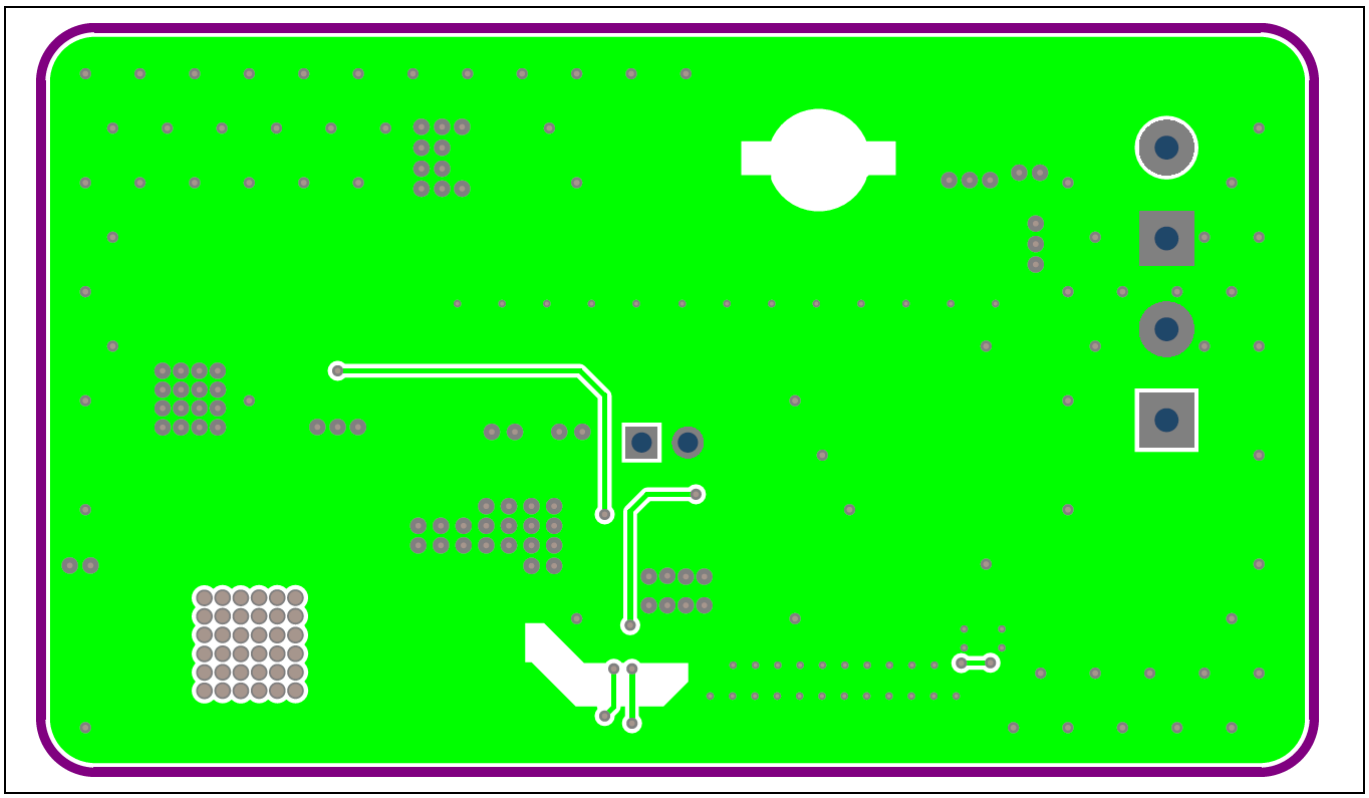

Figure 6 Internal overlay 2

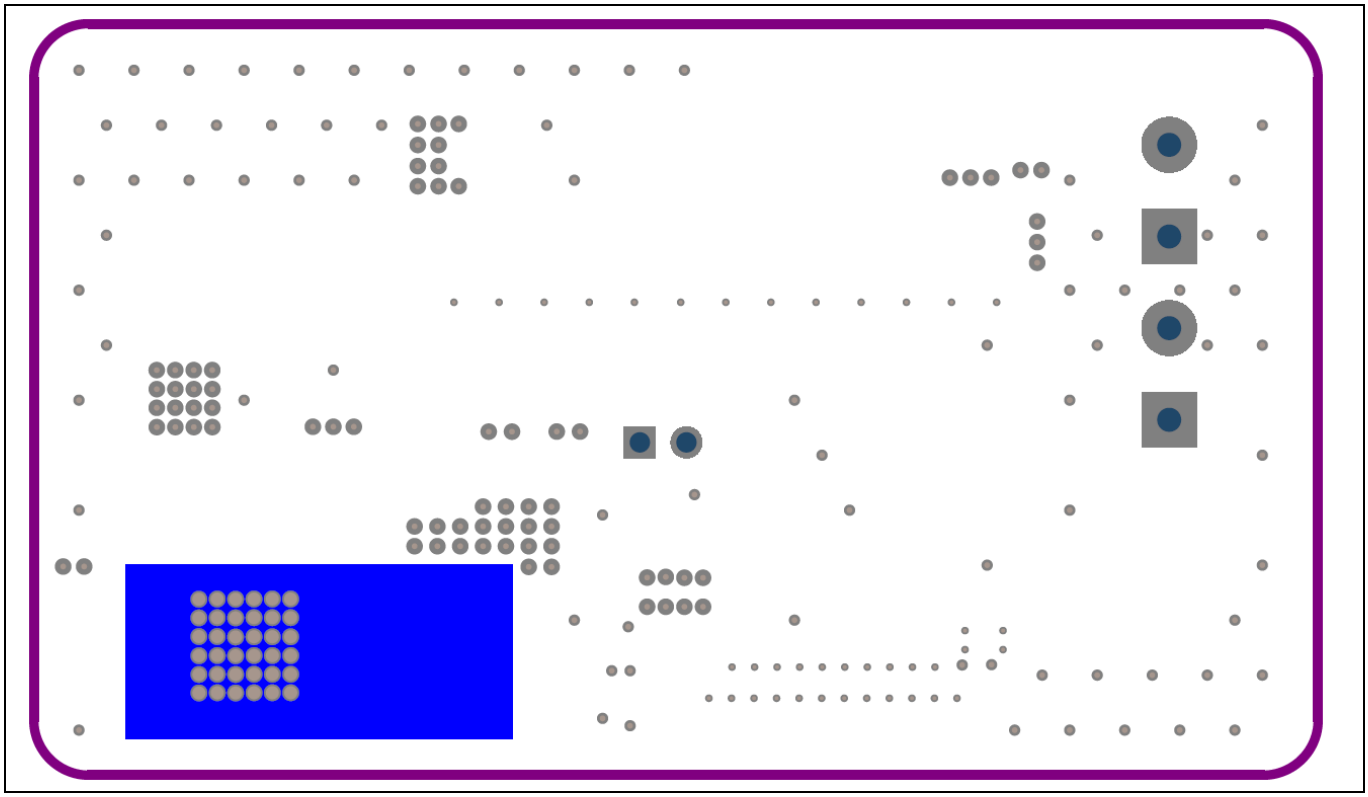

Figure 7 Bottom overlay (top view) – blue area is bare copper for heatsink

In ***Figure 7*** a blue area under the power MOSFET is clearly visible. In this area, solder mask paint has been removed and bare copper is exposed. The aim is to lower the thermal resistance between MOSFET and the heatsink that will be applied on this area as much as possible. Please refer to Chapter 3 of application note **Z8F80033952 - LITIX™ PCB design guideline** ***[1]*** to get guidelines on how to size the heat conduction path through PCB. Furthermore, in ***Chapter 3.10*** of this document all calculations needed to define this area have been reported.

2.4 3D view

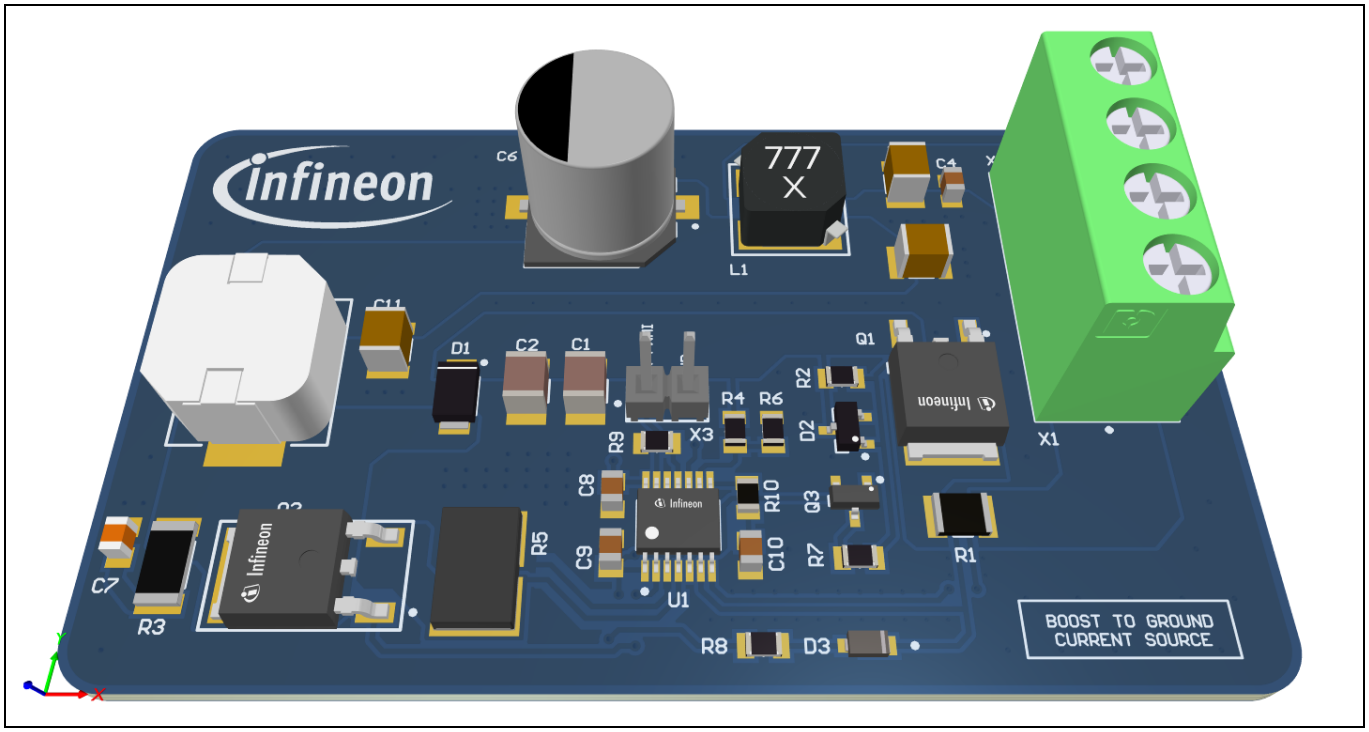

Figure 8 Top view

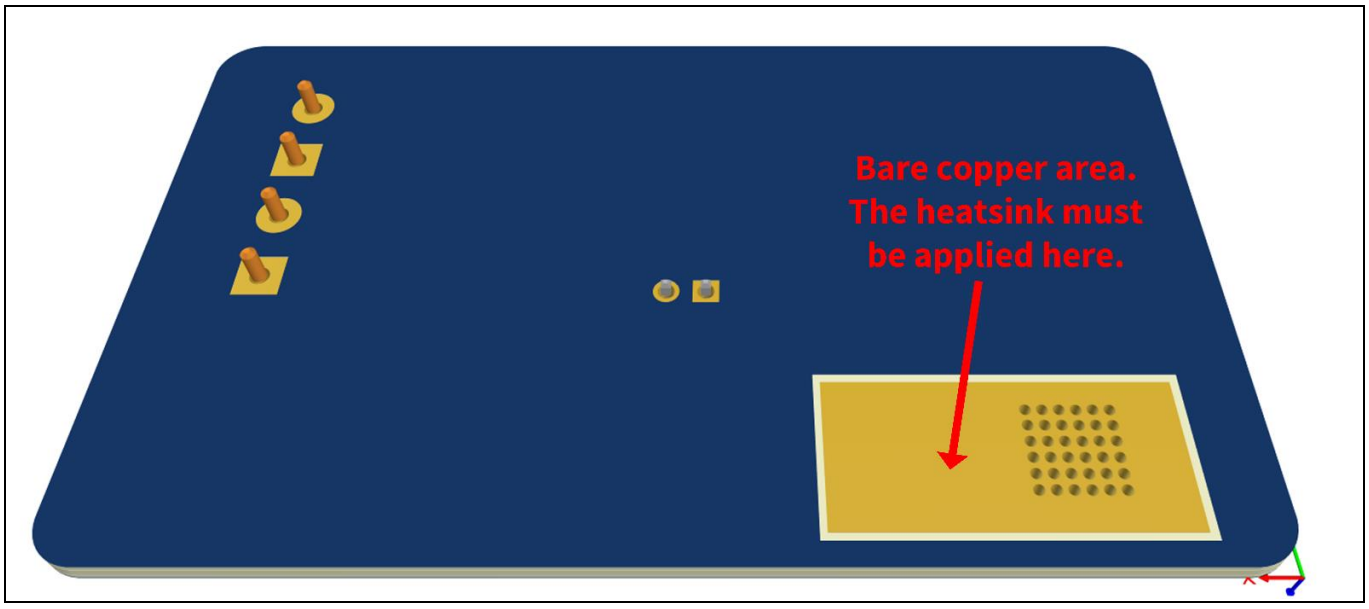

Figure 9 Bottom view

3 PCB Analysis

3.1 Layer stack

Ground plane layer shall be as close as possible to the power stage layer. In this example it is placed on the first overlay, just below the top layer where the power stage components are mounted.

If the power stage dissipates more than 3 W, thickness of external layers should be 0.070 mm at least. In this example the total power loss is:

$$P_{LOSS} = \frac{P_{OUT} \cdot (1-\eta)}{\eta} = \frac{15 \cdot (1-0.85)}{0.85} = 2.6\ W$$

Since the total power loss is less than 3 W, external copper layer thickness can be of 0.035 mm. Thus, the complete layer stack of the board is:

Table 2 Layer stack

Layer name	Thickness [mm]	Function
Top overlay	0.035	Power components
Prepreg	0.320	Insulation
Internal overlay 1	0.035	Ground plane
Core	0.730	Insulation
Internal overlay 2	0.035	Small signals
Prepreg	0.320	Insulation
Bottom overlay	0.035	Small signals

3.2 Trace widths

Refer to Chapter 1.2 of application note **Z8F80033952 - LITIX™ PCB design guideline** *[1]* to obtain a guideline on how to size trace widths. Trace widths should be large enough to limit the power losses on traces below 1% of the maximum output power. Even though power traces that carry the input and output current are not simply rectangular traces with a fixed width, a rough estimation of the power losses on traces can be done. Irregular traces can be converted into rectangular traces. The path drawn by the current can be considered as the length. The minimum width present on the irregular trace can be considered as the width. See ***Figure 10***.

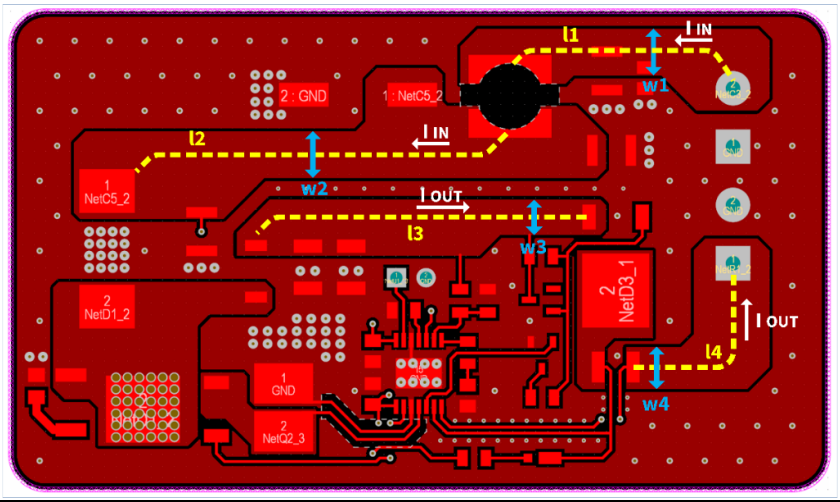

Figure 10 Rectangle trace approximation

- l1 = 21 mm, w1 = 4 mm
- l2 = 34 mm, w2 = 4 mm
- l3 = 30 mm, w3 = 3 mm
- l4 = 17 mm, w4 = 4 mm

The power loss on traces can be estimated with the following relation:

$$P_{LOSS\_TRACES} = \sum R_{TRACE} \cdot I_{RMS}^2 = \frac{\rho}{t_{cu}} \cdot [1 + \alpha \cdot (T_A + \Delta T - 20)] \cdot \sum \left(\frac{l}{w}\right) \cdot I_{RMS}^2 \quad [mW]$$

Where ρ = 0.0168 mΩ·mm, α = 0.004 K^{-1}, T_A is the ambient temperature fixed at 105°C (Class 2, AEC-Q100), Δ*T* is the trace temperature rise with respect to the ambient fixed at 10°C, *l* is the trace length in mm, *W* is the trace width in mm, t_{Cu} is the copper thickness in mm and I_{RMS} is the maximum RMS current in Ampere carried by the trace.

Substituting all values in the formula we obtain:

$$P_{LOSS\_TRACES} = \frac{\rho}{t_{Cu}} \cdot [1 + \alpha \cdot (T_A + \Delta T - 20)] \cdot \left[\left(\frac{l1}{w1} \cdot {I_{IN}}^2\right) + \left(\frac{l2}{w2} \cdot {I_{IN}}^2\right) + \left(\frac{l3}{w3} \cdot {I_{OUT}}^2\right) + \left(\frac{l4}{w4} \cdot {I_{OUT}}^2\right)\right]$$
$$= \frac{0.0168}{0.035} \cdot [1 + 0.004 \cdot (105 + 10 - 20)] \cdot \left[\left(\frac{21}{4} \cdot 2.5^2\right) + \left(\frac{34}{4} \cdot 2.5^2\right) + \left(\frac{30}{3} \cdot 1^2\right) + \left(\frac{17}{4} \cdot 1^2\right)\right]$$

The result of the equation is P_{LOSS_TRACES} = 66 mW, that is less than 1% of output power, fulfilling the initial requirement.

3.3 Trace routing

High frequency currents (as the power MOSFET current) should be free to return to the battery by traveling on the ground plane as close as possible to the opposite conductor. To check this, it is necessary to identify the high frequency currents on the schematic. In addition, the paths of these currents must be identified on the layout, and verified that the return current (see the red line in ***Figure 11***) is free to travel on the ground plane as close as possible to the forward conductor (see the green line in ***Figure 11***) on the top layer.

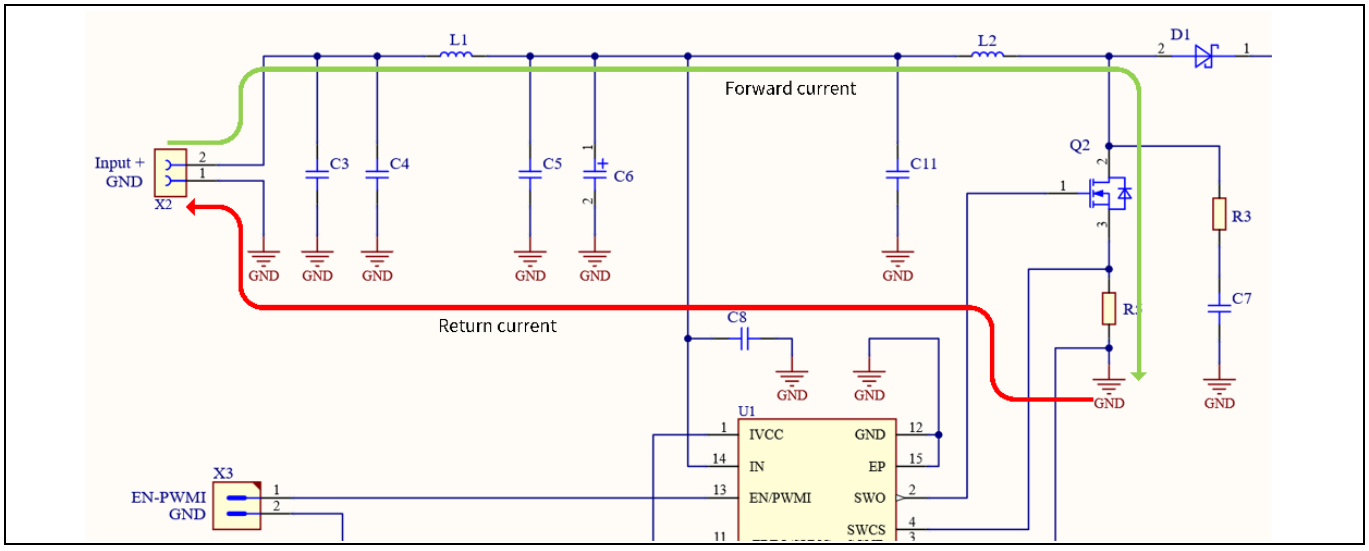

Figure 11 High frequency current

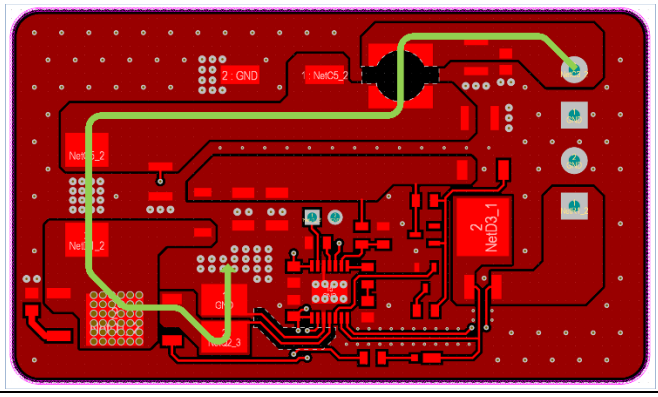

Figure 12 Forward current path on top layer

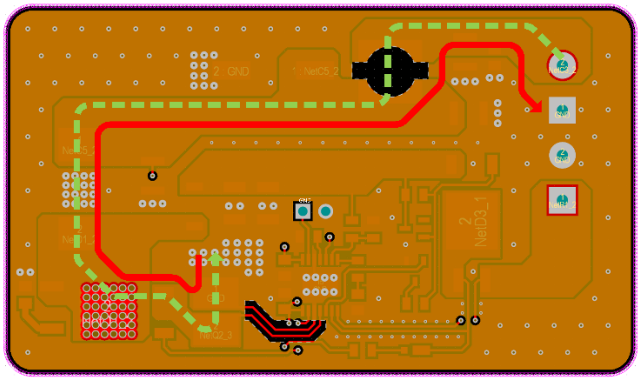

Figure 13 Return current path on ground plane (the forward current path is dashed)

Figure 13 shows clearly that the return current can travel through ground plane roughly close to the forward path, fulfilling the initial requirement.

3.4 Power stage

Commutation loop and switching node must be as small as possible.They are shown in the schematic detail of *Figure 14*.

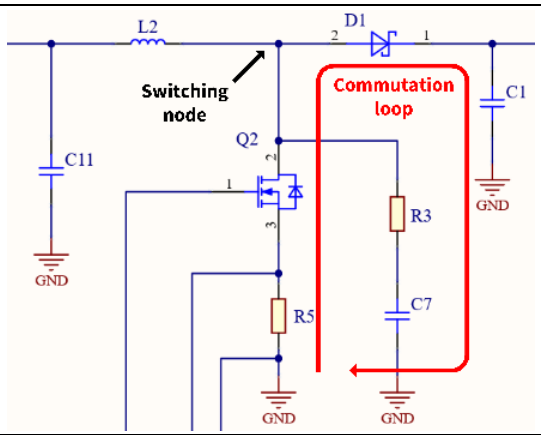

Figure 14 Commutation loop and switching node on schematic

The commutation loop and the switching node highlighted on the PCB layout can be seen in ***Figure 15*** and ***Figure 16***. Their dimensions ensure a good compromise between EME reduction and good thermal dissipation.

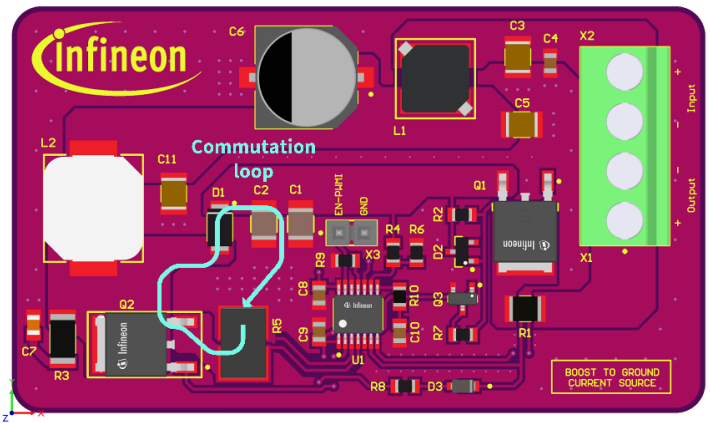

Figure 15 Commutation loop

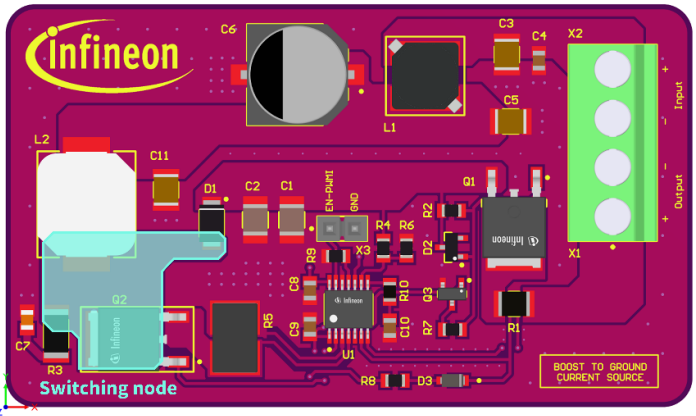

Figure 16 Switching node

3.5 Capacitors

Capacitor connections shall be made with the shortest traces possible, avoiding thermal reliefs. Close to solder lands, each capacitor is connected to ground with multiple vias, in order to keep the parasitic inductance and resistance of the connection lower than 5% of their internal ESL and ESR. Some examples of capacitor connections are depicted in ***Figure 17*** where the red arrows indicate the connection to ground.

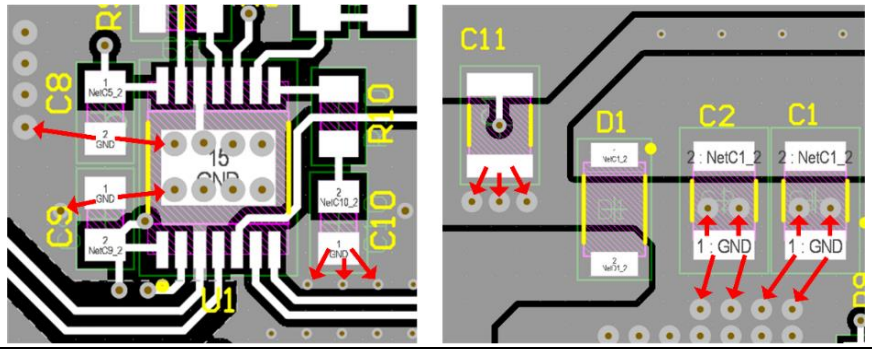

Figure 17 Capacitor connections

In this schematic example, in ***Figure 18,*** critical capacitors, C8, C9 and C10 for good performance of the Infineon controller TLD5098, named U1, are depicted. In ***Figure 18*** it is clearly visible that all these capacitors have been placed as close to the controller case as possible. Refer to schematic in ***Figure 1***.

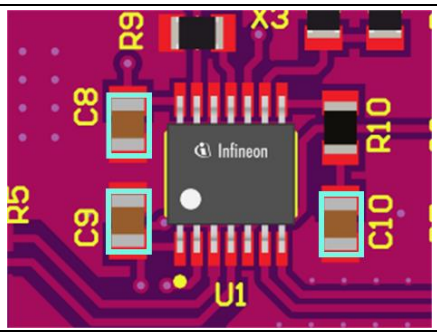

Figure 18 Position of critical capacitors

Input filtering capacitors C3 and C4 shall be placed perpendicularly with respect to the output capacitor C5, as shown in ***Figure 19***.

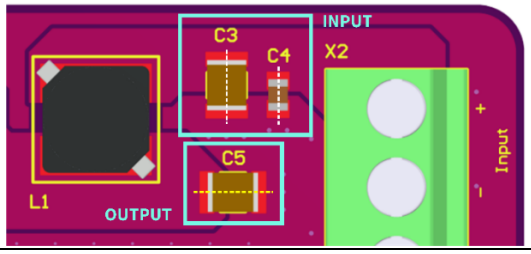

Figure 19 Position of input capacitors

3.6 Inductors

Distance between two different purpose inductors shall be at least twice the diameter of the largest inductor. Inductor L1 is used here as series element of the input PI low pass filter. Inductor L2 is used as magnetic energy storage on the power stage. Diameter of inductor L1 is approximatively 10 mm, whereas diameter of L2 is 15 mm. Thus, the distance between the inductors should be 2 · 15 mm = 30 mm at least.

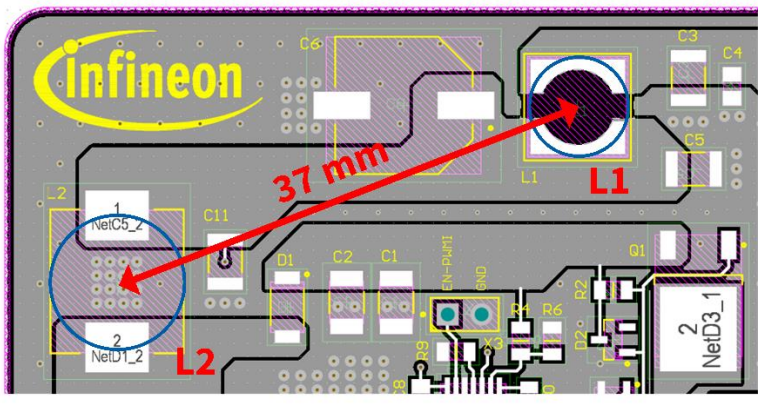

Figure 20 Distance between inductors

3.7 Shunt resistor

Shunt resistors should be connected using differential pair traces, kept as close as possible to each other and far from power inductor. Since the output current must be 1 A and devices TLD5097EP, TLD5098EP and TLD5099EP feature a feedback reference voltage of 0.3 V, output current shunt resistor R1 value is 0.3 Ω (please refers to the datasheets of the devices for more information). Thus, referring to Figure 15, chapter 1.7 of application note **Z8F80033952 -LITIX™ PCB design guideline** *[1]*, the second solution has been chosen, since the resistor value is higher than 1 mΩ.

The differential signal traces FBH and FBL across the resistor terminals should be kept as close as possible to each other and surrounded by copper areas, connected to the underlying ground plane with vias evenly distributed. This item has been highlighted in ***Figure 21***.

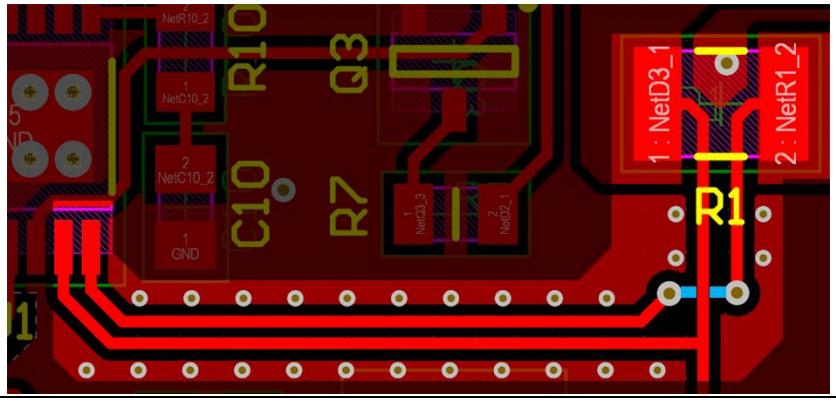

Figure 21 Differential pair FBH-FBL traces and shunt resistor connection

3.8 Power connectors

The input and output power connectors should be placed on the same side and the GND terminals as close as possible to each other. In this example it is clearly visible that input and output connectors X1 and X2 have been placed next to each other with the GND terminals in the central position.

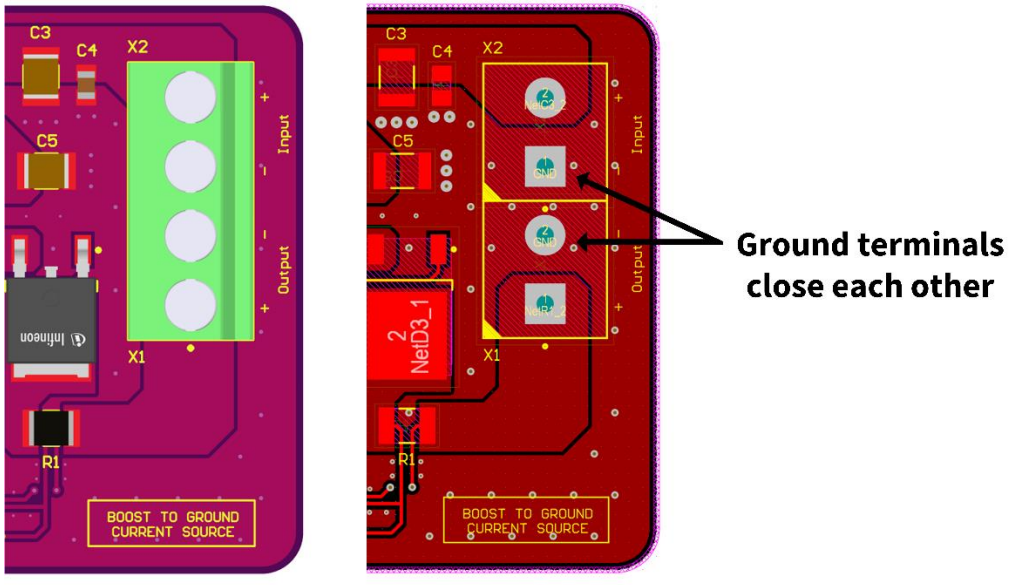

Figure 22 Input and output connectors

3.9 Void areas

Once the PCB has been laid out, it must have copper poured into it and connected to the ground. “Vias stitching” technique should be applied to connect these areas to the ground plane. As clearly visible from ***Figure 4***, ***Figure 5***, ***Figure 6***, ***Figure 7***, all void areas not occupied by traces or components have been filled with solid copper. Furthermore, these copper areas have been connected to ground by a vias stitching network with a distance between vias of 3 mm (see detail in ***Figure 23***). With this characteristic, vias stitching network is able to dampen all electric fields with a frequency up to 3 GHz.

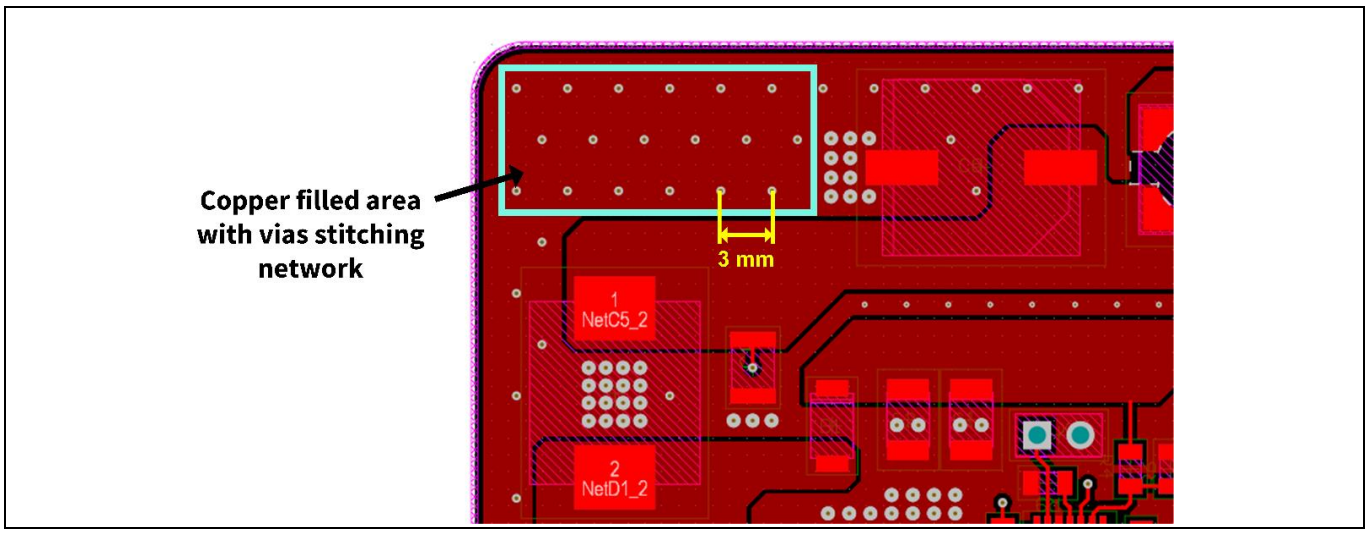

Figure 23 Vias stitching

3.10 Heatsink

If a four-layer is used (and one of the internal layers is designated as ground plane), the best solution to dissipate heat from power MOSFET is to duplicate an area on the bottom layer, equal or larger to the thermal pad of the MOSFET. This bottom copper area should be free of solder mask. Then, with multiple thermal vias, both areas are linked together in order to move the heat produced to the bottom layer. Hence, using a thermal conductive double-sided tape, an appropriate heatsink is applied.

Referring to Chapter 3 of application note **Z8F80033952 - LITIX™ PCB design guideline** ***[1]***, the thermal resistance of the heatsink R_{thHS} can be roughly obtained with the following relation:

$$R_{thHS} \leq \left(\frac{T_{J\_MAX} - T_A}{P_{LOSS\_MOS}}\right) - R_{thJC} - \left(\frac{R_{thVIA}}{N_{VIAS}}\right) - R_{thTAPE} \quad [K/W]$$

where T_{J_MAX} is the maximum junction temperature of the MOSFET allowed in °C, T_A is the ambient temperature in °C, P_{LOSS_MOS} is the maximum power in watt lost in the MOSFET, R_{thJC} is the thermal resistance between junction and the MOSFET case in K/W, R_{thVIA} is the thermal resistance of one via in K/W, N_{VIAS} is the number of thermal vias in parallel under the MOSFET case (vias should have all the same size) and R_{thTAPE} is the thermal resistance of double-sided tape applied between PCB and heatsink.

The MOSFET case is a D-PAK, of which the thermal pad dimensions are roughly 6 x 6 mm. In this area up to 36 thermal vias with an internal diameter of 0.7 mm can be placed. Fixing the via plating thickness to 0.018 mm and the PCB height to 1.6 mm, the thermal resistance of a single via is R_{thVIA} = 101 K/W.

To stick the heatsink on the bottom bare copper area, thermal conductive double-sided tape must be used. A good choice can be 3M type 8805. This tape has a thickness t_{TAPE} = 0.125 mm and a thermal conductivity λ_{TAPE} = 0.6 W/m·K. If all thermal vias cover a surface area equal to the thermal pad of the power MOSFET in a D-PAK case, the conduction area of the tape is at least 6 x 6 mm = 36 mm².

Thus, the thermal resistance of double-sided tape R_{thTAPE} applied between PCB and heatsink, is:

$$R_{thTAPE} = \frac{1}{\lambda_{TAPE}} \cdot \frac{t_{TAPE}}{A_{TP}} \cdot 10^3 = \frac{1}{0.6} \cdot \frac{0.125}{36} \cdot 10^3 = 5.8\ K/W$$

Using the data given from the circuit designer, thermal resistance of the heatsink R_{thHS} is the following:

$$R_{thHS} \leq \left(\frac{160 - 105}{0.8}\right) - 5.1 - \left(\frac{101}{36}\right) - 5.8 = 55\ K/W$$

A good choice can be the heatsink Fischer model ICKSMDF17 depicted in ***Figure 24***, with a thermal resistance of 42 K/W and a contact base of 17 x 8 mm. For this scope, a bare copper area of 20 x 10 mm where sticking the heatsink has been realized under power MOSFET, as shown by blue squared area in ***Figure 9***.

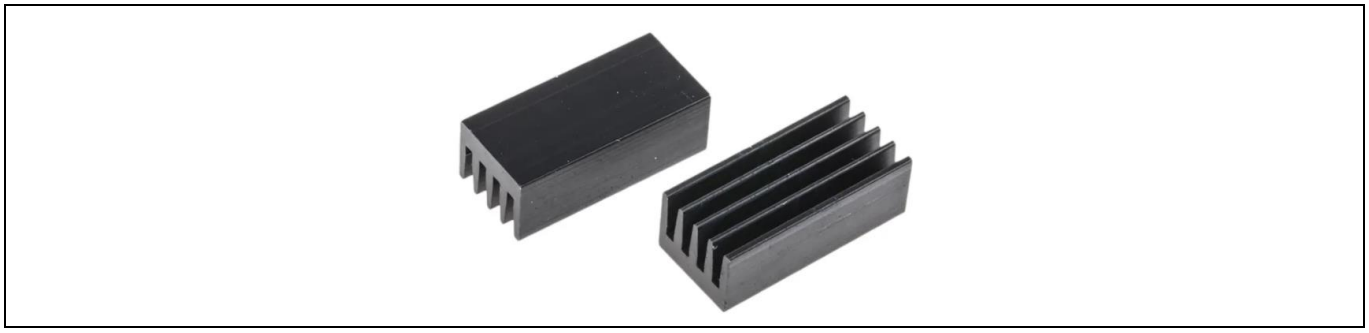

Figure 24 Heatsink Fischer model ICKSMDF17

4 List of references

[1] Infineon Z8F80033952 LITIX™ PCB design guidelines AN Rev.1.00

[2] Infineon TLD5097EP DS Rev.1.00

[3] Infineon TLD5098EP DS Rev.1.40

[4] Infineon TLD5099EP DS Rev.1.00

Revision history

Document version	Date of release	Description of changes
Rev.1.00	2021-02-08	Initial release

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