LITIX™ PCB design guidelines

LITIX™ Power, LITIX™ Power Flex

About this document

Scope and purpose

This application note is intended to provide guidance on how to design an optimized PCB with Infineon LITIX™ Power or LITIX™ Power Flex DC-DC controller families.

This application note shall be used in conjunction with the latest Infineon LITIX™ Power and LITIX™ Power Flex datasheets for a detailed component description. It is meant as an add-on to the datasheets and not as a document explaining the devices in detail. It is also not a replacement for the datasheets.

Note: *The following information is given as a hint for the implementation of the LITIX™ Power and LITIX™ Power Flex devices only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.*

Intended audience

Hardware engineers in the design of PCB layout with a LITIX™ Power or LITIX™ Power Flex controller.

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1 Main recommendations

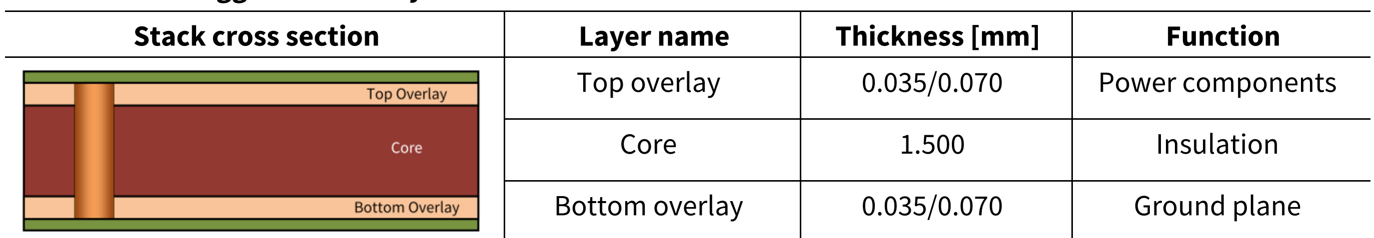
A DC-DC converter is characterized by fast current and voltage transients. Due to high speed change of these parameters, a DC-DC converter could be affected by troublesome issues such as high electromagnetic emissions (EME) and high voltage transients. Such issues could be reduced or enhanced depending on the component connections and positioning. Particular attention should be paid to the power stages that are often affected by high EME that could compromise the integrity of low voltage signals.

Therefore, a well-designed DC-DC converter is not only a result of a good schematic design but also of an impeccable PCB layout. Thus, when designing the PCB of a DC-DC converter, designer must be aware that the overall performance of the converter depends significantly on the layout arrangement. Ignoring these rules may cause low efficiency, instability, faults and high EME.

1.1 Layer stack

A generic DC-DC converter could be routed in a two-layer or four-layer PCB. One of these layers shall be set as ground plane. When a four-layer stack is used and the power stage components are placed on the top overlay, ground plane shall be the internal overlay 1. Good layer stack configuration for a DC-DC converter with a power rating of a few tenths of watts is suggested in ***Table 1***.

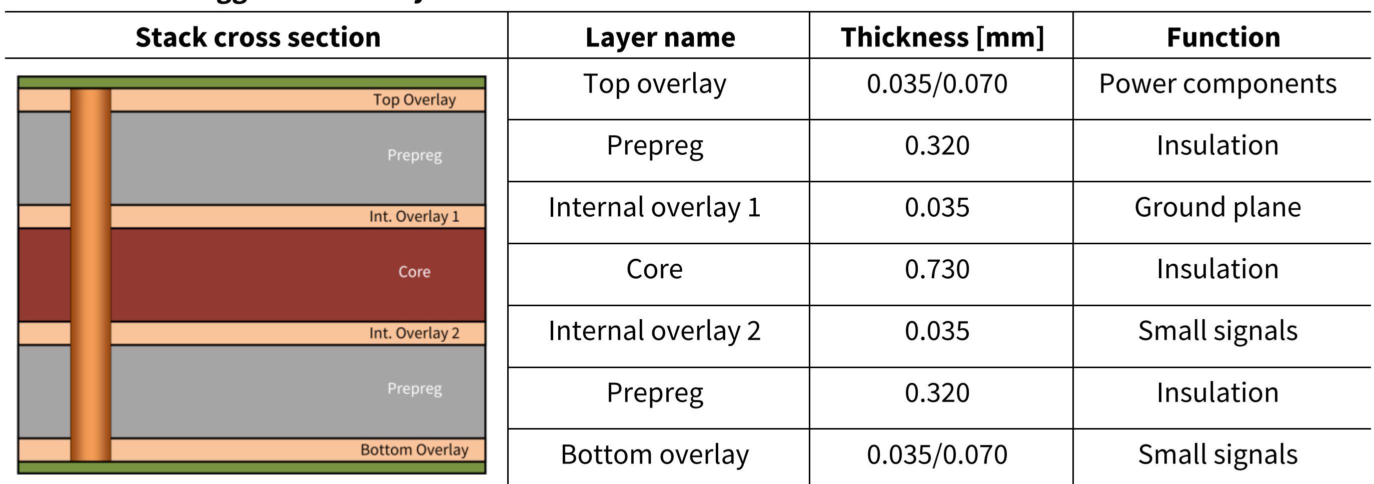
Table 1 Suggested two-layer stack



Stack cross section	Layer name	Thickness [mm]	Function
	Top overlay	0.035/0.070	Power components
	Core	1.500	Insulation
	Bottom overlay	0.035/0.070	Ground plane

If together with good electromagnetic compatibility (EMC) performance, a suitable heat dissipation is needed, a four-layer stack would be preferred as is depicted in ***Table 2***.

Table 2 Suggested four-layer stack



Stack cross section	Layer name	Thickness [mm]	Function
	Top overlay	0.035/0.070	Power components
	Prepreg	0.320	Insulation
	Internal overlay 1	0.035	Ground plane
	Core	0.730	Insulation
	Internal overlay 2	0.035	Small signals
	Prepreg	0.320	Insulation
	Bottom overlay	0.035/0.070	Small signals

At least 0.035 mm of external copper layers are recommended for all DC-DC converter designs. If the power stage dissipates more than 3 W, thickness of external layers should be increased to 0.070 mm, in order to lower the thermal resistance of the surfaces. In both cases, a well sized heatsink applied to the heat sources is recommended. Refer to ***Chapter 3, Thermal dissipation*** for further information about the heatsink application.

1.2 Traces width

Unless otherwise specified on the reference standards, keep the power traces as short as possible and provide a minimum width as suggested by standard IPC-2221, according to the following relation:

$$w = \frac{\left[\frac{I}{k \cdot \Delta T^{b}}\right]^{\frac{1}{c}}}{t_{Cu}} \cdot 0.645 \cdot 10^{-3} \quad [mm]$$

Where k = 0.024 for internal traces and k = 0.048 for external, b = 0.44, c = 0.725, *I* is the maximum current in Ampere carried by the trace, ΔT is the trace temperature rise with respect to the ambient and t_{Cu} is the copper thickness in mm.

ΔT should be less than the difference between the maximum ambient temperature and the maximum withstand temperature of the PCB insulating material. In automotive environment, especially for LED driver circuits, typical ambient temperature considered is 105°C (Class 2, AEC-Q100). All basic PCB materials can withstand to a working temperature of at least 130°C. Thus, ΔT should be set to 130°C-105°C = 25°C maximum. Typical safety level assumed for ΔT is 10°C. ***Table 3*** shows a quick evaluation of the minimum trace width, calculated for ΔT = 10°C and t_{Cu} = 0.035 mm:

Table 3 Trace width versus current

Maximum current [A]	Minimum trace width [mm]	
	Internal	External
0.3	0.2	0.1
0.6	0.4	0.2
1.0	0.8	0.3
2.0	2.0	0.8
3.0	3.6	1.4
4.0	5.3	2.0

Once the width has been calculated, it is necessary to estimate the power loss of the trace. This parameter depends on the length of the trace and on the ambient temperature, according to the following relation:

$$P_{LOSS_TRACE} = R_{TRACE} \cdot I_{RMS}^{2} = \rho \cdot [1 + \alpha \cdot (T_A + \Delta T - 20)] \cdot \left(\frac{l}{w \cdot t_{Cu}}\right) \cdot I_{RMS}^{2} \quad [mW]$$

Where ρ = 0.0168 mΩ·mm, α = 0.004 K^{-1}, T_A is the ambient temperature in °C, *l* is the trace length in mm, *w* is the trace width in mm, t_{Cu} is the copper thickness in mm and I_{RMS} is the maximum RMS current in Ampere carried by the trace.

For a high efficiency converter, the total power losses on traces should be kept lower than 1% of the maximum output power. Thus, if the power losses are higher, choose a larger trace width.

Note: These formulas are valid if the current frequency is lower than 1 MHz. Higher frequencies might lower the equivalent conduction section of the trace due to skin effect.

1.3 Traces routing

Parasitic inductance of a trace can be enhanced or decreased depending on its path. If not contained, parasitic inductance could create many disadvantages, especially at high frequencies:

- Increase EME issues due to their emitted electromagnetic field
- Reduce the filtering efficiency of capacitors
- Generate high voltage transients during commutations

Every conductor as a trace or a copper plane, has its own parasitic inductance. To reduce parasitic inductance to a minimum, for every conductor carrying high-frequency current, a path along it where the current can return to the source must be guaranteed. This path should be as close as possible to the conductor, in order to reduce the loop area drawn by conductor and the current return path.

Keep in mind that:

- **Low frequency currents < 1 kHz** tend to travel on the **lowest resistive path**—they will find the shortest path to exit and to return to the source. See blue line in ***Figure 1***.
- **High frequency currents > 10 kHz** tend to travel on the **lowest inductive path**—they will try to return to the source by travelling as close as possible to the opposite conductor. See red line in ***Figure 1***.

In ***Figure 1***, high and low frequency currents are free to move because of a solid ground plane without any interruption. Therefore, low frequency currents will return to the source through the shortest (and also the less resistive) path, as shown by the blue line. High frequency currents will return through the path with the lowest inductance, by traveling on the ground plane as close as possible to the opposite conductor, as shown by the red line.

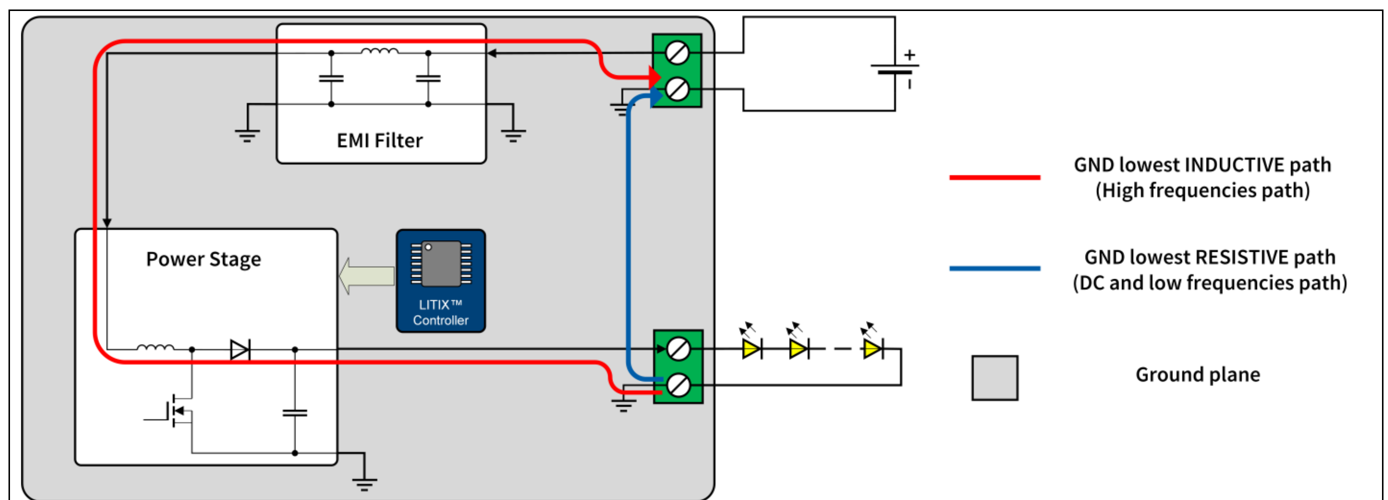


Figure 1 Lowest inductive and resistive path

The high frequency path should be as free as possible of obstacles, slots on board and plane interruptions.

If the return current finds an obstacle that keeps it away from the opposite conductor, it will create a different path with a larger loop area and thus increases inductance, as shown in ***Figure 2***. If, for instance, a separated copper area is created under a trace, its return current is forced to stay away from this, creating a loop area which increases parasitic inductance (yellow line in ***Figure 2***).

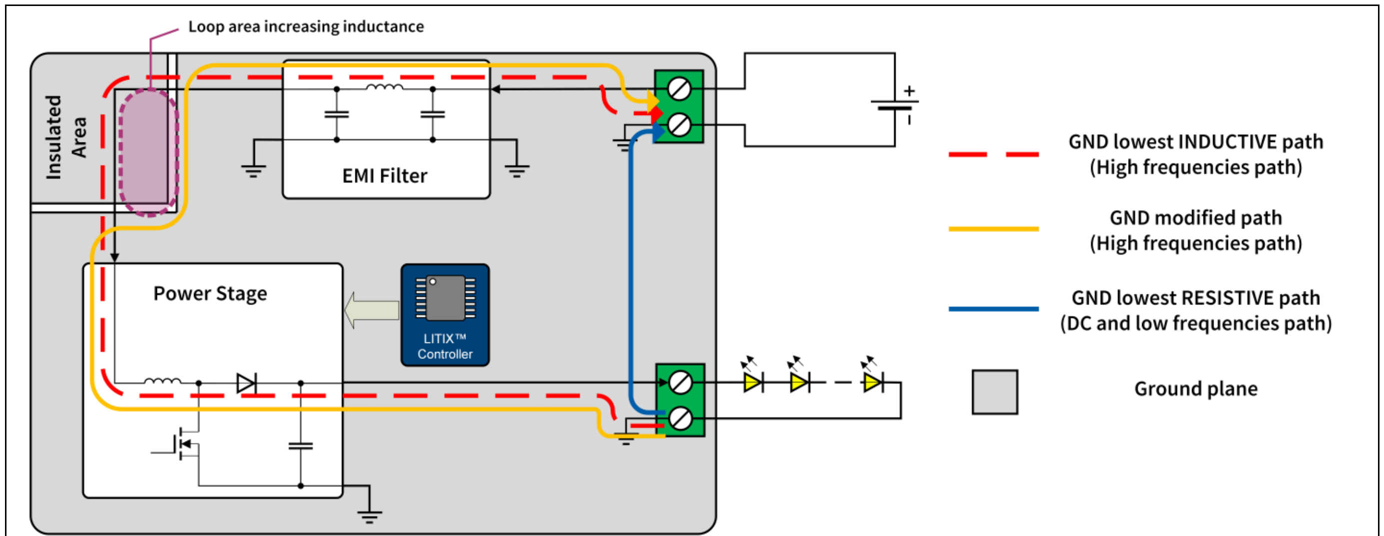


Figure 2 Increased parasitic inductance

Under power stages, where the frequency is high, the most common error is to pass through the ground plane with one or more traces. In this case return currents are forced to find another (and longer) path to return to GND terminal. This will increase parasitic inductance and thus, EME. In ***Figure 3*** an example of a power stage layout is depicted. The high-frequency forward-current towards the MOSFET (in yellow) and its return current (in red) are highlighted. On the left, the traces FBH and FBL cross the ground plane under the power stage area, forcing the return current away from the forward current path: this will inevitably increase the parasitic inductance. A well-designed layout is visible on the right. Using an optimized component layout, breaking traces have been removed from the ground plane under power stage.

Therefore, the lowest EME is obtained when the ground plane under power stage is solid, without any interruption.

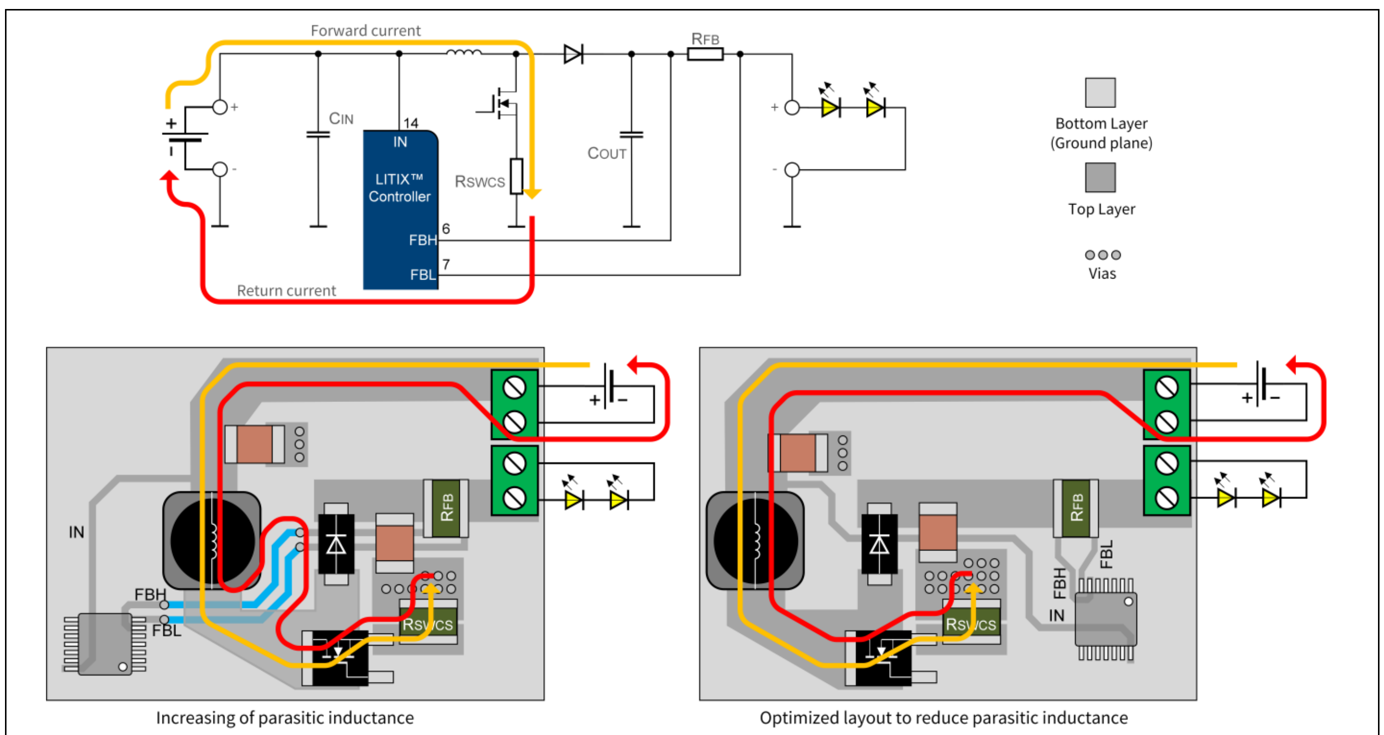


Figure 3 Increased parasitic inductance under power stage

1.4 Power stage

Based on the DC-DC converter topology, two important and critical parts can be found in the power stage:

- **Commutation loop**, also called **hot loop**: every electric loop in the power stage that contains at least one MOSFET, an active element such as a diode or a second MOSFET, and does not involve an inductor. During the commutation period, the current moves from one active part to another. Therefore, this loop is relevant for fast current transients.
- **Switching node**: a node of the power stage connected directly (or via capacitor) to at least one MOSFET and subject to high voltage variations during the commutation period. This node is relevant for fast voltage transients. A well sized R-C snubber network is useful to dampen them.

The larger the commutation loops, the stronger the magnetic field emitted. The bigger the switching nodes, the stronger the electric field emitted. Therefore, in order to reduce EME, tighten the commutation loops and reduce the dimensions of switching nodes as much as possible. Unfortunately, switching nodes often have the arduous task of acting as a heatsink for the power MOSFET and so the dimensions cannot be reduced to a specific minimal dimension (See ***Chapter 3 Thermal dissipation*** for further information).

Figure 4, ***Figure 5***, ***Figure 6*** and ***Figure 7*** depict an example for each configuration of what could be a good placement for the components of the power stage, in order to reduce commutation loops and dimensions of the switching nodes.

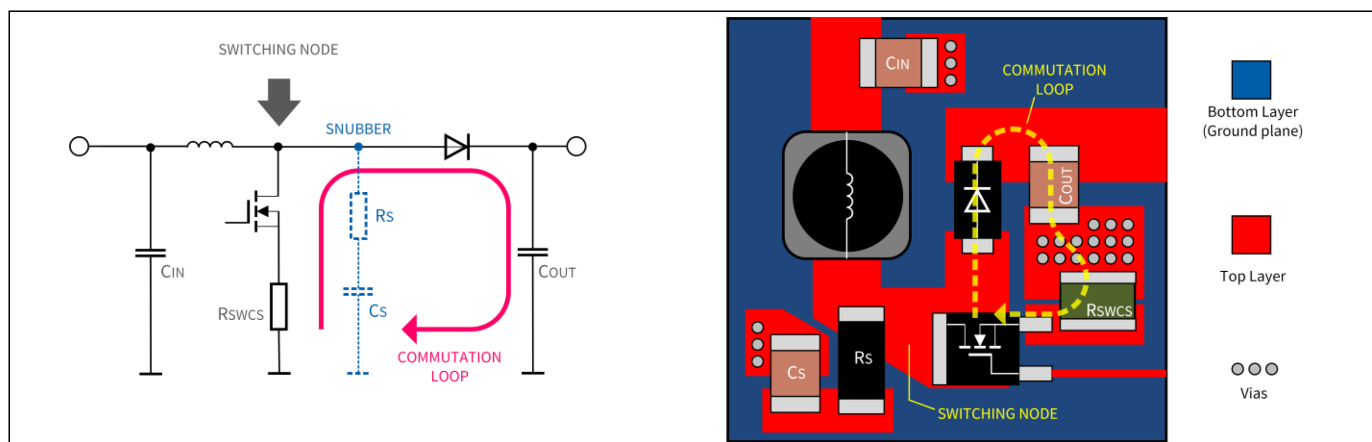


Figure 4 Boost to ground power stage layout

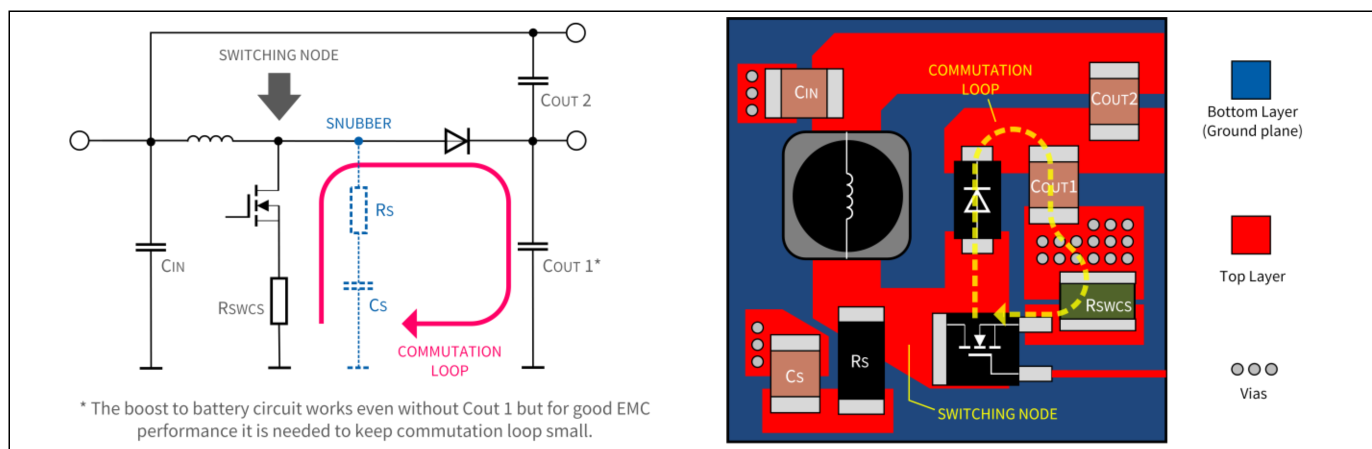


Figure 5 Boost to battery power stage layout

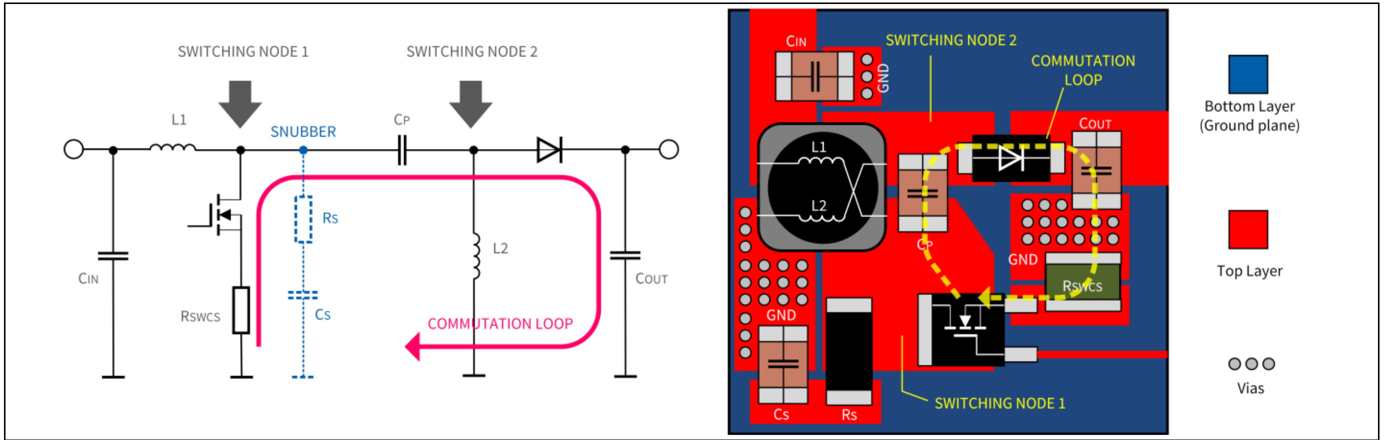


Figure 6 **SEPIC power stage layout**

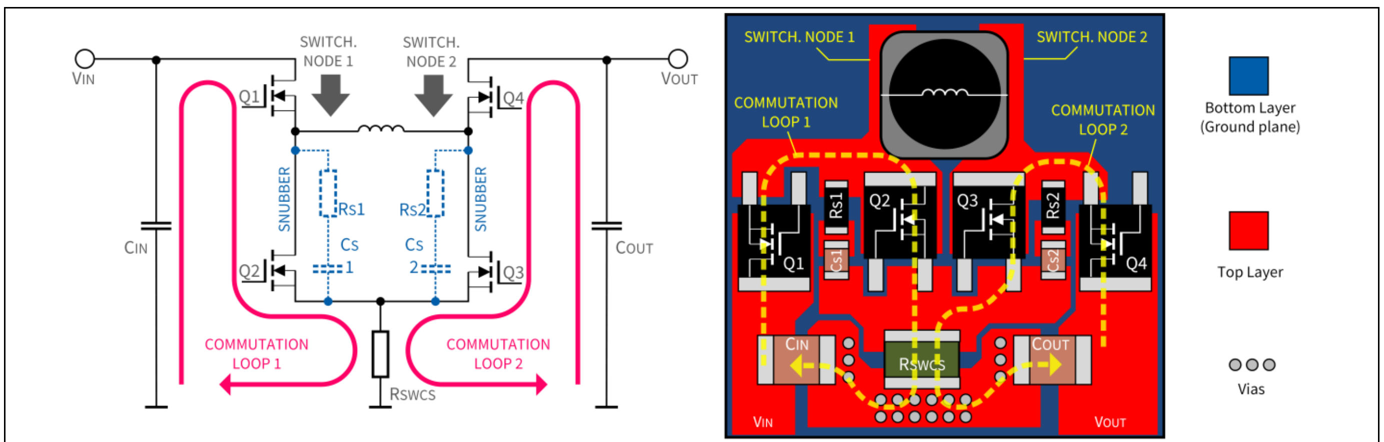


Figure 7 **H-bridge power stage layout**

When starting a new DC-DC layout, the components of the power stage should be placed first. Placing all power stage components on the same side can help in containing EM emissions.

Avoid routing sensitive signal traces underneath the power stage, unless an internal ground plane between the power stage and the signal traces is present as a shield.

1.5 Capacitors

Placement of capacitors, especially for filtering purposes, is essential to achieve the best performances in EM compliance. Accurate position and connection are crucial, especially to filter high frequency disturbances.

All capacitors should have an optimal ground connection with a very low parasitic resistance and inductance.

This aim could be achieved by connecting all capacitors with high width traces to reduce parasitic resistance and to avoid connection with long straight traces reserved for each capacitor to reduce parasitic inductance (especially for small high-frequency multi-layer ceramic capacitors – MLCC, with very low ESR).

Keep in mind that each millimeter of trace will add in series to the capacitor roughly 1 nH of parasitic inductance; thus, connections on capacitors should be made with the shortest traces possible.

Avoid using thermal relief land patterns with capacitors, especially those with very low ESR.

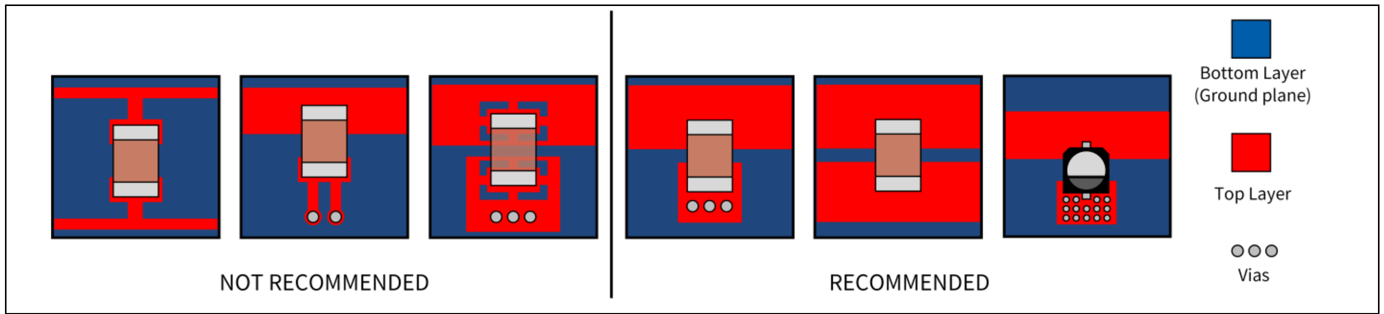


Figure 8 Capacitor connections

The number of vias to be used is essential to ensure a good ground connection: place more than one via in parallel to reduce their overall parasitic parameters. Indeed, parasitic resistance and inductance of N vias in parallel are roughly the parasitic resistance and inductance of one single via divided by N.

Table 4 depicts a quick view of parasitic parameters of one single copper via with a thickness of 1.6 mm and a temperature of 105°C.

Note: *This inductance calculation method merely gives an* estimation of what the parasitic inductance of vias would be, since it does not consider the distance from the return current path. *When the inductance really matters, a more accurate approximation is needed* **[1].**

Table 4 Vias resistance and estimated inductance

Via hole diameter [mm]	Via resistance R_{VIA} @ 105°C [mΩ]		Via estimated inductance L_{VIA} [nH]
	0.018 mm plating	0.025 mm plating	
0.1	5.4	3.7	1.7
0.2	2.9	2.0	1.4
0.3	2.0	1.4	1.3
0.5	1.2	0.9	1.1
0.7	0.9	0.6	1.0
1.0	0.6	0.4	0.9

The results of the ***Table 4*** are obtained using the following approximate formulas valid for copper vias only:

$$R_{VIA} = \frac{\rho \cdot [1 + \alpha \cdot (T_{VIA} - 20)] \cdot t_{PCB}}{\pi \cdot \left[\left(t_{PL} + \frac{D}{2}\right)^2 - \left(\frac{D}{2}\right)^2\right]} \quad [m\Omega]$$

$$L_{VIA} = 0.2 \cdot\ t_{PCB} \cdot \left[\ln\left(\frac{4 \cdot t_{PCB}}{D}\right) + 1\right] \quad [nH]$$

Where ρ = 0.0168 mΩ·mm, α = 0.004 K^{-1}, T_{VIA} is the via temperature in °C, t_{PCB} is the thickness of the PCB in mm, t_{PL} is the thickness plating of the via in mm and D is the internal diameter of via in mm.

To make these parasitic parameters negligible, they should be kept under 5% of the parasitic resistance and inductance of capacitor to be connected.

Example: A ceramic capacitor of 1 µF must be connected to the ground plane. Considering that its parasitic resistance is about 10 mΩ, the total parasitic resistance of vias should be less than 0.5 mΩ (5% of 10 mΩ). This value can be achieved for example placing 3 vias with 0.3 mm of diameter and 0.025 mm plating thickness which show a total resistance of 1.4 mΩ/3 = 0.47 mΩ, fulfilling the initial requirement.

Particular attention should be paid to capacitors that deal with high frequency signals such as the disturbance bypass capacitors. In most cases, the capacitors used here are ceramic, with a capacitance of typically between 100 pF and 10 µF. Critical capacitors that are crucial for a good performance of the LITIX™ controllers are:

- Bypass capacitors on the power supply pins
- Bulk capacitors on the output voltage reference pins (as IVCC, VREF)
- Capacitors in the compensation network
- Low-pass filters capacitors

Some of these capacitors have been highlighted in *Figure 9*, where a simple DC-DC boost LED power-supply controlled by a LITIX™ Power TLD5097EP is used as an example:

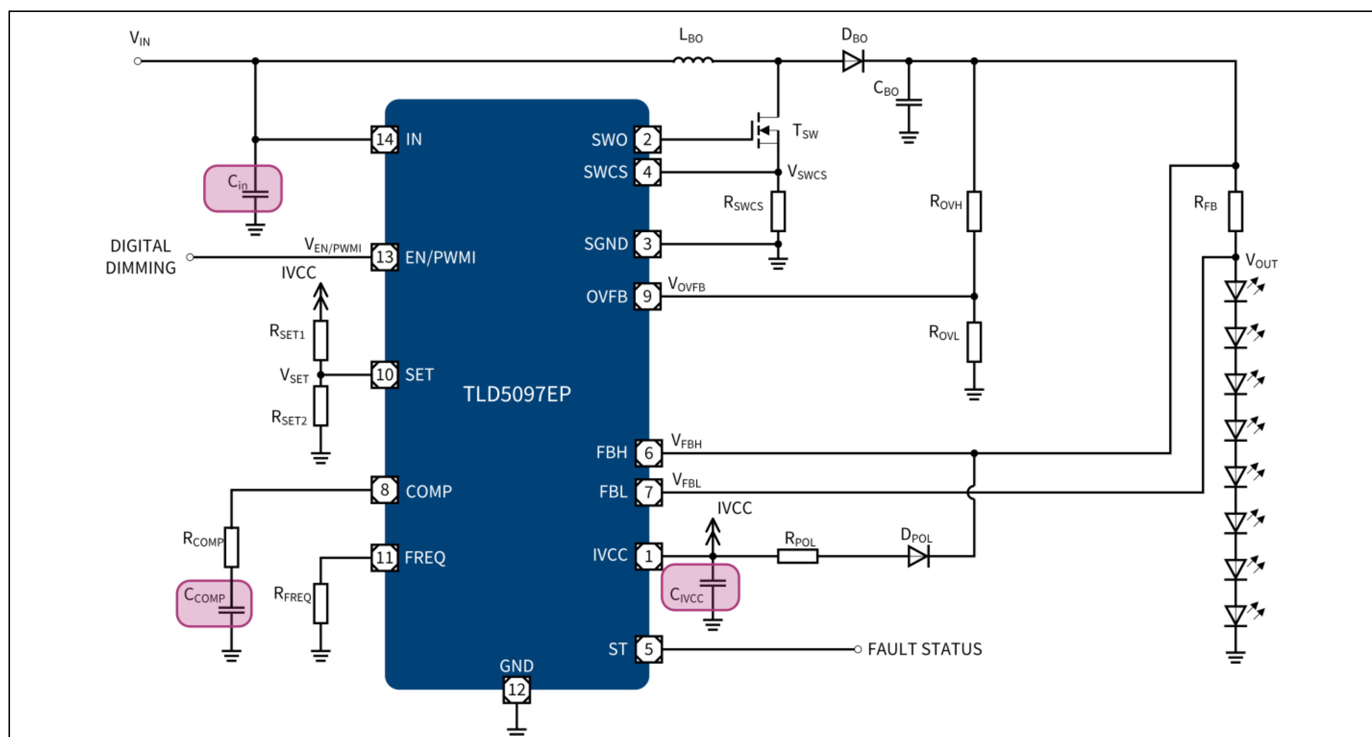


Figure 9 **Example of critical capacitors**

The capacitors must be placed as close as possible to the controller pins, in order to decrease parasitic inductance and avoid unwanted behavior. Suggested positions for these capacitors are shown in *Figure 10*.

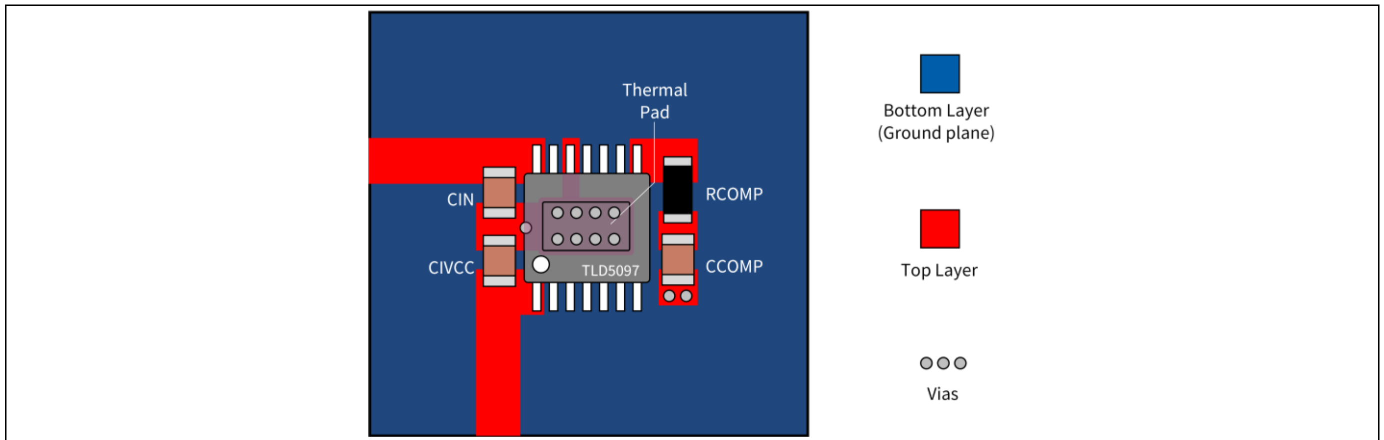


Figure 10 Position of critical capacitors

Capacitors of the EMI input filter could bypass the blocking function for high frequencies if incorrectly positioned, canceling the filter effect. Considering a classic PI EMI input filter composed of one series inductor and two capacitors (one on the input side and one on the output), the worst position for both capacitors is when they are placed close and in parallel to each other. In this case, leaked electric field emitted by the capacitors and the magnetic field generated by capacitive currents flowing through one of these capacitors are well coupled with the other, transferring noise from one side of the inductor to the other side and thus, bypassing it. This phenomenon is accentuated if the capacitors are very close to each other. The best results will be obtained if the capacitors are placed perpendicularly, as shown in ***Figure 11***.

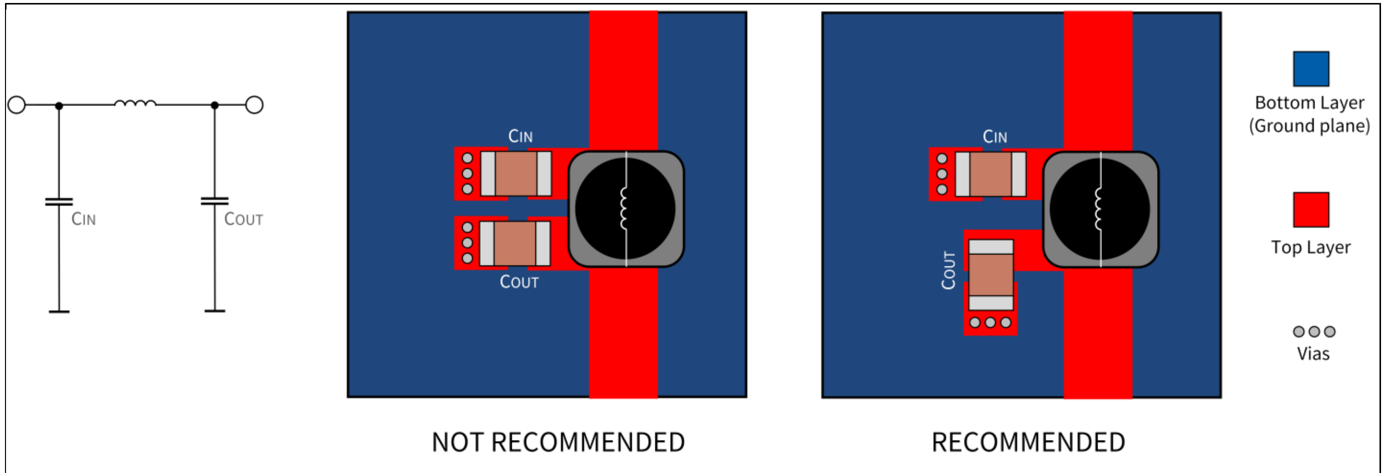


Figure 11 Input filter capacitor placement

1.6 Inductors

Leakages of magnetic flux can be observed among all inductors, especially non-shielded or partially shielded inductors. In this case magnetic flux goes outside the inductor and may couple with another inductor, often used for different purposes. Typical is the case, where the inductor used to store energy on the power stage, produces flux that is coupled with the inductor used on the EMI input filter. In this situation the magnetic noise produced by the power stage is coupled with the input inductor, canceling the filter effect.

To minimize this unwanted phenomenon, it is necessary that inductors used for different purposes shall be maintained far from each other. A rule of thumb, is to ensure a distance between inductors of, at least, twice the diameter of the largest inductor, as shown in ***Figure 12***.

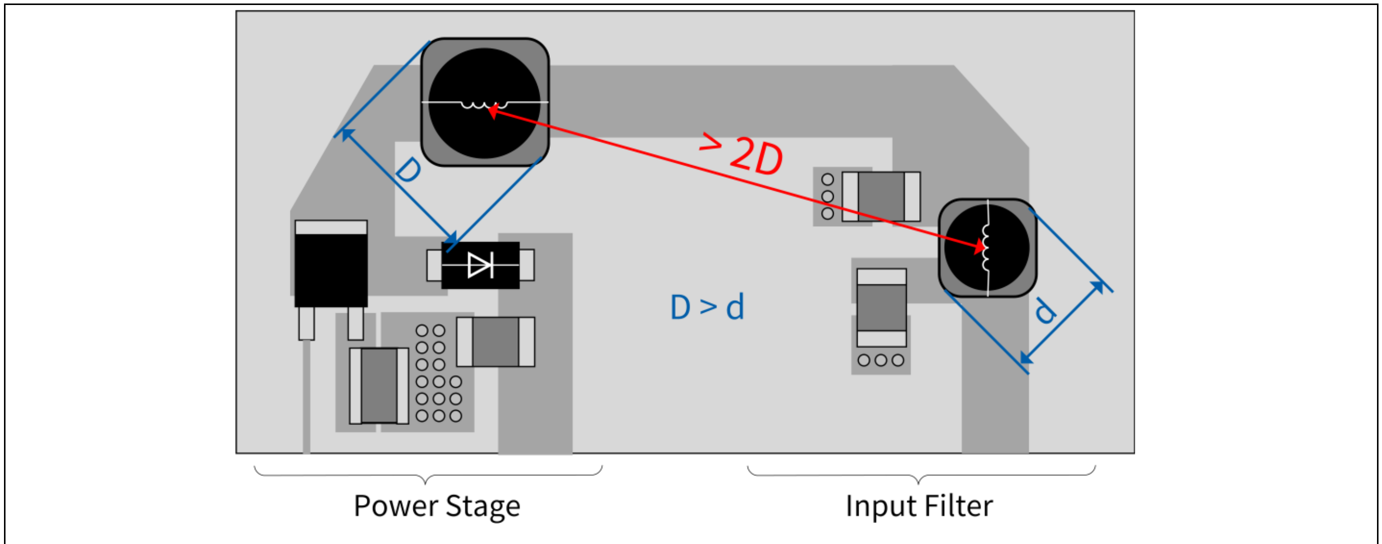


Figure 12 Distance between inductors

Additionally, orientation of the power inductor can help in containing EME. The terminal connected with the inner winding should be oriented toward the switching node, as depicted in ***Figure 14***. In this way, the EME from switching node will be shielded by the outer windings.

Figure 13 Inner and outer winding terminals

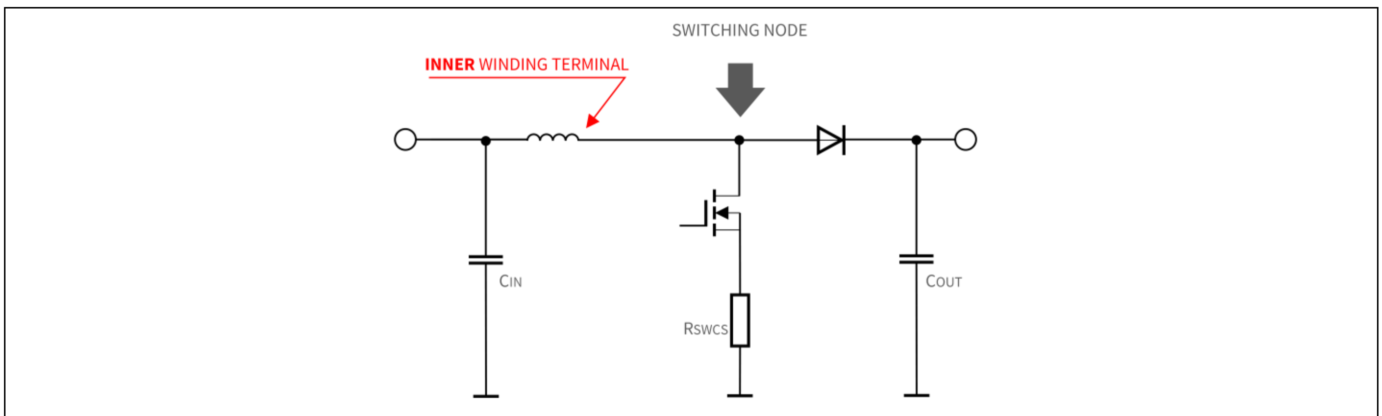


Figure 14 Inner winding terminal connection

1.7 Shunt resistors

A low inductive shunt is no guarantee for a low noise measurement signal. The quality of the signal depends on the layout and where the traces used to connect the shunt to the controller are routed. A general guideline is as follows:

- Use four-wire sense approach with symmetric sense lines
- Avoid inductive coupling into the sense wires by keeping lines far from power inductors

Keep traces as close as possible to each other

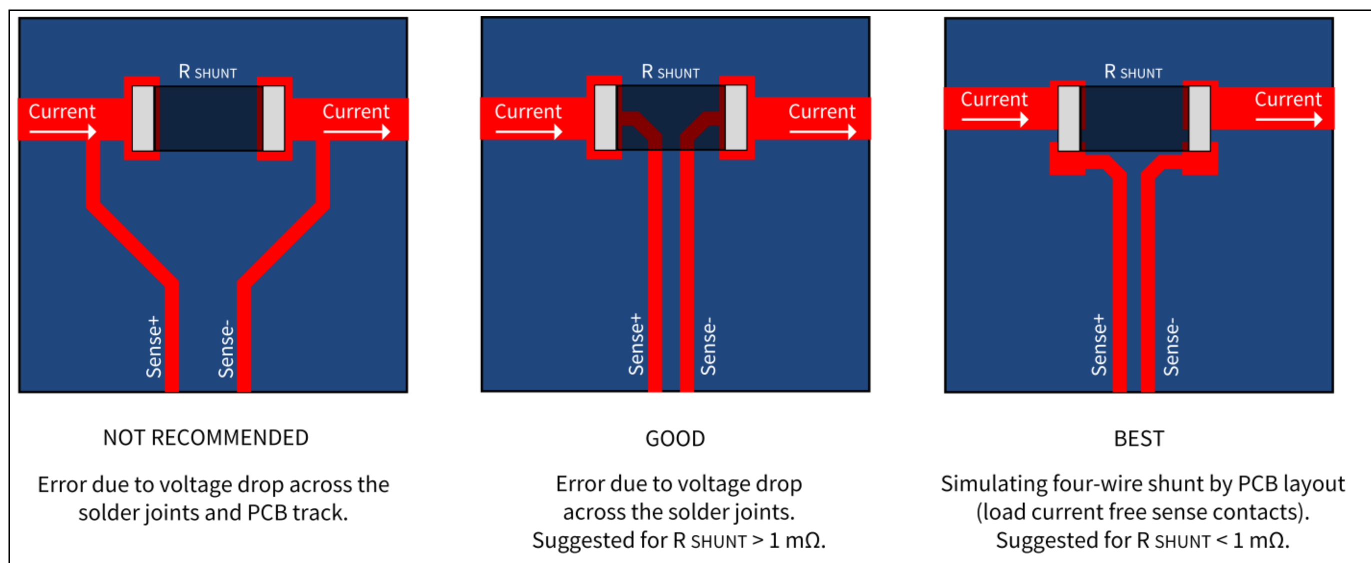


Figure 15 Shunt resistor connections

Depending on what the value of the shunt resistor is, a “good” and “best” solution can be chosen. If the value is lower than 1 mΩ, the “best” solution should be preferred, since the solder resistance of pads (estimated roughly around 10 µΩ) could affect the reading. Since this solution could cause hidden shorts between sense and pad terminals during the soldering process, SMD shunt resistors with four pads have become available on the market. *Figure 16* depicts an example from Bourns CSS4J-4026 series.

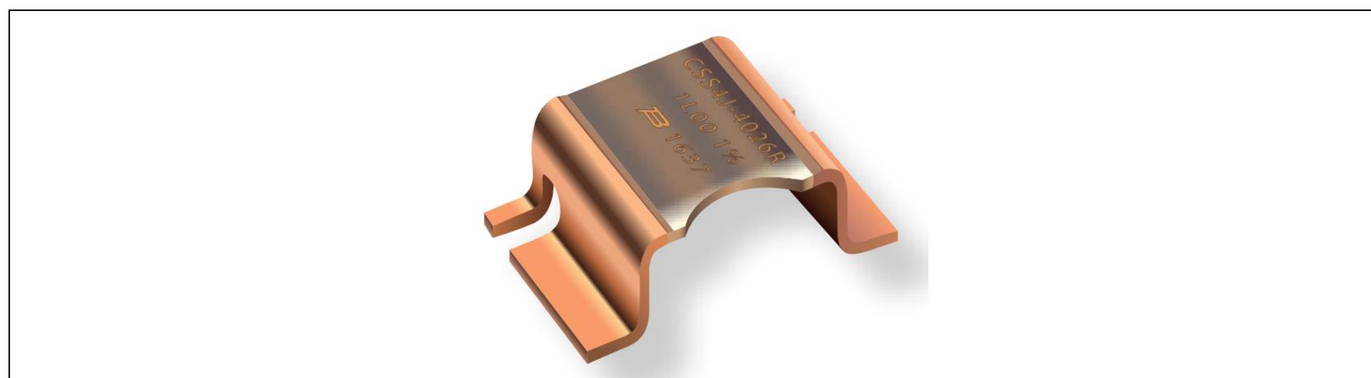


Figure 16 Four-pad shunt resistor

2 Additional recommendations

In the following chapters a few simple rules that can be applied during the layout design phase are discussed. The aim is to improve the correct functioning of the converter and decrease the level of EME.

2.1 Power connectors

Electromagnetic emission is mainly radiated by the PCB and the attached cables. The cables are very efficient antennas especially for common mode currents. Loops on the PCB are regarded as good emitting antennas. Loops inside an IC are considered to be small compared to the external loops on PCB and cabling. EME from the IC can be neglected in most cases.

Wires that carry the power from and to the DC-DC board can irradiate more or less EM energy depending on the position of power connectors. The lowest emissions are obtained when the input and output power connectors are placed on the same side, with the GND terminals as close as possible to each other as is depicted in ***Figure 17***.

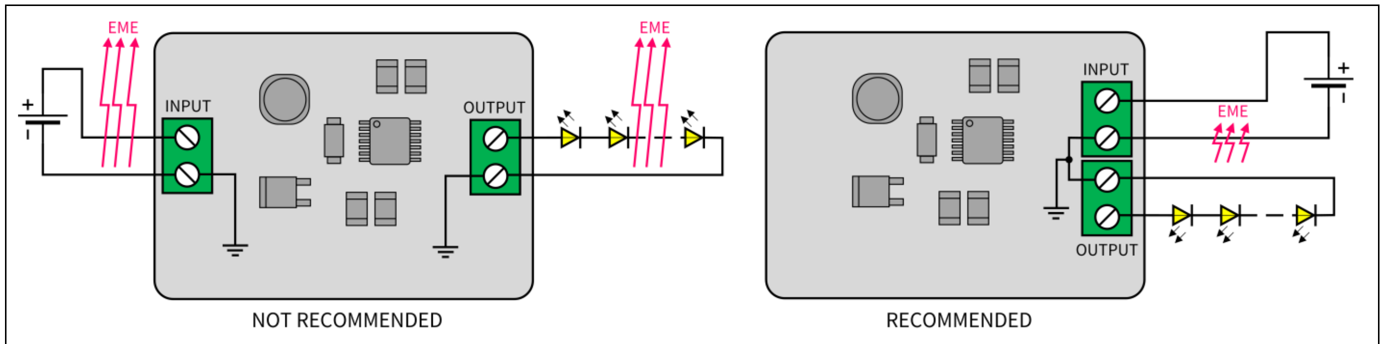


Figure 17 Power connectors placement

2.2 Void areas

Void areas over top, middle or bottom layers should be filled with GND plane. This will help to contain electric field emissions.

Pay attention to traces that carry extremely low voltage signals (for example FBH and FBL signals) to shield them from commutation noise coming from the switching area. Make sure that these traces are completely surrounded by copper areas connected to the underlying ground plane, with a large number of vias evenly distributed along the traces. See ***Figure 18***.

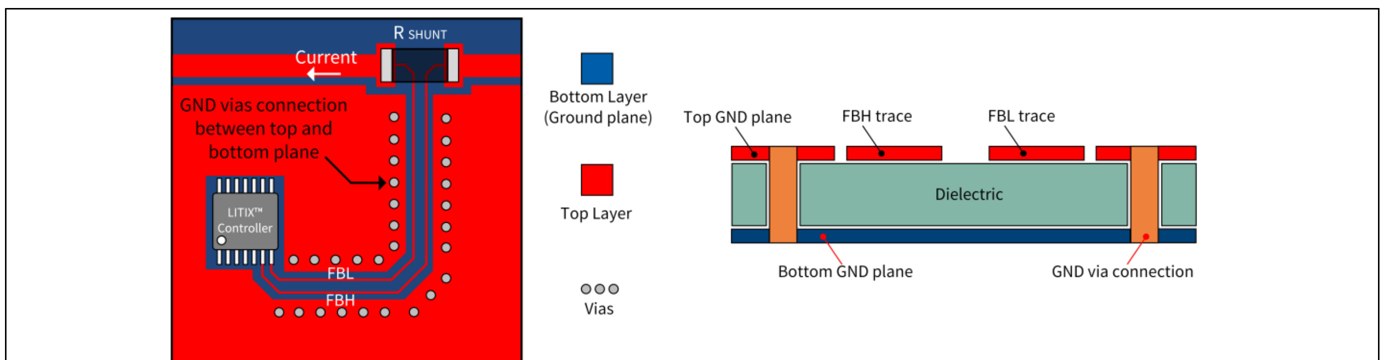


Figure 18 Filling void areas around traces

In some situations, it is not suggested to place the differential pair traces over the underlying bottom ground plane. This may be when the ground plane is affected by fast current transients, as in the zones close to the power stage area. Since the ground plane is not ideal and shows its own parasitic inductance, in the presence of fast current transients, local voltage spikes will appear on the ground plane, transferring their energy onto the traces nearby. In these cases, it may be helpful to remove the ground plane under differential pair traces and keep them as far as possible from the remaining ground plane edges.

A good example is examined in ***Figure 19***. The controller features a MOSFET current measurement by utilizing two wires that sense the differential voltage across a shunt resistor in series with the MOSFET source. In this case, since the shunt resistor and thus, the sense traces connected to its terminals are close to the power stage area, the ground plane below them has been removed.

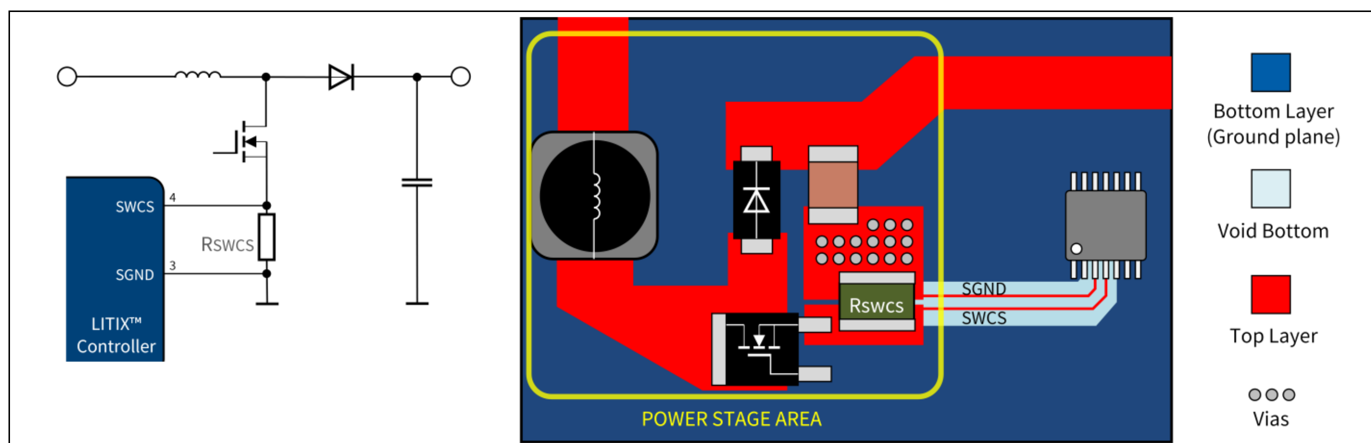


Figure 19 Removing ground plane

Furthermore, if possible avoid extending ground plane under input filter inductor: it could bypass inductor's effect, slightly transferring disturbances directly to the input.

2.3 Vias stitching

Connection between all GND areas should be made using the "Vias stitching" technique. It entails placing a distributed number of vias that make connections between all GND areas, in order to spread the electric field as evenly as possible amongst these different copper regions, as shown in ***Figure 20***.

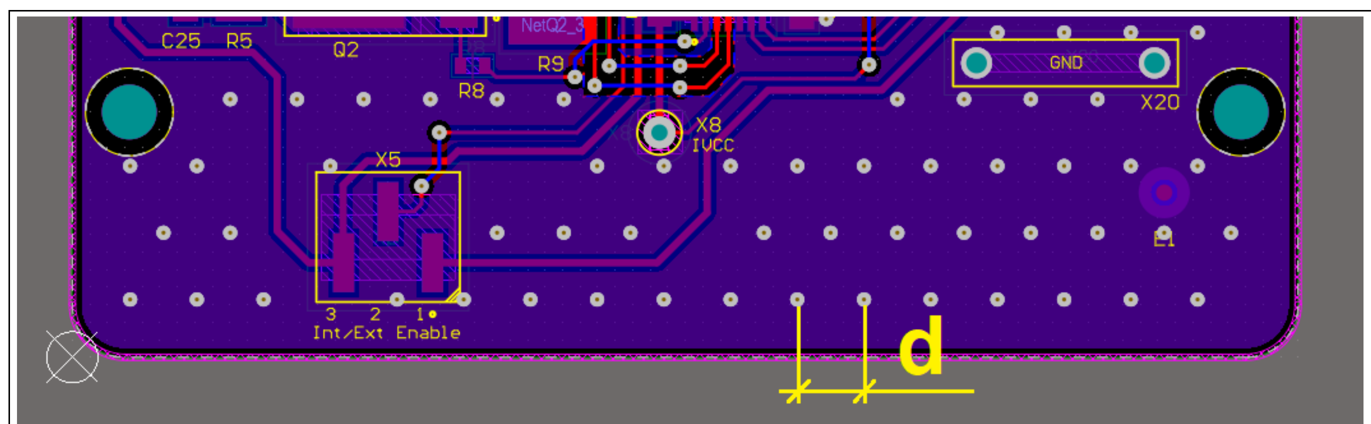


Figure 20 Vias stitching technique

Considering that electric field waves are not distributed uniformly on a conductor since they move roughly at light speed, a maximal distance between stitching vias must be adopted in order to limit the potential difference between two different points of ground plane and thus the EME.

If a generic material such as FR4 is used as dielectric layer between copper layers, the speed of electric field waves could be estimated at 60% of light speed.

As a generic safe rule, we can assume that the electric field between different copper areas is almost uniform if the distance *d* between two vias is:

$$d \leq \frac{0.6 \cdot c}{20 \cdot f}$$

where c is the speed of light: 300.000.000 m/s and *f* is the frequency of the electric field in Hz [2].

Frequency *f* should be chosen as the maximum frequency that will be analyzed/measured during the EME tests. *Table 5* depicts a sample of results:

Table 5 Vias stitching distance

Maximum frequency [GHz]	Two vias maximum distance [mm]
0.5	18.0
1.0	9.0
1.5	6.0
2.0	4.5
2.5	3.6
3.0	3.0

If frequency is unknown, in the automotive environment assume *f* = 2.5 GHz.

Vias length should not be longer than the distance *d*.

3 Thermal dissipation

LITIX™ Power and LITIX™ Power Flex devices are well known controllers for good EME performance. This could lead to a reduced number of components to filter unwanted harmonics and help the designer to reach the target of small PCB. One of the aims planned by the circuit designer is that PCB dimensions should be as small as possible. However, sometimes it becomes a challenge for the PCB designer to develop a small board that ensures the necessary heat dissipation, in comparison with the waste power produced by the DC-DC converter.

3.1 Heatsink

In most cases, the component that produces the highest amount of waste heat are the power MOSFETs. Almost always, the thermal pad of the MOSFET corresponds with its drain, often the terminal connected to the switching node. As explained in ***Chapter 1.4, Power stage***, switching node should be as small as possible, whereas for a good thermal dissipation it should be as large as possible, causing another constraint. It is clear that a compromise between these two requirements has to be reached.

If a four-layer is used (and one of the internal layers is designated as ground plane), the solution comprises of duplicating an area on the bottom layer, equal or larger to the thermal pad of the power MOSFET. This bottom copper area should be free of solder mask. Then, with multiple thermal vias, both areas are linked together in order to move the heat produced to the bottom layer. Hence, using a thermal conductive double-sided tape, an appropriate heatsink is applied.

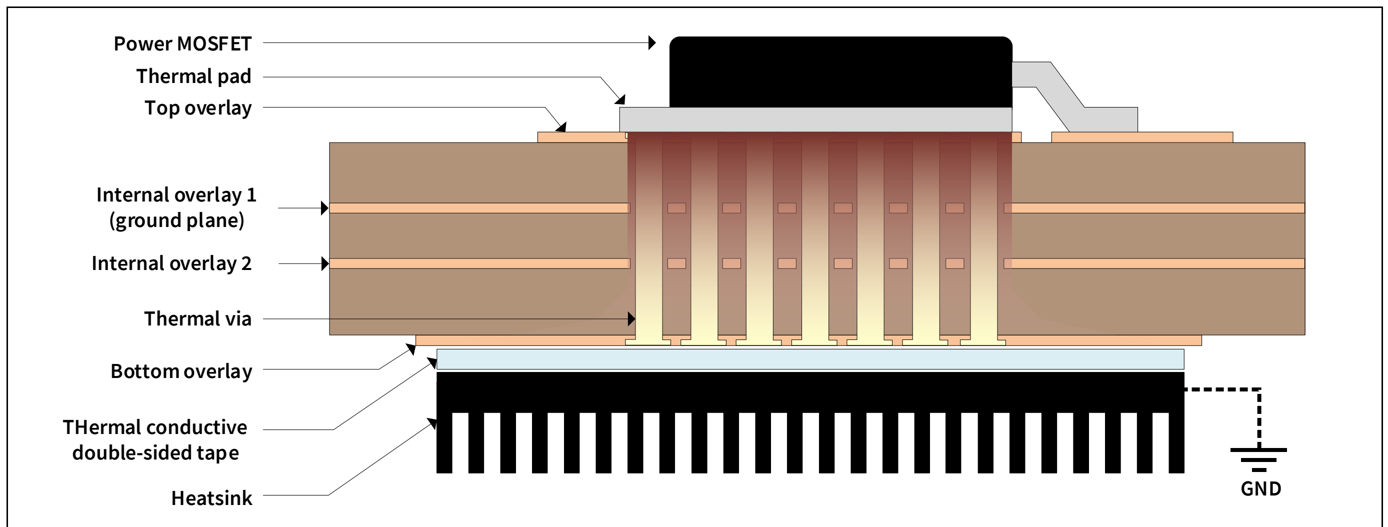


Figure 21 Heatsink application

Thermal resistance of a via can be roughly estimated by means of the following approximate formula, valid for copper vias only:

$$R_{thVIA} = \frac{t_{PCB}}{\lambda_{Cu} \cdot \pi \cdot \left[\left(t_{PL} + \frac{D}{2}\right)^2 - \left(\frac{D}{2}\right)^2\right]} \quad [K/W]$$

Where t_{PCB} is the thickness of the PCB in mm, λ_{Cu} = 0.39 W·mm^{-1}·K^{-1}, t_{PL} is the thickness of the via plating in mm and D is the inner diameter of via in mm.

Table 6 depicts a sample of results, related to one via with a height of 1.6 mm made of copper.

Table 6 Vias thermal resistance

Via hole diameter [mm]	Thermal resistance [K/W]	
	0.018 mm plating	0.025 mm plating
0.1	615	418
0.2	333	232
0.3	228	161
0.5	140	100
0.7	101	72
1.0	71	51

When N vias are used together (for example with a via array that covers all the thermal pad area of the MOSFET, as depicted in *Figure 21*), global equivalent thermal resistance could roughly be estimated by dividing the thermal resistance of one via by N. Should the extension area of the vias exceed the thermal pad of the MOSFET, this is no longer valid because the temperature is not uniform outside the thermal pad area and the via array should no longer be considered as a perfect parallel of vias. Thus, the higher the distance of one via from the heat source, the lower its contribution to the heat transfer towards the bottom.

Thermal conductive double-sided tape could be a ceramic filled tape that must fulfill two requirements. It should feature a high thermal conductivity and, if the heatsink is connected to a different potential than the thermal pad (often to ground), it has to withstand the voltage difference between these two points. A good choice could be the 3M type 8805 and 8810 that have a thermal conductivity λ_{TAPE} = 0.6 W/m·K.

The thermal resistance of the heatsink R_{thHS} can be roughly obtained with the following relation:

$$R_{thHS} \leq \left(\frac{T_{J_MAX} - T_A}{P_{LOSS_MOS}}\right) - R_{thJC} - \left(\frac{R_{thVIA}}{N_{VIAS}}\right) - R_{thTAPE} \quad [K/W]$$

where T_{J_MAX} is the maximum junction temperature of the MOSFET allowed in °C, T_A is the ambient temperature in °C, P_{LOSS_MOS} is the maximum power loss in watt of the MOSFET, R_{thJC} is the thermal resistance between junction and case of the MOSFET in K/W, R_{thVIA} is the thermal resistance of one via in K/W and N_{VIAS} is the number of thermal vias in parallel under the MOSFET thermal pad (vias should have all the same size). R_{thTAPE} is the thermal resistance of double-sided tape applied between PCB and heatsink, calculated as:

$$R_{thTAPE} = \frac{1}{\lambda_{TAPE}} \cdot \frac{t_{TAPE}}{A_{TP}} \cdot 10^3 \quad [K/W]$$

where λ_{TAPE} is the thermal conductivity of the tape material in W/m·K, t_{TAPE} is the thickness of the tape in mm and A_{TP} is the area of the thermal pad of the MOSFET in mm^2.

In *Chapter 1.4 Power stage* it was explained that the bigger the switching node, the stronger the electric field variations emitted. Therefore, in order to reduce EME, it is necessary to reduce the dimensions of the switching node as much as possible. Unfortunately, by applying a heatsink the dimensions of the switching node are extended despite the presence of insulating double-sided tape. High frequencies will be transmitted through the tape due to capacitive effect and the heatsink will act as a big antenna. What can be done in this case is to connect the heatsink to local ground of the circuit, to force the heatsink potential to zero and stop EME. Frequently, the heatsink is the chassis or the metallic box wherein the circuit is contained.

4 List of references

[1] H. Johnson-M. Graham, *High-Speed digital design*, Prentice Hall

[2] M.K. Armstrong*, PCB design techniques for lowest-cost EMC compliance,* IEEE Journal, 1999

Revision history

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