OPTIREG™ PMIC TLF30682QVS01 application board user manual

About this document

Scope and purpose

The scope of this Application Note is limited to the OPTIREG™ PMIC TLF30682QVS01 Multi-Voltage System Supply IC. The purpose is to describe the setup, operation, testing and key features of the TLF3068x Application Board.

Intended audience

This Application Note is intended for users of Infineon's TLF30682QVS01 Multi-Voltage System Supply IC.

Table of contents

1 TLF3068x application board overview

The TLF3068x Application Board is shown in Figure 1. The schematic is shown in Chapter 4 and the printed circuit board (PCB) layout in Chapter 5. The application board includes the essential components and circuits needed to evaluate the TLF30682QVS01 in typical user applications. A more detailed description of the TLF30682QVS01 and its operation can be found in the device data sheet. The TLF3068x Application Board includes:

- TLF30682QVS01 Multi-Voltage System Supply IC with output filters for Buck1, Buck 2 and Boost 1
- Power connectors for the battery input voltage
- Connectors for all control signals including the interface to an Aurix™ microcontroller, SPI signals and analog measurement points
- Connectors for monitoring and control of two external voltage rails (VM1 and VM2)
- Slammer loads for transient load tests on Buck 1 and Buck 2
- Reverse battery protection for the battery input voltage – passive or active protection
- A two stage (common mode and differential mode) electromagnetic interference (EMI) filter
- Capability to interface to a TLF3068x Companion Board that includes an Aurix™ microcontroller

TLF3068x application board overview

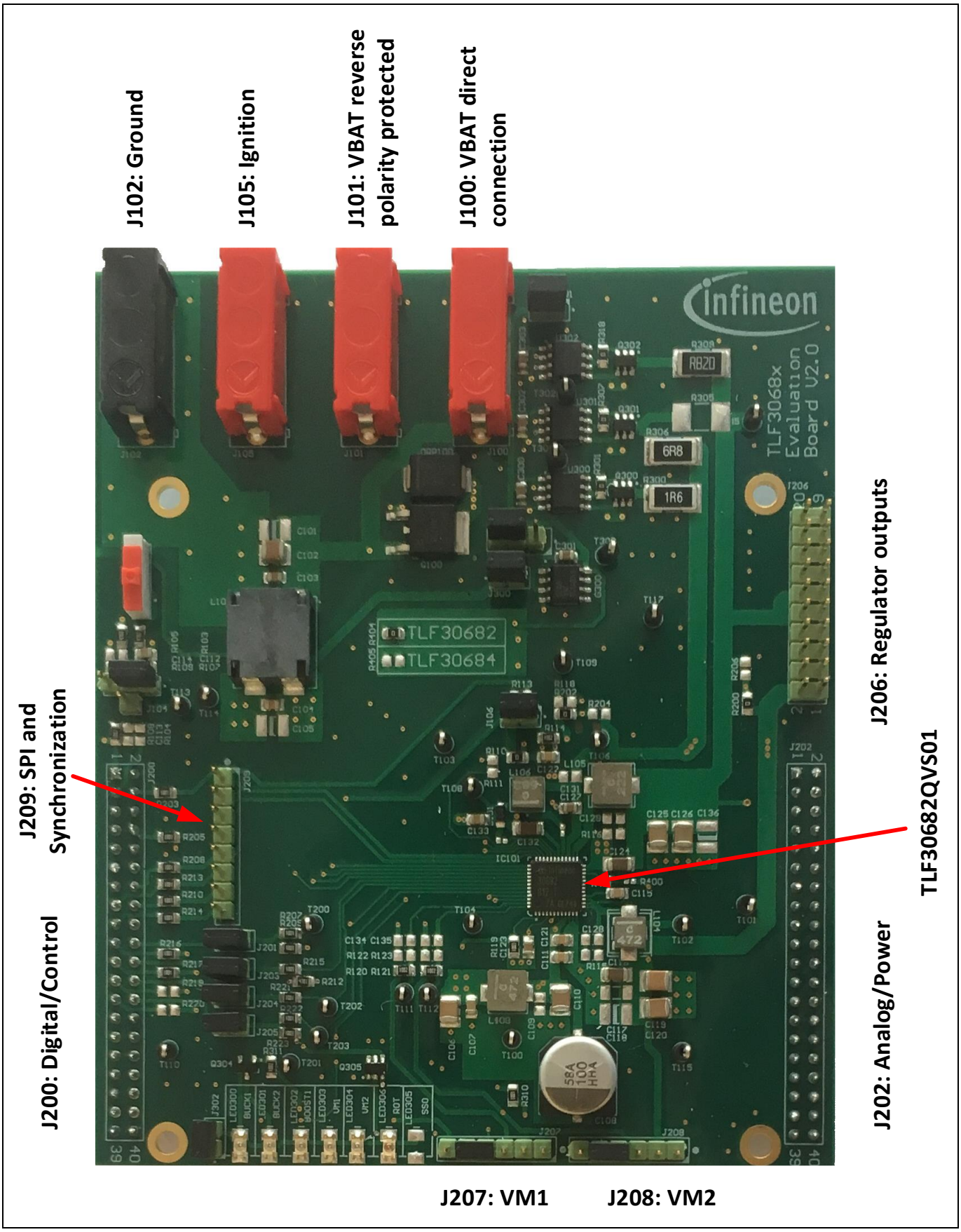

Figure 1 **TLF3068x Application Board and Connector Locations**

1.1 Functional range

The functional range of the TLF3068x Application Board is shown in Table 1.

Table 1 TLF3068x Application Board Functional Range

Parameter	Min.	Typ.	Max.	Unit
Input Voltage (VS) Normal Operation T100 to T115	5	13.5	35.0	V
Input Voltage (VS) Derated Operation T100 to T115	3.7		5	V
Buck1 load current[1] Normal Operation Derated Operation	 0 0		 3.5 2.0	 A A
Buck2 load current	0		2.0	A
Boost1 load current	0		0.25	A
Operating temperature[2]	0	25	85	°C

1.2 Connectors

The connectors used on the TLF3068x Application Board are shown in Table 2, Table 3, Table 4, Table 5 and Table 6 with placement locations shown in Figure 1.

Table 2 TLF3068x Application Board Connectors

Connector	Description
J100	Battery supply voltage - no reverse polarity protection
J101	Battery supply voltage - with reverse polarity protection
J102	Ground for battery supply voltage
J105	Ignition signal - connected to the ENA pin of the TLF30682QVS01 via J104
J200	Digital control signals. The connector is intended for connection with the TLF3068x Companion Board
J202	Supply voltages and control signals for the slammer load. The connector is intended for connection with the TLF3068x Companion Board
J206	External load connector with access to the outputs of Buck1, Buck2 and Boost1 (see Table 3)
J207	External voltage 1 monitoring and control - VM1 (see Table 4)

[1] Includes the Buck2 and Boost1 regulator loading.

[2] The operating range for the TLF3068x Application Board is limited by some of the external components used on the board. Please refer to the TLF30682QVS01 Data Sheet for information about the operating temperature range of the TLF30682QVS01.

TLF3068x application board overview

Connector	Description
J208	External voltage 2 monitoring and control - VM2 (see Table 5)
J209	SPI interface and synchronization signals (see Table 6)

Table 3 J206 Output Load Connector Pin Out

Pin	Signal Name
1, 2, 3, 4	BUCK1 VOUT
9, 10, 11, 12	BUCK2 VOUT
17, 18	BOOST1 VOUT
5, 6, 7, 8, 13, 14, 15, 16, 19, 20	GND

Table 4 J207 Connector Pin Out

Pin	Signal Name	Description
1, 5	GND	Ground
2	BUCK1 VOUT	Buck1 output voltage
3	VM1	External post regulator 1 output voltage to be monitored
4	VM1EN	Enable signal from the TLF30682QVS01 to external post regulator 1
6	SYNCO	Output synchronization signal from the TLF30682QVS01 to an external post regulator.

Table 5 J208 Connector Pin Out

Pin	Signal Name	Description
1, 5	GND	Ground
2	BUCK1 VOUT	Buck1 output voltage
3	VM2	External post regulator 2 output voltage to be monitored
4	VM2EN	Enable signal from the TLF30682QVS01 to external post regulator 2
6	SYNCO	Output synchronization signal from the TLF30682QVS01 to an external post regulator.

Table 6 J209 Connector Pin Out

Pin	Signal Name	Description
1	SYNCO	Output synchronization signal from the TLF30682QVS01 to an external post regulator.
2	SYNCI	Optional input synchronization signal to the TLF30682QVS01
3, 4	GND	Ground

TLF3068x application board overview

Pin	Signal Name	Description
5	SCS	SPI signal chip select
6	SCL	SPI signal clock
7	SDI	SPI signal data input
8	SDO	SPI signal data output

2 Initial board power up

Follow these steps for the initial TLF3068x Application Board power up.

1. Ensure that the following jumpers are set on the application board:
   - J103 - Place a jumper between pin 2 and 3 to enable the active reverse polarity protection
   - J104 - Place a jumper between pin 1 and 2 to select switch S100 as enable signal for the device
   - J106 - Place a jumper to enable MPS mode (Microcontroller Programming Support). The TLF30682QVS01 must be operated in MPS mode when there is no microcontroller connected to the device
   - J207 - Place a jumper between pin 4 and 5 to disable External Voltage Monitoring Channel VM1
   - J208 - Place a jumper between pin 4 and 5 to disable External Voltage Monitoring Channel VM2
   - J300 - No jumper should be placed to disable the 5V LDO supplying the drivers for the slammer loads
   - J301 - No jumper should be placed to disable the slammer loads
   - J302 - Place a jumper to enable the indicator LEDs on the TLF3068x Application board
   - J201, J203, J204 and J205 - Jumpers should be placed on these headers if the TLF3068x Application Board is used in conjunction with the TLF3068x Companion board
2. Connect an external power supply to the input connectors J101(+) and J102(-)
   - The power supply must be able to supply up to 35V and 4A of current to be able to test the full capabilities of the TLF3068x Application Board. A power supply with reduced operating range can be used for some specific tests with a reduced operating range of the TLF30682QVS01.
3. Set the output voltage of the external power supply to 13.5V.
4. Enable the output of the external power supply. The application board should now be operating:
   - The output voltages of Buck1 (3.3V), Buck2 (1.25V) and Boost1 (5.0V) should now be present on J206
   - The current consumption of the shall be approximately 10mA
   - The LEDs LED300, LED301 and LED302 shall be ON
5. Please contact your Infineon support team in case the application board does not show the described behavior.

3 Board configuration and testing

The TLF3068x Application Board has been designed to enable the testing of all the key features of the TLF30682QVS01 Multi-Voltage System Supply IC.

3.1 Dynamic load testing

The TLF3068x Application Board has three slammer loads intended for testing the dynamic load step response of Buck1 and Buck2. The slammer loads consist of a power resistor in series with a power MOSFET connected between the output of either Buck1 or Buck2 and GND. The power MOSFETs are driven by high performance MOSFET drivers that can turn the MOSFETs ON and OFF very fast. Therefore, it possible to generate load steps on the output of Buck1 and Buck2 with current slew rates in excess of 100 A/µs.

Jumpers J300 and J301 must be placed to enable the slammer loads. It is recommended only to place these jumpers when dynamic load measurements are performed.

The slammer loads can be controlled two ways (use only one method):

- Control by a function generator driving the logic inputs of the MOSFET drivers at inputs GML1, GML2 and GML3 which are available at test points or the J202 connector. The logic signal to the MOSFET driver input should be a square wave with an amplitude of 5V peak (referenced to ground), less than 50% duty cycle and frequency less than 50 kHz. Recommend not connecting the TLF3068x Companion Board when using this method.
- TLF3068x Companion Board can provide the GML1, GML2 and GML3 control signals at the J202 connector.

Table 7 describes the application board slammer loads and control signals. For different load step conditions, an external load that can be connected to the output of Buck1 or Buck2 on J206 (Table 3).

Table 7 Slammer Loads

TLF30682QVS01 Output	Load Resistor	Nominal Load Current (Percent of Maximum Nominal Load)	Control Signal
Buck1	1.6 Ω	2.06 A (59%)	GML3 (J202-38, T300)
Buck1	6.6 Ω	0.5 A (14%)	GML2 (J202-37, T301)
Buck2	0.82 Ω	1.46 A (73%)	GML1 (J202-36, T302)

Note: The dynamic slammer loads on the TLF3068x Application board have been designed to operate with a frequency less than 50 kHz and with a duty cycle less than 50% to avoid damage to the load resistors.

3.2 External voltage monitoring

The TLF30682QVS01 can control and monitor two external voltage regulators. The TLF3068x Application Board does not include these external voltage regulators. However, the application board provides the interface for

the control and monitoring of these external voltage regulators on connectors J207 (Table 4) and J208 (Table 5).

There are two different external regulator configurations options. The first option in Figure 2 is only for low power regulators that can be supplied with 3.3V from Buck1 of the TLF30682QVS01. The current drawn from the BUCK1VOUT pin of header J207/J208 should be limited to 100mA due to PCB layout limitations.

The second option in Figure 3 can be used if the external voltage regulators require an input supply voltage greater than 3.3V and/or an input current draw of more than 100mA. This option uses an external power supply to provide the input voltage to the external voltage regulator (instead of the Buck1 output voltage). This can be the same power supply that is used to power the application board.

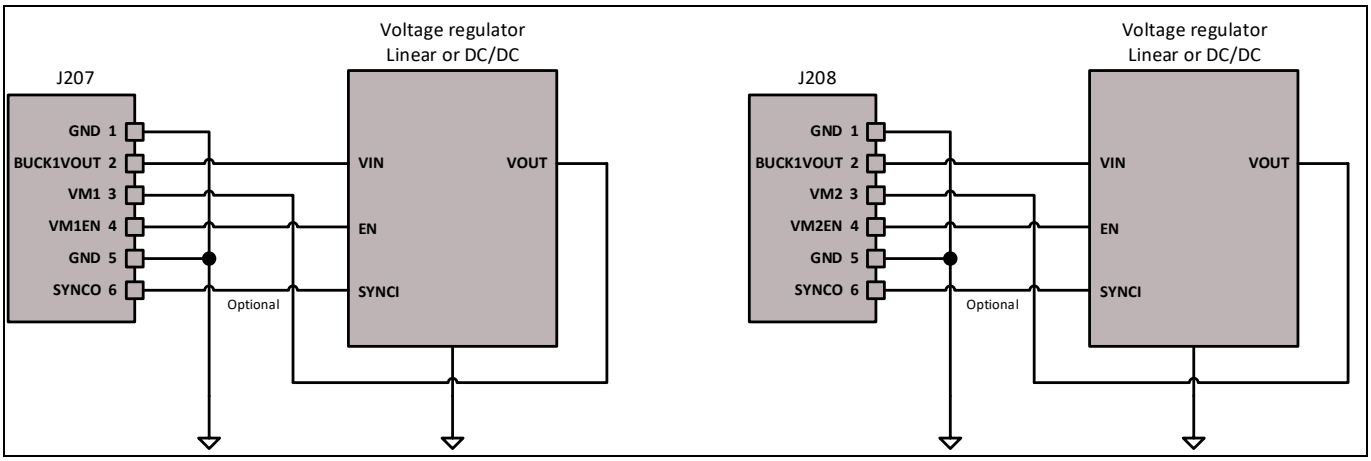

Figure 2 External Voltage Monitoring channels 1 and 2 BUCK1VOUT as a supply

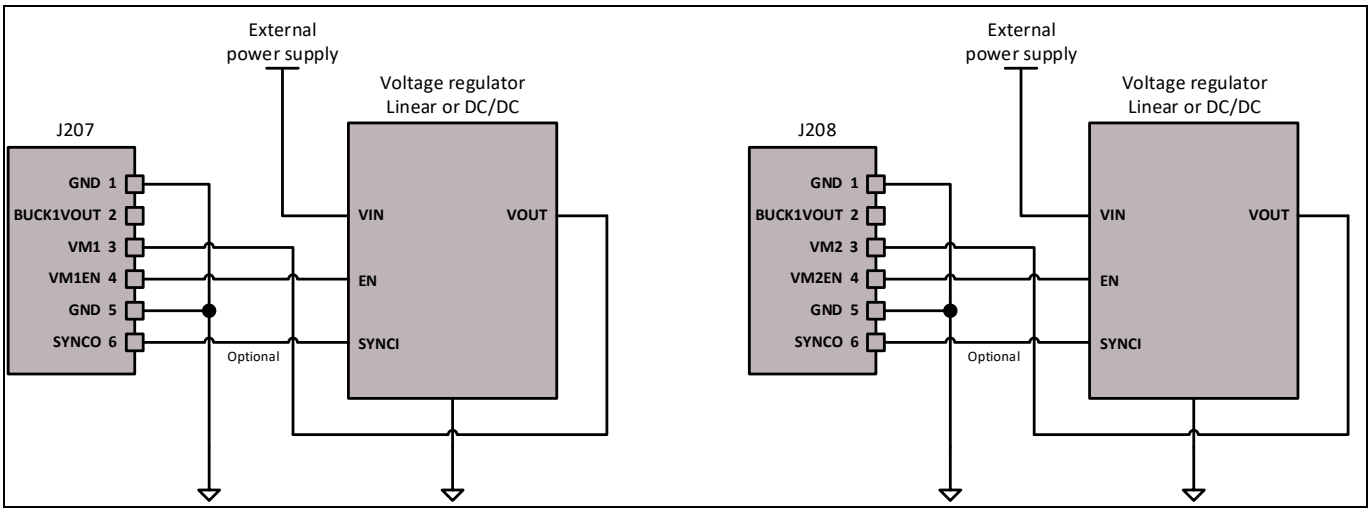

Figure 3 External Voltage Monitoring channels 1 and 2 using an external power supply

The TLF30682QVS01 external voltage monitors have an internal reference of 0.8V. Therefore, it is required to have a resistor divider on the output of the external voltage regulator that scales the voltage down to 0.8V on the VM1FB and VM2FB pins of the TLF30682QVS01. The application board includes footprints for the required resistor dividers. The resistors in the dividers need to be selected to fulfill the following equations:

$$V_{VM1} \cdot \frac{R122}{R120 + R122} = 800 \cdot mV$$

$$V_{VM2} \cdot \frac{R123}{R121 + R123} = 800 \cdot mV$$

V_{VM1} and V_{Vm2} are the nominal output voltages of the monitored external voltage regulators.

The recommended resistance for R120 and R121 is 10kΩ.

The application board is initially configured with R120 = R121 = 10kΩ and R122 = R123 = 0Ω.

3.3 Enable functionality

The TLF3068x Application Board provides three options to configure the TLF30682QVS01 enable (ENA) pin:

- The ENA pin is connected to the J105 Ignition signal input through a resistor divider. This option can be used in the lab to access the ENA pin via the banana plug J105 connector. To select this option, place a jumper between pin 2 and 3 of J104.
- The ENA pin is connected to the CON_ENA pin of J200-3. This option can be used to allow the Aurix™ microcontroller on theTLF3068x Companion Board to control the enable functionality of the TLF30682QVS01. To select this option, place a jumper between pin 2 and 4 of J104 and place resistor R104 (100Ω).
- The ENA pin is connected to VBATP through a resistor divider and switch S100. The VBATP signal is derived from the J100 or J101 input battery supply voltage. This option can be used to have simple way of toggling the ENA pin between low and high using switch S100. Place a jumper between pin 1 and 2 of J104 to select this option.

The TLF30682QVS01 will not automatically turn off all outputs if the ENA pin is toggled from high to low. However, the TLF30682QVS01 will pull the INT pin low which signals to the microcontroller to read the TLF30682QVS01 status registers. It is then up to the microcontroller to change the state of the TLF30682QVS01 from ACTIVE to DISABLE through the SPI interface.

If the TLF30682QVS01 is in either the DISABLED or LOCKED state, a transition from low to high on ENA will trigger a transition to the ACTIVE state.

3.4 Indicator LEDs

The TLF3068x Application Board has six status LED indicators:

- Buck1 – Green indicating voltage on the Buck1 output.
- Buck2 – Green indicating voltage on the Buck2 output.
- Boost1 – Green indicating voltage on the Boost1 output.
- VM1 – Green indicating greater than approximately 2V on the External Voltage Regulator 1 output.
- VM2 – Green indicating greater than approximately 2V on the External Voltage Regulator 2 output.
- ROT – Red indicating a microcontroller reset condition.

The LEDs on the application board will draw a few milliamps of current from the different voltage rails. The LEDs can be disabled for efficiency and quiescent current measurements by removing the J302 jumper.

3.5 Reverse polarity protection

The TLF3068x Application Board has components allowing either passive or active reverse polarity protection. Reverse polarity protection is available when the battery input power supply is connected to J101. The Application Board can also be tested without reverse polarity protection by connecting the battery input power supply to J100 instead of J101.

Active reverse polarity protection is provided by MOSFET Q100 when a jumper is placed between pin 2 and 3 on J103 header. Q100 will be turned on when the output of Boost1 of the TLF30682QVS01 is ON.

Diode DRP100 provides passive reverse polarity protection when a jumper is placed between pin 1 and 2 on J103 header.

Active reverse polarity protection will be more efficient with lower losses than passive reverse polarity protection. This is because the Q100 voltage drop will be less the DRP100 voltage drop.

4 Schematic

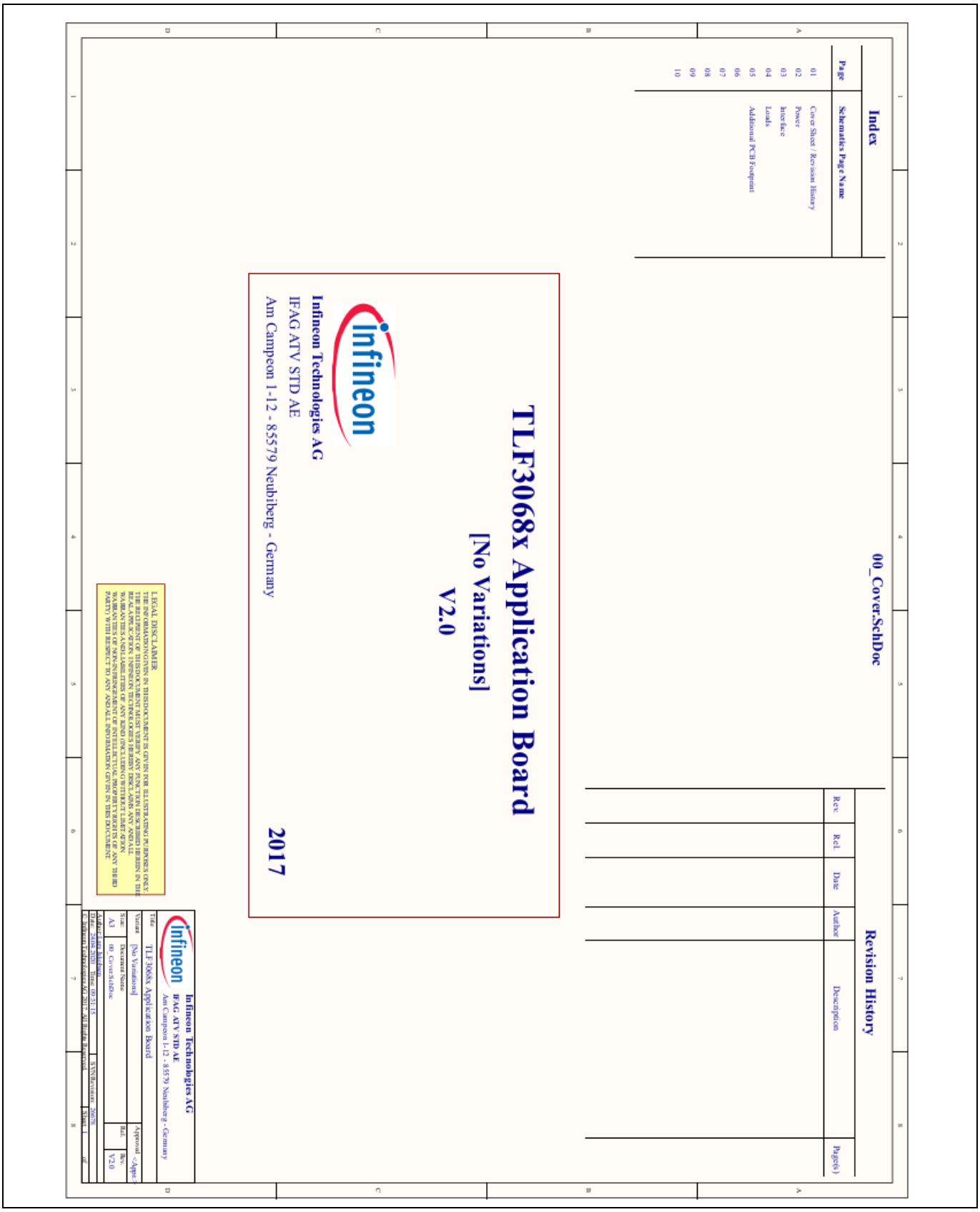

Figure 4 TLF3068x Application Board Schematic – Cover Page

Schematic

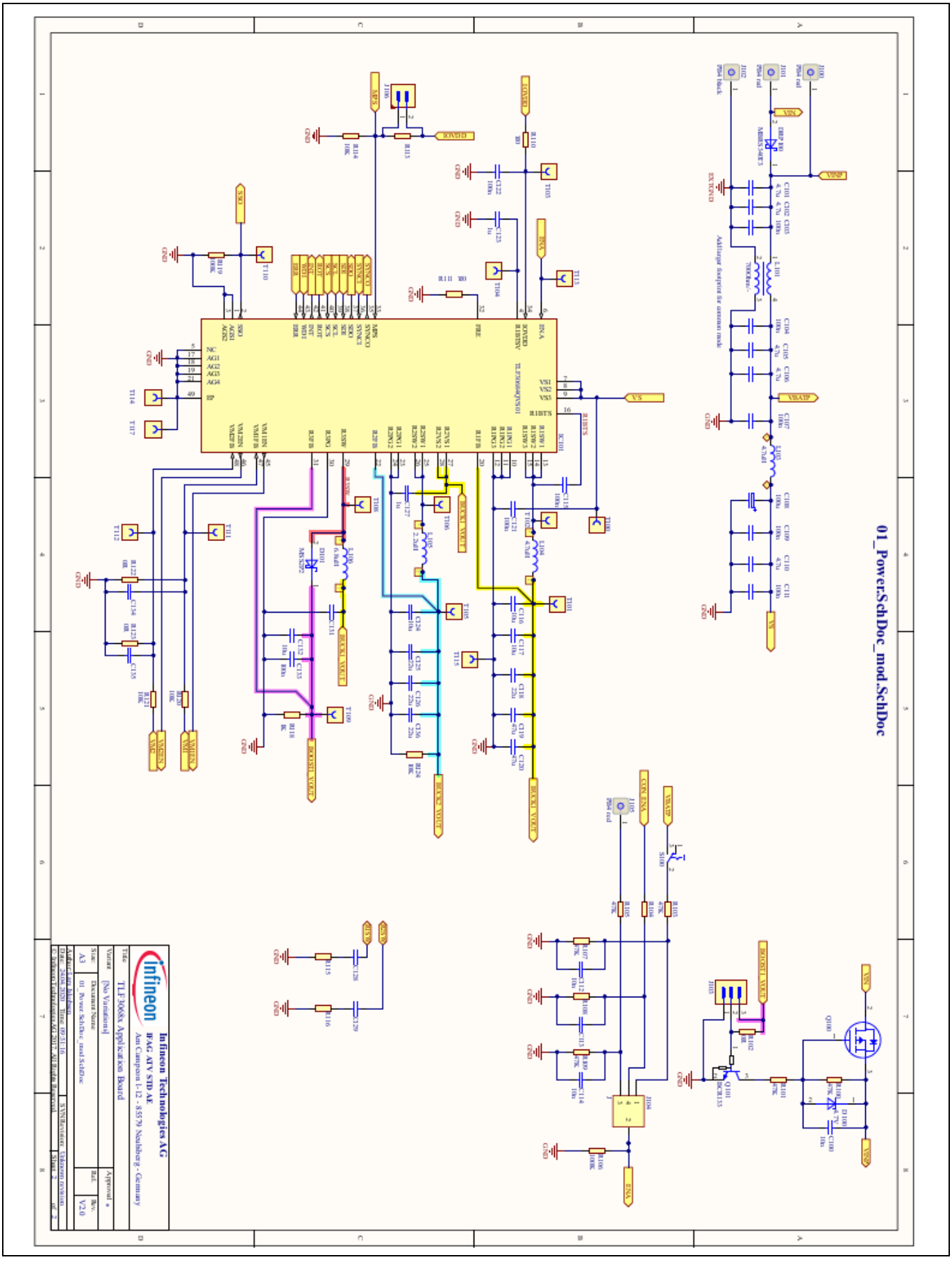

Figure 5 TLF3068x Application Board Schematic – TLF30682QVS01 Application Circuit

Schematic

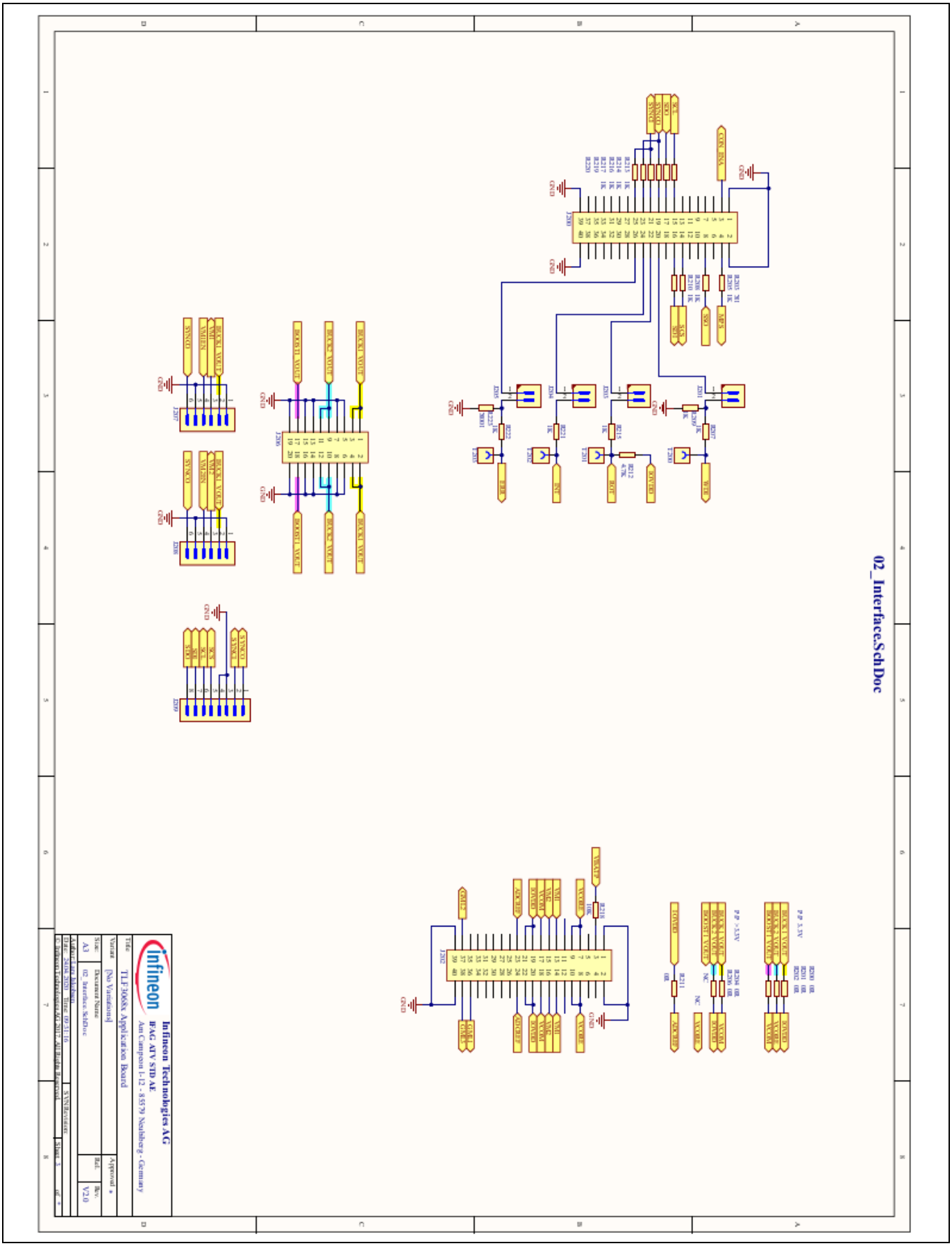

Figure 6 TLF3068x Application Board Schematic - Connectors

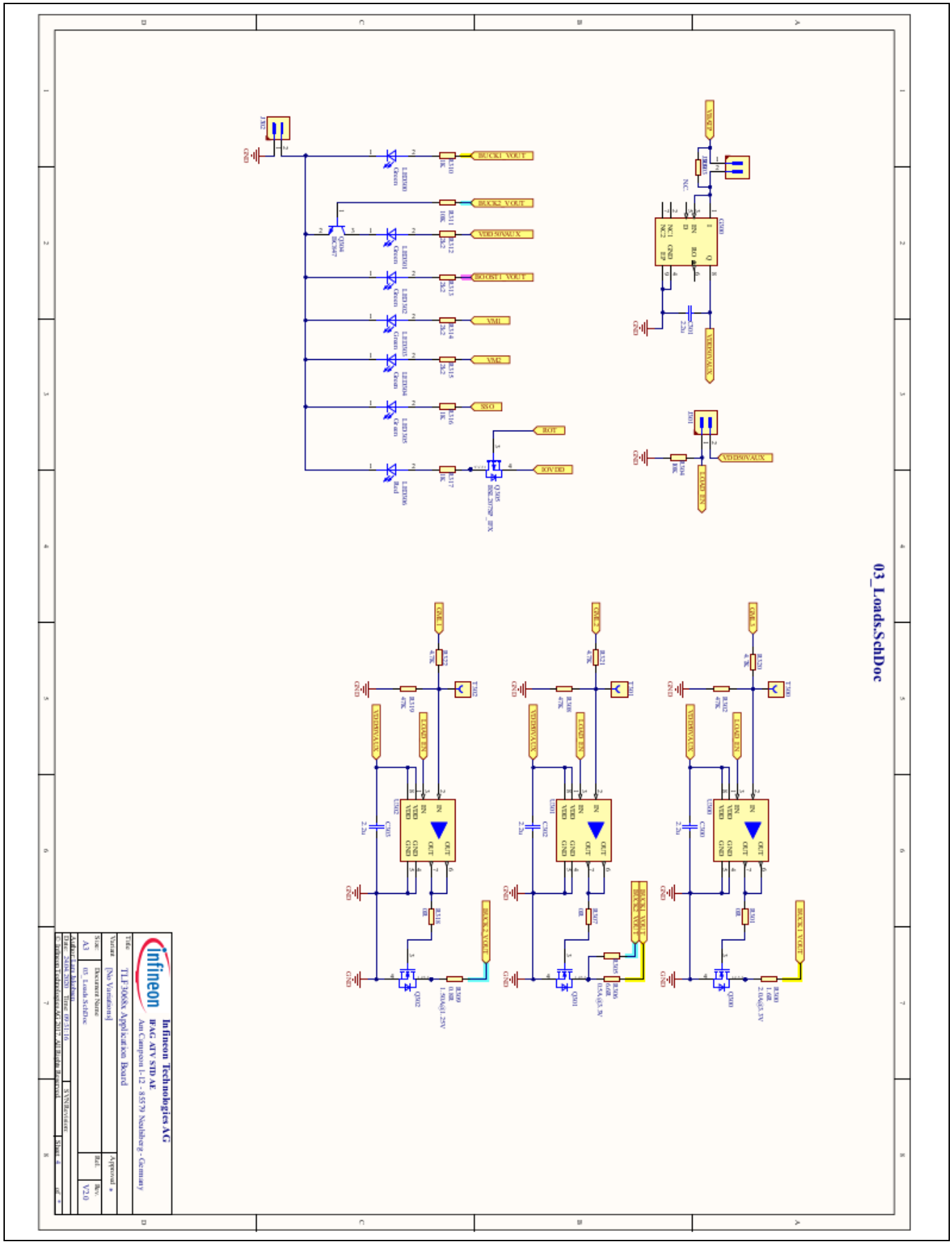

Figure 7 TLF3068x Application Board Schematic – Dynamic Loads and LEDs

Schematic

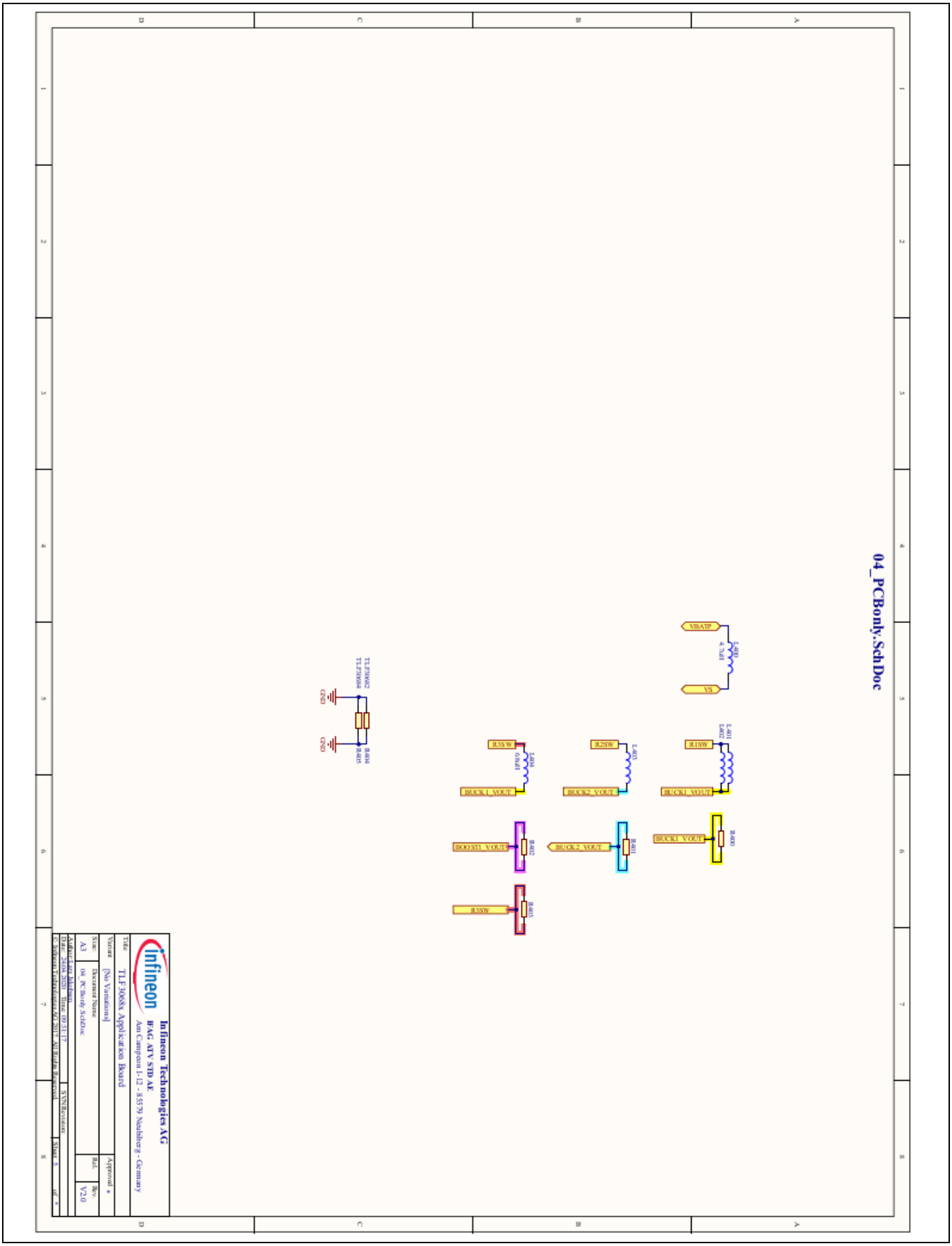

Figure 8 TLF3068x Application Board Schematic – Miscellaneous

5 PCB Layout

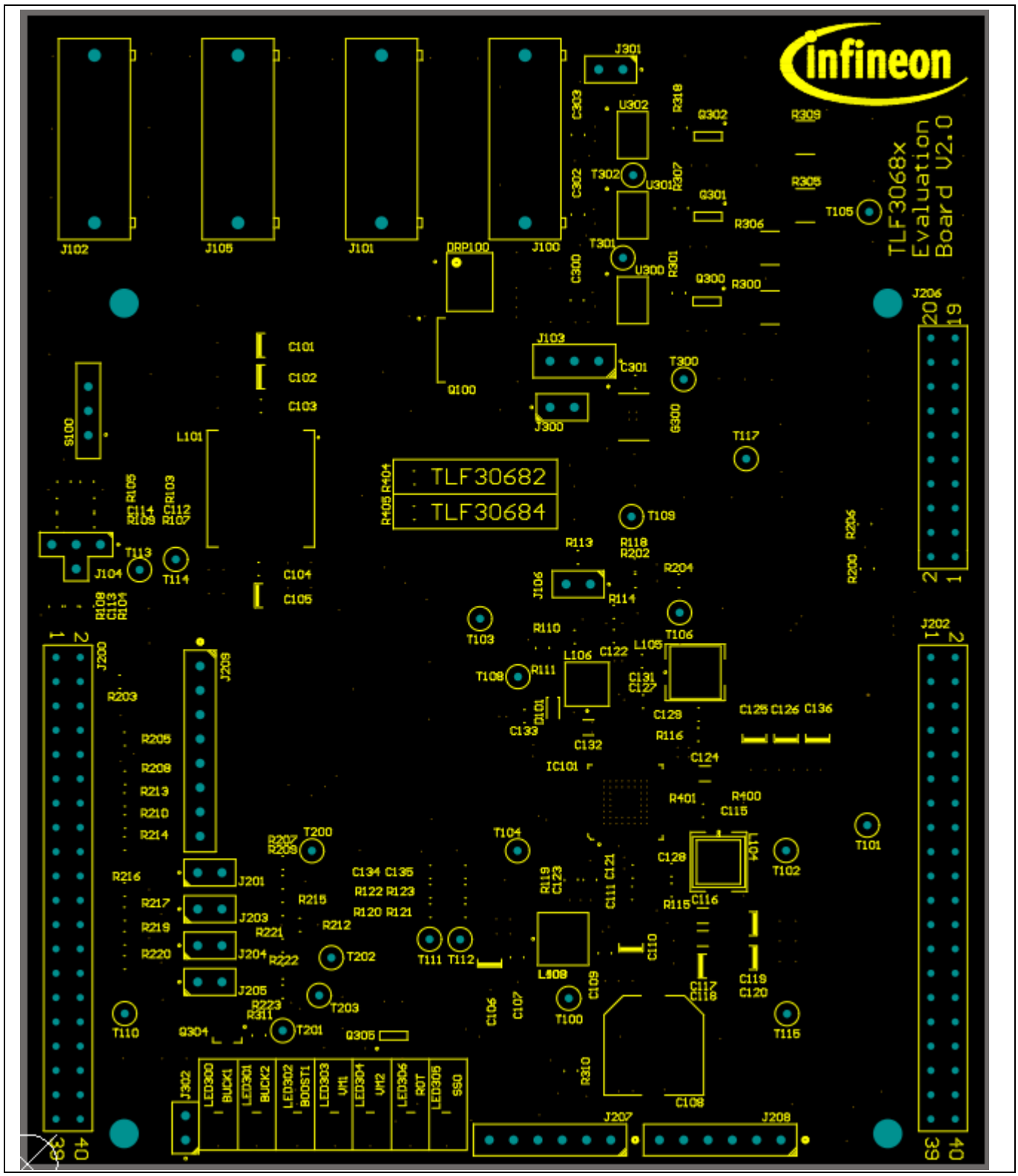

Figure 9 TLF3068x Application Board - Silkscreen Layer 1 (Top)

PCB Layout

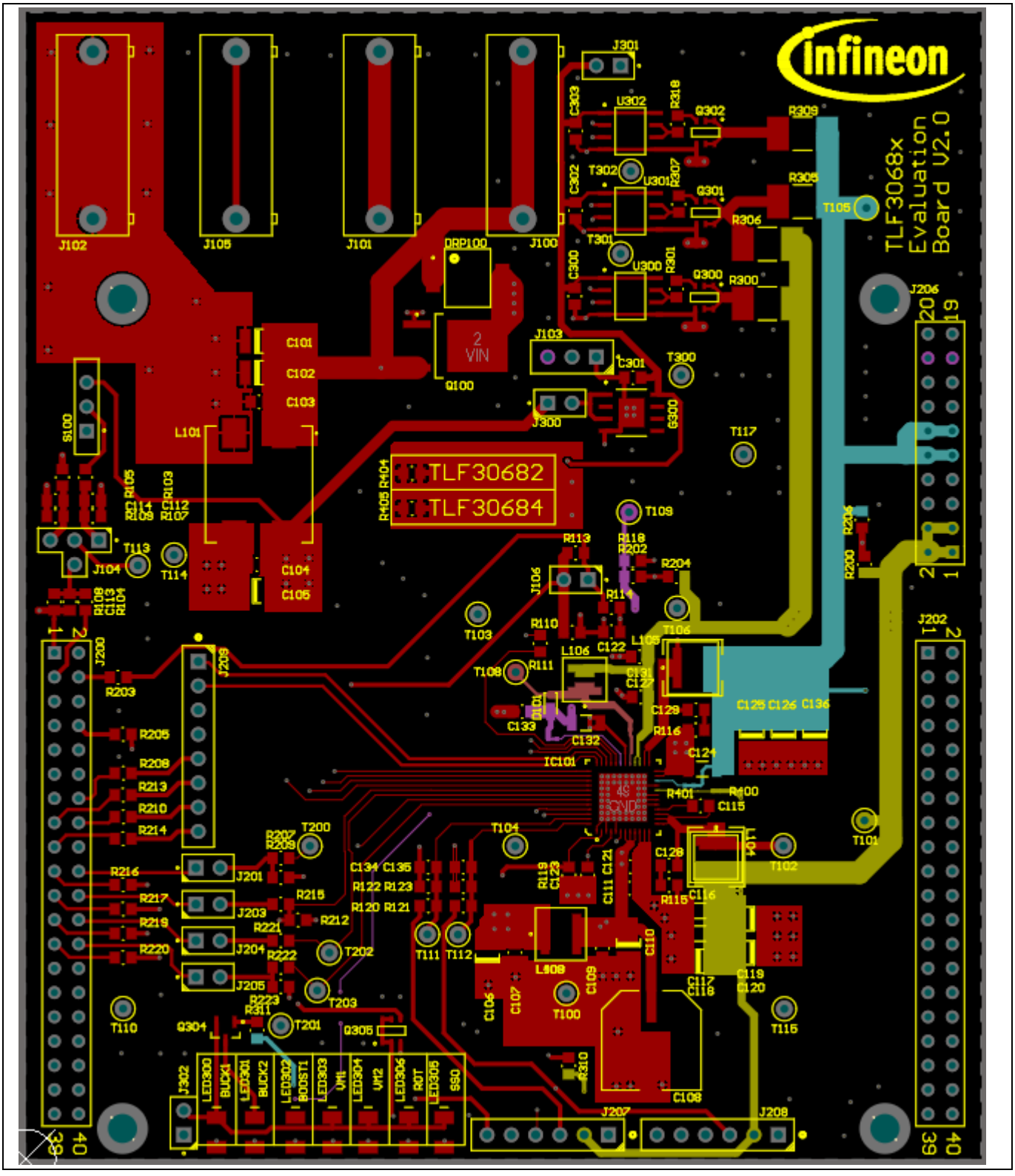

Figure 10 TLF3068x Application Board - Layer 1 (Top)

PCB Layout

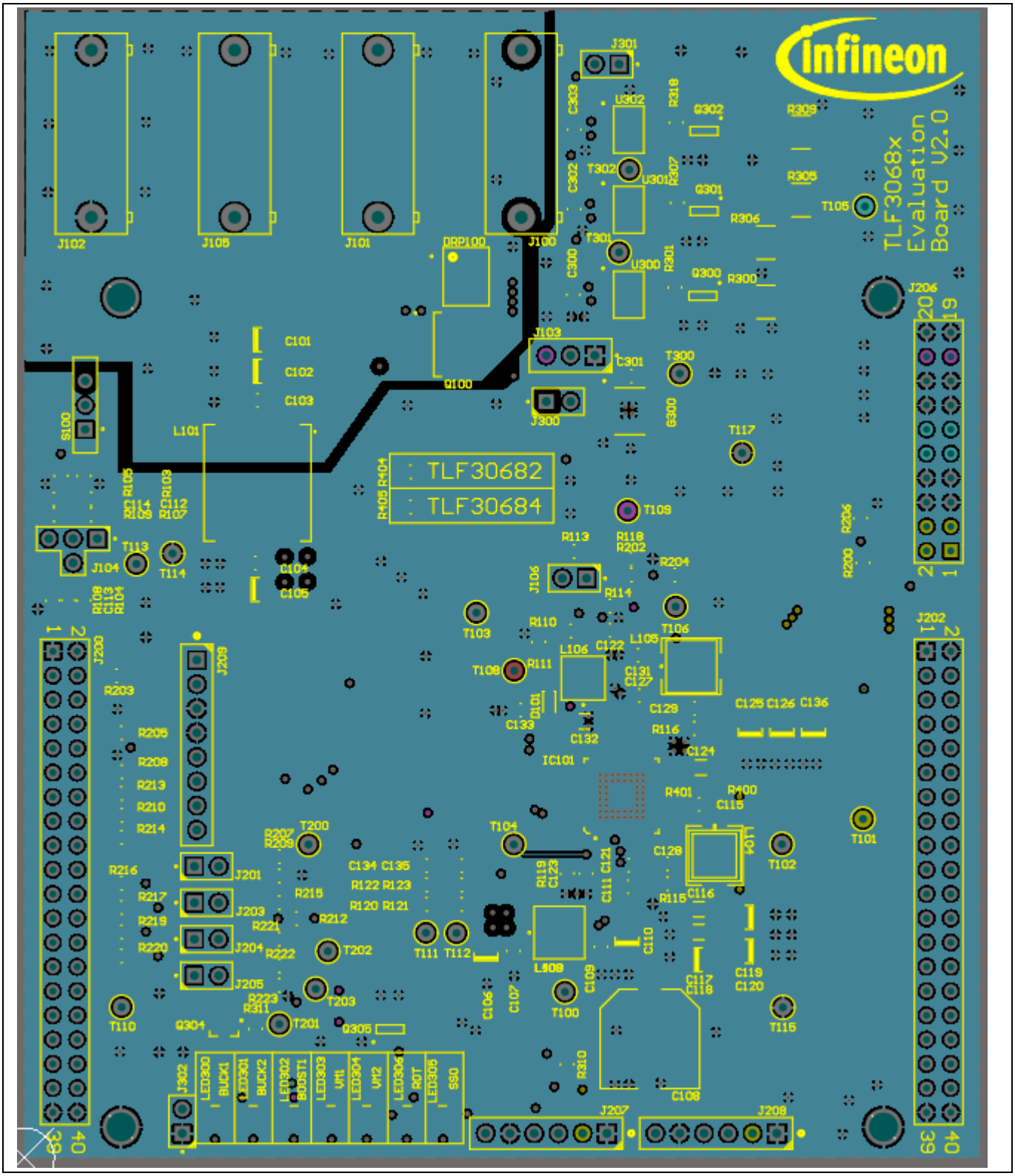

Figure 11 TLF3068x Application Board - Layer 2

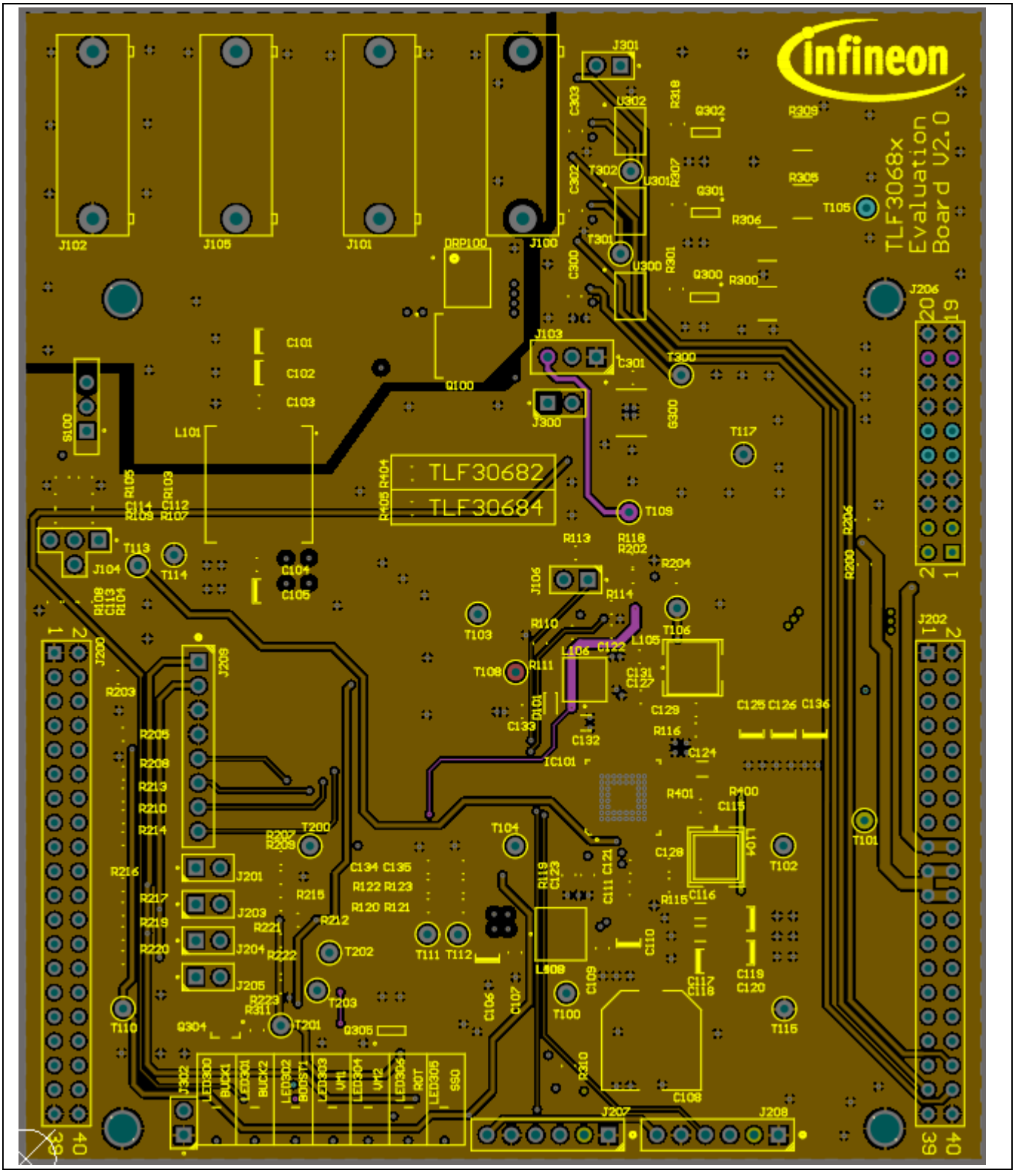

Figure 12 TLF3068x Application Board - Layer 3

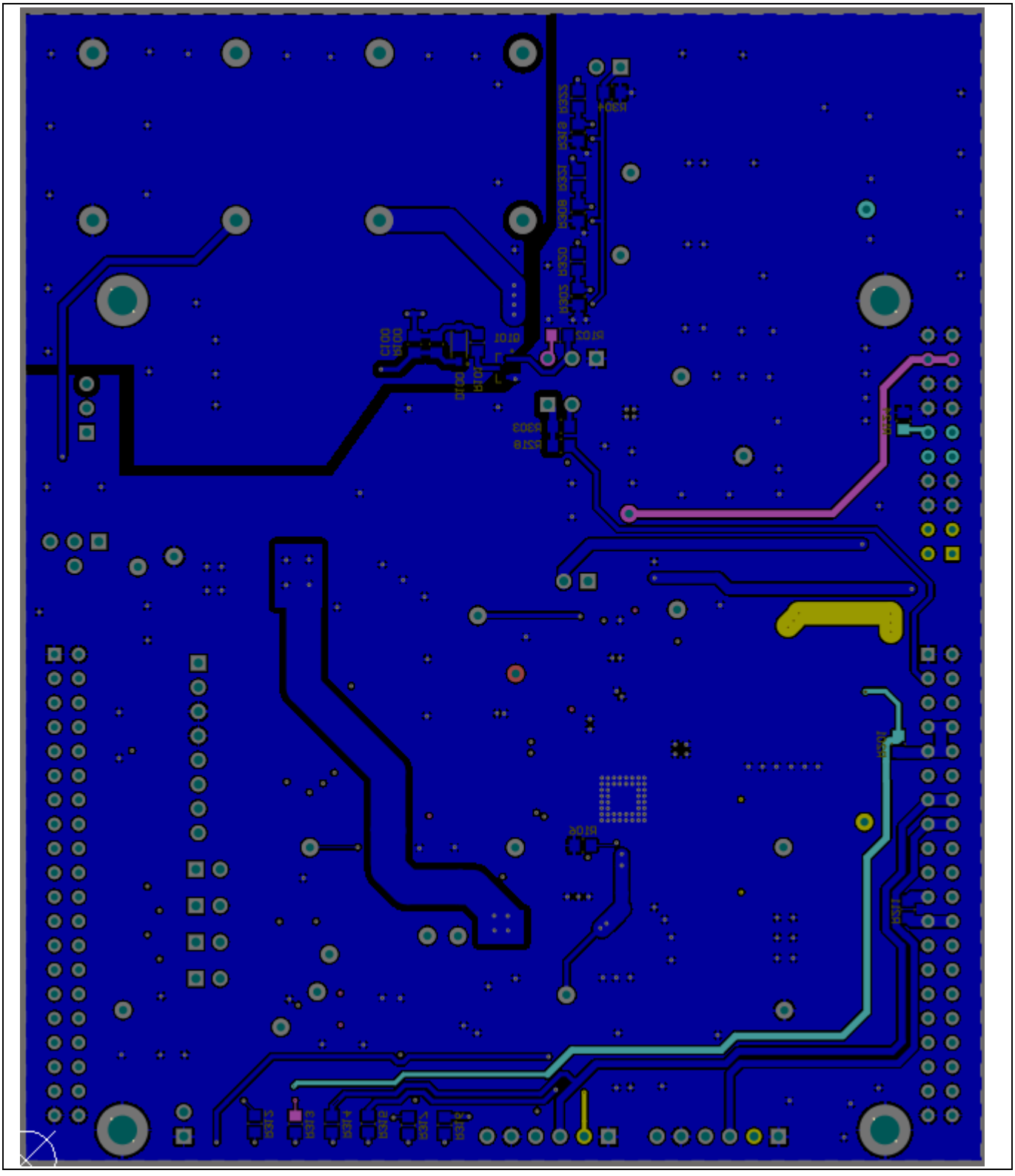

Figure 13 TLF3068x Application Board - Layer 4 (Bottom)

PCB Layout

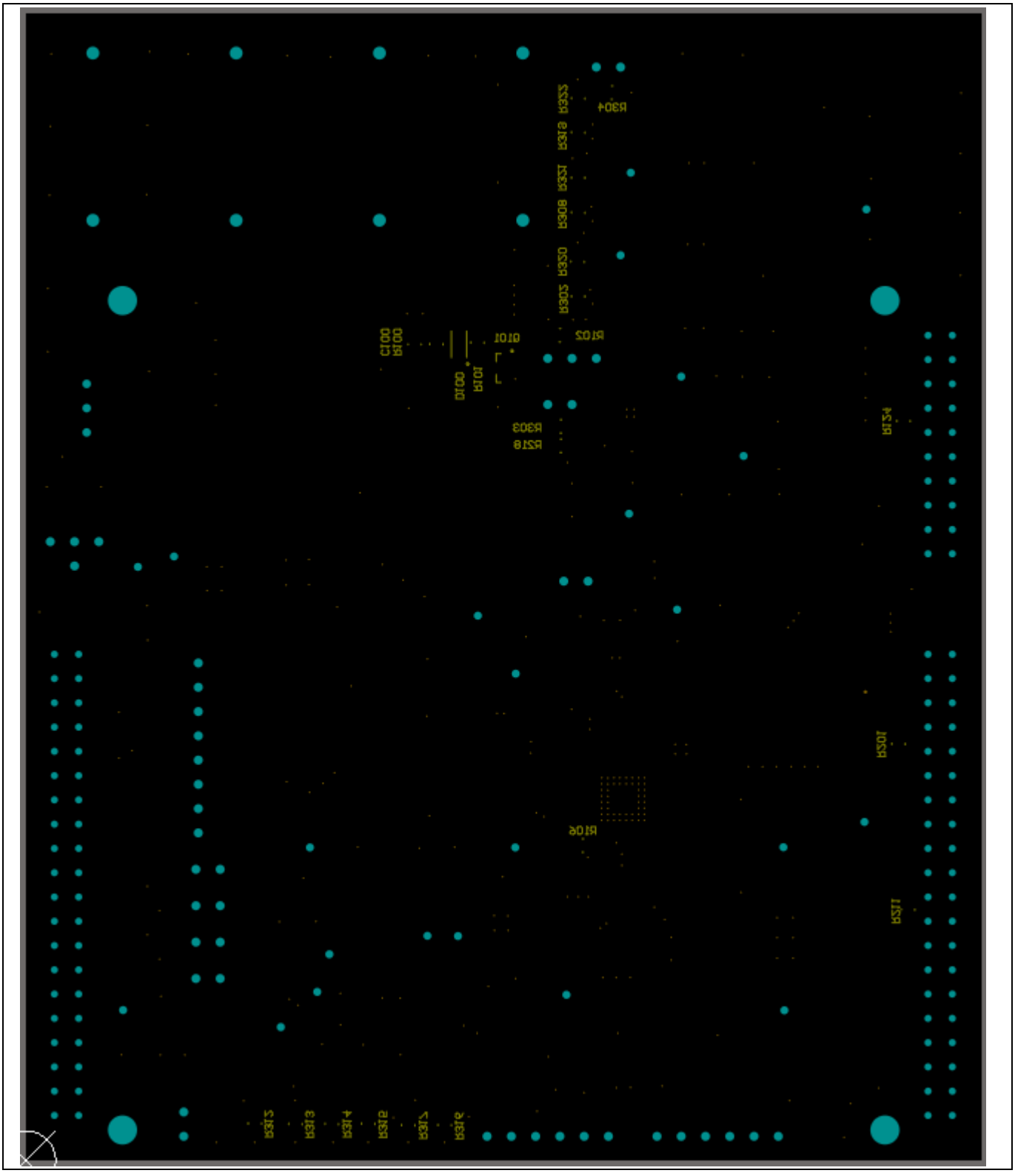

Figure 14 TLF3068x Application Board - Silkscreen Layer 4 (Bottom)

Revision history

Document version	Date of release	Description of changes
1.0	2020-05-05	Initial appnote

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