Voltage pre-regulation for Adaptive Drive Beam systems with LITIX™ TLD5501-2QV

About this document

Scope and purpose

The TLD5501-2QV is a synchronous DUAL Channel DC/DC buck controller with built in protection features and SPI interface. It can be well used as voltage pre-regulator, e.g. in headlamps supplying Adaptive Driving Beam (ADB) systems. This application note guides design engineers through the design process of the TLD5501-2QV.

Intended audience

Hardware designers

Table of contents

1 Introduction

In the automotive industry, new application scenarios for front lighting include the possibility to selectively and dynamically control the light shape and brightness of specific light functions (mainly high beam, but not only) with increasing demand for light beam resolution.

ADB is enabling many new use cases, from glare free high beam up to car to X communication (C2X) via symbols projection.

Several technologies have been analyzed in the latest years to address these new functions:

- LCD technology
- DMD technology
- Monolithic LED matrix
- Micro LED matrix

One of the most promising to maximize the efficiency with good performances in terms of light shaping and coverage of the field of view is the Micro LED matrix light sources.

Both the monolithic LED matrix and micro LED matrix technologies require a voltage pre-regulation in order to optimize the efficiency and reduce significantly the thermal losses inside the devices.

In this application note a solution to implement a pre-regulated voltage supply for monolithic LED or Micro LED light source using Infineon LITIX™ TLD5501-2QV is shown.

In the following chapters to refer to both monolithic LED and micro LED technologies the abbreviations MLM will be used.

2 System overview

For several aspects, MLM can be considered as a low voltage, high power load.

The typical supply voltage needed by a MLM device can be considered as the sum of the LED forward voltage plus the overdrive voltage required by the linear current source. Thus considering 3.5V as maximum LED forward voltage and adding typical 0.3V for the linear current source, the total voltage needed is usually less than 4V.

In automotive environment the source of power is the battery having an operative range from 8V to 18V. For these reasons a Buck DC-DC is a good choice to generate the needed power supply voltage.

The output power to be provided by the voltage pre-regulator to the MLM load is typically 60W, up to 80W in particular conditions, per headlamp. It turns out that a current up to 24A shall be provided by the voltage pre-regulator.

Depending on the number of MLM devices different approaches could be used:

- Two MLM devices with each one sinking a current up to 12A: use two independent buck DC-DC channels.
- More than two MLM devices or if the current per MLM device is higher than 15A: use a multiphase DC-DC approach.

Since the DC-DC is placed in a different ECU compared to the MLM load, the wire harness drop shall be taken into account due to the high current levels. For instance if we consider a cable with a length of 0.5 meter and a diameter of 1 millimeter, for both the power path and the ground path, a total of 30 mΩ series resistance (at 125°C) shall be taken into account during the DC-DC output voltage design.

Considering the case of having a load current up to 12A, a drop of almost 360 mV can be observed, and for this reason a DC-DC output voltage around 4.5V is a good choice to compensate the cables drop.

Another important aspect to optimize the efficiency is the capability of the voltage pre-regulator to adapt the output voltage in order to minimize the power losses into the MLM devices.

For both the proposed system approaches Infineon offers the LITIX™ TLD5501-2QV.

TLD5501-2QV is a dual channel synchronous buck DC-DC controller explicitly designed for high power applications. The two channels can work independently or in multiphase operations. It implements an SPI interface to control and retrieve the status of the DC-DC. The switching frequency is adjustable in the range of 200 kHz to 700 kHz. It can be synchronized to an external clock source. A built in programmable Spread Spectrum switching frequency modulation and the forced continuous current regulation mode improve the overall EMC behavior. Furthermore, the current mode regulation scheme provides a stable regulation loop maintained by small external compensation components. The adjustable soft start feature limits the current peak as well as voltage overshoot at start-up. The device implements the analog dimming feature that allows to further control the output voltage by adjusting the feedback error amplifier voltage reference.

Figure 1 shows a concept example for the system power supply strategy where two Micro LED matrix devices are individually supplied by a buck regulator driven by Infineon LITIX™ TLD5501-2QV.

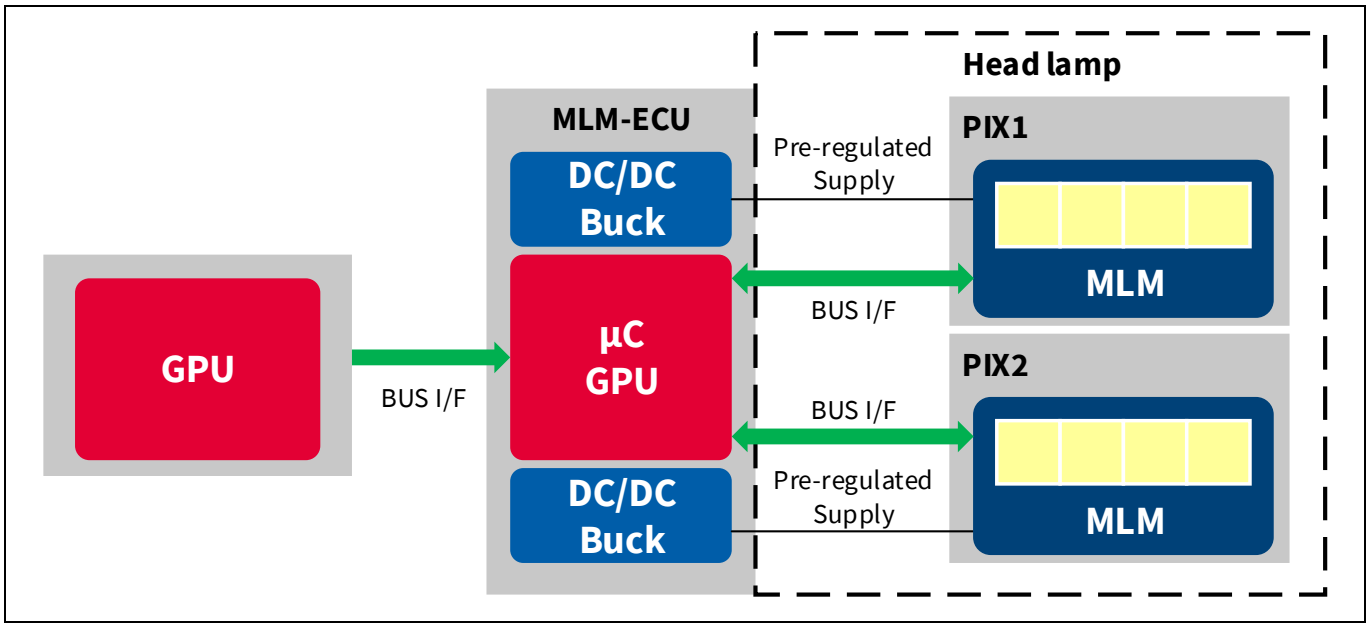

Figure 1 Automotive pixel light system architecture example: two Micro LED Matrix devices

Figure 2 shows a concept example for the system power supply strategy where three Monolithic LED matrix devices are supplied by a multiphase buck regulator driven by Infineon LITIX™ TLD5501-2QV.

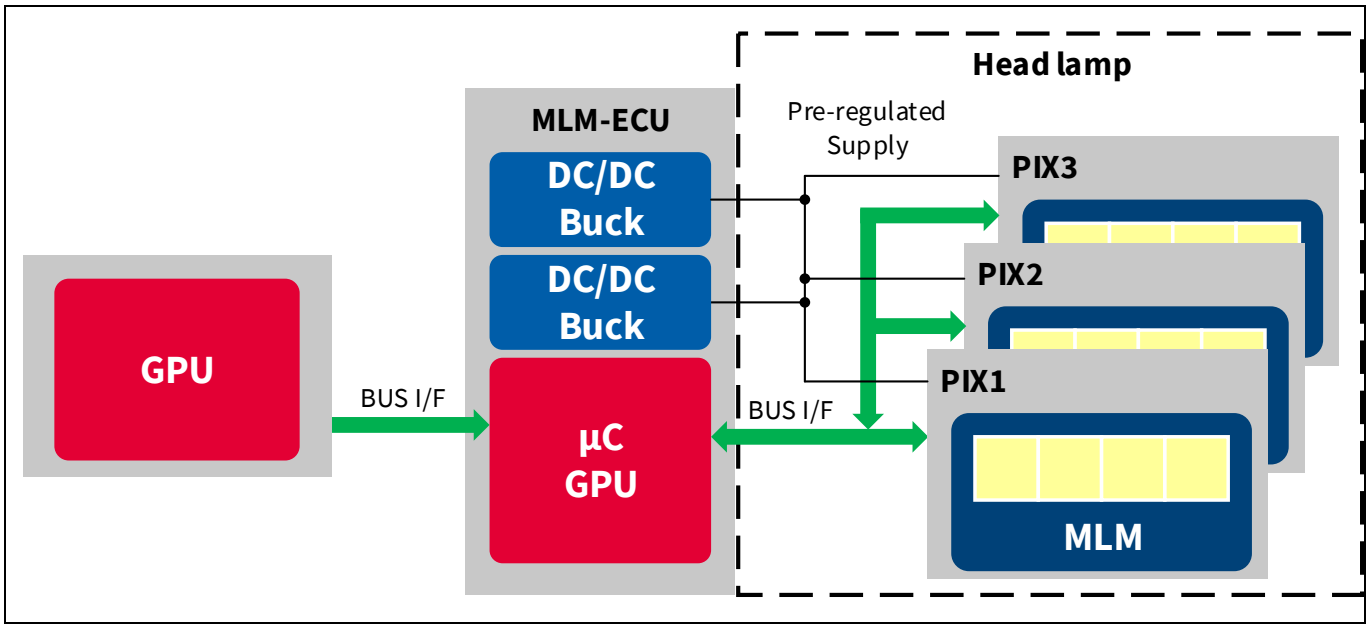

Figure 2 Automotive pixel light system architecture example: three Monolithic LED matrix devices

2.1 Buck DC-DC converter

Buck topology is one of the simplest academic examples of DC-DC converters. It is used when there is the need to step down the input voltage to a regulated output one.

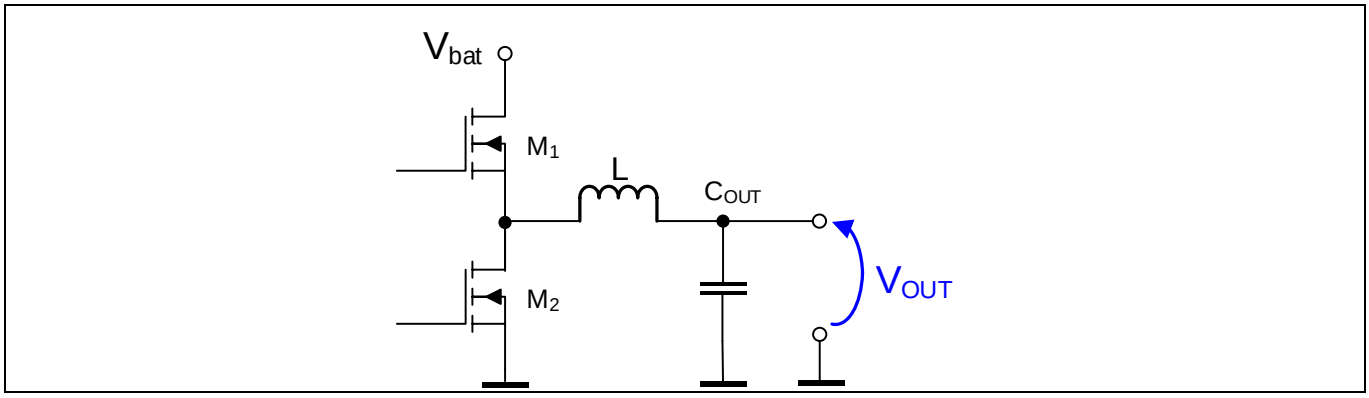

Figure 3 Synchronous BUCK DC-DC block diagram

Figure 3 depicts a block diagram describing the buck converter topology. It consists of an inductor L, two power MOSFETs M_1 and M_2 and an output capacitor C_{OUT}.

The Buck is a step down DC-DC converter topology that provides a positive regulated output voltage from V_{bat}. This means that the output voltage can be below the input voltage.

2.2 Buck operation

To understand the behavior of the topology the circuitry in continuous conduction mode (CCM) will be analyzed. Figure 4 shows the powering phase of the DC-DC converter: the primary switch M_1 is ON and M_2 on the secondary side is OFF for a time window "t_{ON}". The voltage on the inductor L is equal to the difference between the input voltage V_{bat} and the output voltage V_{OUT}, with the consequence of a linear increase of the inductor current I_L from the initial value I_{LMIN}:

$$I_L = I_{LMIN} + \frac{V_{bat} - V_{OUT}}{\mathrm{L}} \cdot t$$

The inductor current variation is defined then by:

$$\Delta_{ILON} = I_{LMAX} - I_{LMIN} = \frac{V_{bat} - V_{OUT}}{\mathrm{L}} \cdot t_{ON}$$

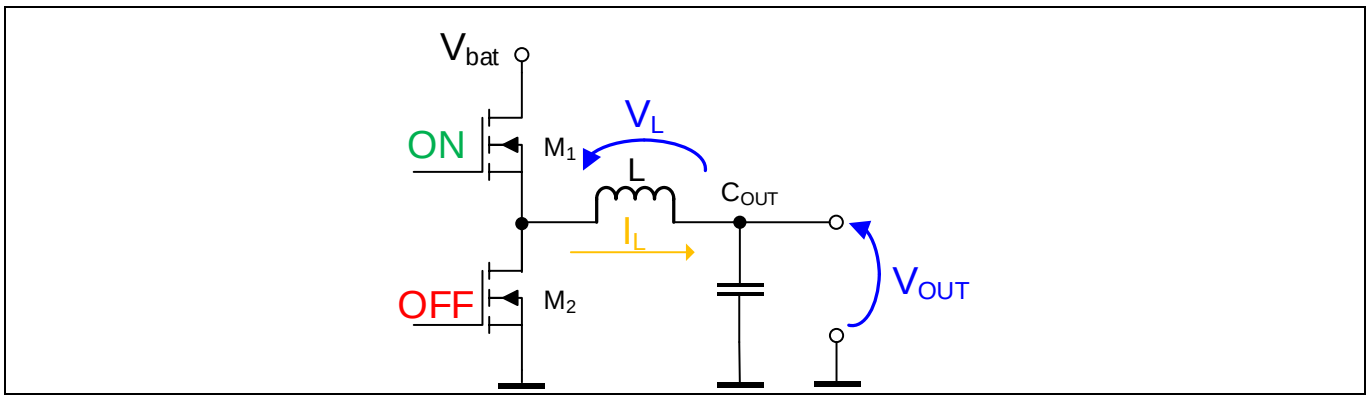

Figure 4 Buck Operation during powering phase

In Figure 5 it is shown the freewheeling phase of the DC-DC converter: the primary switch M_1 is OFF and M_2 is ON for a time window "t_{OFF}". During this phase the energy stored on the inductor L is transferred to the output

capacitor C_{OUT} and to the load. The voltage on the inductor L is equal to $-V_{OUT}$, with the consequence of a linear decrease of the inductor current I_L from the initial value I_{LMAX}:

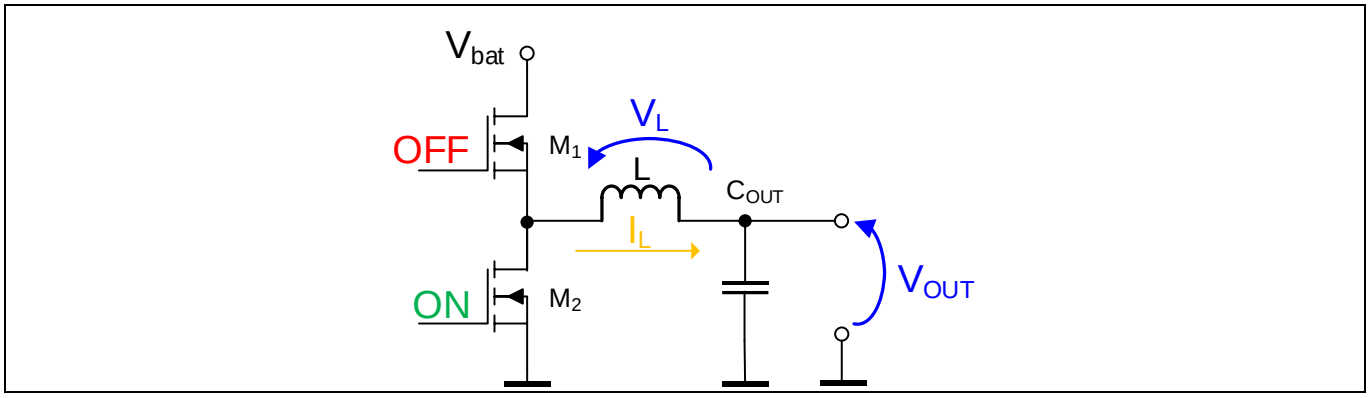

Figure 5 Buck Operation during freewheeling phase

$$I_L = I_{LMAX} - \frac{V_{OUT}}{\mathrm{L}} \cdot t$$

The inductor current variation is defined then by:

$$\Delta_{ILOFF} = I_{LMAX} - I_{LMIN} = \frac{V_{OUT}}{\mathrm{L}} \cdot t_{OFF}$$

Considering that in steady state the variation of the inductor current are equal during the powering phase and the freewheeling phase we obtain the following equation:

$$\Delta_{ILON} = \Delta_{ILOFF} = \Delta_{IL} = \frac{V_{bat} - V_{OUT}}{\mathrm{L}} \cdot t_{ON} = \frac{V_{OUT}}{\mathrm{L}} \cdot t_{OFF}$$

Assuming an ideal Buck converter without losses, and considering that $t_{OFF} = T_S - t_{ON}$, where T_S is the switching period, the duty cycle (D) in CCM can be calculated using the following equation:

$$V_{OUT} = \frac{t_{ON}}{T_S} \cdot V_{bat} = \mathrm{D} \cdot V_{bat}$$

Figure 6 shows the behavior of the voltages and currents across all the components over a few switching cycles.

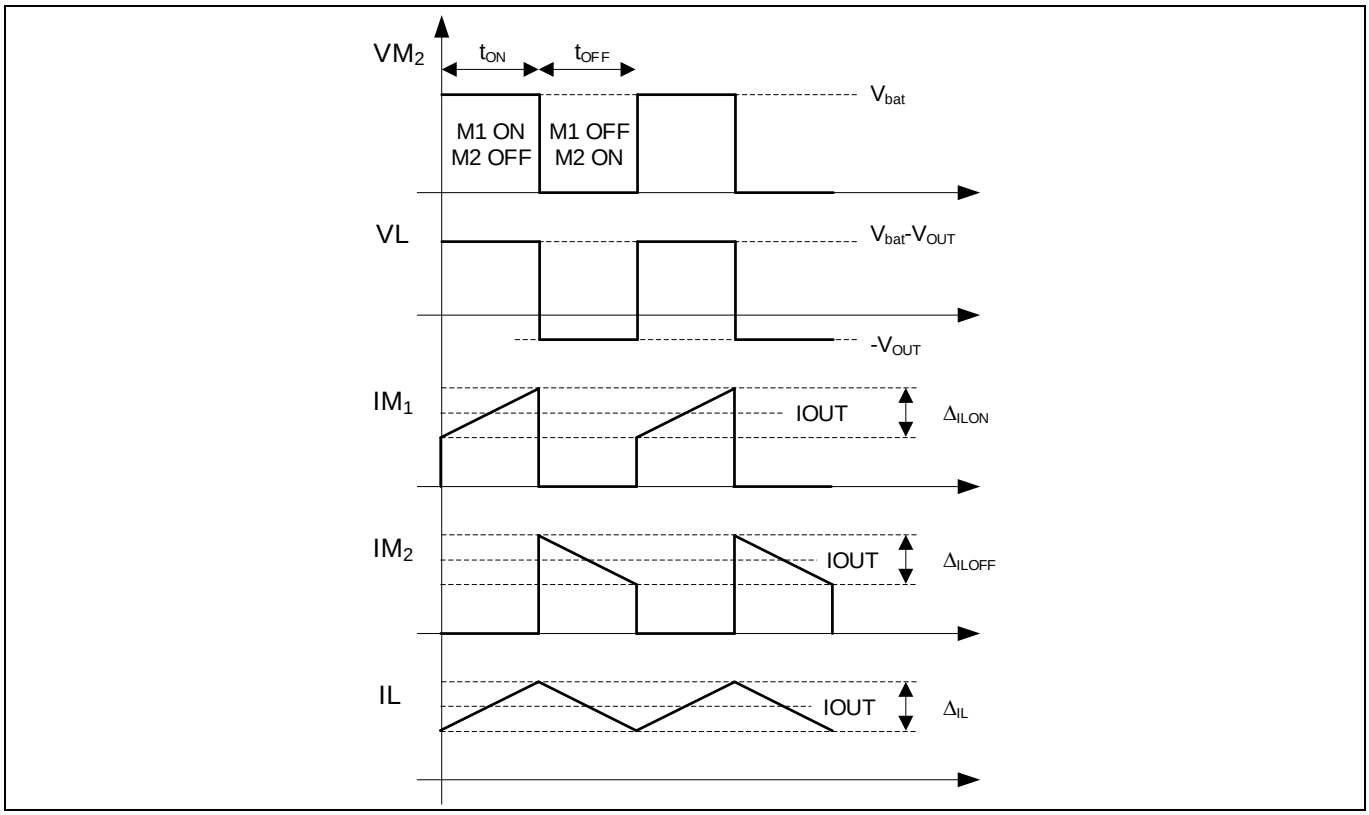

Figure 6 Buck voltage and current behaviors

It has been shown that by controlling properly the duty cycle (D) it is possible to generate a regulated output voltage V_{OUT} from the input voltage V_{bat}. In the next chapters an example of DC-DC design using the Infineon LITIX™ TLD5501-2QV controller will be shown.

3 Voltage pre-regulator design with LITIX™ TLD5501-2QV

3.1 Application example

In this application note a voltage pre-regulator for two MLMs devices is considered, like the system described in Figure 1, with the following requirements:

Table 1 Voltage pre regulator example

Output voltage	Typical 4.5 V
Output voltage ripple	+/- 1%
Output current	Max 12 A per MLM device
Load step overshoot	Max 10% @ 12A load current step
DC-DC Switching Frequency	400KHz
Input voltage supply	8 - 18 V functional range Max 26 V during jump start
EMC requirements	CISPR class V

Each channel of the TLD5501-2QV is used to supply one MLM device like shown in Figure 7.

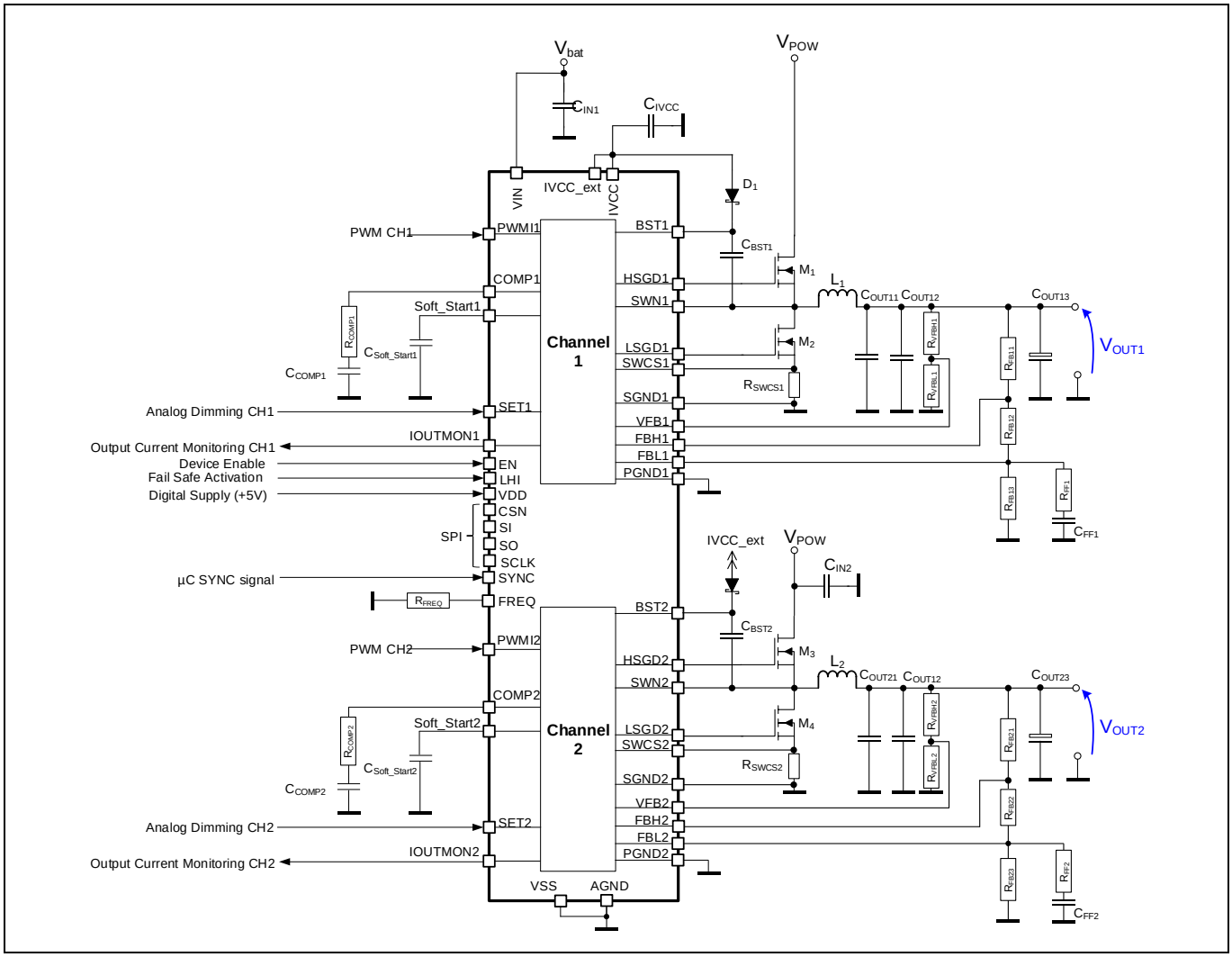

Figure 7 Application diagram of TLD5501-2QV as buck voltage regulator

3.2 Main regulator design

The required output voltage is 4.5V. The duty cycle (D) of the DC/DC regulator is a function of input and output voltage. Supposing a 90% of overall efficiency η, the formula for a buck converter is:

$$V_{OUT} = \mathrm{D} \cdot V_{bat} \cdot \eta$$

DC varies with the battery voltage and its limits are reported in Table 2.

Table 2 Duty cycle vs. input voltage

Input voltage V_{IN} [V]	Duty cycle [%]
8 V (maximum Duty cycle) Transient undervoltage	62.5 %
13.5 V (typical condition) Nominal battery	37 %
26 V (minimum Duty cycle) Jump start	19.2 %

3.2.1 Inductor

The inductor in a buck converter is selected by fixing a certain ratio between average current and ripple current $\Delta i_{L\_TYP(P-P)}$ (as peak to peak measurement) in typical condition. Usually, the peak to peak current is in the range of 20% to 40% of the average value (in this application 30% has been chosen). Since TLD5501-2QV is a synchronous buck controller with forced CCM, the CCM is granted for any selected inductor value.

The following equation determines the inductor value to obtain the required ripple current with typical voltage at input.

$$L_{MIN} \geq D_{TYP} \cdot \frac{V_{bat\_TYP} - V_{OUT}}{\Delta i_{L_{TYP(P-P)}} \cdot f_{sw}} = 0.37 \cdot \frac{13.5\ V - 4.5\ V}{0.3 \cdot 12\ A \cdot 400\ kHz} = 2.31\ \mu H$$

The closest standard value that satisfies the equation is 3.3 µH.

With this value, the actual peak to peak current in worst condition (i.e. when input voltage is at maximum) can be calculated as:

$$\Delta_{IL\_MAX} = D_{MIN} \cdot \frac{V_{bat_{MAX}} - V_{OUT}}{L \cdot f_{sw}} = 0.192 \cdot \frac{26\ V - 4.5\ V}{3.3\ \mu H \cdot 400\ kHz} = 3.13\ A$$

And then, the maximum peak current into inductor is:

$$I_{L-MAX} = I_{OUT} + \frac{\Delta i_{L(P-P)}}{2} = 12\ A + 1.565\ A = 13.565\ A$$

The important key parameters to select an inductor are then:

- Inductance ≥ 3.3 µH
- Saturation current > 13.565 A

An inductor that fulfills the above requirements (nominal inductor value and saturation current) is the Coilcraft XAL7070-332ME.

3.3 Output capacitor

Output capacitor affects the bandwidth of the system and also the output current ripple performance. In steady state the average current into the output capacitor is null. Usually, for this kind of application multilayer ceramic capacitors (MLCC) with low ESR are preferred over electrolytic capacitors.

The waveforms of the current and voltage across the output capacitor are reported in Figure 8.

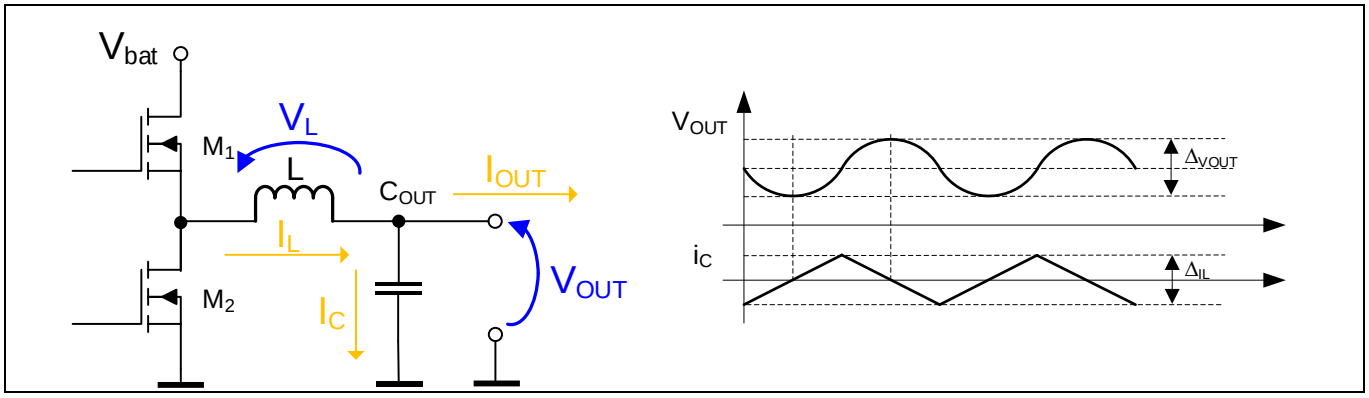

Figure 8 Waveform of output voltage ripple and output capacitor current

The output voltage ripple is defined by:

$$\Delta V_{OUT} = \frac{1}{C_{OUT}} \int i_C \, dt = \frac{\Delta_{IL}}{8 \cdot f_{sw} \cdot C_{OUT}}$$

The requirement is to have $\Delta V_{OUT} < 90$ mV. This implies that:

$$C_{OUT} \geq \frac{\Delta_{IL\_MAX}}{8 \cdot f_{sw} \cdot \Delta V_{OUT}} = \frac{3.13\ A}{8 \cdot 400\ KHz \cdot 90\ mV} = 10.86\ \mu F$$

Another important aspect of the output capacitor design is to consider the output transient response to a load step. The output voltage deviation is given by the time the inductor takes to adapt to the increased or reduced output current needs.

The following formula can be used to calculate the necessary output capacitance for a desired maximum voltage overshoot:

$$C_{OUT} \geq \frac{{\Delta_{IOUT}}^2 \cdot \mathrm{L}}{2 \cdot V_{OUT} \cdot V_{OS}}$$

It implies that with the described application assumptions we obtain:

$$C_{OUT} \geq \frac{{\Delta_{IOUT}}^2 \cdot \mathrm{L}}{2 \cdot V_{OUT} \cdot V_{OS}} = \frac{(12\ A)^2 \cdot 3.3\ \mu H}{2 \cdot 4.5\ V \cdot 450\ mV} = 117\ \mu F$$

From this equation is evident that the output capacitor design is driven by the load step response. A capacitor of 120 µF is then considered.

Also the equivalent series resistor (ESR) of the capacitor affects the ripple of the output voltage:

$$\Delta V_{ESR} = R_{ESR} \cdot I_C = \frac{\Delta_{IL} \cdot {R_{ESR}}^2 \cdot C_{OUT}}{2} \cdot \frac{f_{sw}}{D \cdot (1 - D)}$$

To make it negligible we consider a contribution of 20% of the ΔV_{OUT}. From the equations above, it is possible to calculate the maximum ESR acceptable by the application.

$$R_{ESR} \leq \sqrt{\frac{2 \cdot 0.2 \cdot \Delta V_{OUT} \cdot D_{MIN} \cdot (1 - D_{MIN})}{\Delta_{IL_{MAX}} \cdot f_{sw} \cdot C_{OUT}}} = \sqrt{\frac{2 \cdot 0.2 \cdot 90\,mV \cdot 0.192 \cdot (1 - 0.192)}{3.13\,A \cdot 400\,KHz \cdot 120\,\mu F}} = 6.1\,m\Omega$$

To fulfil the equation, the ESR of the used capacitors bank has to be lower than 6.1 mΩ which is a reasonable value for several ceramic capacitors put in parallel.

Note: MLCC capacitors show quite good value of capacitance related to small package and also very good performances related to ESR, but they show a variation of the capacitance as a function of the applied voltage. During the selection take into account this degradation and in such a case, use an adequate parallel of capacitors to overcome this drawback.

As an example, in Figure 9 the behavior of TDK C2012JB1H475K125AB is shown.

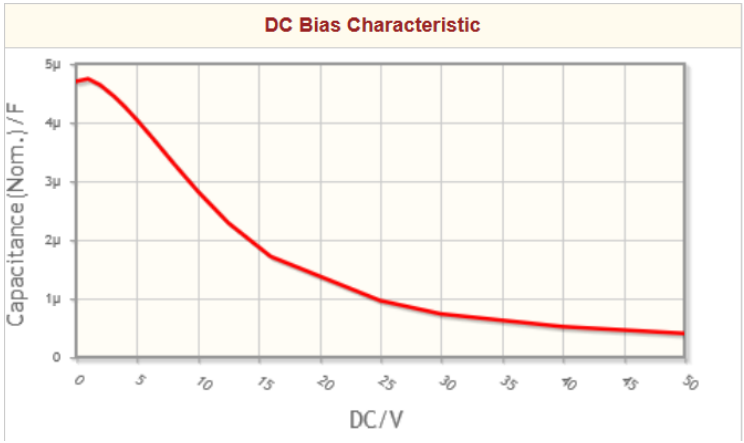

Figure 9 DC bias characteristic of TDK C2012JB1H475K125AB

For the application described in this document, a good choice is the paralleling of five MLCC 4.7 µF capacitors plus a 100 µF electrolytic capacitor at the output of the buck converter.

3.4 Input PI filter

A PI filter is a common choice for filtering undesired frequency components within the spectrum in the required bands.

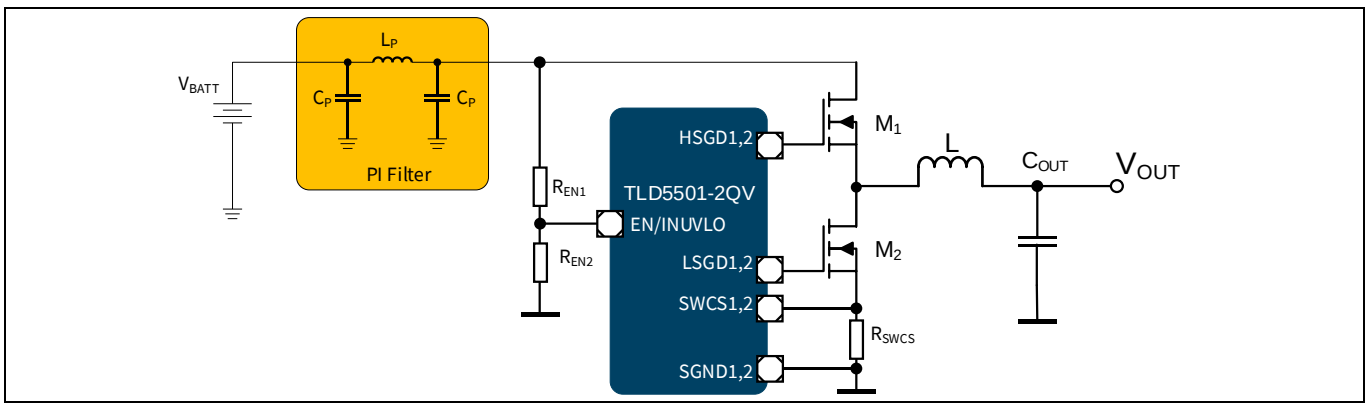

Figure 10 PI filter schematic simplified

Parasitic of capacitors and inductor shape the high frequency response of the PI filter and it works fine up to 5-10 MHz. Above this frequency fast transients on MOSFET dominate the emissions. To mitigate this effect a good PCB layout helps a lot.

To achieve good results the damping zone of the filter has to be put where harmonics of switching frequency cause problems in the AM band (500 kHz – 1.8 MHz).

To design the PI filter, the following rules of thumb can be used:

- Select L_p in the range of 1 µH to 10 µH: 1 µH is selected
- Put the corner frequency of PI filter 1/10 of the switching frequency of DC-DC: $f_{PI} = 0.1 * f_{SW} = 40$ kHz
- Have equal capacitance distribution on both sides of PI-Filter and value

$$C_P = \frac{1}{4 \cdot \pi^2 \cdot L_P \cdot f_P^2} = \frac{1}{4 \cdot \pi^2 \cdot 1\ \mu H \cdot (40\ kHz)^2} = 16\ \mu F$$

Then, for each side of PI filter at least 16 µF is needed; a possible choice is to have 3 capacitors of 10 µF (due to reduction of value at nominal battery value) that minimize parasitic effects.

For this purpose CGA5L3X5R1H106M160AB is a good candidate for the capacitors while the inductor could be Coilcraft XEL4020-331ME

3.5 Transistors

NMOS type devices are used as switching elements of the proposed DC/DC. The switching behavior is depicted in Figure 6.

The average current of the NMOS M_1 is equal to the input average current and can be estimated using the formulas below:

$$< I_{IN\_MAX} >=< I_{M1\_MAX} >= \frac{P_{OUT}}{V_{bat\_MIN} \cdot \eta} = \frac{V_{OUT} \cdot I_{OUT}}{V_{bat\_MIN} \cdot \eta} = D_{MAX} \cdot I_{OUT} = 0.625 \cdot 12\ A = 7.5\ A$$

On the same way we can also calculate the average current of the NMOS M_2 using the following formula:

$$< I_{M2\_MAX} >= (1 - D_{MIN}) \cdot I_{OUT} = (1 - 0.192) \cdot 12\ A = 9.7\ A$$

During the switching activity NMOS M_1 is also stressed by the voltage equal to the input voltage V_{bat} while the voltage drop on NMOS M_2 is negligible.

For EMI reason, it is common practice to put in series a resistor (R_{gate}) of approximately 5 to 15 Ω. This helps in reducing the current spikes at the gate and also having smooth transitions from OFF state to ON state. On the other hand, this lowers the overall efficiency of the converter.

Infineon offers a wide variety of MOSFET suitable for this purpose; the IAUC100N04S6L025 is a good compromise of gate charge and R_{ds_on} for this application.

3.6 Inductor current sense resistor

There are still a few components impacting the behavior of the main regulation loop.

One of them is the resistor limiting the current into the switching NMOS and inductor. It is placed below the transistor M_2 (please refer to Figure 11) and improves the stability (current mode control loop). This resistor converts the current flowing into the transistor in a voltage sensed by SWCS1,2 pins. The maximum voltage across the resistor must not reach the V_{SWCS} threshold of -50 mV neither in steady state nor in transition phases.

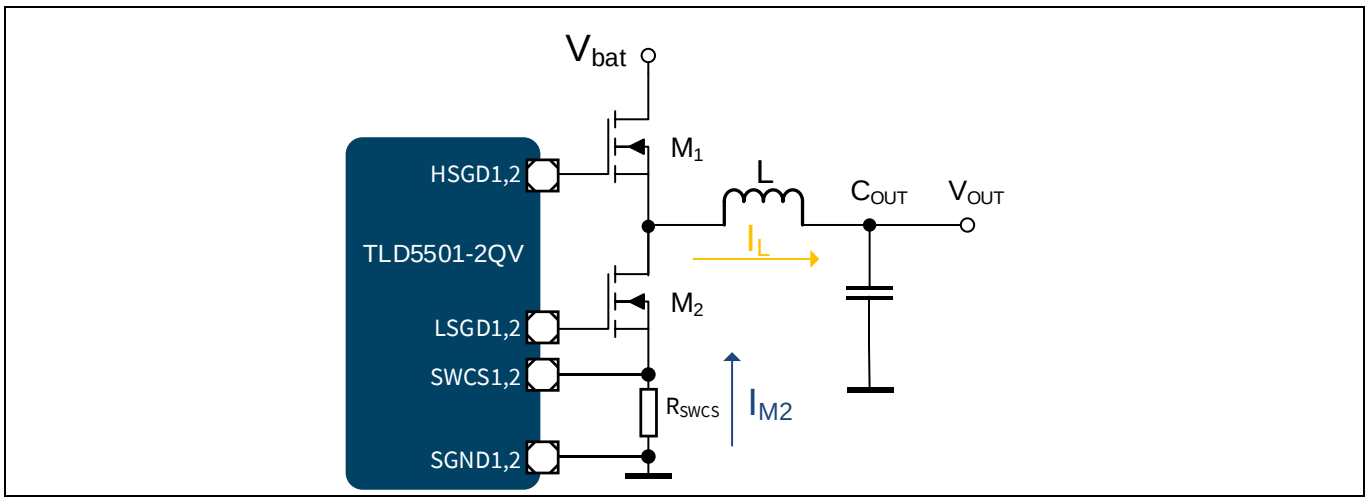

Figure 11 Peak current sensing resistor

For example, with a system phase margin of 46°, the output current has an overshoot of about 50%. It affects also the input current and switching current too. Taking into account the corner case with minimum V_{IN}, the maximum current through R_{SWCS} is calculated with the following equation

$$R_{swcs} < \frac{V_{SWCS}}{1.5 \cdot I_{L\_MAX}} = \frac{50\ mV}{1.5 \cdot 13.565\ A} = 2.46\ m\Omega$$

A safety margin of 2 mΩ is a good choice.

The RMS current flowing into the resistor is equal to the current flowing into power NMOS M_2. The following formula can be used to calculate the RMS current:

$$I_{Rswcs_{rms},max} = \sqrt{\frac{t_{OFF}}{3T_{sw}}\left(I_{L\_min}^2 + I_{L\_min} \cdot I_{L\_max} + I_{L\_max}^2\right)}$$
$$= \sqrt{\frac{(1 - D_{MIN})}{3}\left((10.435\ A)^2 + 10.435\ A \cdot 13.565\ A + (13.565\ A)^2\right)} = 10.82\ A$$

Then the power dissipated by the resistor is

$$P = R_{swcs} \cdot {I_{Rswcs_{rms},max}}^2 = 2\ m\Omega \cdot (10.82\ A)^2 = 234.1\ mW$$

To avoid overheating of the resistor it is a common practice to use resistors with a rating 4 times higher than the required power. For this application a low inductive component has to be chosen. The WSL25122L000FEA from Vishay satisfies the requirements.

3.7 Output voltage sense resistors and Analog Dimming

The output voltage is sensed via a resistor divider as shown in Figure 12. The proper design of these resistors has the target to set the needed output voltage.

Another important aspect to optimize the efficiency is the capability of the voltage pre-regulator to adapt the output voltage in order to minimize the power losses into the MLM devices.

The TLD5501-2QV has the analog dimming feature in order to adapt the output voltage: it is a programmable 8-bit register to adjust the internal reference of the devices to control the output voltage (see Figure 13).

Considering to set $R_{FB11,2}$ to zero, the V_{OUT} can be calculated using the following equation:

$$V_{OUT1,2} = \left(\frac{V_{FBH1,2-FBL1,2}}{R_{FB21,2}} - I_{FBL1,2}\right) \cdot R_{FB31,2} + V_{FBH1,2-FBL1,2}$$

In order to allow the capability to increase the output voltage with the analog dimming feature, it is suggested to set the nominal 4.5V output voltage regulation for 90% of analog dimming value:

$$V_{FBH} - V_{FBL} = 0.9 \cdot 150mV = 135mV$$

It turns out that the output voltage at 90% of analog dimming capability is set then by:

$$V_{OUT1,2} = \left(\frac{135mV}{R_{FB21,2}} - I_{FBL}\right) \cdot R_{FB31,2} + 135mV$$

I_{FBL} in case of high side current sensing has a typical value of 30µA.

By selecting $R_{FB21,2}$ = 120 ohm and $R_{FB31,2}$ = 4.02K ohm, VOUT is equal to 4.537V at 90% of analog dimming.

$V_{OUT1,2}$ can be increased up to 5.05V at 100% of analog dimming and can be decrease down to 2.47V at 50% of analog dimming.

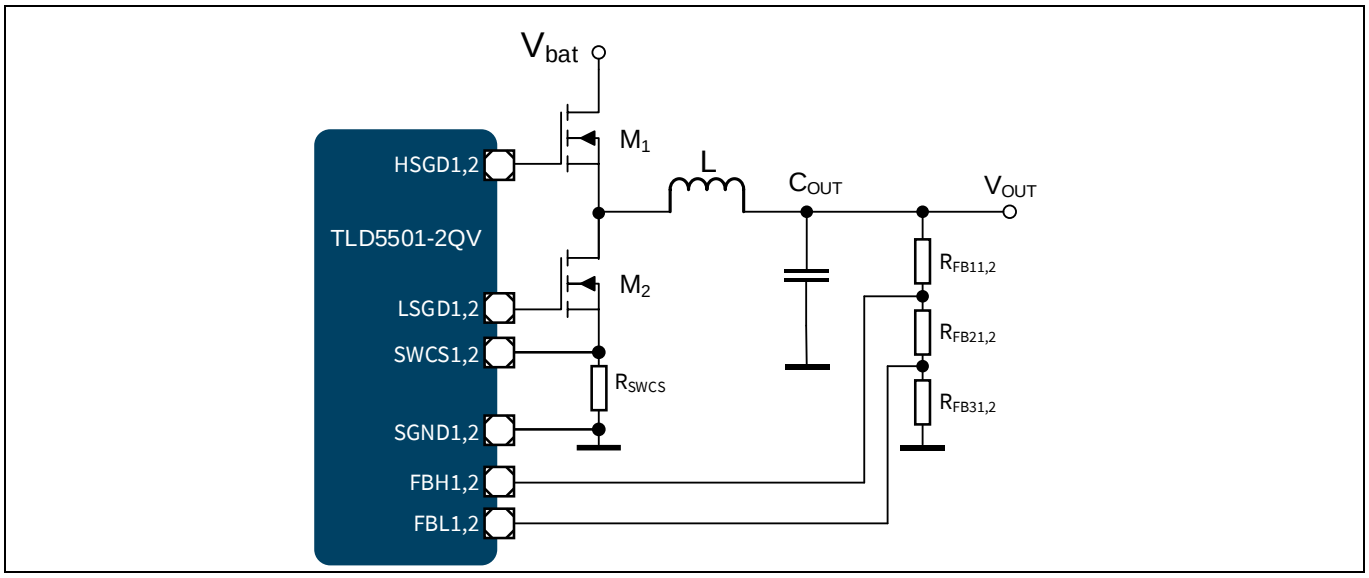

Figure 12 Output voltage sensing resistors

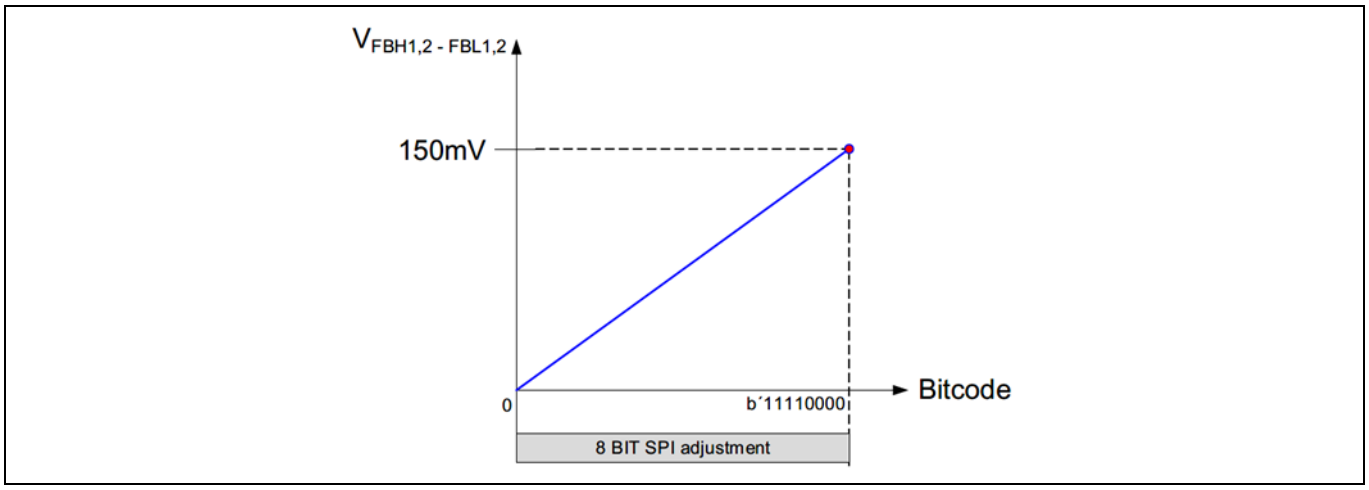

Figure 13 TLD5501-2QV analog dimming overview

3.8 Input undervoltage protection

The TLD5501-2QV offers input undervoltage protection. The threshold value is set by the voltage divider applied on the EN/INUVLO pin like illustrated in Figure 14.

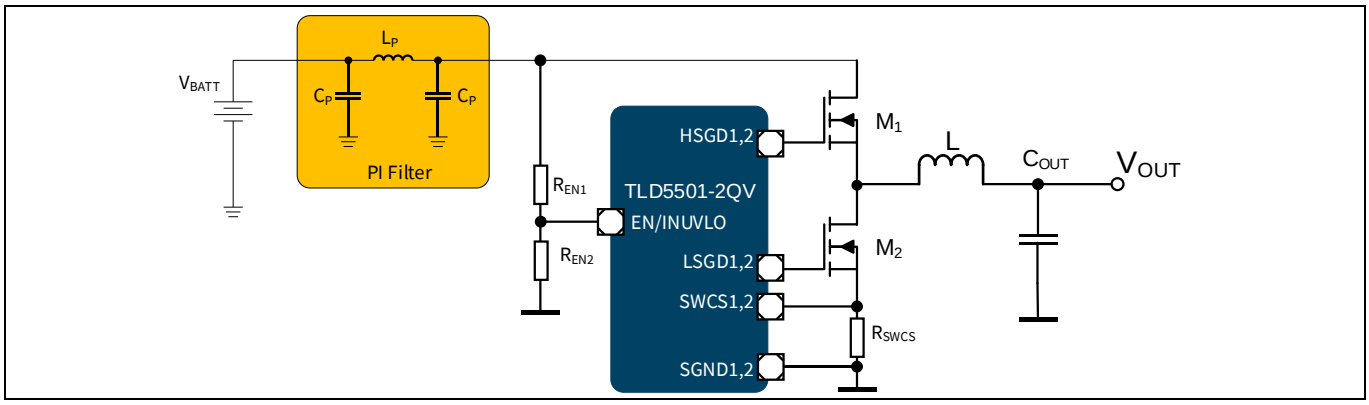

Figure 14 Input voltage monitor resistor divider - EN/INUVLO

The input undervoltage threshold is defined by the following equation:

$$V_{INUVLO} = \frac{R_{EN1} + R_{EN2}}{R_{EN2}} \cdot V_{EN/INUVLOth}$$

The required functional V_{IN} range is 8 V – 26 V and therefore the input undervoltage (V_{UVset}) is set to 5.5 V. For $V_{IN} \leq 5.5$ V the device is put into “sleep” mode with very low power consumption and all the registers content is reset and all the outputs are off.

$$R_{EN1} = \left(\frac{V_{INUVLO}}{V_{EN/INUVLOth}} - 1\right) \cdot R_{EN2} = \left(\frac{5.5\ V}{1.9\ V} - 1\right) \cdot R_{EN2} = 1.89 \cdot R_{EN2}$$

The suggested values are:

R_{EN1} = 22 kΩ

R_{EN2} = 12 kΩ

3.9 Output overvoltage and short to ground (S2G) protections

In the TLD5501-2QV both the output overvoltage and S2G protections are set via the VFB pin as illustrated in Figure 15.

Usually the MLM devices are low voltage devices, for this reason they need to be protected from any overvoltage conditions from the supply. Assuming a 5V technology for the MLM device, it is suggested to set the output overvoltage threshold to 5.5 V.

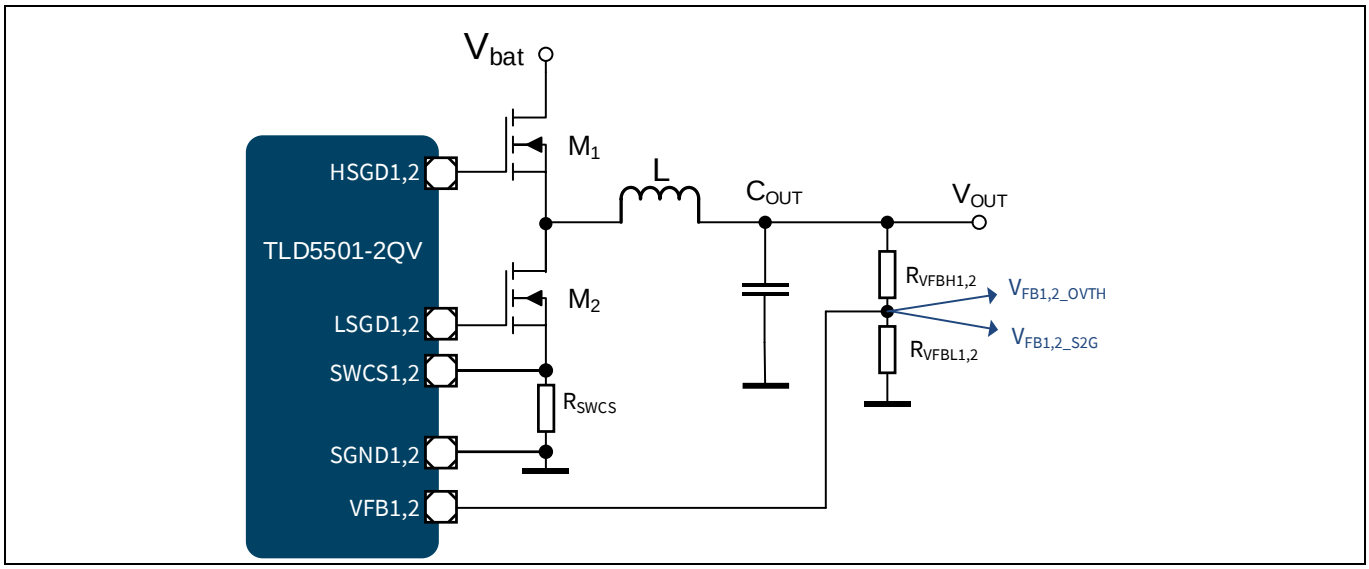

Figure 15 VFB resistor divider

The overvoltage threshold is set using the following equation:

$$V_{OUT1,2\_OV} = V_{FB1,2\_OVTH} \cdot \frac{R_{VFBH1,2} + R_{VFBL1,2}}{R_{VFBL1,2}}$$

$$R_{VFBH1,2} = \left(\frac{V_{OUT1,2\_OV}}{V_{FB1,2\_OVTH}} - 1\right) \cdot R_{VFBL1,2} = \left(\frac{5.5\ V}{1.46\ V} - 1\right) \cdot R_{VFBL1,2} = 2.77 \cdot R_{VFBL1,2}$$

So the proposed values for the resistor divider on VFB are:

$R_{VFBL1,2}$ = 1.69 kΩ

$R_{VFBH1,2}$ = 4.7 kΩ

Considering the accuracy on the $V_{FB1,2\_OVTH}$ threshold it turn outs that the maximum overvoltage threshold is set to 5.67 V. It is suggested to check the maximum absolute ratings of the MLM device to avoid any disruptive scenario.

With the suggested resistors sizing the default output short to ground (S2G) threshold is set to:

$$V_{OUT1,2\_S2G} = V_{FB1,2\_S2G} \cdot \frac{R_{VFBH1,2} + R_{VFBL1,2}}{R_{VFBL1,2}} = 0.091\ V \cdot \frac{1.69\ K\Omega + 4.7\ K\Omega}{1.69\ K\Omega} = 0.344\ V$$

It is possible to change the S2G threshold by changing the $V_{FB1,2\_S2G}$ parameter using the LEDCHAIN_CH1,2 bits in the MFSSETUP1_CH1,2 SPI register.

4 Supply stability at MLM during load steps transients

In a system based on MLM devices another important parameter is the load regulation: it is the capability of the voltage regulator to keep the output voltage stable (within a desired tolerance) despite load current changes. In these systems a simultaneous switch ON or OFF of many pixels at the same time can induce a huge load current step up to 12A.

In literature the load regulation is defined as the maximum supply variation for a given load change:

$$LR(V_{supply}) \stackrel{\text{def}}{=} V_{supply(max)} - V_{supply(min)}$$

If we consider the MLM system as described in Figure 1 we can observe that the MLM devices are connected to the buck DC-DC voltage regulator via a wire harness.

The application assumption is to have a wire harness of a length of 50 cm and a diameter of 1mm. Then we have to consider the following parasitic parameters:

Supply cable resistance [mΩ]	GND cable resistance [mΩ]	Total cable resistance [mΩ]
15	15	30
Supply cable inductance [µH]	GND cable inductance [µH]	Total cable inductance [µH]
0.65	0.65	1.3

The cable resistance is causing a supply static drop due by the current flowing into the wire. In addition, the load step transient is causing the highest source of supply variation, and then it should be properly taken into account for the local filter dimensions.

If no margin are taken, a supply drop due to a load step can induce to a temporary LED current decrease.

Figure 16 shows a simplified but effective model to consider the dynamic effects of a load step.

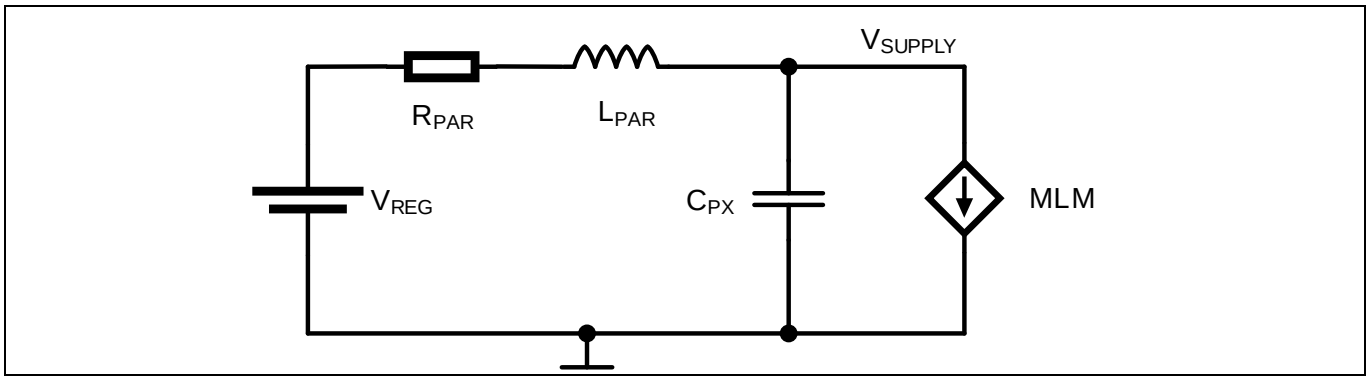

Figure 16 Supply network simplified model for the evaluation of the step response transient

Where V_{REG} is the supply voltage from the pre regulator (including local filtering), R_{PAR} and L_{PAR} the wire harness equivalent parasitic components and C_{PX} the MLM local filter capacitance. The resulting simplified RCL network is then easy to analyze.

An instantaneous load step ΔI_L will likely cause at V_{SUPPLY} a static drop due to R_{PAR} and a damped oscillation in case that the under-damping condition is verified:

$$\frac{R_{PAR}}{2 \cdot L_{PAR}} \ll \frac{1}{\sqrt{L_{PAR} \cdot C_{PX}}}$$

At V_{SUPPLY} the damped oscillation has maximum theoretical amplitude

$$\Delta V_{SUPPLY} \leq \Delta I_L \cdot \sqrt{\frac{L_{PAR}}{C_{PX}}} + R_{PAR} \cdot \Delta I_L$$

This equation is a very good starting point to dimension the right filter capacitance close to V_{SUPPLY} pins. The static drop is already taken into account via increasing the output voltage. Assuming 0.7V maximum supply cable drop the filter capacitor has to be:

$$C_{PX} \geq \frac{L_{PAR}}{\left(\frac{\Delta V_{SUPPLY(max)}}{\Delta I_L}\right)^2} = \frac{1.3\ \mu\text{H}}{\left(\frac{0.7\ \text{V}}{12\ \text{A}}\right)^2} = 382\mu F$$

Then 400 µF are suggested as filter capacitor on the MLM device.

It's important to notice that the static drop over the parasitic resistance is not negligible (≈360 mV), and needs to be considered in the undershoot case (when a positive load step happens). On the other hand, a high-ohmic value in the series path makes the supply network over-dumped with the implication to reduce the dynamic overshoot.

Figure 17 and Figure 18 show the V_{SUPPLY} drop as a function of the filter capacitance in case of positive or negative load steps.

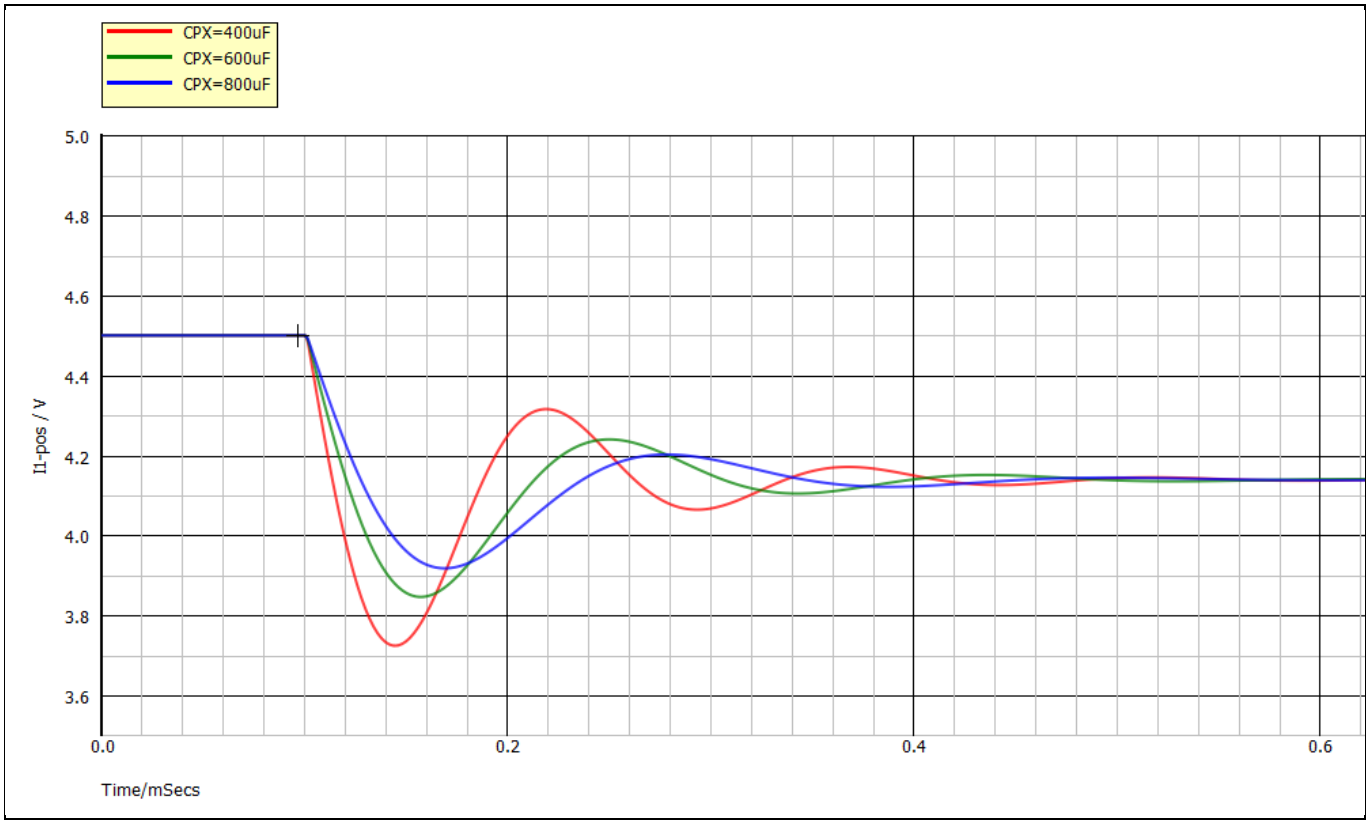

Figure 17 V_{SUPPLY} diagram load step of +12A and filter capacitance C_{PX}=400, 600 and 800uF

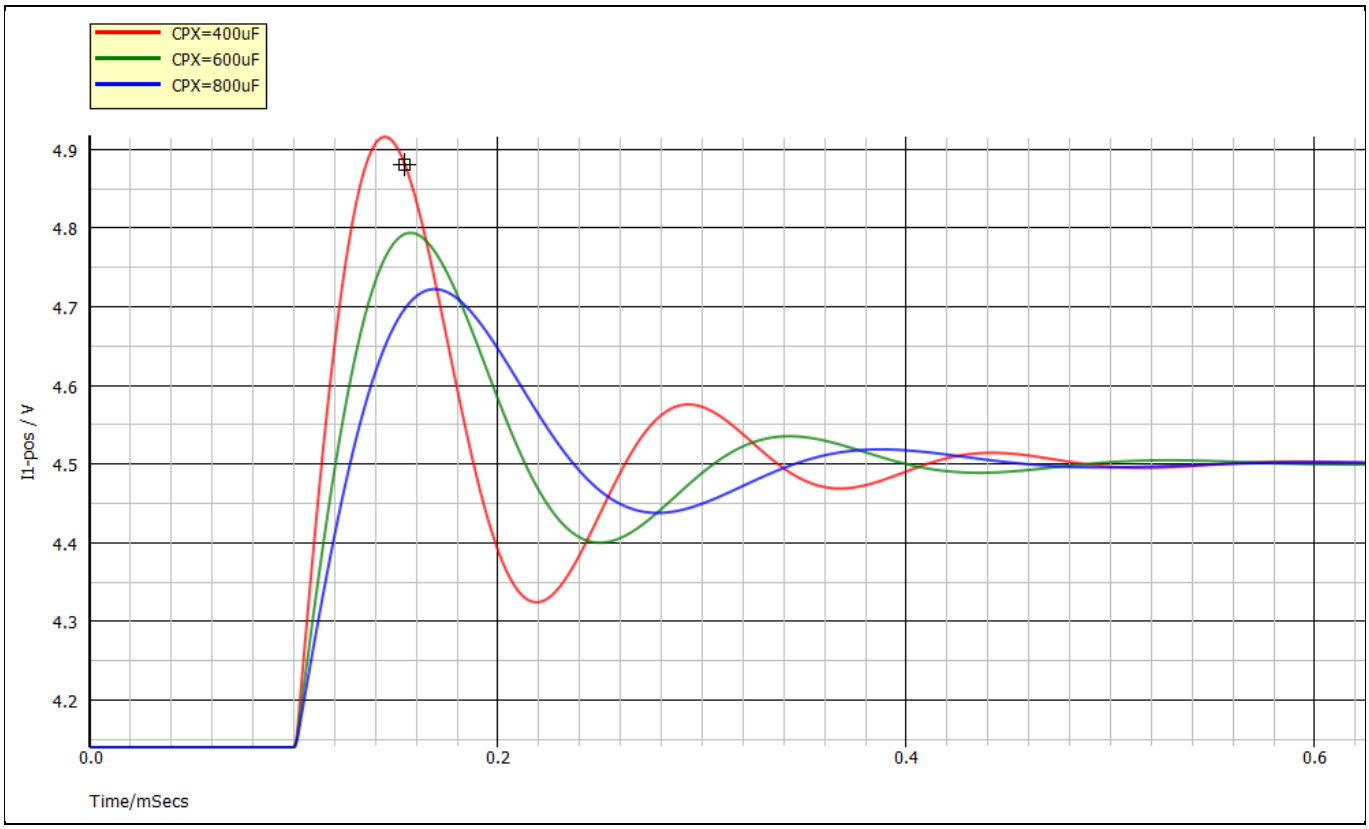

Figure 18 V_{SUPPLY} diagram load step of -12A and filter capacitance C_{PX}=400, 600 and 800uF

The above diagram also highlight a potential risk with using low capacitance filters: the voltage overshoot in the supply due to sudden load drop may result above MLM max ratings (e.g. 5.5V) and temporary or permanently damage the device. If this risk is considered too high (as high supply voltages, close to max ratings, are expected to be used) and the filter value cannot be increased, than an external protection clamp circuitry must be placed.

5 Conclusions

In this application note the design of a voltage pre regulator for headlamps ADB systems with LITIX™ devices have been proposed.

One scenario with specific requirements have been analyzed and Infineon devices offer the best fit for the requirement fulfilment in the harsh automotive environment.

Revision history

Major changes since the last revision

Page or Reference	Description of change
2020-03-26	Rev. 1.00 - First release

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