TLD5099EP

LED driver in boost to battery topology

About this document

The TLD5099EP is a flexibly usable DC/DC boost controller with built in diagnosis and protection features especially designed to drive LEDs. It also includes an embedded pulse width modulator to easily implement a dimming function with reduced color shifting and spread spectrum modulator.

This document explains how to design a DC/DC in boost to battery topology for automotive LED lighting.

The solution proposed is tailored on characteristics of TLD5099EP, showing how to enable all the features embedded on it.

Scope and purpose

The purpose of this application note is to give to the audience some design hints related to boost to battery topology

Intended audience

This application note is intended for hardware engineers.

Table of contents

1 Introduction

Boost to battery is a topology very close to boost to ground, where the output current recirculates back to the positive pole of the battery instead of flowing to ground. A simplified schematic is shown in Figure 1. TLD5099EP is a multitopology controller that easily enables this topology.

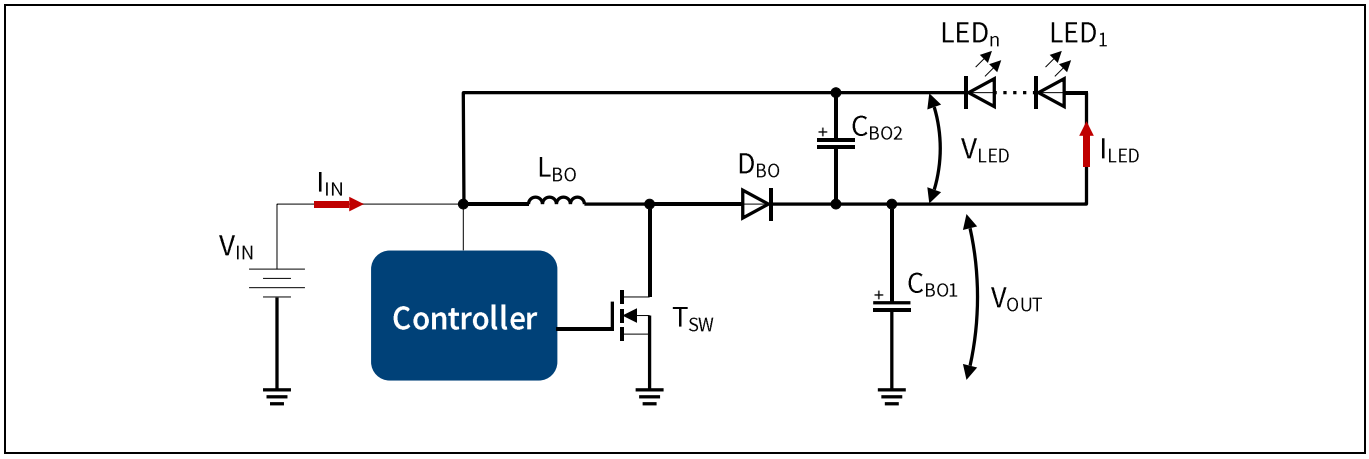


Figure 1 Boost to ground topology simplified

The core of the DC/DC is a boost regulator. The system generates at the positive output (cathode of D_{BO}) a higher voltage than input voltage. As depicted in Figure 1, the load is connected from the cathode of D_{BO} back to the positive pole of the battery. In this way a buck boost topology is realized because the voltage across the LED string can be lower or higher than input voltage (at the cathode of D_{BO}, the voltage is always higher than V_{BATT}).

1.1 Application example

The LED driver module (LDM) with TLD5099EP presented in this note is for automotive application and it has to fulfil the following requirements:

Table 1 LDM requirements

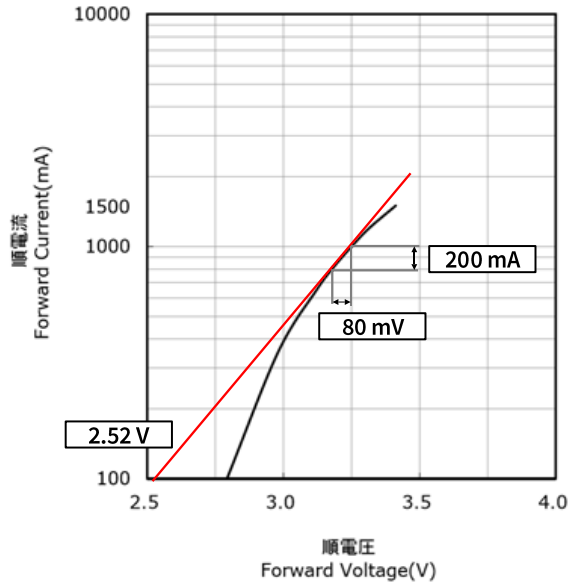
	Target
Number of LED	5 (Reference Nichia NCSW170DT)
LED current	0.9 A
Current ripple	+/- 5 %
Switching frequency	400 kHz
EMC requirements	CISPR class V
Battery voltage	13.5 V

The board works with every kind of white high power LED and current ratings higher than 1.0 A. Thermal management of LED has to be taken into account by the user.

2 Main regulator design

The key points related to the stability of the DC/DC are the load characteristics and the boundary conditions.

As mentioned in the Application example section, the load is a string of 5 LEDs. The LED string is considered as an equivalent voltage source with an equivalent series resistor (Thevenin equivalent circuit transformation). The equivalent voltage source is the sum of all forward voltages of the LEDs, while the equivalent resistor is the sum of all equivalent resistors. The LED equivalent resistor is calculated as incremental ratio of voltage versus current in the around of working point. The LED forward voltage is calculated as the intercept on x-axis of the line tangent to the curve on the desired working point. For the reference LED, Figure 2 shows graphically how to extrapolate $V_{forward}$ and R_{LED}



$$R_{LED} = \frac{\Delta V}{\Delta I} = \frac{80\ mV}{200\ mA} = 0.4\ \Omega$$

Figure 2 LED characteristic curve.

The load is described in a typical condition by the equivalent parameters below

$$V_{LED} = n_{LED} \cdot V_{forward} = 5 \cdot 2.52\ V = 12.6\ V$$

$$R_{LED\_string} = n_{LED} \cdot R_{LED} = 5 \cdot 0.4\ \Omega = 2.0\ \Omega$$

Due to the back connection of the load to the positive pole of the battery, the voltage at the output of DC/DC is a sum of battery voltage and load voltage.

$$V_{OUT\_MIN} = V_{IN\_MIN} + V_{LED} + R_{LED\_string} \cdot I_{LED} = 8\ V + 12.6\ V + 2\ \Omega * 0.9\ A = 22.4\ V$$

$$V_{OUT\_TYP} = V_{IN\_TYP} + V_{LED} + R_{LED\_string} \cdot I_{LED} = 13.5\ V + 12.6\ V + 2\ \Omega * 0.9\ A = 27.9\ V$$

$$V_{OUT\_MAX} = V_{IN\_MAX} + V_{LED} + R_{LED\_string} \cdot I_{LED} = 26\ V + 12.6\ V + 2\ \Omega * 0.9\ A = 40.4\ V$$

The duty cycle (DC) of the DC/DC regulator is a function of input and output voltage. The formula for the boost converter is

$$DC = 1 - \frac{V_{IN}}{V_{OUT}}$$

It shows that the duty cycle DC varies with input voltage and output voltage. In case of typical forward voltage of LED string, DC variation is reported in Table 2.

Table 2 Duty cycle vs. input voltage

Input voltage V_{IN} [V]	Duty cycle [%]
8 V (maximum DC) Transient undervoltage	64.3 %
13.5 V (typical condition) Nominal battery	51.6 %
26 V (minimum DC) Jump start	35.6 %

Considering the output power is related to V_{LED} and not to V_{OUT}, the average input currents (maximum, typical and minimum) are estimated by equalizing the input power and output power with the effect of the efficiency. The formulas below report the value of the average input current supposing 90% of overall efficiency

$$< I_{IN\_MAX} >= \frac{P_{OUT}}{V_{IN\_MIN} \cdot \eta} = \frac{V_{LED} \cdot I_{OUT}}{V_{IN\_MIN} \cdot \eta} = \frac{(V_{OUT\_MIN} - V_{IN\_MIN}) \cdot I_{OUT}}{V_{IN\_MIN} \cdot \eta} = \frac{(22.4\,V - 8\,V) \cdot 0.9\,A}{8\,V \cdot 0.9} = 1.80\,A$$

$$< I_{IN\_TYP} >= \frac{P_{OUT}}{V_{IN\_TYP} \cdot \eta} = \frac{V_{LED} \cdot I_{OUT}}{V_{IN\_TYP} \cdot \eta} = \frac{(V_{OUT\_TYP} - V_{IN\_TYP}) \cdot I_{OUT}}{V_{IN\_TYP} \cdot \eta} = \frac{(27.9\,V - 13.5) \cdot 0.9\,A}{13.5\,V \cdot 0.9} = 1.07\,A$$

$$< I_{IN\_MIN} >= \frac{P_{OUT}}{V_{IN\_MAX} \cdot \eta} = \frac{V_{LED} \cdot I_{OUT}}{V_{IN\_MAX} \cdot \eta} = \frac{(V_{OUT\_MAX} - V_{IN\_MAX}) \cdot I_{OUT}}{V_{IN\_MAX} \cdot \eta} = \frac{(40.4\,V - 26\,V) \cdot 0.9\,A}{26\,V \cdot 0.9} = 0.55\,A$$

The values reported are useful to define the ratings of the components during the design in the following part of the document.

2.1 Inductor

The inductor in a boost converter is designed based on the specified average and ripple current. Usually, the peak current is in the range of 20% to 40% of the average value (in this application 30% has been chosen). To be fast in react on input voltage steps, the DC/DC is designed to work in continuous conduction mode. Then, two equations are needed to choose the correct value of inductor for the DC/DC.

The first equation determines the inductor value to obtain the required ripple current with typical voltage at input.

$$L_{MIN1} \geq D_{TYP} \cdot \frac{V_{IN\_TYP}}{\Delta i_{L\_TYP(P-P)} \cdot f_{sw}} = 0.516 \cdot \frac{13.5\,V}{2 \cdot 0.2 \cdot 1.07\,A \cdot 400\,kHz} = 40.69\,\mu H$$

The second equation determines the minimum inductor to prevent discontinuous conduction mode when the input current is at minimum (i.e. with maximum input voltage that is the worst condition)

$$L_{MIN2} \geq D_{MIN} \cdot \frac{V_{IN_{MAX}}}{2 \cdot < I_{IN_{MIN}} > \cdot f_{sw}} = 0.356 \cdot \frac{26\ V}{2 \cdot 0.55\ A \cdot 400\ kHz} = 21.04\ \mu H$$

The closest standard value that satisfies both equations is 47 µH.

With this value, the actual peak current in worst condition (i.e. when input voltage is at minimum) can be calculated as:

$$\Delta i_{L(P-P)} = D_{MAX} \cdot \frac{V_{IN_{MIN}}}{L \cdot f_{sw}} = 0.643 \cdot \frac{8\ V}{47\ \mu H \cdot 400\ kHz} = 0.30\ A$$

And then, the maximum peak current into inductor is:

$$I_{L-MAX} = < I_{IN\_MAX} > + \frac{\Delta i_{L(P-P)}}{2} = 1.80\ A + 0.30\ A = 2.1\ A$$

The important key parameters to select an inductor are then:

- Inductance > 47 µH
- Saturation current > 2.1 A

An inductor that fulfills above requirements (nominal inductor value and saturation current) is the Coil Craft MSS1246T-473ML.

2.2 Output capacitor

The output capacitor acts as an energy tank when the diode is in reverse polarity and for this reason it sees a high ripple current. This component affects the bandwidth of the system and also the output current ripple performance. Usually, for this kind of application multilayers ceramic capacitors (MLCC) with low ESR are preferred over electrolytic capacitors.

Figure 3 depicts how the system manages the current into reactive components and LED string.

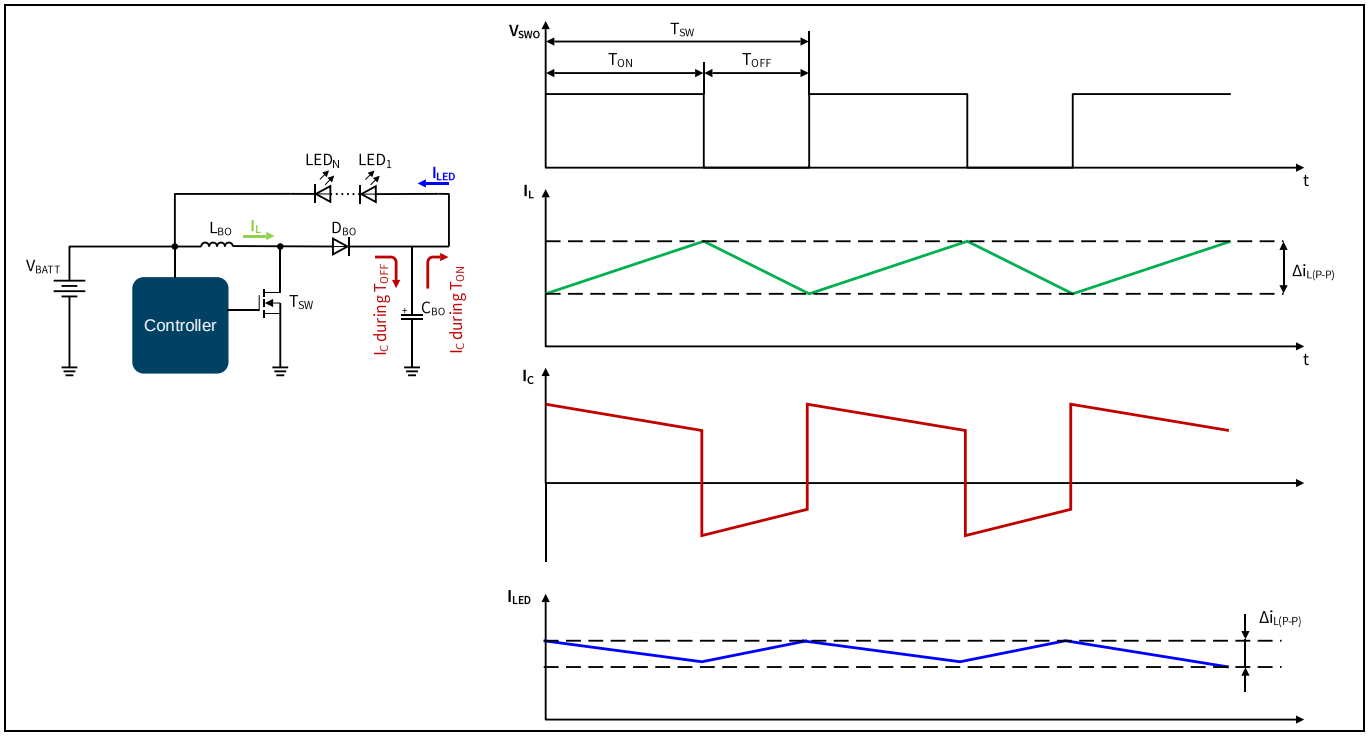


Figure 3 Waveform of current in reactive components and LED string

The output voltage ripple can be approximated by:

$$\Delta V_{OUT} = \Delta I_{OUT} \cdot R_{LOAD} = I_{OUT} \cdot ripple_{OUT} \cdot R_{LOAD} = 900\ mA \cdot 0.1 \cdot 2.0\ \Omega = 0.18\ V$$

Assuming the capacitor is discharged by a constant current (equal to average output current) for a time equal to t_{ON}, its value can be calculated in worst case condition when duty cycle is maximum by:

$$C \geq \frac{I_{OUT}}{\Delta V_{OUT}} \cdot \frac{D_{MAX}}{f_{sw}} = \frac{900\ mA}{0.18\ V} \cdot \frac{0.643}{400\ kHz} = 8.0\ \mu F$$

Also the equivalent series resistor (ESR) of the capacitor affects the ripple of the output voltage. Its effect is calculated during two phases:

- During capacitor discharging it is described by

$$\Delta V_{ESR} = R_{ESR} \cdot I_{OUT}$$

- During the charging phase it is described by

$$\Delta V_{ESR} = R_{ESR} \cdot (I_L - I_{OUT})$$

To make it negligible (for example less than 10% of the ripple imposed by capacitor), its contribution has to be lower than ΔV_{OUT} on both cases. From the equations above, it is possible to calculate the maximum ESR acceptable by the application.

$$R_{ESR} \leq \frac{\Delta V_{ESR}}{I_{OUT}} = \frac{0.1 \cdot \Delta V_{OUT}}{I_{OUT}} = \frac{0.1 \cdot 0.18\ V}{900\ mA} = 20\ m\Omega$$

$$R_{ESR} \leq \frac{\Delta V_{ESR}}{I_{L\_MAX} - I_{OUT}} = \frac{0.1 \cdot \Delta V_{OUT}}{I_{L\_MAX} - I_{OUT}} = \frac{0.1 \cdot 0.18\ V}{2.1\ A - 900\ mA} = 15\ m\Omega$$

To fulfil both equations, ESR of the capacitor bank has to be lower than 15 mΩ. This is a reasonable value for a ceramic capacitor.

Note: MLCC capacitors show quite good value of capacitance related to small package and also very good performances related to ESR, but they show a strong variation of the capacitance as a function of the applied voltage. As an example, in Figure 4 the behavior of TDK CGA9N2X7R2A475K230KA is shown.

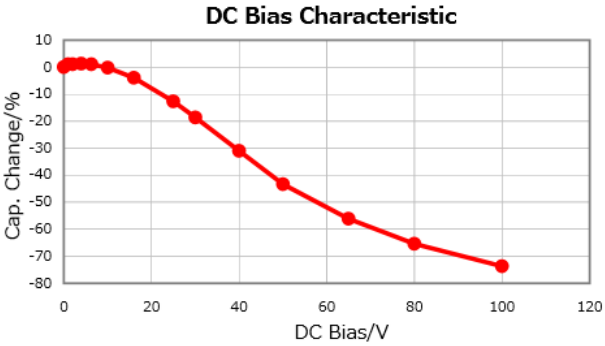


Figure 4 DC bias characteristic of TDK CGA9N2X7R2A475K230KA

The capacitor is rated 100 V to work properly at maximum of V_{OUT} = 40.4 V, but it shows a 30% drop of its nominal value.

Here a good choice is a 4.7 µF capacitor at the output of the boost converter referred to ground (mainly to lower the EMC emission) and two 3.3 µF capacitors across the load (stressed by V_{LOAD}); with this solution, the total capacitor is 4.7 µF * 0.7 + 2 * 3.3 µF = 9.89 µF (no degradation of 3.3 µF capacitor has been taken into account for 100 V rated component because it is biased with V_{LOAD} only)

2.3 Input PI filter

A PI filter is a common choice for filtering out the undesired frequency components in the standardize bands.

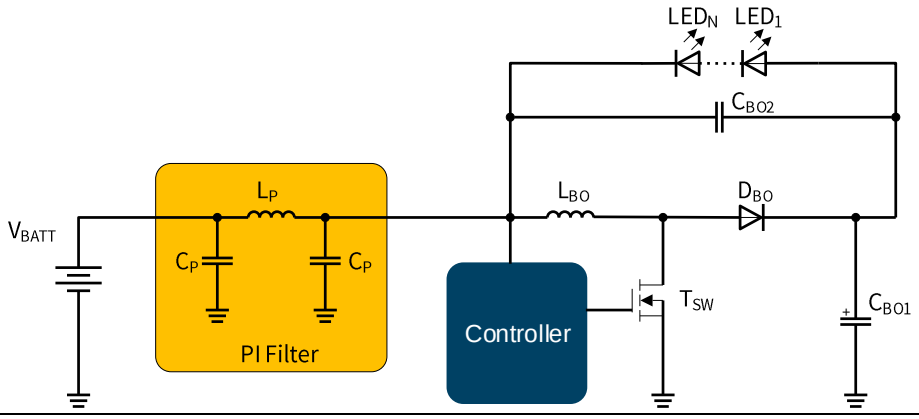


Figure 5 PI filter schematic simplified

Parasitic effects on capacitors and inductor shape the high frequency response of PI filter and for this reason, it works fine up to 5-10 MHz Above this frequency fast transients signals dominate the emissions. To mitigate this effect a good PCB layout is important.

To achieve good results damping zone of the filter has to be put where harmonics of the switching frequency causes problems in AM band (500 kHz – 1.8 MHz).

Rule thumb to design the PI filter is the following:

- Select L_p lower 1/10 * L_{BO}
- Put the corner frequency of PI filter 1/10 of the switching frequency of DC/DC: $f_{PI} = 0.1 * f_{SW}$
- Have equal capacitance distribution on both sides of PI-Filter and value

$$C_P = \frac{1}{4 \cdot \pi^2 \cdot L_P \cdot f_P^2} = \frac{1}{4 \cdot \pi^2 \cdot 33/10\ \mu H \cdot (0.1 \cdot 400\ kHz)^2} = 4.8\ \mu F$$

For each side of the PI filter at least 4.8 µF is needed. Considering the reduction of the capacitor with the applied voltage a possible choice is to have 2 capacitor of 3.3 µF.

For this purpose CGA5L3X7R1H475K160AB is a good candidate for the capacitors while the inductor could be Coilcraft XGL4020-472ME

2.4 Transistor

The switching element of the boost to battery DC/DC is the T_{SW} transistor. It is an n-type MOSFET. The switching activity behavior and how the current is split into the transistor and the diode is depicted in the Figure 6.

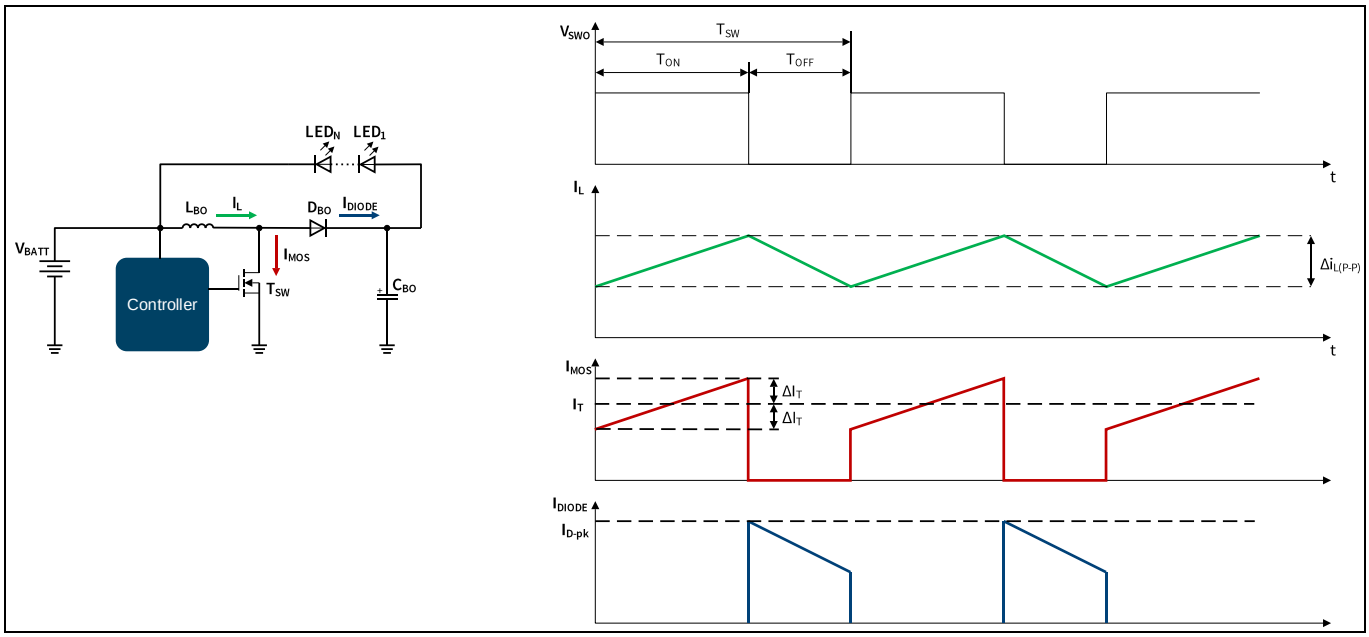


Figure 6 Waveform of current in power devices and inductor

The RMS value of the repetitive trapezoidal current waveform into the transistor is calculated as:

$$I_{T\_rms} = \sqrt[2]{\frac{1}{T}\int_0^T i_{MOS}(t)^2 dt} = \sqrt[2]{\frac{1}{T}\int_0^T \left(\frac{(I_T + \Delta I_T - I_T + \Delta I_T)\cdot t}{T_{ON}} + (I_T - \Delta I_T)\right)^2 dt}$$

$$= \sqrt{\frac{T_{ON}}{3T}\left(I_{MOS\_min}^2 + I_{MOS\_min}\cdot I_{MOS\_max} + I_{MOS\_max}^2\right)}$$

$$= \sqrt{\frac{D}{3}\left(I_{MOS\_min}^2 + I_{MOS\_min}\cdot I_{MOS\_max} + I_{MOS\_max}^2\right)}$$

During the ON state the MOSFET conducts the inductor current. Then it has a maximum when V_{IN} is minimal (also duty cycle is maximum) and it can be calculated as:

$$I_{T\_rms,max}\sqrt{\frac{D_{MAX}}{3}\left(\left(I_{L\_MAX} - \Delta i_{L(P-P)}\right)^2 + \left(I_{L\_MAX} - \Delta i_{L(P-P)}\right)\cdot I_{L\_MAX} + I_{L\_MAX}^2\right)}$$

$$= \sqrt{\frac{0.643}{3}\left((2.1\ A - 0.3\ A)^2 + (2.1\ A - 0.3\ A)\cdot 2.1\ A + (2.1\ A)^2\right)} = 1.56\ A$$

During switching, it is also stressed by the voltage equal to output voltage (voltage drop on diode is not taken into account).

For EMI reasons, it is common practice to put in series a resistor (R_{gate}) of approximately 5 to 15 Ω. This helps reducing the current spikes into the gate and also having a smooth transition from OFF state to ON state. On the other hand, this lowers the overall efficiency of the converter.

Infineon offers a wide variety of MOSFET suitable for this purpose; IPD25N06S4L-30 is a good compromise of gate charge and R_{ds_on}.

2.5 Diode

The diode D_{BO} is the rectification device of the DC/DC. The current flowing into the device is shown in blue in Figure 6. It has a trapezoidal waveform as the current into the transistor and it is described by a similar equation. Changing the limits in the integral on the equation of transistor current, the current into the diode D_{BO} is described by the following equation

$$I_{D\_rms,max} = \sqrt{\frac{T_{OFF}}{3T}\left(\left(I_{L\_MAX} - \Delta i_{L(P-P)}\right)^2 + \left(I_{L\_MAX} - \Delta i_{L(P-P)}\right) \cdot I_{L\_MAX} + I_{L\_MAX}^2\right)}$$

$$= \sqrt{\frac{0.357}{3}\left((2.1\ A - 0.30\ A)^2 + (2.1\ A - 0.30\ A) \cdot 2.1\ A + (2.1\ A)^2\right)} = 1.17\ A$$

During the ON state of the transistor, the voltage across the diode is V_{OUT} = 40.4 V (voltage drop on the transistor and sensing resistor is not taken into account). Adding some margin, the next higher voltage class should be taken, e.g. a 60 V Schottky.

A good choice for this application could be the Vishay VSS8D2M6 that provides also low forward voltage.

2.6 Current sense resistors

There are still few components that are needed to be chosen for a proper behavior of the main regulation loop. Two of these are resistors needed to sense the current into the switching transistor, and the output current.

The first resistor limits the current into the switching NMOS and inductor. It is placed below the transistor (please refer to Figure 7) and it is useful to improve the stability (current mode control loop). This resistor converts the current flowing into the transistor in a voltage sensed by SWCS pin. The maximum voltage across the resistor must not reach the V_{SWCS} threshold of 150 mV. This has to be true not only during the steady state but also during the transition phase.

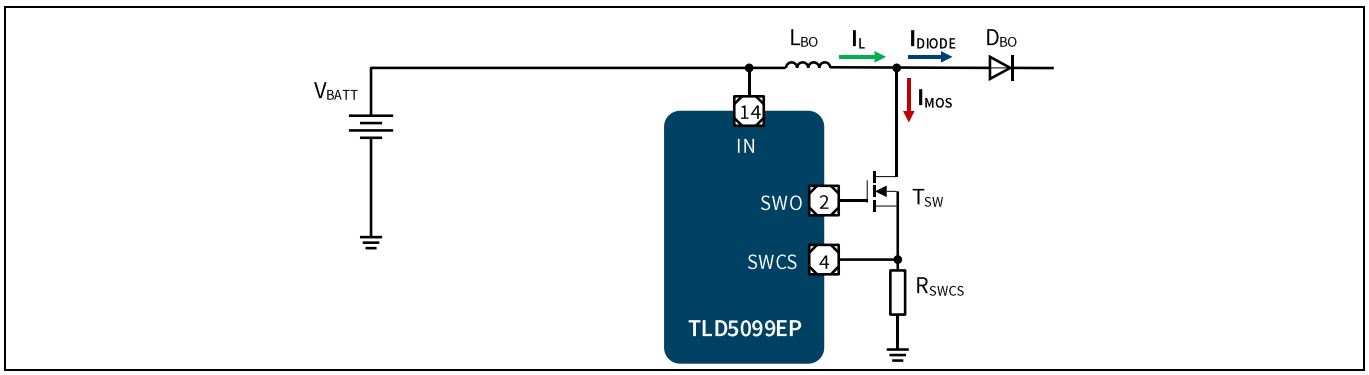


Figure 7 Peak current sensing resistor

For example, with system phase margin of 45° (the reasonable bandwidth for a stable system), the output current has an overshoot about 50%; it affects also the input current and switching current too. Taking into account the corner case with minimum V_{IN}, the maximum current in the R_{SWCS} is calculated with the following equation

$$R_{swcs} < \frac{V_{SWCS}}{1.5 \cdot I_{L\_MAX}} = \frac{150\ mV}{1.5 \cdot 2.1\ A} = 47.6\ m\Omega$$

Adding some margin, 22 mΩ is selected (the effects on stability of DC/DC, will be evaluated in Section 3.The RMS current flowing into the resistor is equal to the current flowing into power NMOS. Therefore the power dissipated by the resistor is

$$P = R_{swcs} \cdot I_{NMOS}^2 = 22\ m\Omega \cdot (1.56\ A)^2 = 53.5\ mW$$

To avoid overheating of the resistor it is a common practice to use resistors with 4-5 times power rating needed. For this application RCWL2010R022JQ from Vishay satisfies the requirements. It is a low inductive resistor that is needed to sense current with steeply edges.

The second component involved in the regulation loop is the output current sensor (please refer to Figure 8). It can be easily calculated by imposing the feedback voltage V_{REF} regulated by the device with the required output current.

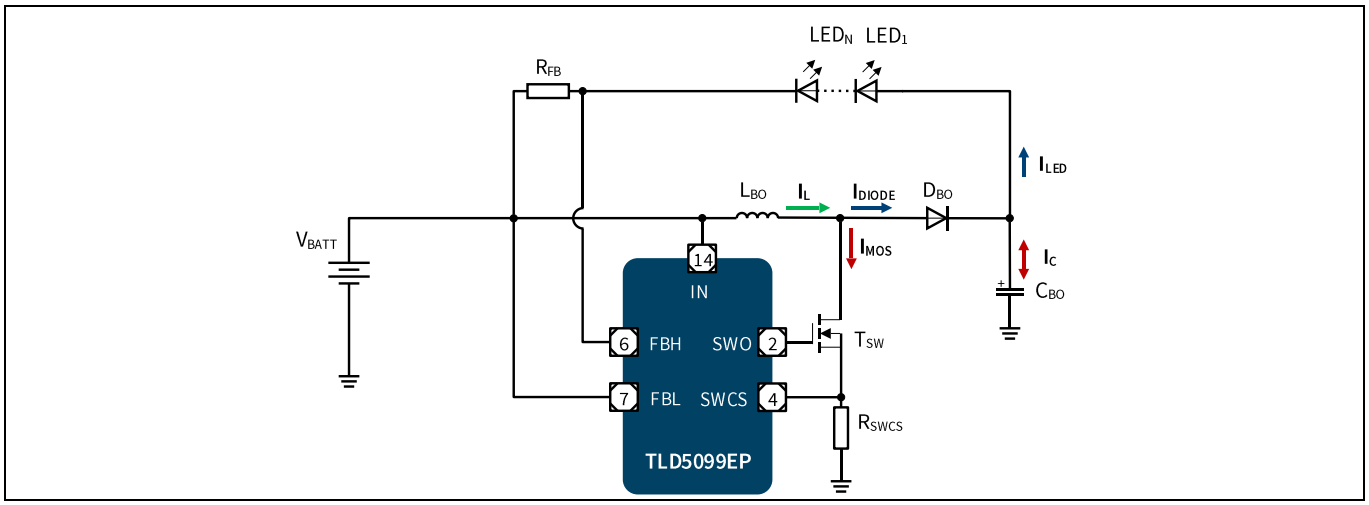


Figure 8 Output current sensing resistor

For this application, the resistor can be calculated as:

$$R_{FB} = \frac{V_{REF}}{I_{OUT}} = \frac{0.3\ V}{900\ mA} = 0.33\ \Omega$$

The power rating of this device can be calculated as

$$P = R_{FB} \cdot I_{OUT}^2 = 0.33\ \Omega \cdot (900\ mA)^2 = 0.27\ W$$

To avoid overheating of the resistor it is a common practice to use resistors with 4-5 times power rating needed; for this application RCWL2512R330JQ from Vishay is a good candidate.

3 Features

3.1 Overvoltage protection

This feature helps to avoid overvoltages during open fails of the load (for example if the load is disconnected). This voltage has to be set higher than the maximum voltage of the load. To avoid unwanted tripping it is designed at minimum threshold of the device.

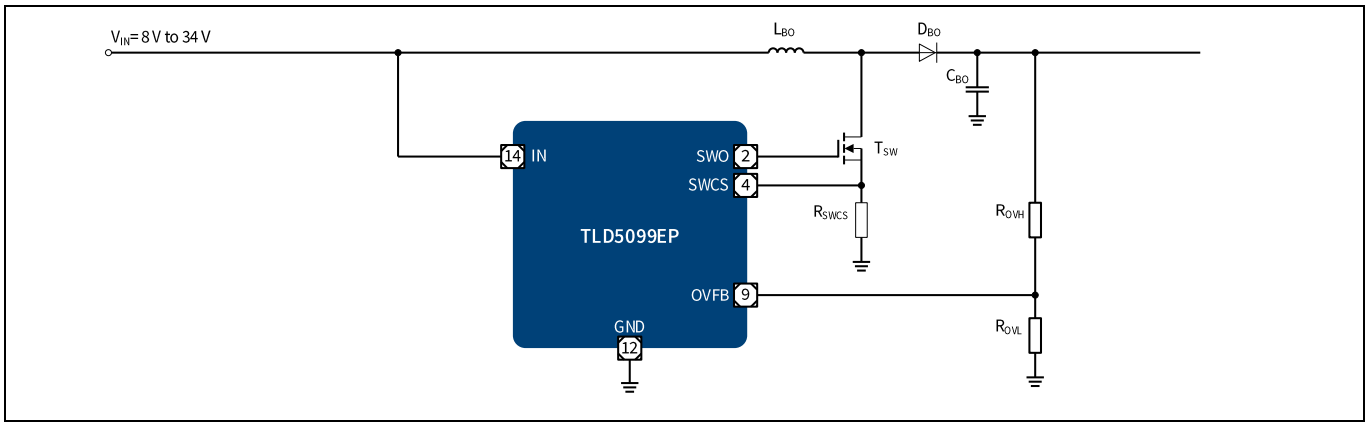


Figure 9 Overvoltage protection schematic

Overvoltage is triggered when the voltage on OVFB pin reaches 1.21 V. The resistor divider to enable this feature is shown on Figure 9

To reduce the parasitic effects of the moisture, the resistors of this path cannot be too high. A reasonable value for resistance of the string is below 100 kΩ. This means the current in this path has to be higher than 0.6 mA during the overvoltage (61 V is the maximum absolute rating for the output voltage). With this current, R_{OVL} has to be lower than 2 kΩ. Adding some margin a reasonable value for R_{OVL} is 1 kΩ. With this resistor at low side, the current flowing into the string during the overvoltage is 1.21 mA. It is calculated by dividing the V_{OFFB,TH_min} by R_{OVL}. Then, R_{OVH} is calculated as:

$$R_{OVH} = \frac{V_{OUT\_MAX} - V_{OVFB,TH\_min}}{I_{R-OVFB}} = \frac{40.4\ V - 1.21\ V}{1.21\ mA} = 32.39\ k\Omega$$

The closest value as off the shelf component on E96 series is 33.2 Ω. It provides the over voltage protection at 41.4 V.

3.2 Protection diodes for short to ground protection

To increase the reliability of the system, three extra diodes at the output are needed. A possible solution is depicted on Figure 10.

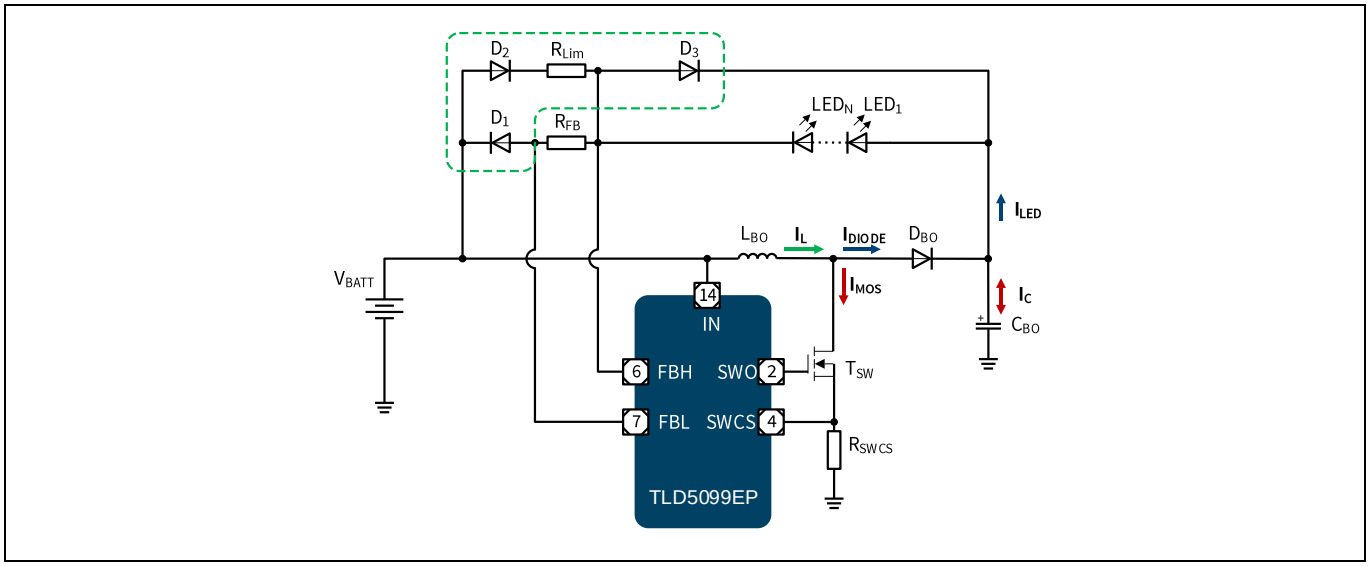


Figure 10 Protection diodes

Main purpose is to protect the system from short to ground failures that could accidentally happen at load terminals.

- D_1 protects in case of a short of cathode of LED string and it prevents to burn R_{FB}. It has to be able to sustain load current, because it is a part of the output current path. Vishay VSS8D2M6 fits well for this the load current.
- D_2 plus R_{Lim} are needed to bias FBH pin at start up. FBH and FBL are not biased from the battery due to the presence of D_1; in this condition TLD5099EP recognizes a short to ground (V_{FBH} and V_{FBL} = 0 V) and then switching activity is disabled. D_2 and R_{Lim} network correctly biases FBH and to ensure the stat-up. The current flowing on this branch is limited by R_{Lim} (10 kΩ). BAS16 is a good candidate for this application.
- D_3 acts in case of short to ground of positive terminal of the LED string. If a short is present at the output of the DC/DC, the switching activity is not disabled because any fault is detected. This diode needs to bias FBH pin below the V_{FBH,FBL_S2G} and this freezes the switching activity. The current flowing on this branch is limited by R_{Lim}. And then also here BAS16 can be used.

3.3 Protection switch

A PMOS transistor is used to protect the load in case of failures at load side. The application is illustrated on Figure 11. In case of a fault, T_{DIM2} disconnects the load from the positive terminal of DC/DC. The level shifter (needed for properly bias the PMOS) is made up of transistor T_{DIM1}, resistors R_{DIM1} and R_{DIM2}. When the transistor T_{DIM1} is in conduction state (no fault detected), a current flows into the resistor string R_{DIM1} and R_{DIM2}. Then the voltage across R_{DIM2} has to be enough to bias the gate of transistor T_{DIM2}. The 10 V Zener protects the gate of PMOS T_{DIM2}.

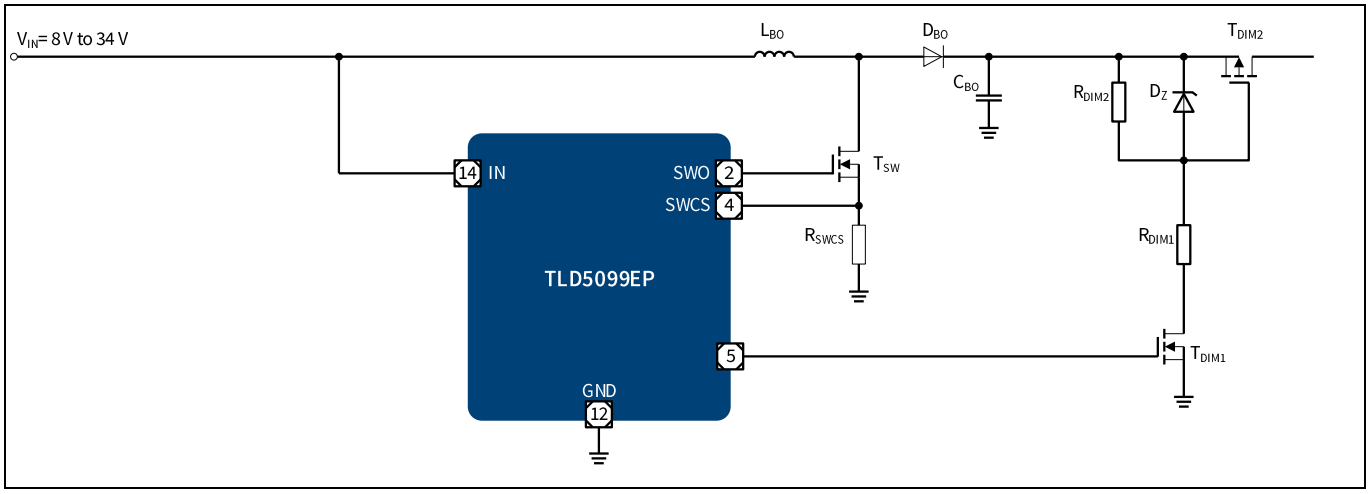


Figure 11 Dimming PMOS setup

T_{DIM2} manages the load current. Therefore the current rating of transistor should be higher than 900 mA. The voltage between drain and source can reach 60 V when the transistor is in open state, its V_{DS} can reach 60 V. A suitable product for T_{DIM1} and T_{DIM2} is BSO615CG provided by Infineon. It is a dual N and P channel MOSFET in one package.

The threshold voltage of PMOS is 2V. In order to minimize the R_{DSon} a gate to source voltage of 10V can be applied. Fixing the current on the NMOS to 1 mA, R_{DIM2} is easily calculate as ratio between the desired V_{GS} of PMOS transistor and the current

$$R_{DIM2} = \frac{V_{GS\_PMOS}}{I_R} = \frac{10\ V}{1\ mA} = 10\ k\Omega$$

While R_{DIM1} can be calculated as:

$$R_{DIM1} = \frac{V_{OUT\_min} - V_{GS\_PMOS}}{I_R} = \frac{31.2\ V - 10\ V}{1\ mA} = 21.2\ k\Omega$$

The closest value on E24 series is 22 kΩ.

3.4 Spread Spectrum

The spread spectrum modulator helps the designer to mitigate EMI issues by moving the energy from the narrow peaks of the spectrum into a broad band signal. The switching frequency is internally modulated by a triangular waveform running at 7 kHz. By using the spread spectrum technique, it is possible to optimize the input and output filters to fulfil the EMC requirements.

This feature is easily activated by selecting the correct resistor set. To switch at 400 kHz with spread spectrum activated, a resistor can be selected by equation:

$$R_{FREQ\_SSMon} = \frac{1}{\left(600 \cdot 10^{-12} \cdot f_{FREQ}\right)^{0.943}} - 600 = \frac{1}{\left(600 \cdot 10^{-12} \cdot 400\ kHz\right)^{0.943}} - 600 = 1.99\ k\Omega$$

Here 2.0 kΩ (E96 series) has to be selected and connected between pin 11 and ground.

3.5 Binning resistor

LED manufactures sort products based on forward voltage and light flux emitted in standard conditions. For the LED selected in this application, the binning table is presented in Figure 12

Item	Rank	Min	Max	Unit
Forward Voltage	-	2.75	3.55	V
Luminous Flux	R425	425	450	lm
	R400	400	425	
	R375	375	400	
	R350	350	375	
	R325	325	350	

Figure 12 LED binning table

Using the embedded PWM engine, it is possible to keep the total amount of flux of the headlamp constant also when higher ranks of LED are used. PWM operation is used in order to adjust the light output according to LED rank neglecting the non-linearity between LED current and output flux. Moreover, modulating the LED current, the color shift is minimal.

The basic circuit to enable the embedded PWM engine is shown in Figure 13.

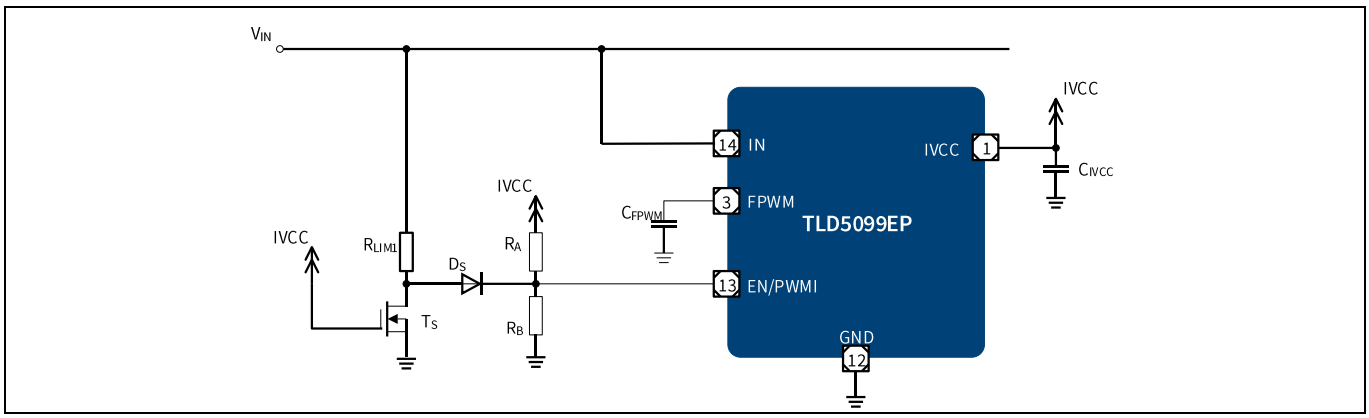


Figure 13 Embedded PWM engine application scheme

For this application 500 Hz (C_{FPWM} = 390 pF) has been used as a dimming frequency. Such high frequency does not provide any flickering effects to human eyes. The duty cycle of the modulation is fixed by selecting a proper analog voltage on EN/PWMI pin. It has to be included between a valid logic “low” level and a valid logic “high” level. The desired duty cycle can be calculated by

$$DC[\%] = \frac{V_{EN/PWMI} - 0.32 \cdot V_{IVCC}}{0.24 \cdot V_{IVCC}}$$

From this formula, $V_{EN/PWMI}$ is calculated by using the equation below

$$V_{EN/PWMI} = (0.32 + 0.24 * DC) \cdot V_{IVCC}$$

Fixing R_A to 10 kΩ, it is possible to calculate R_B as a function of $V_{EN/PWMI}$.

$$R_B = \frac{V_{EN/PWMI}}{I_R} = \frac{R_A}{(V_{IVCC} - V_{EN/PWMI})} \cdot V_{EN/PWMI} = 10k \cdot \frac{V_{EN/PWMI}}{(V_{IVCC} - V_{EN/PWMI})}$$

All the data related to the binning are reported in Table 3

Table 3 Summary of different LED rank and R_B

Rank	Current reduction	DC	$V_{EN/PWMI}$	R_B
R325	0	100 %	5 V	Not mounted
R350	7.6 %	92.4 %	2.71 V	11.8 kΩ
R375	7.1%	85.3 %	2.62 V	11 kΩ
R400	6.6 %	78.7 %	2.54 V	10.2 kΩ
R425	6.2 %	72.5 %	2.47 V	9.76 kΩ

For the start-up network R_{LIM}, T_S and D_S are needed. R_{LIM} = 10KΩ satisfies equation 7.4 of the datasheet. The transistor and the diode are for small signal applications (suggestion are IRLML0100TRPBF-1 and 1N4148)

4 Compensation network

The TLD5099EP has one dedicated pin where a second type of compensation network can be applied (proportional and integral -PI- compensation or only integral compensation).

In small signal approximation, the open loop transfer function of a DC/DC is the product of modulator transfer function and the feedback network transfer function.

The modulator transfer function can be expressed as product of two main parts: the gain of the error amplifier and the gain of the current mode modulator.

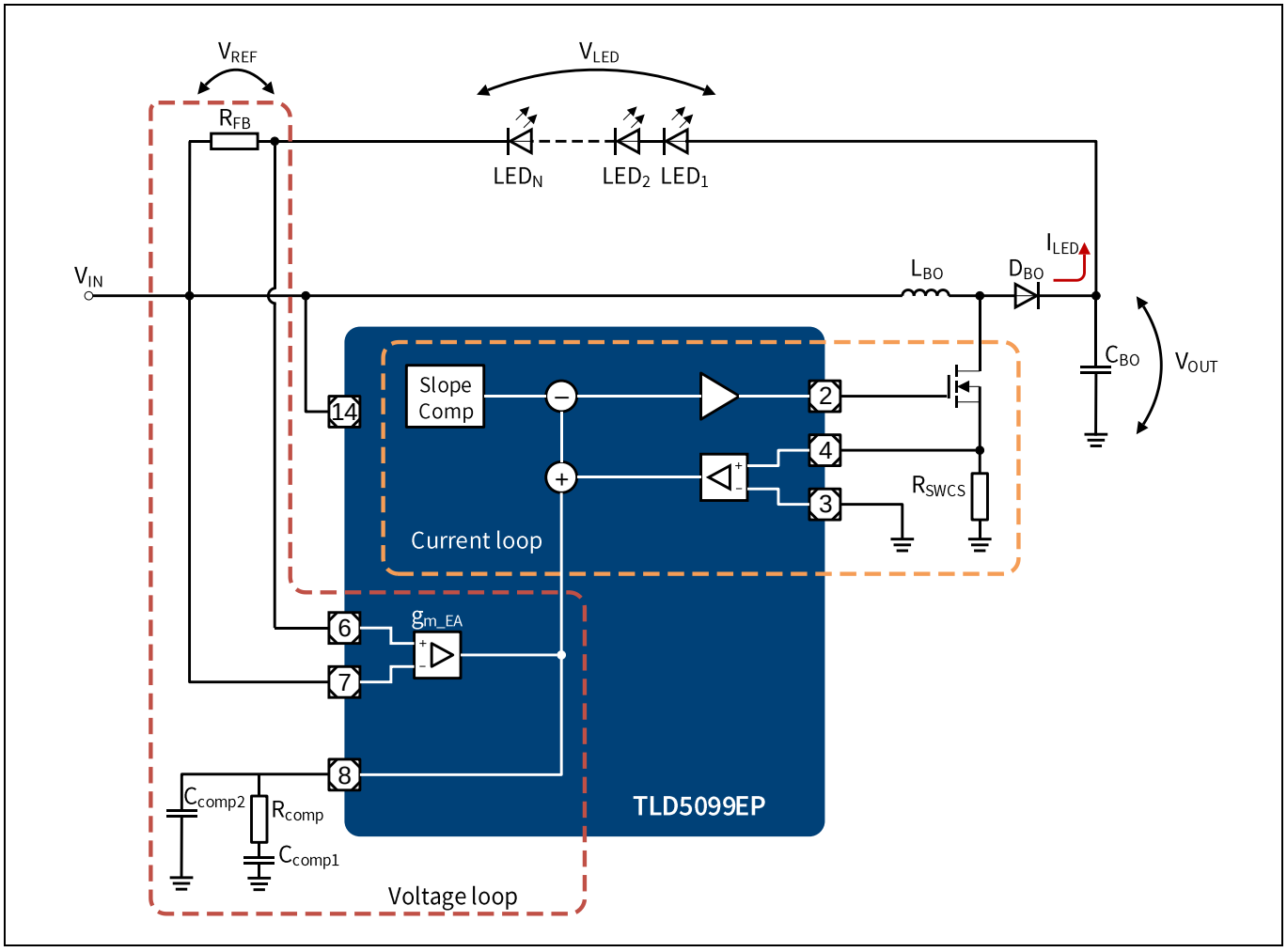


Figure 14 Compensation network schematic

The gain of the error amplifier is described with the following formula:

$$A_{EA}(s) = g_{m\_EA} \cdot R_{EA} \cdot \frac{(1 + s \cdot \tau_{z1})}{(1 + s \cdot \tau_{p1}) \cdot (1 + s \cdot \tau_{p2})}$$

Where

- g_{m_EA} is the trans-conductance of the error amplifier (typical 600 µs)
- R_{EA} is the output resistance of the error amplifier (typical 2.5 MΩ)
- $\tau_{z1} = C_{comp1} \cdot R_{comp}$ is the zero of compensation network

- $\tau_{p1} = (C_{comp1} + C_{comp2}) \cdot R_{EA}$ is the pole associated to compensation network and the resistor of error amplifier
- $\tau_{p2} = C_{comp2} \cdot R_{comp}$ is a pole associated to compensation network

The gain of the current mode modulator can be described following the model presented by R.B Ridley (*Reference: Ridley, R. B.; "A new Continuous Time Model for Current Mode Control"; IEEE Transaction on Power Electronics; Vol. 6; Issue 2; pp. 271-280; 1991*). It can be mathematically described as:

$$A_{CM}(s) = \frac{0.2 \cdot (1-D) \cdot R_{load}}{\left(1 + \frac{V_{ref}}{V_{OUT} + V_{ref}}\right) \cdot R_{swcs}} \cdot \frac{(1 + s \cdot \tau_{z2})}{(1 + s \cdot \tau_{p3}) \cdot \left(1 + \frac{s}{\omega_n \cdot Q} + \frac{s^2}{\omega_n^2}\right)}$$

Where:

R_{load} is the total resistor at the output of DC/DC and it is the sum of R_{FB} and R_{LED_string}

V_{REF} is the voltage reference across FBH and FBL (typical 300 mV)

V_{OUT} is the voltage on LED string V_{LED} plus input voltage V_{IN} (Voltage across PMOS has been neglected)

$\tau_{z2} = -\frac{L_{BO}}{(1-D)^2} \cdot \frac{(I_{OUT})}{(V_{OUT}+V_{ref})}$ is the zero (RHP) of the boost DC/DC with the return to battery

$\tau_{p3} = \frac{C_{OUT} \cdot R_{LED}}{1+\frac{V_{ref}}{V_{OUT}+V_{ref}}}$ is the pole associated to boost converter with the return to battery

$\omega_n = \pi \cdot \frac{f_s}{2}$ is the natural pulsation of the system

$Q = \frac{1}{\pi \cdot \left(\left(1+\frac{S_e}{S_n}\right) \cdot (1-D) - 0.5\right)}$ is the quality factor of a second order system, where S_e is the slope of current compensation circuit (coefficient fixed by internal references) and S_n is the slope of the current sensed by R_{swcs}.

$$S_e = 50 \cdot 10^{-6} \cdot f_{sw}$$

$$S_n = \frac{V_{IN} \cdot R_{SWCS}}{L_{BO}} \cdot 10^{-3}$$

Using the data previously calculated, it is possible calculate the gain in DC and cross over frequency f_c and the phase margin.

The transfer function of the feedback network is the ratio between R_{FB} and the R_{LED}

$$\beta = \frac{R_{FB}}{R_{LED\_string}}$$

For the gain calculation in typical conditions, the three part to be calculated are:

$$A_{EA}(0) = g_{m\_EA} \cdot R_{EA} = 0.0006\ S \cdot 2.5\ M\Omega = 1500$$

$$A_{CM}(0) = \frac{0.2 \cdot (1-D) \cdot R_{load}}{\left(1 + \frac{V_{ref}}{V_{OUT} + V_{ref}}\right) \cdot R_{swcs}} = \frac{0.2 \cdot (1 - 0.516) \cdot 2.33\ \Omega}{\left(1 + \frac{0.3\ V}{27.9\ V + 0.3\ V}\right) \cdot 0.022\ \Omega} = 10.14$$

$$\beta = \frac{R_{FB}}{R_{LED\_string}} = \frac{0.33\ \Omega}{2\ \Omega} = 0.165$$

And then the gain in DC can be calculated as:

$$T(0)|_{dB} = 20 \cdot \log(A_{EA}(0) \cdot A_{CM}(0) \cdot \beta) = 20 \cdot \log(1500 \cdot 10.14 \cdot 0.165) = 67.99\ dB$$

Using just a proportional and integrative compensation with R_{comp} = 698 Ω and C_{comp} = 33 nF, the constant time elements are:

$$\tau_{p1} = \left(C_{comp1} + C_{comp2}\right) \cdot R_{EA} = (33\ nF + 0) \cdot 2.5\ M\Omega = \ 0.0825\ sec$$

$$\tau_{p2} = \ C_{comp2} \cdot R_{comp} = 0\ F \cdot 698\ \Omega = 0\ sec$$

$$\tau_{p3} = \frac{C_{OUT} \cdot R_{LED\_string}}{1 + \frac{V_{ref}}{V_{OUT} + V_{ref}}} = \frac{9.89\ \mu F \cdot 2\ \Omega}{1 + \frac{0.3\ V}{27.9\ V + 0.3\ V}} = 19.57 \cdot 10^{-6}\ sec$$

$$\tau_{z1} = \ C_{comp1} \cdot R_{comp} = 33\ nF \cdot 698\ \Omega = 23.0 \cdot 10^{-6}\ sec$$

$$\tau_{z2} = -\frac{L_{BO}}{(1-D)^2} \cdot \frac{(I_{OUT})}{\left(V_{OUT} + V_{ref}\right)} = -\frac{47\ \mu H}{(1 - 0.516)^2} \cdot \frac{0.9\ A}{27.9\ V + 0.3\ V} = -6.40 \cdot 10^{-6}\ sec$$

$$\omega_n = \pi \cdot \frac{f_{sw}}{2} = \pi \cdot \frac{400\ kHz}{2} = 628 \cdot 10^3\ \ rad/sec$$

$$Q = \frac{1}{\pi \cdot \left(\left(1 + \frac{S_e}{S_n}\right) \cdot (1 - D) - 0.5\right)} = \frac{1}{\pi \cdot \left(\left(1 + \frac{50\mu \cdot 400\ kH}{0.001 \cdot \frac{13.5\ V}{47\ \mu H} \cdot 0.022\ \Omega}\right) \cdot (1 - 0.516) - 0.5\right)} = 0.16$$

For stability reasons, it is common practice to have Q below 1; in case Q is too high, it is necessary to lower it by increasing the value of inductor or/and increasing the switching frequency and/or reducing R_{SWCS}.

By using a mathematical analysis tool, it is possible to extract the cutoff frequency and phase margin of the system. The Bode plot graph is reported on Figure 15.

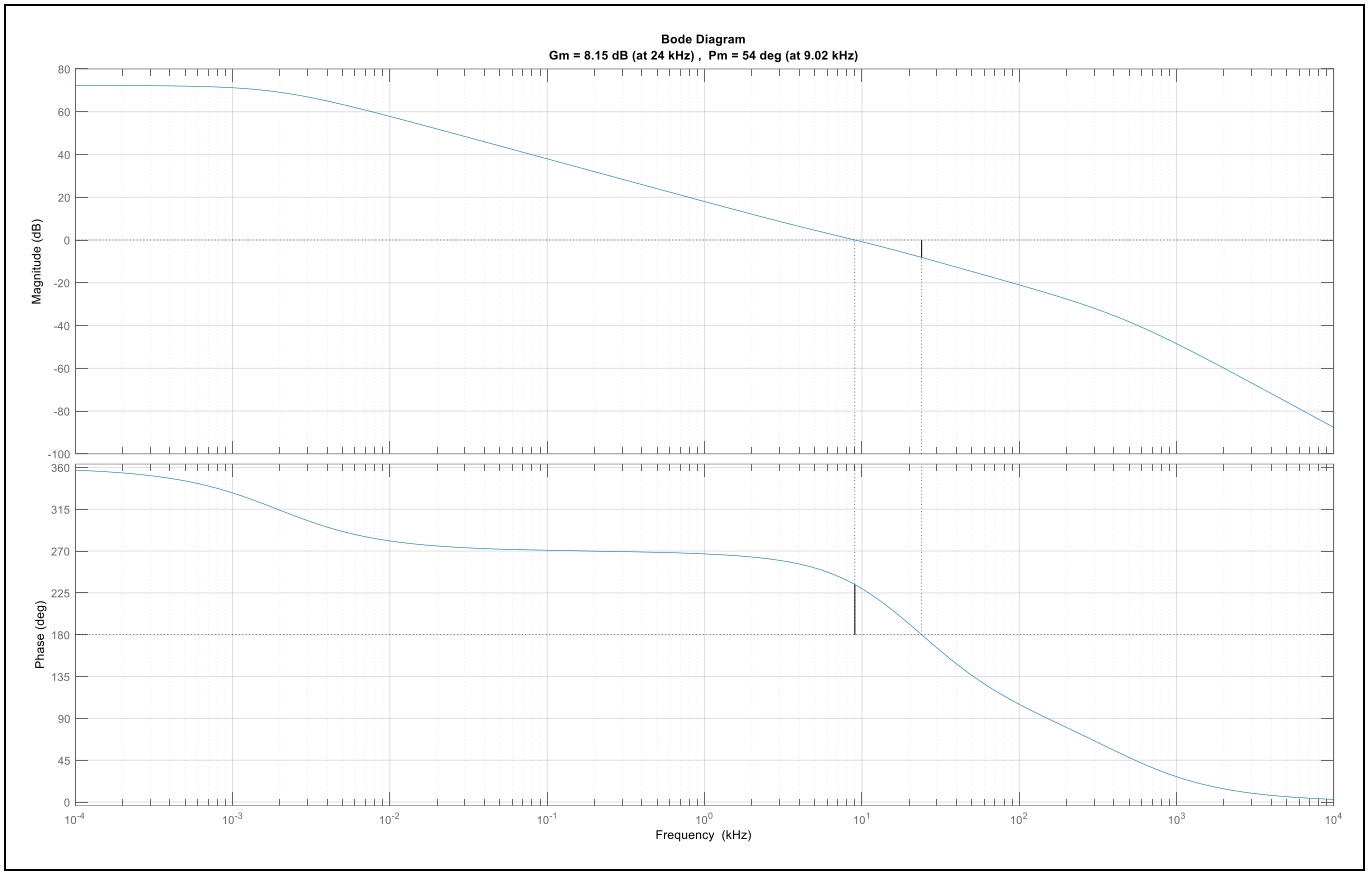


Figure 15 Cutoff frequency and phase margin calculated

As a rule of thumb, τ_{p1} is the dominant pole and changing the value of C_{comp1} it is possible to tailor the bandwidth of the system. The zero generated by C_{comp1} and R_{comp} is needed to compensate the pole τ_{p3}. If needed, C_{comp2} can be used to reduce the second order effects.

Infineon also provides SPICE models of the device for electrical simulations.

5 Layout considerations

For a DC/DC converter, the PCB design is a critical task as well as the component selection. Even if the circuit topology and components selection are reasonable, if the PCB layout is not good enough, the performances of the whole system will be lower than expected. Due to parasitic coupling between traces, high ripple and poor regulation could appear. Even EMC problems can be mitigated with a proper layout.

The regulation is directly related on the voltage across FBH and FBL pins. To avoid poor regulation use a Kevin connection from the sensing resistor (R_{FB}) to TLD5099EP; if possible, route these traces as a differential pair and avoid coupling with noisy lines. A possible layout of these traces are shown in Figure 16

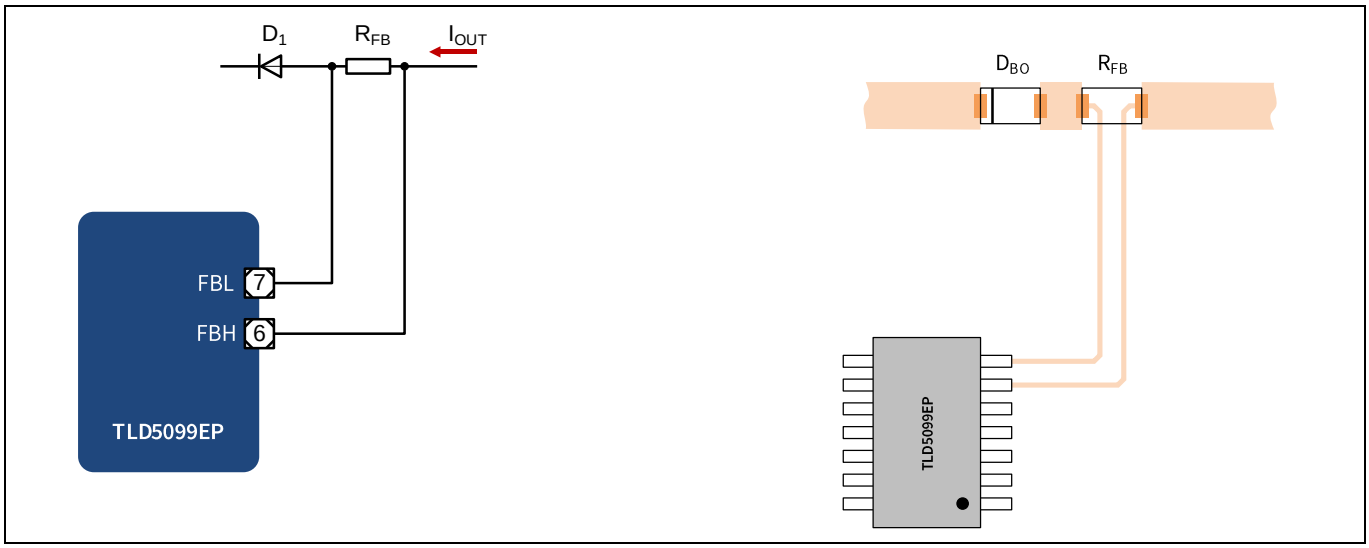


Figure 16 Possible layout of sensing resistor R_{FB}

The path of high impedance pins has to be as short as possible or shielded by the ground plane. High impedance pins sensitive to noise are:

- FPWM
- FBH and FBL
- OVP

Exposed pad aids to dissipate the power through the PCB. Adding several vias under the device to connect the bottom of the package to bottom layer improves the thermal resistance. The diameter of the vias has to be carefully selected with the PCB manufacturer: holes too big suck the tin paste during the welding process and produce voids under the device, lowering the expected thermal performances; holes too small are not completely filled during welding process, lowering also in this case the expected thermal performances.

A good grounding of the device and of current loop sensing resistor (R_{SWCS}) helps to reduce the noise on the references and improves the regulation and the stability performances. A good grounding means having very low ohmic path (also at high frequency) between the GND pin of the TLD5099EP and the returning pad of R_{SWCS}. A suggested layout is proposed on Figure 17.

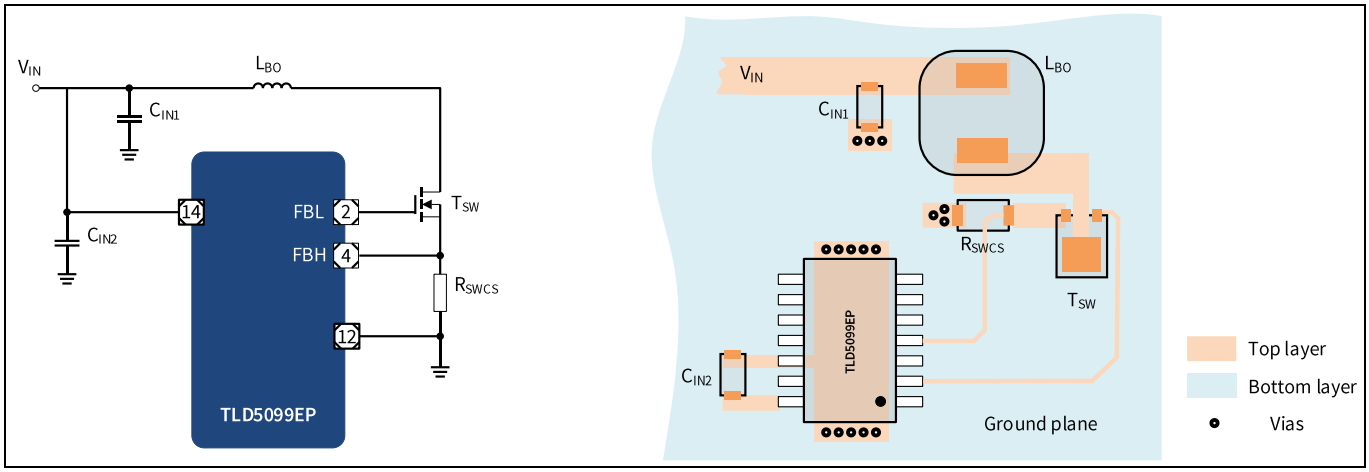


Figure 17 Possible layout of switching path

Discontinuous currents are critical for the electromagnetic interferences. On a boost converter, discontinuous current flows on switching elements (transistor T_{SW} and diode D_{BO}).Particular attention has to be paid when routing these paths. Inductor, switching transistor and rectifier diode have to be placed as close as possible. The switching node (drain of T_{SW}) is sensitive to capacitive coupling due to high dv/dt. Therefore the copper area related to this node shall be minimized. A possible layout solution with switching transistor in TDSON-8 package is proposed in Figure 18.

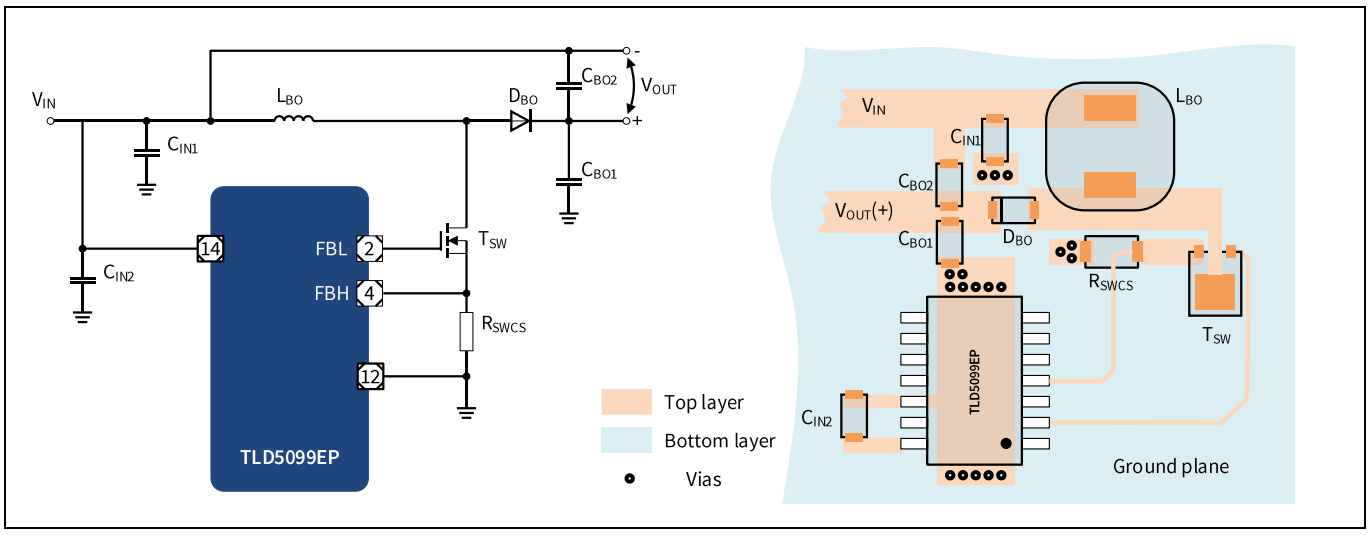


Figure 18 Possible layout solution with transistor in TSDON-8

Revision history

Major changes since the last revision

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