OPTIREG™ switcher TLS412xD0EPVxx demoboard

Z8F68163134


Family overview


Support

Preface

Scope and purpose

This document describes the usage of the OPTIREG™ switcher TLS412xD0EPVxx demoboard for the OPTIREG™ switcher TLS412xD0EPVxx family from Infineon Technologies AG. Please also refer to the corresponding datasheets.

Intended audience

This document is intended for engineers who develop applications.

Table of contents

1 Introduction

1.1 General description

The OPTIREG™ switcher TLS412xD0EPVxx is a family of synchronous step down regulators especially designed for automotive applications.

The devices reduce the required amount of external components and thus system cost and board space due to:

- integrated power stages
- soft-start feature
- integrated compensation networks

The wide input voltage range and a 100% duty cycle operation mode make the devices suitable for battery cranking scenarios in automotive applications. The wide switching frequency range allows the selection of appropriate coils and capacitors. The switching frequency can be synchronized to an external clock signal. Spread spectrum frequency modulation can be activated to improve the EMI performance in PWM operation. The devices offer low current consumption in PFM mode at light loads to optimize efficiency. The OPTIREG™ switcher TLS412xD0EPVxx can detect undervoltage and overvoltage conditions of the output voltage and indicate this via the reset output signal. Overcurrent and overload protection avoid excessive current to protect the device in short circuit condition at the buck converter output. The integrated thermal shutdown feature protects the device from overheating. The enhanced PG-TSDSO-14 exposed pad package offers advantageous thermal performance in the application.

This demoboard supports all members of the OPTIREG™ switcher TLS412xD0EPVxx family, see ***Table 1***. For each product of the family, the demoboard is available in two different configurations. One configuration is populated with passive components to support the low switching frequency (LF) region of the device, while the other configuration supports the high switching frequency (HF) region.

Table 1 OPTIREG™ switcher TLS412xD0EPVxx family overview

Sales name	Output current	Output voltage
TLS4120D0EPV33	2 A	3.3 V
TLS4120D0EPV50	2 A	5.0 V
TLS4120D0EP	2 A	adjustable (3 V to 10 V)
TLS4125D0EPV33	2.5 A	3.3 V
TLS4125D0EPV50	2.5 A	3.3 V
TLS4125D0EP	2.5 A	adjustable (3 V to 10 V)

1.2 OPTIREG™ switcher TLS412xD0EPVxx features

- Input voltage from 3.7 V to 35 V
- Current capability up to 2.5 A
- ±1.5% feedback voltage accuracy in PWM mode
- Ultra low current consumption: typically 31 µA
- Integrated high side and low side power MOSFETs
- Peak current mode PWM regulation
- Light load PFM mode with improved efficiency
- Switching frequency range: 320 kHz to 560 kHz or 1.6 MHz to 2.8 MHz
- 100% duty cycle operation
- Synchronization input
- Spread spectrum frequency modulation for improved EMI performance
- Soft-start feature
- Integrated compensation network
- Output discharge function in disabled state
- Ultra low current consumption in disabled state: typically 1 µA
- Undervoltage monitoring
- Overvoltage monitoring
- Overcurrent protection and overload protection
- Input undervoltage shutdown
- Wide temperature range T_j = -40°C to 150°C
- Green Product (RoHS compliant)

1.3 Block diagrams

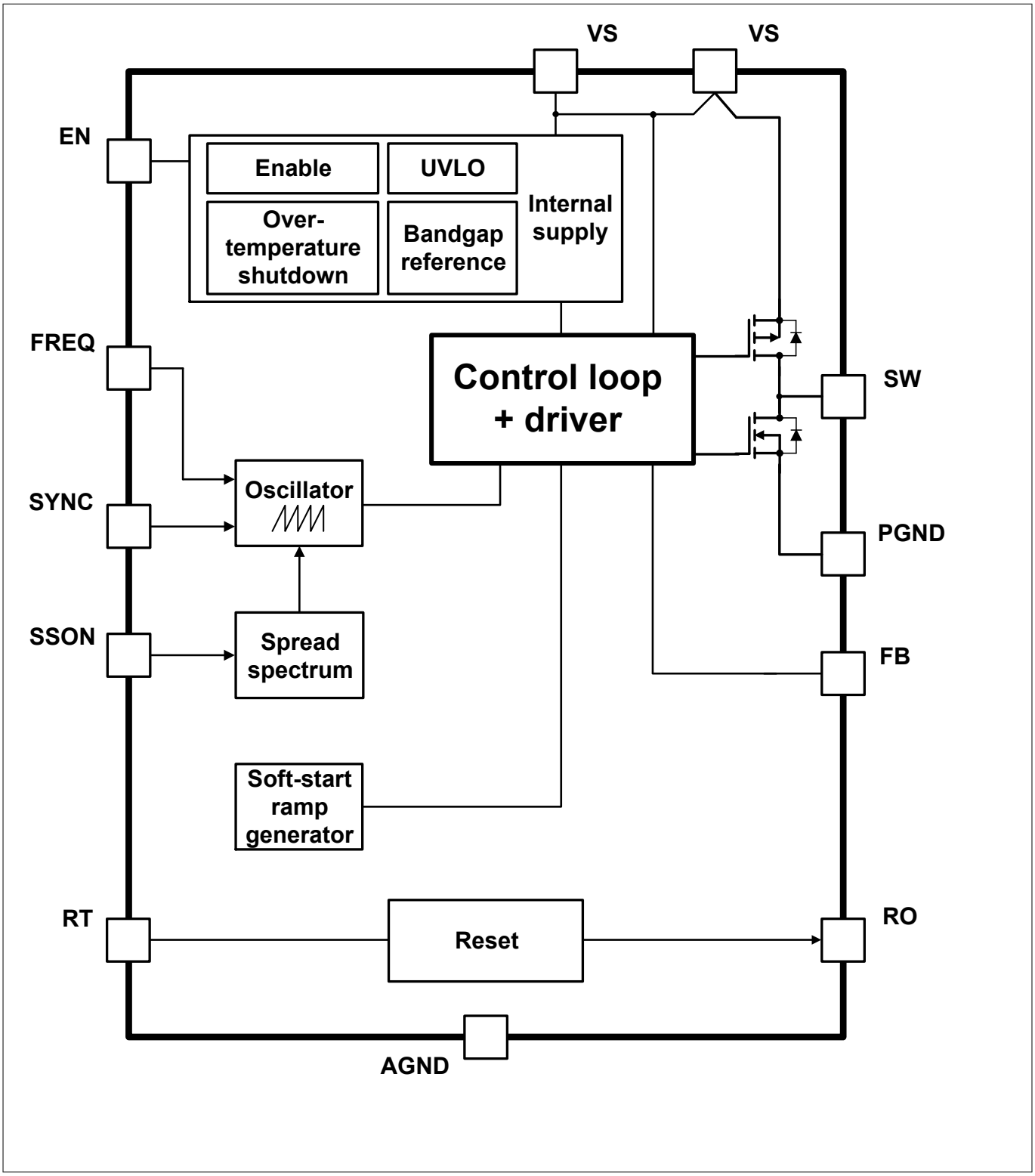

Figure 1 Block diagram fixed output voltage variants

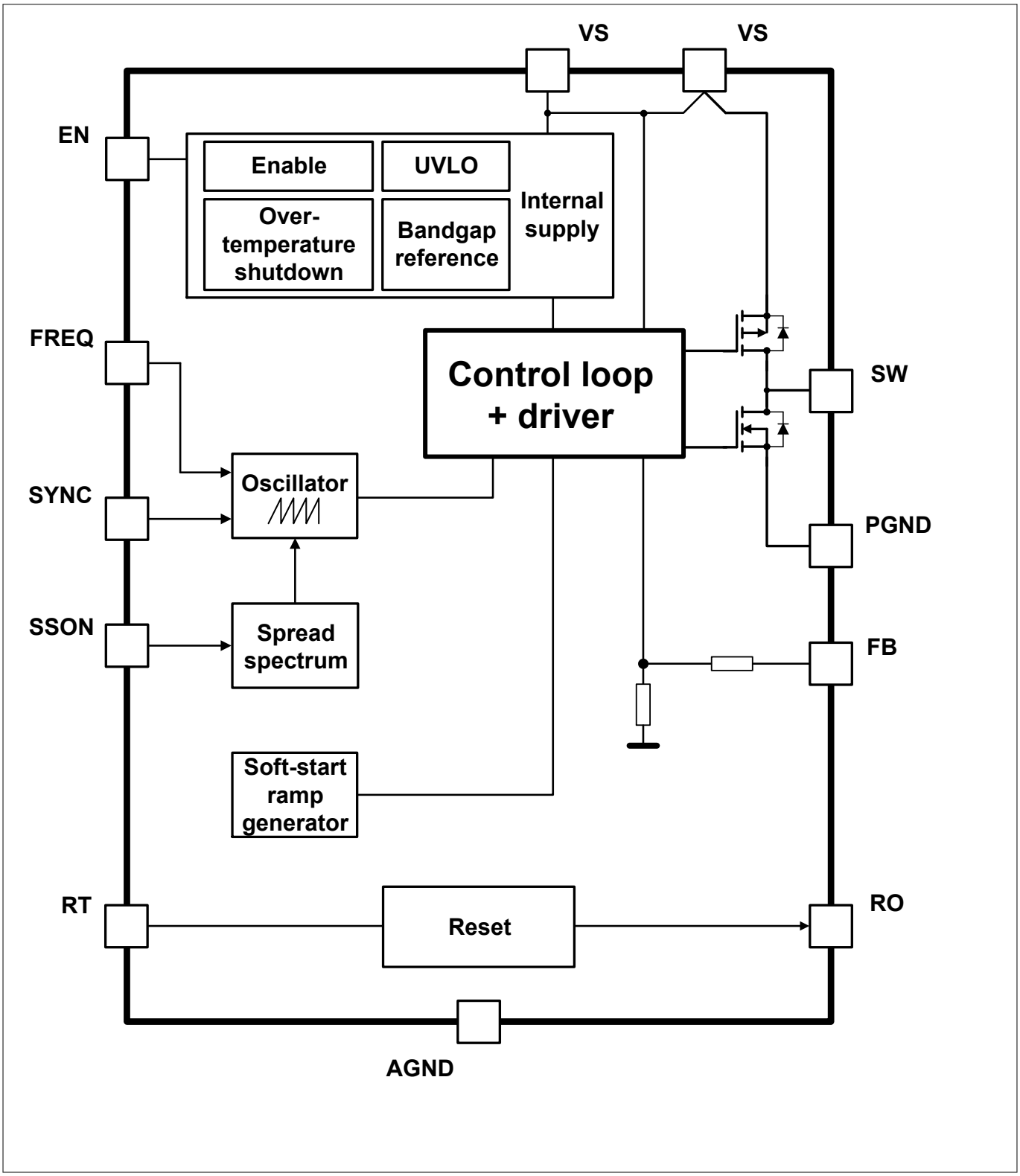

Figure 2 Block diagram adjustable variants

2 Demoboard

2.1 Assembly

There are two different demoboard assemblies available. One for the fixed output voltage variants and one for the adjustable variants. They differ only by the resistor configuration around the FB pin. In addition to these two assemblies, there exist two configurations for each product. One is supporting the low switching frequency (LF) range, while the other supports the high switching frequency range (HF). The difference between these configurations can be seen in the ***Bill of materials***.

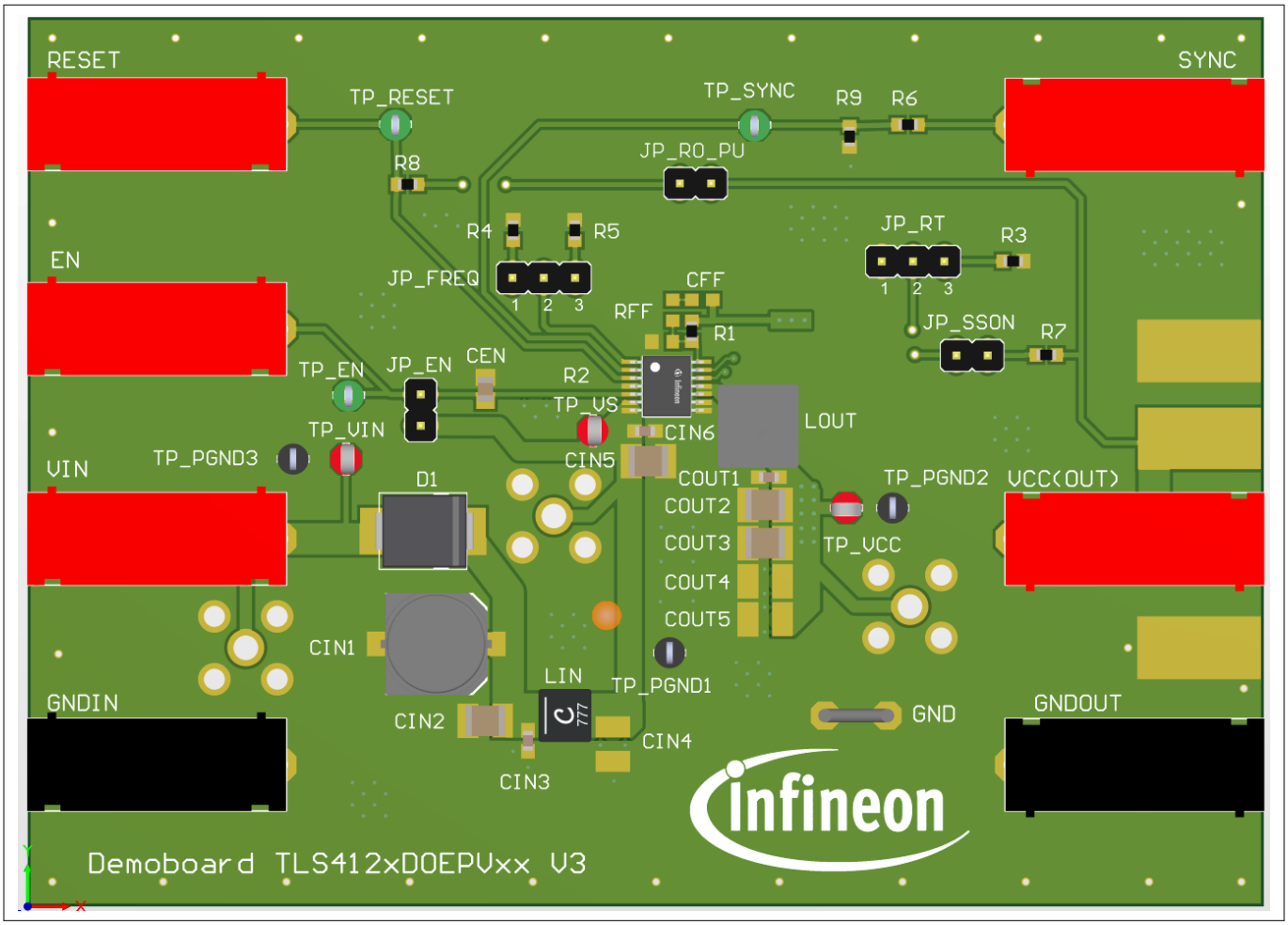

Figure 3 Assembly fixed output voltage variant in HF configuration

Demoboard

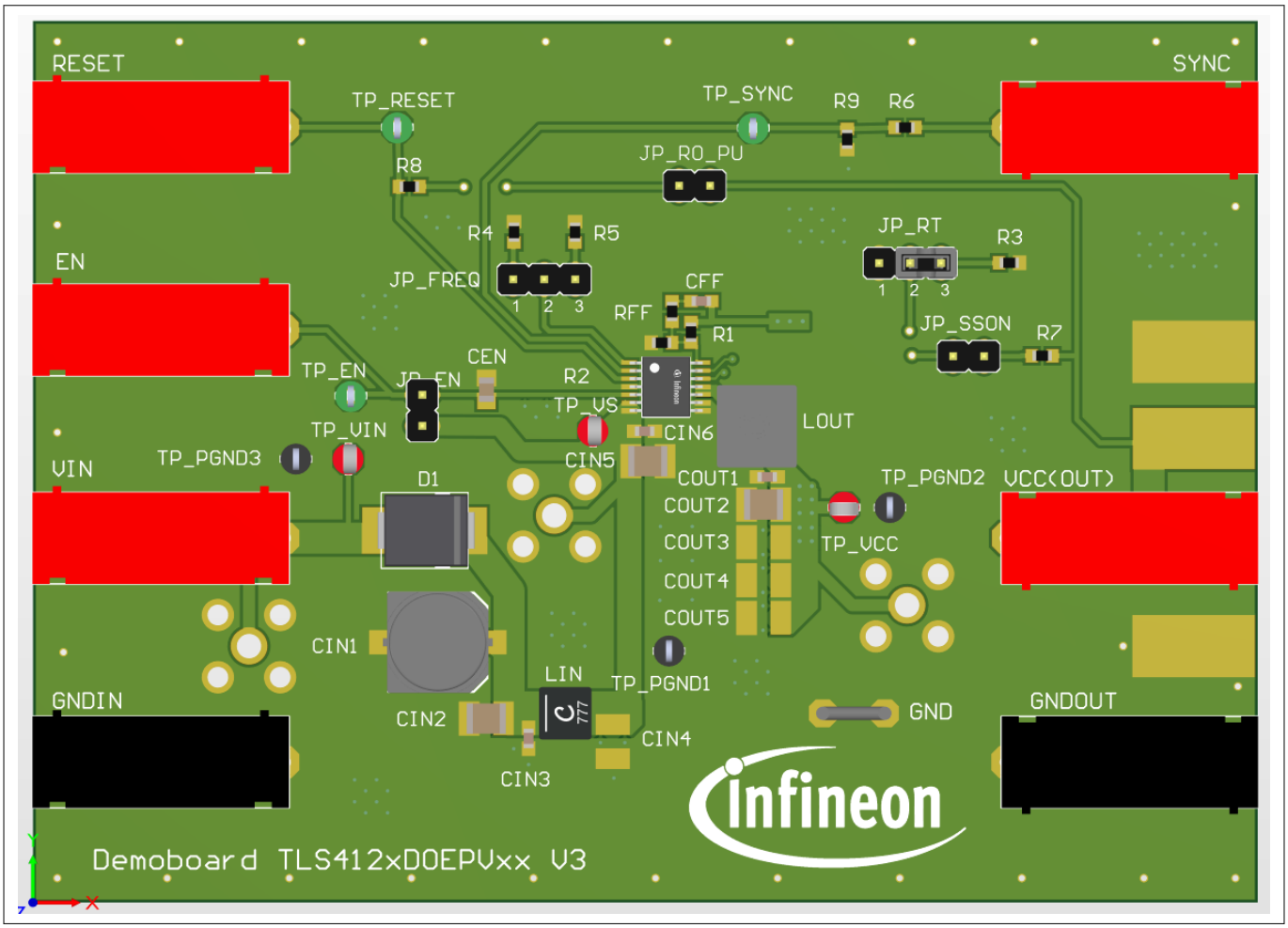

Figure 4 Assembly adjustable output voltage variant in HF configuration

Demoboard

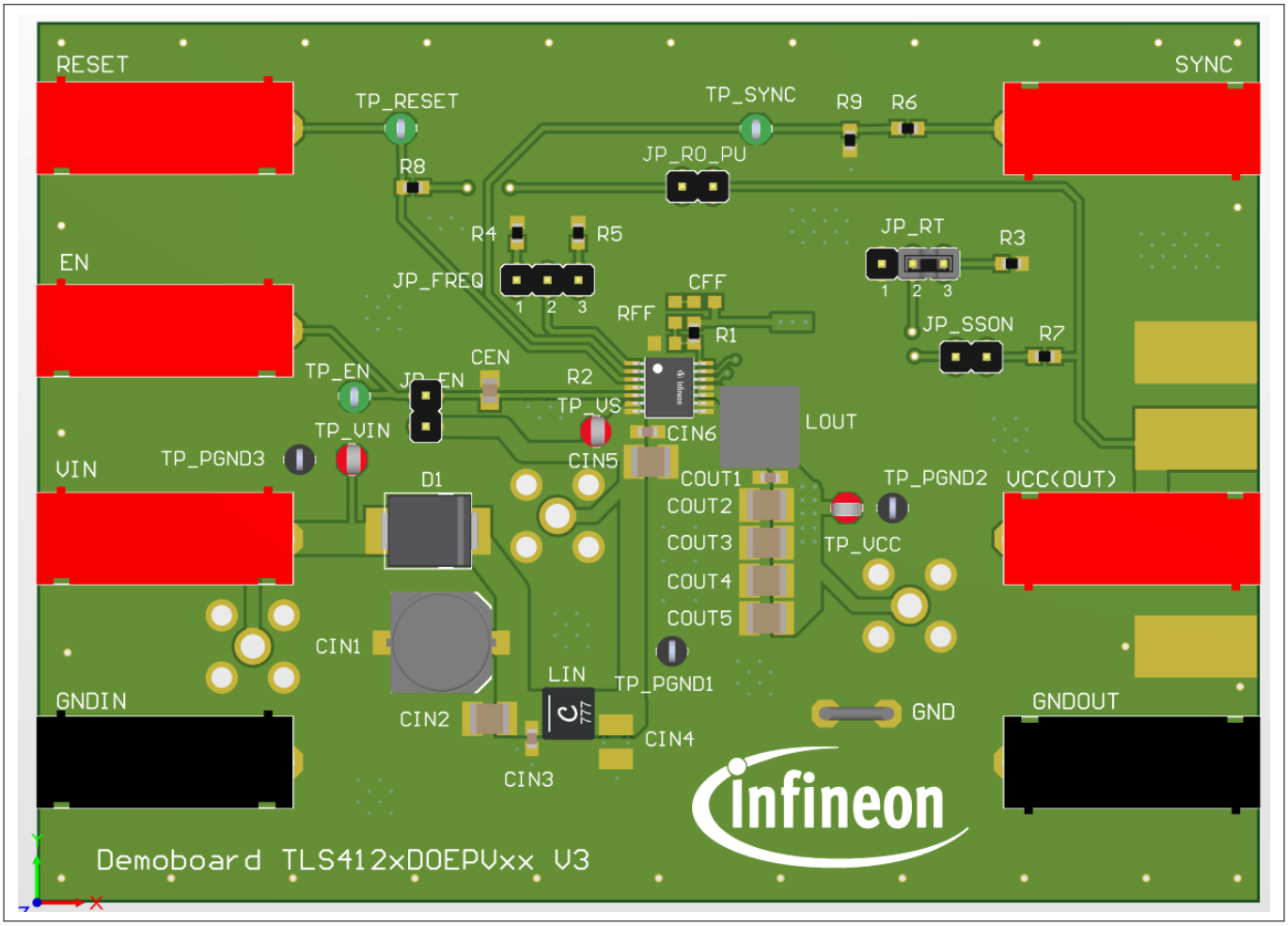

Figure 5 Assembly fixed output voltage variant in LF configuration

Demoboard

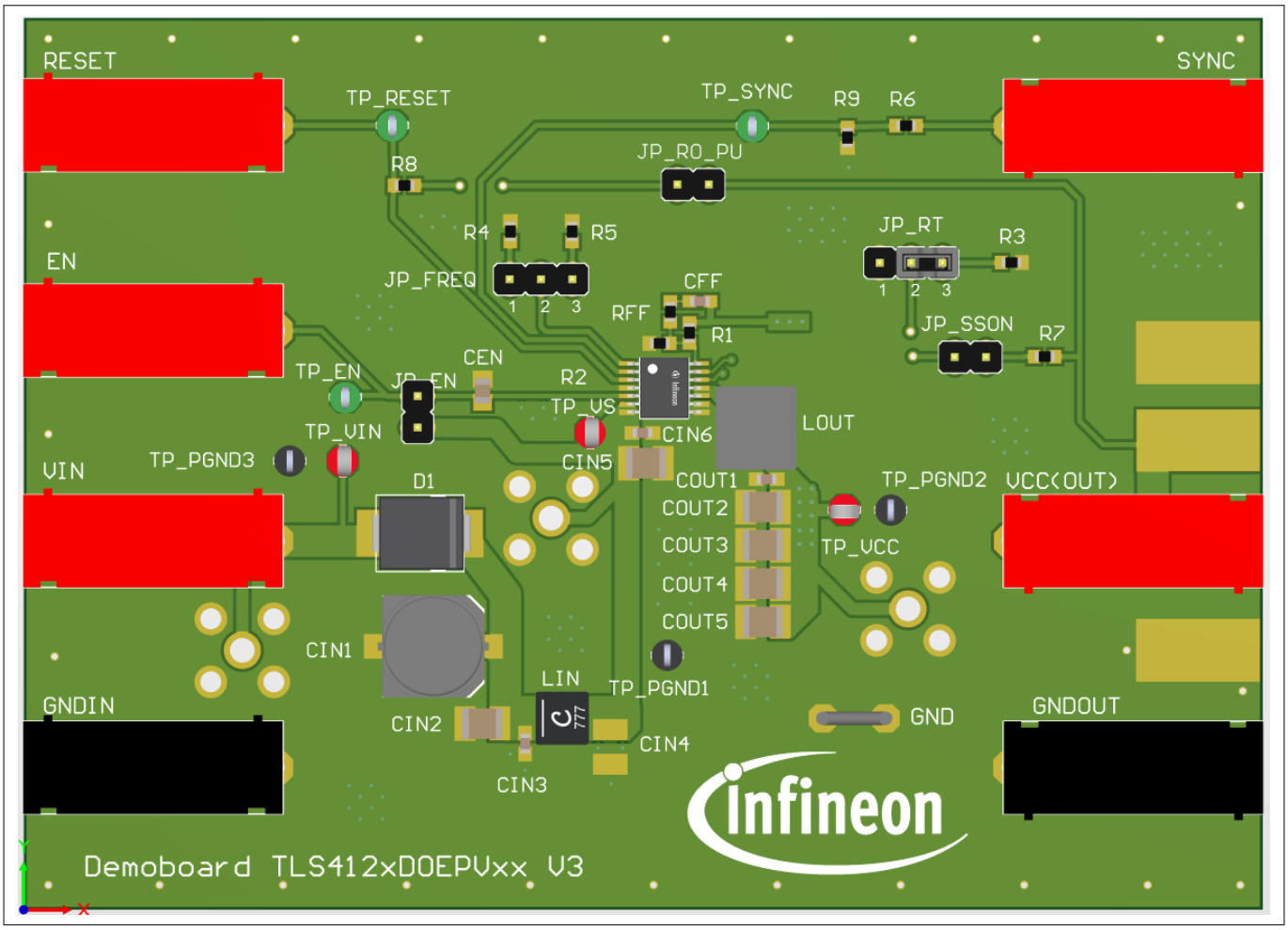

Figure 6 Assembly adjustable output voltage variant in LF configuration

2.2 Operating conditions

To avoid electrical damage of the demoboard, the values in ***Table 2*** must be maintained.

Table 2 Limit values for operation[1)]

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Board supply voltage	V_{IN}	0	–	35	V	–
Output voltage	$V_{CC(OUT)}$	-0.3	–	V_{IN} + 0.3	V	[2)]
Output current	$I_{CC(OUT)}$	0	–	2.5	A	TLS4125D0EPV and TLS4125D0EPVxx variants only
Output current	$I_{CC(OUT)}$	0	–	2	A	TLS4120D0EPV and TLS4120D0EPVxx variants only
Enable	V_{EN}	0	–	35	V	Can be connected to V_{IN} via jumper
Reset, Sync	V_{RO}, V_{Sync}	0	–	5.2	V	TLS412xD0EPV50 and TLS412xD0EP variants only
Reset, Sync	V_{RO}, V_{Sync}	0	–	3.5	V	TLS412xD0EPV33 variants only
Ground voltage	V_{GND}	0	–	0	V	–

1 T_A = 25°C.
2 Absolute maximum rating.

2.3 Configuration

The demoboard can be easily configured via jumpers on the board.

The board provides the following configuration options:

- connect the enable signal EN to VIN
- select the reset undervoltage threshold $V_{RT,UV,th}$ and reset delay time t_{RD}
- determine the switching frequency f_{OSC}
- pull up RO to VCC(OUT) with a resistor
- pull up SSON to VCC(OUT) with a resistor

2.3.1 EN selection

The EN pin can be connected to VIN by placing a jumper as shown in ***Figure 7***. The EN pin is always connected to the external banana plug. When the jumper is placed, do not connect an external signal to EN.

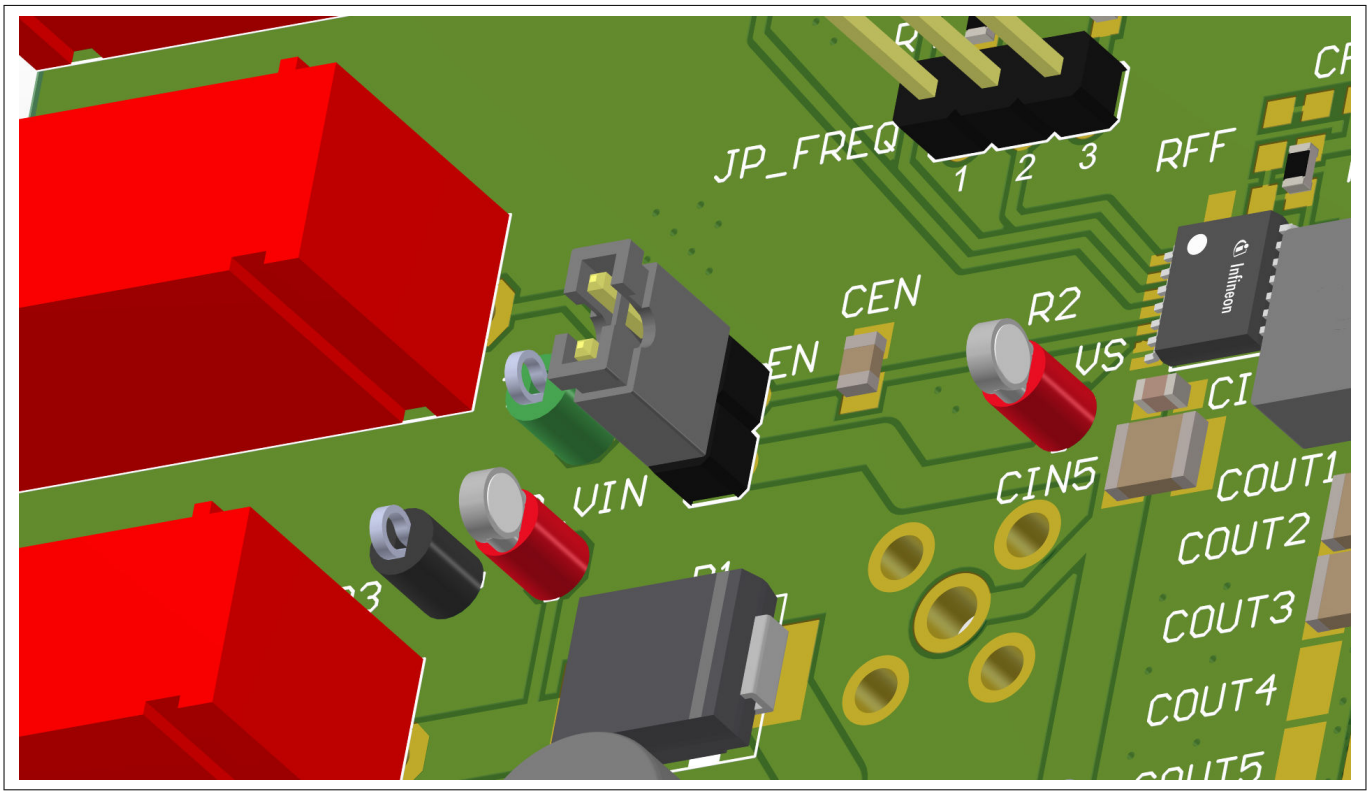

Figure 7 JP_EN jumper used to connect EN to VIN

2.3.2 RT selection

Place the jumper as shown in ***Figure 8*** to choose the following

- undervoltage reset threshold $V_{RT,UV,th}$
- reset delay time t_{RD}

For settings different from ***Table 3***, change the value of resistor R3.

Table 3 JP_RT jumper settings

Jumper setting	$V_{RT,UV,th}$ [% of V_{FB}]	t_{RD} [ms]
1 ↔ 2	-8	0.03
2 ↔ 3	-8	1.3
not placed	-8	5.1

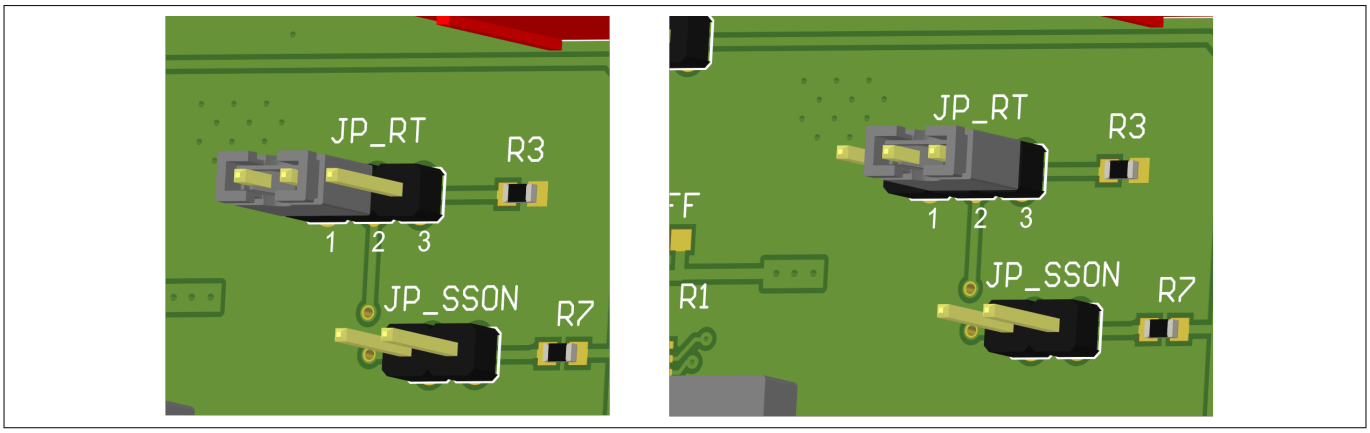

Figure 8 JP_RT jumper placement

2.3.3 FREQ selection

The jumper shown in ***Figure 9*** sets the switching frequency f_{OSC}. The selectable options depend on whether the board is configured for the high switching frequency range (HF) or the low switching frequency range (LF). To allow for different settings than shown in ***Table 4*** and ***Table 5***, change the value of resistor R4 and R5.

Table 4 JP_FREQ jumper settings for HF board configuration

Jumper setting	f_{OSC} [MHz]
1 ↔ 2	1.6
2 ↔ 3	2.8
not placed	2.2

Table 5 JP_FREQ jumper settings for LF board configuration

Jumper setting	f_{OSC} [MHz]
1 ↔ 2	0.440
2 ↔ 3	0.320
not placed	2.2

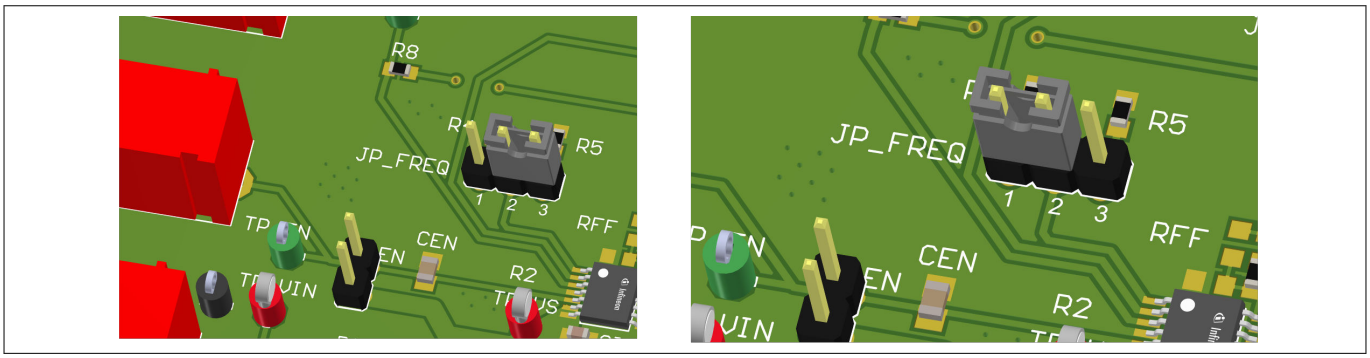

Figure 9 JP_FREQ jumper placement

2.3.4 RO and SSON pull-up resistors

The RO and SSON pins can be pulled up to VCC(OUT) by placing the jumpers JP_RO_PU and JP_SSON, respectively, see ***Figure 10***. When placing the jumper on the adjustable variants TLS412xD0EPV make sure to maintain the ***Operating conditions***. Depending on the nominal output voltage set-point, the functional range criteria might not be fulfilled. In this case, connect a compliant external voltage to the pins via a series resistor. The RO pin is an open drain output. When JP_RO_PU is not placed, then connect an external resistor via the RESET connector to monitor the pin state. Alternatively, the external voltage can be applied to pin 1 of JP_RO_PU to reuse the onboard pull-up resistor R8. Placing the JP_SSON jumper enables the spread spectrum feature.

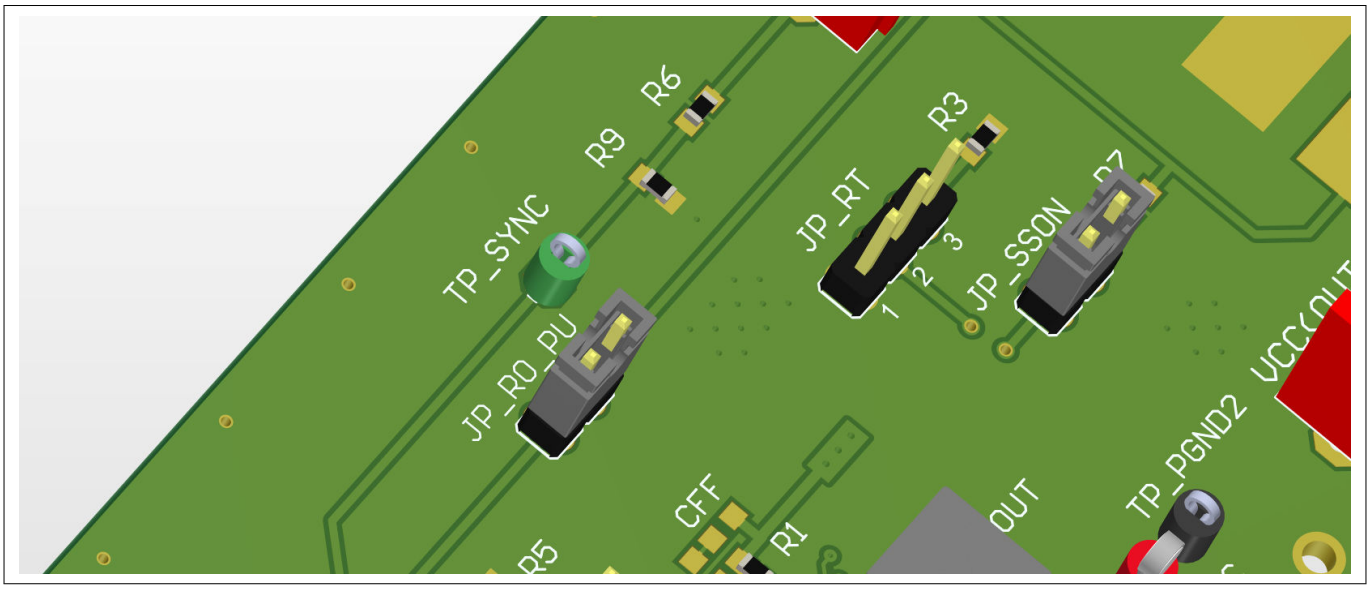

Figure 10 JP_RO_PU and JP_SSON jumpers

2.3.5 Output voltage adjustment

For the adjustable variants TLS412xD0EPV the resistor divider consisting of R1 and R2 sets the nominal output voltage level. The default output voltage level for these variants is 6.45 V. To set a different voltage level change the resistor values according to ***Equation 1***. V_{FB} = 0.8 V (typ) can be assumed.

$$R_1 = R_2\left(\frac{V_{CC(OUT)}}{V_{FB}} - 1\right)$$

Equation 1 Relationship between feedback resistors and output voltage

A feedforward capacitor CFF and a feedforward resistor RFF are placed for the adjustable variants, see ***Figure 11***. For the fixed output voltage variants TLS412xD0EPVxx RFF, CFF and R2 are not placed. For R1 a resistor of 0 Ω shorts the output voltage directly to the FB pin.

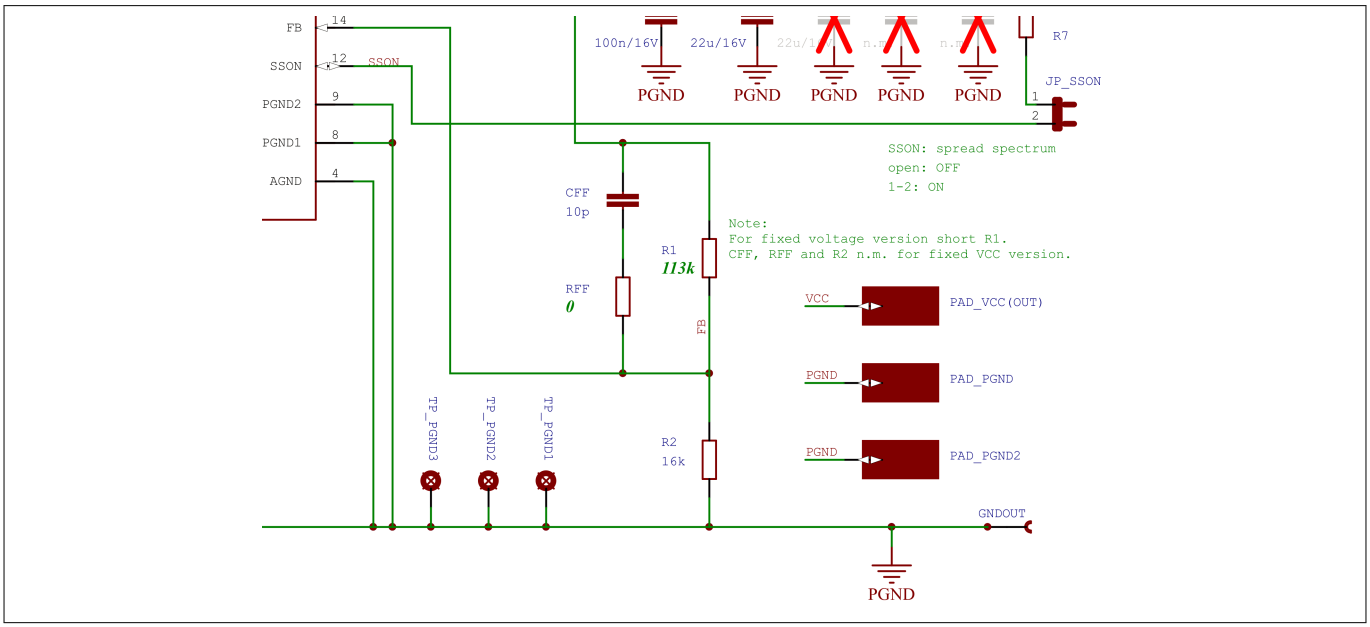

Figure 11 Feedback network for adjustable variants

2.3.6 Signal adaption

For easy signal adaption, for example connecting probes of an oscilloscope, the PCB offers test points. The TP_... label of each test point indicates the probed signal. For further information on the mapping between test points and signals see ***Schematic***. The GND clip of the probe can be attached to the ground clamp as shown in ***Figure 12***.

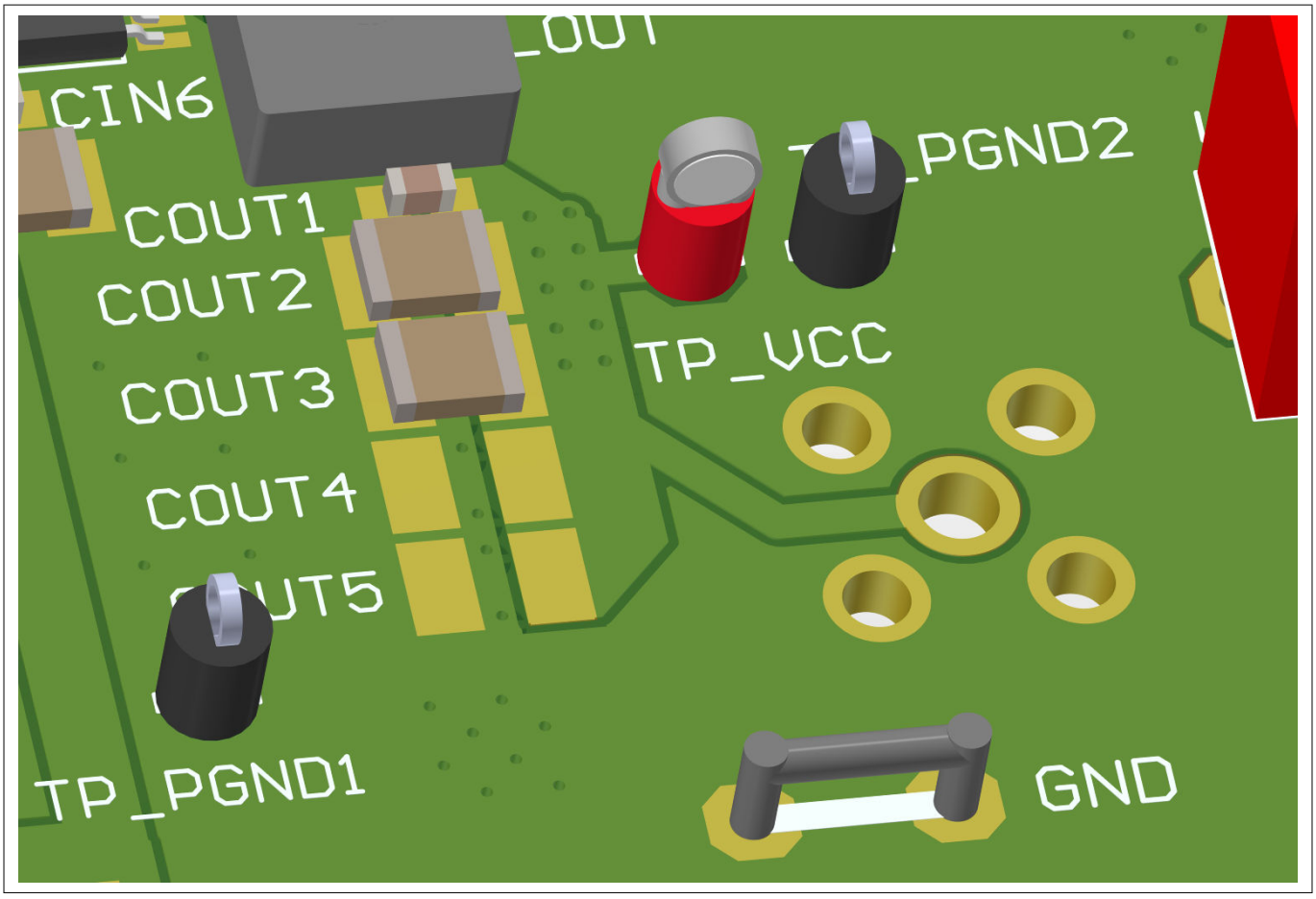

Figure 12 Test point and GND clamp example

3 Schematic and layout

3.1 Schematic

The schematic of the OPTIREG™ switcher TLS412xD0EPVxx demoboard is available in the following variants:

- fixed output voltage variants TLS412xD0EPVxx in HF configuration, see ***Figure 13***
- fixed output voltage variants TLS412xD0EPVxx in LF configuration, see ***Figure 14***
- adjustable variants TLS412xD0EPV in HF configuration, see ***Figure 15***
- adjustable variants TLS412xD0EPV in LF configuration, see ***Figure 16***

Parts not mounted are optional and marked with a red cross.

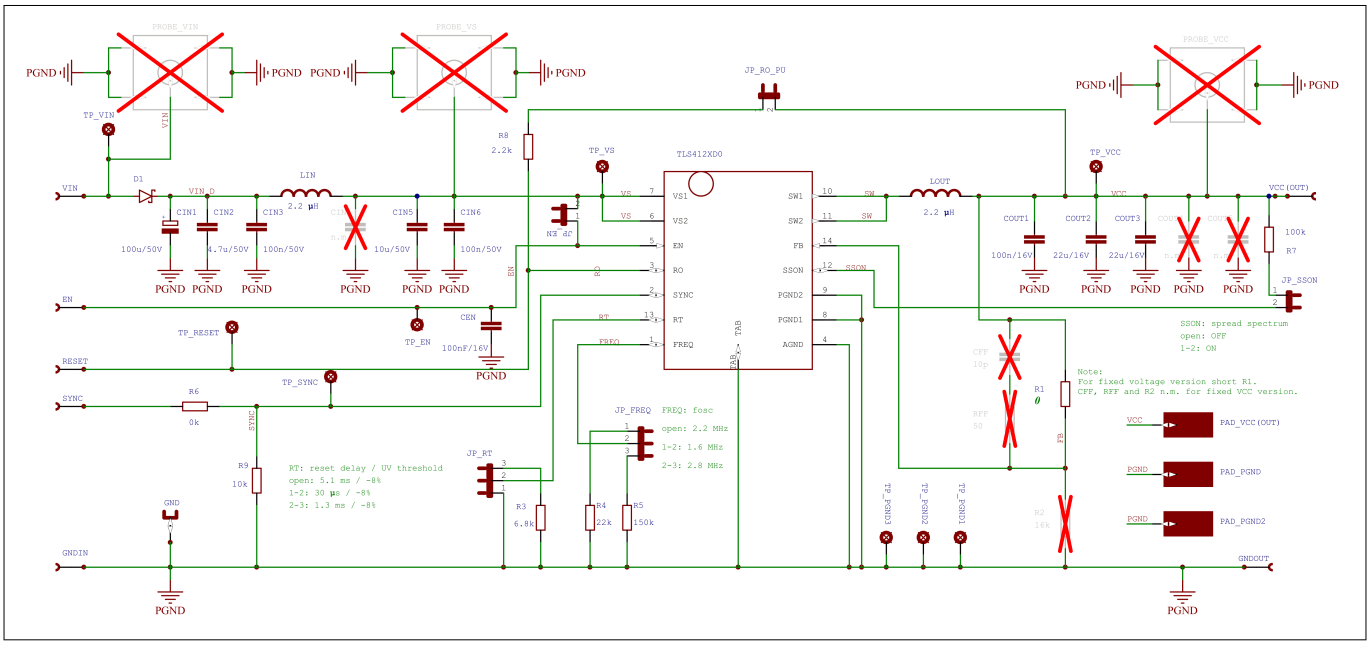

Figure 13 Schematic for fixed output voltage variants in HF configuration

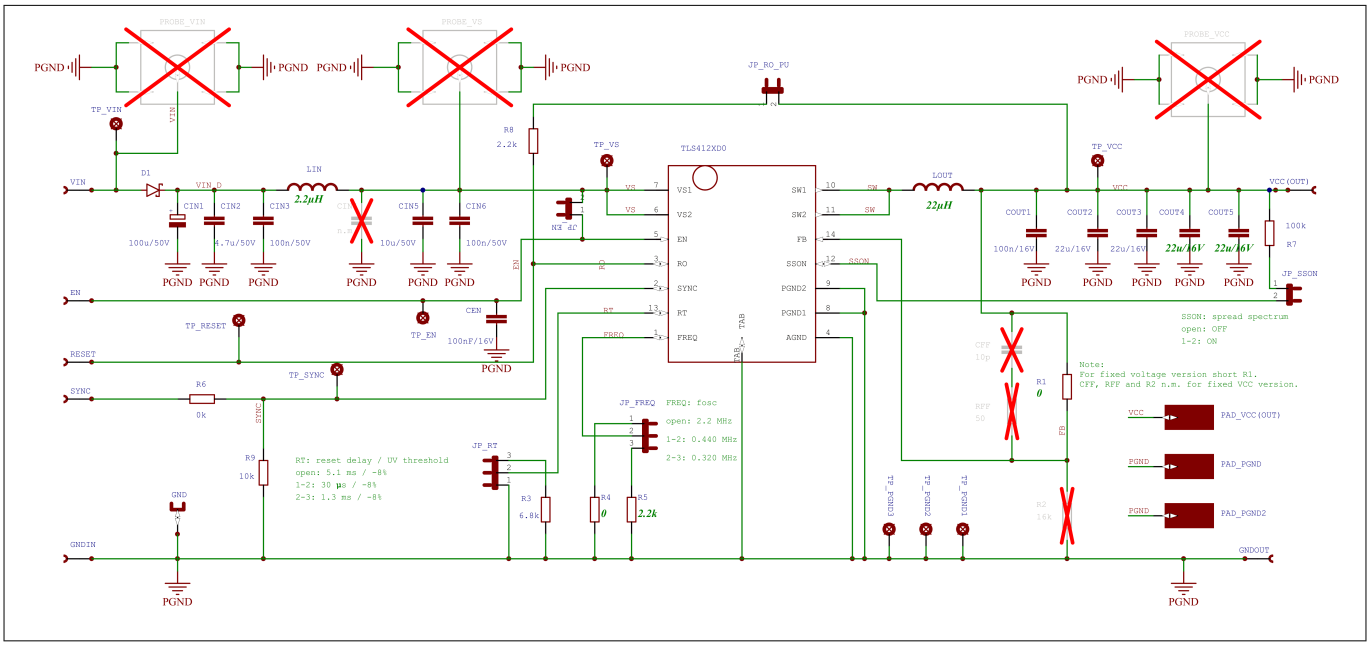

Figure 14 Schematic for fixed output voltage variants in LF configuration

Schematic and layout

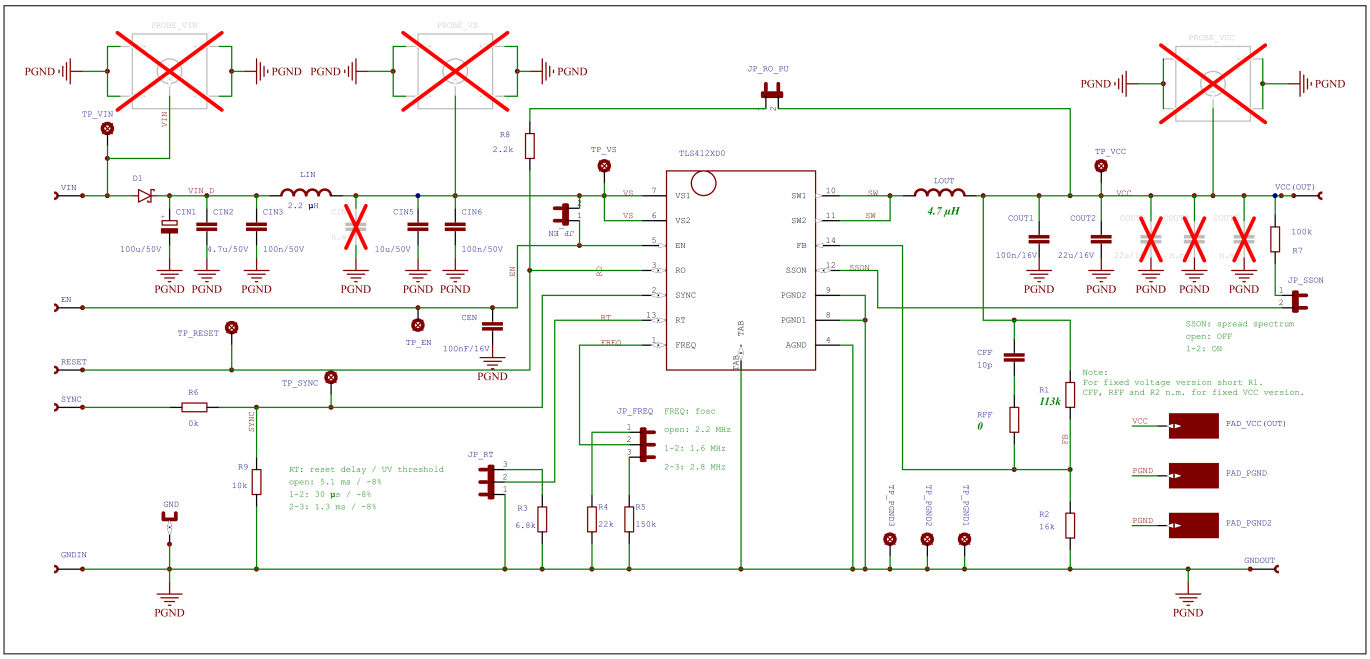

Figure 15 Schematic for adjustable variants in HF configuration

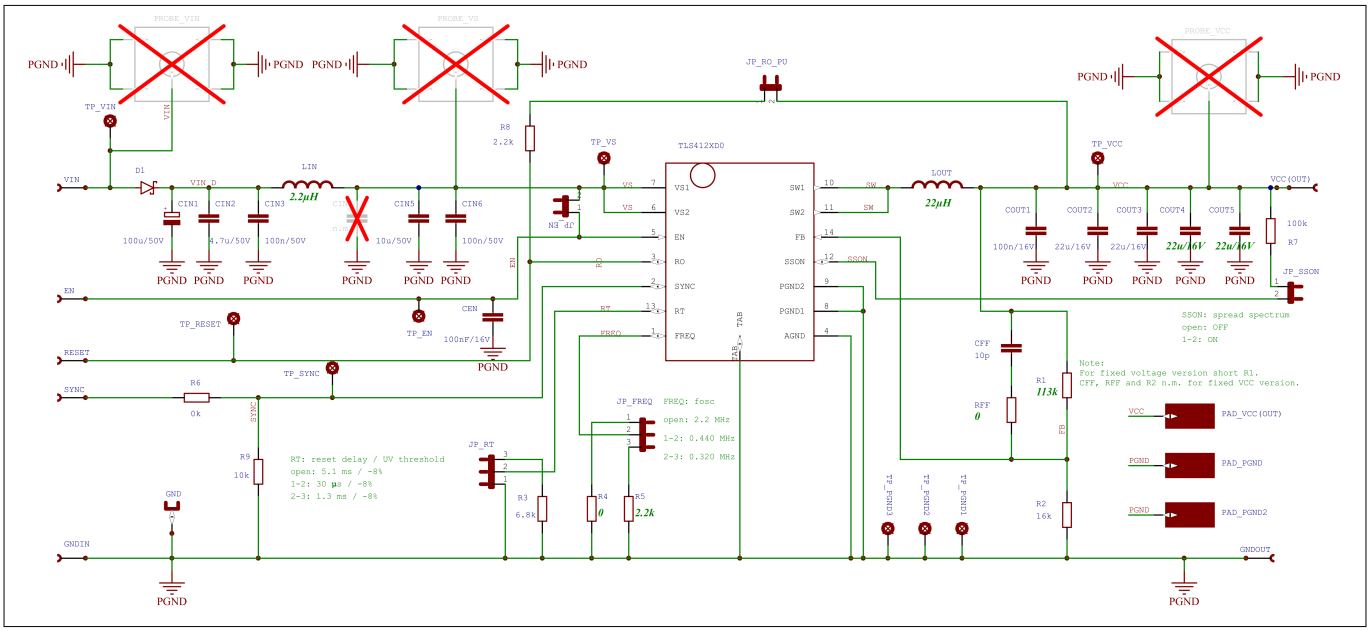

Figure 16 Schematic for adjustable variants in LF configuration

3.2 Layout

The PCB uses a four layer standard stack-up. The product can also be soldered to double layer boards. However, four layers offer better thermal characteristics. The configuration on this demoboard is comparable to the 2s2p thermal interface situation.

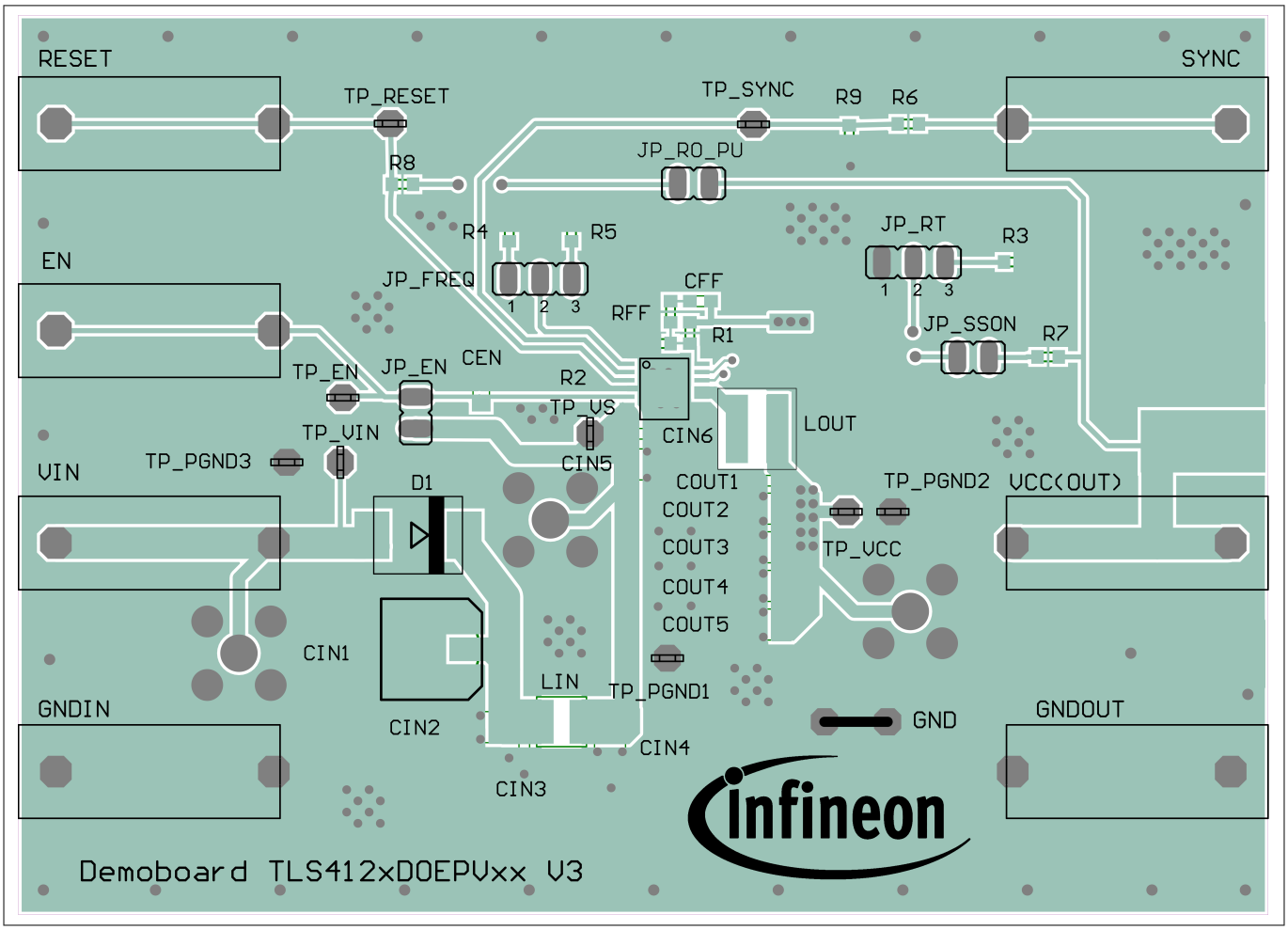

Figure 17 Top layer and components

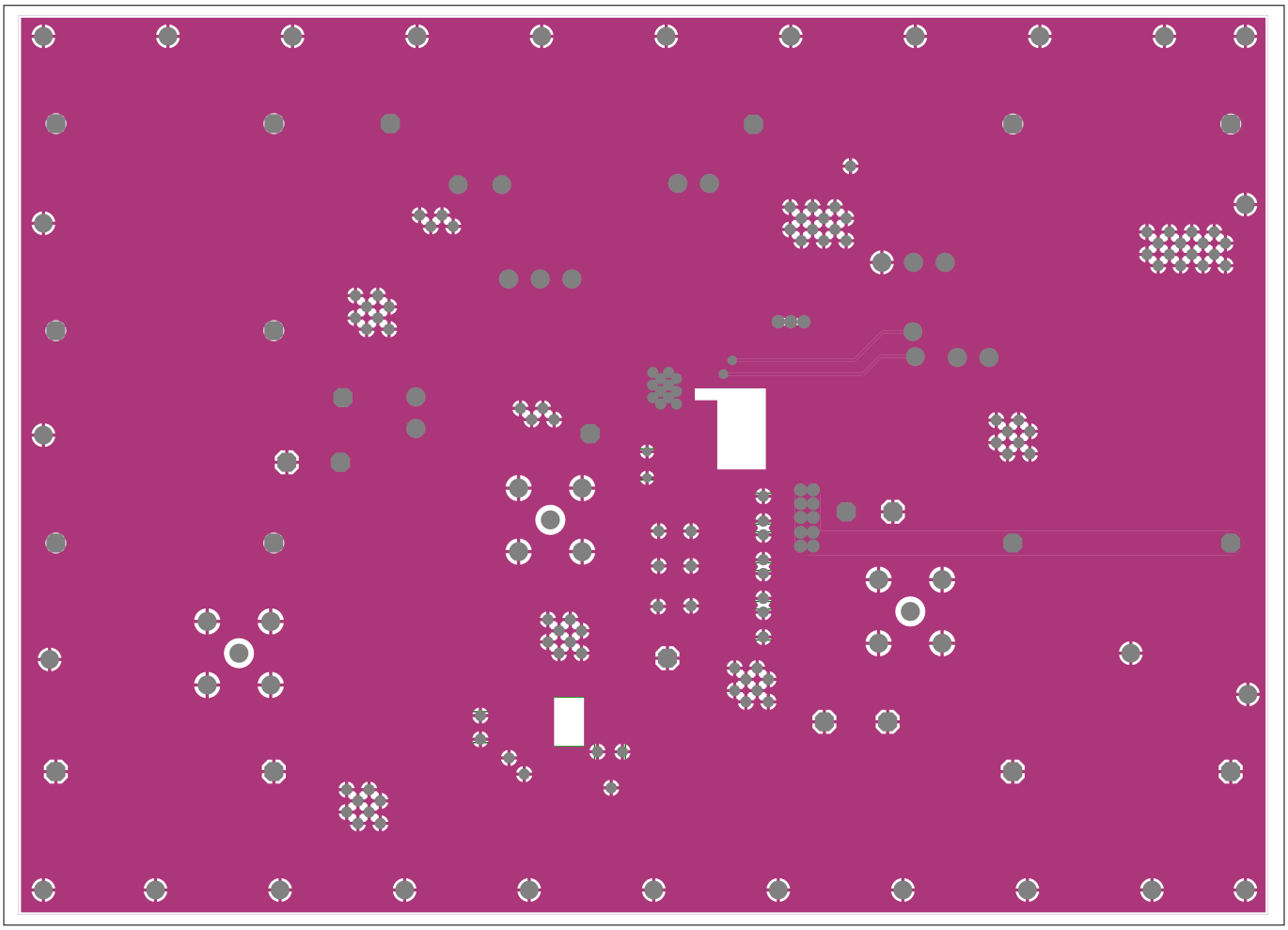

Figure 18 Internal layer 1

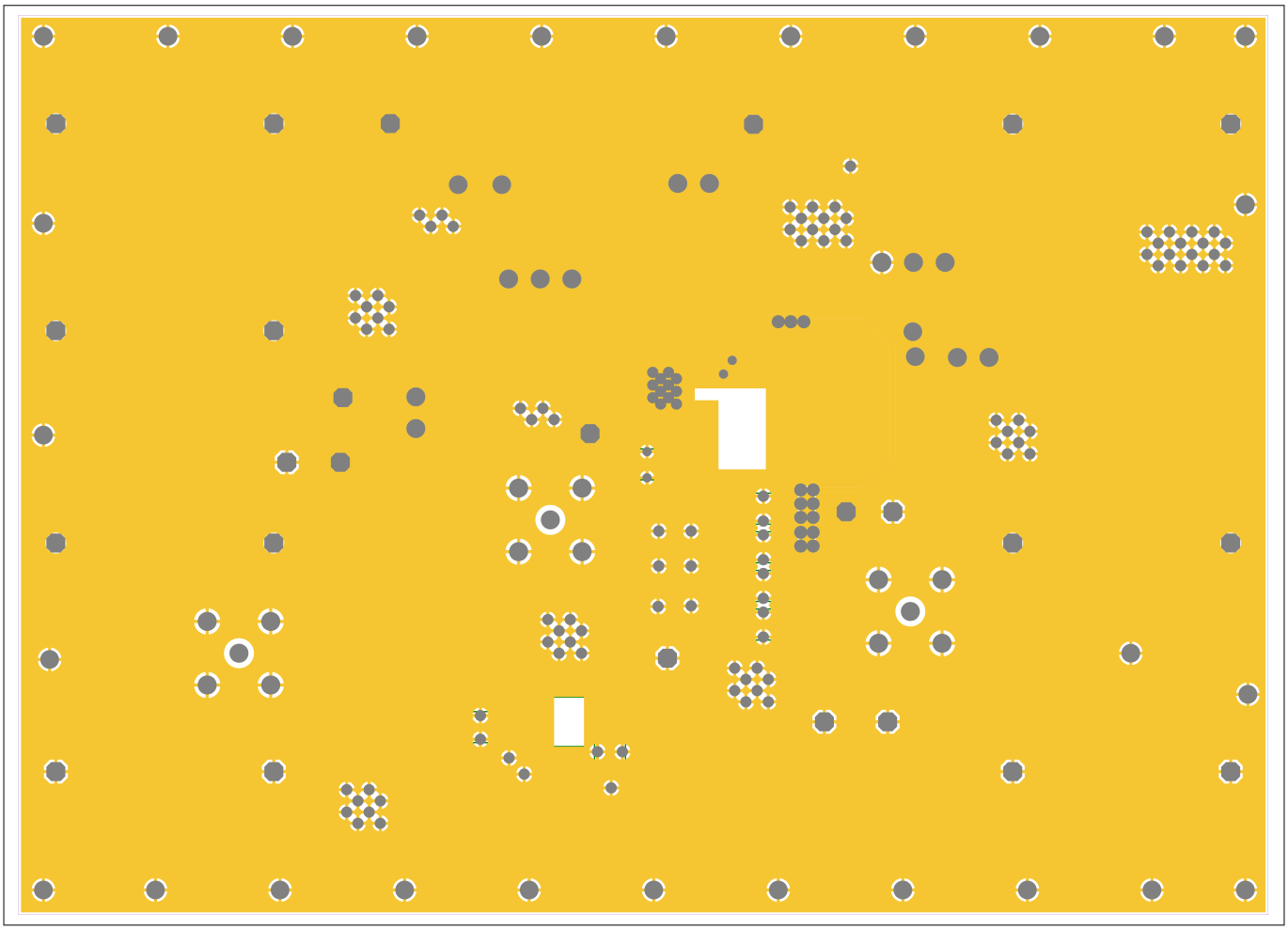

Figure 19 Internal layer 2

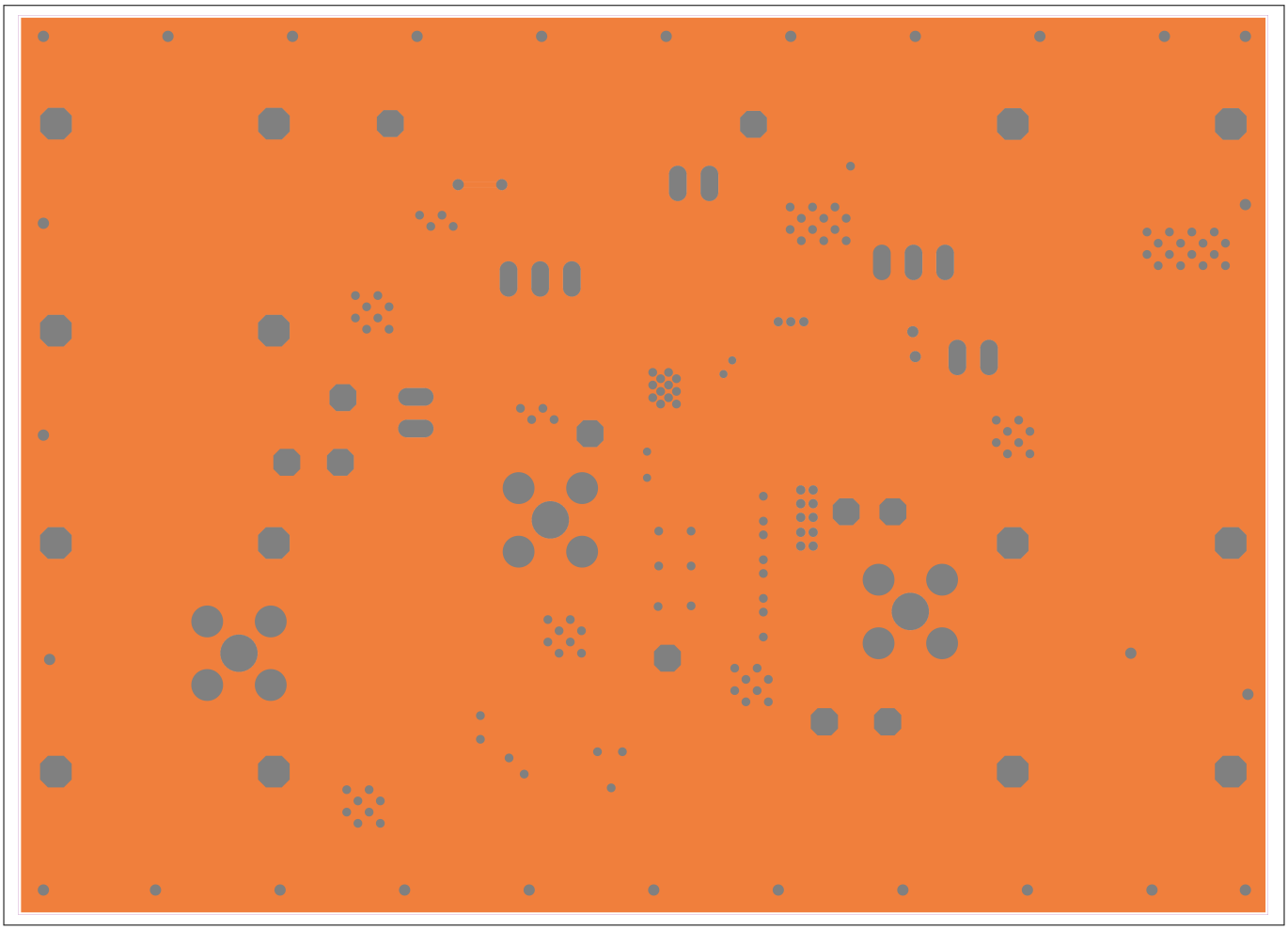

Figure 20 Bottom layer

4 Bill of materials

The bill of materials shows the components on the OPTIREG™ switcher TLS412xD0EPVxx demoboard. For the mounting condition of each component see the ***Schematic***. Mechanical parts, such as connectors or test-points are not mentioned. Note that for each product a low switching frequency range (LF) and a high switching frequency range (HF) configuration is available. The bill of materials is therefore split.

Table 6 Bill of materials of common components for LF and HF configuration

Part	Value	Package
CIN3, CIN5, CIN6, COUT1, CEN	100 nF	0603
D1	MBRS340T3	SMC
CIN1	100 µF / 50 V	E12
CIN2	4.7 µF / 50 V	1210
CIN5	10 µF / 16 V	1210
LIN	2.2 µH	TFM252012ALMA2R2M
R3	6.8 kΩ	0603
R6	0 Ω	0603
R1	0 Ω[3]	0603
R2	16 kΩ[4]	0603
R3	6.8 kΩ	0603
R9	10 kΩ	0603
R7	100 kΩ	0603
R8	2.2 kΩ	0603
RFF[4]	0 Ω	0603
CFF	10 pF[4]	0603

Table 7 Bill of materials HF configuration only

Part	Value	Package
COUT2, COUT3[5]	22 µF / 16 V	1210
LOUT	2.2 µH, 4.7 µH[4]	XAL5030-222/XAL6060-472
R4	22 kΩ	0603
R5	150 kΩ	0603

Table 8 Bill of materials LF configuration only

Part	Value	Package
COUT2, COUT3, COUT4, COUT5	22 µF / 16 V	1210
LOUT	22 µH	XAL6060-223

3 113 kΩ for adjustable variants.
4 Only mounted for adjustable variants.
5 Only mounted for fixed output voltage variants.

Bill of materials

Table 8 Bill of materials LF configuration only (continued)

Part	Value	Package
R4	0 Ω	0603
R5	2.2 kΩ	0603

5 Restrictions

This demoboard offers limited features only for evaluation and testing of Infineon products. The demoboard is not an end product or finished appliance, nor is it intended or authorized by Infineon to be integrated into end products. The demoboard may not be used in any production system.

For further information please visit ***www.infineon.com***.

Revision history

Revision	Date	Changes
1.11	2021-02-15	Editorial changes
1.1	2020-06-30	Added LF and HF variant description
1.0	2020-05-27	Document created

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