TLD5099EP

Daytime running light (DRL) driver realized in boost to ground topology

About this document

This document covers the design steps to realize a DC/DC for LED automotive application in boost to ground topology with TLD5099EP.

It describes the equations behind the choice of all the critical components needed.

Scope and purpose

The purpose of this application note is to inform the audience about many aspects related to the design of DC/DC converter for automotive lighting application and then offering a reliable solution with Infineon Technologies products. Moreover, the document address the reader on how to address all the features of TLD5099EP.

Intended audience

This application note is intended for designer engineers who want to better understand how to design a DC/DC in boost to ground topologies.

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1 Introduction

Boost to ground topology is the simplest and first academic example of DC/DC converter; it easily boosts the input voltage to higher output voltage. As a difference from the classic topology, LED driver controller regulates a constant current instead of a constant voltage. TLD5099EP is multitopology controller that can easily address this topology.

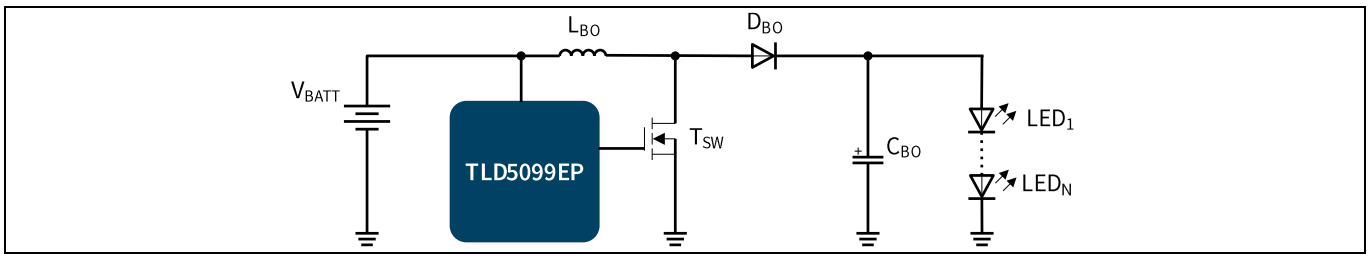


Figure 1 Boost to ground topology simplified

As a boost regulator, it only generates higher voltage at the output than input voltage. The voltage of LED string at the output has to be higher than the input voltage also during load dump battery transient. If input voltage is higher than output, a direct path from the battery to the output is present, then LED string could be damaged.

1.1 Application example

LED driver module (LDM) with TLD5099EP presented in this note is for automotive application and it has to fulfil the following requirements:

Table 1 LDM requirements

Functions	Daytime running light and position light
Number of LED	12 (Seoul Semiconductor WICOP-C SWW0CS07S)
LED current	350 mA
Current ripple	+/- 1%
PWM frequency	350 Hz
Duty Cycle of PWM when position light is switched on	10%
Switching frequency	400 kHz
EMC requirements	CISPR class V
Voltage supply	8-26 V without degradation on output current (typical value is 13.5)

The module can work with every kind of white LED with 3 V forward voltage and current ratings higher than 350 mA. Thermal management of LED has to be taken into account by the user.

2 Main regulator design

During the design of DC/DC there are few parameters that are needed as a base for defining and selecting electronic components and devices. The duty cycle (DC) of the PWM of the main regulator is one of these; it is derived by the minimum and maximum voltage of the input and output. The formula for a voltage mode boost converter is

$$DC = 1 - \frac{V_{IN}}{V_{OUT}}$$

V_{OUT} is derived from the equivalent model of LED as depicted in Figure 2.

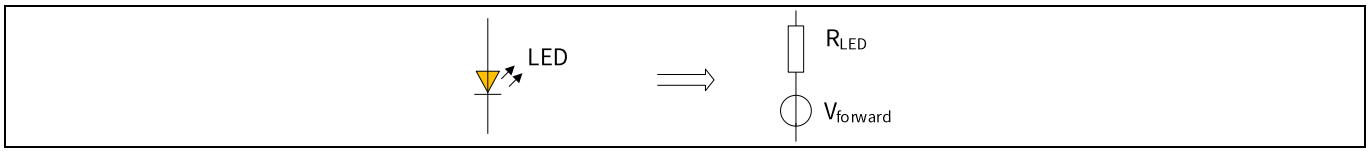


Figure 2 Equivalent circuit of LED

LED string can be considered as an equivalent voltage source with an equivalent series resistor (Thevenin equivalent circuit transformation). The equivalent voltage source is the sum of all forward voltage of the LEDs in the string, while the equivalent resistor is the sum off all resistors plus the feedback resistor, which is neglected at this point. The LED resistor is calculated as incremental ratio of voltage versus current in the around of working point. Forward voltage is calculated as the intercept on x-axis of the line tangent to the curve on the desired working point.

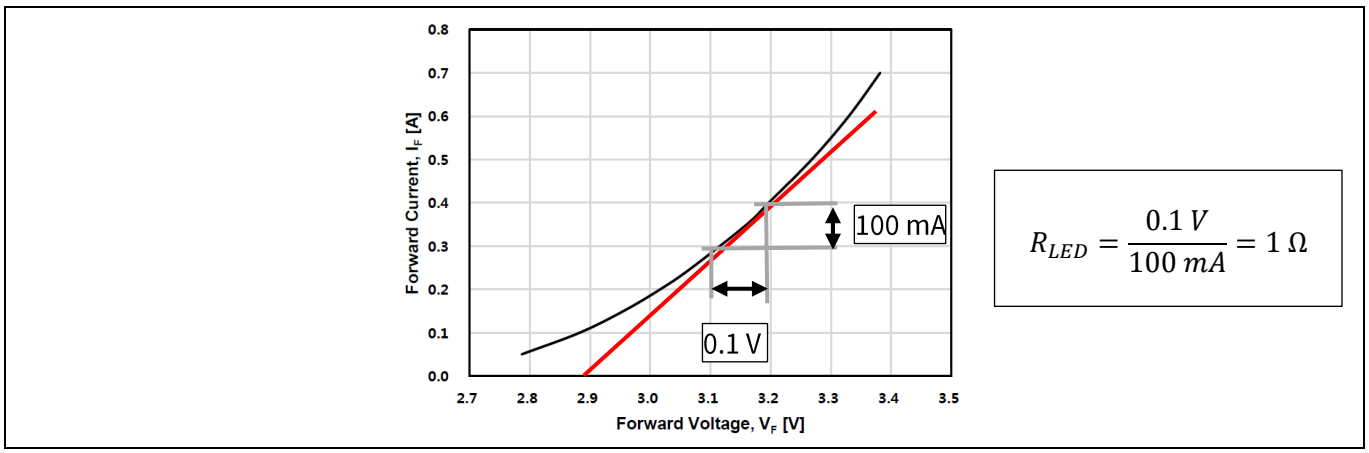


Figure 3 LED characteristic curve

For the LED considered in this application note, the load can be described in a typical condition by the equivalent parameters below

$$V_{LED} = (number\ of\ LED) \cdot V_{forward} = 12 \cdot 2.9\,V = 34.8\,V$$

$$R_{LED} = (number\ of\ LED) \cdot R_{LED} = 12 \cdot 1\,\Omega = 12\,\Omega$$

$$V_{OUT} = V_{LED} + R_{LED} \cdot I_{OUT} = 34.8\,V + 12\,\Omega \cdot 0.35\,mA = 39.0\,V$$

The possible values of duty cycle can be calculated for the different input voltages

Table 2 Duty cycle vs. input voltage for VOUT_TYP = 39. 0V

V_{IN_MIN} = 8 V (Transient undervoltage)	79%
V_{IN_TYP} = 13.5 V	65%
V_{IN_MAX} = 26 V (Jump start)	33%

Another value to take into account is the average input current as a function of battery voltage. The maximum average input current is needed to define the ratings of many components, while the minimum is needed to check if the converter works in discontinuous conduction mode. The average current (maximum, typical and minimum) is estimated by the formulas below, by supposing 90% of overall efficiency

$$< I_{IN\_MAX} >= \frac{P_{OUT}}{V_{IN\_MIN} \cdot \eta} = \frac{V_{OUT} \cdot I_{OUT}}{V_{IN\_MIN} \cdot \eta} = \frac{39\ V \cdot 0.35\ A}{8\ V \cdot 0.9} = 1.90\ A$$

$$< I_{IN\_TYP} >= \frac{P_{OUT}}{V_{IN\_TYP} \cdot \eta} = \frac{V_{OUT} \cdot I_{OUT}}{V_{IN\_TYP} \cdot \eta} = \frac{39\ V \cdot 0.35\ A}{13.5\ V \cdot 0.9} = 1.12\ A$$

$$< I_{IN\_MIN} >= \frac{P_{OUT}}{V_{IN\_MAX} \cdot \eta} = \frac{V_{OUT} \cdot I_{OUT}}{V_{IN\_MAX} \cdot \eta} = \frac{39\ V \cdot 0.35\ A}{26\ V \cdot 0.9} = 0.58\ A$$

2.1 Inductor selection

The inductor in a boost converter is selected by fixing a certain ratio between average current and ripple current $\Delta i_{L\_TYP(P\text{-}P)}$ (as peak to peak measurement) in typical condition. Usually, the peak current is in the range of 20% to 40% of the average value (in this application, 30% has been chosen). This value must guarantee the continuous conduction mode when LDM delivers constant current to the load in other possible battery voltages. Then, two equations are needed to choose the correct value of inductor for the DC/DC.

The first equation determines the inductor value to obtain the required ripple current with typical voltage at input.

$$L_{MIN1} \geq D_{TYP} \cdot \frac{V_{IN_{TYP}}}{\Delta i_{L\_TYP(P-P)} \cdot f_{sw}} = 0.65 \cdot \frac{13.5\ V}{2 \cdot 0.3 \cdot 1.12\ A \cdot 400\ kHz} = 32.64\ \mu H$$

The second equation determines the minimum inductor to prevent discontinuous conduction mode when the input current is at minimum (i.e. with maximum input voltage that is the worst condition)

$$L_{MIN2} \geq D_{MIN} \cdot \frac{V_{IN_{MAX}}}{2 \cdot < I_{IN\_MIN} > \cdot f_{sw}} = 0.33 \cdot \frac{26\ V}{2 \cdot 0.58\ A \cdot 400\ kHz} = 18.49\ \mu H$$

The closest standard value that satisfies both equations is 33 µH.

With this value, the actual peak current in worst condition (i.e. when input voltage is at minimum) can be calculated as:

$$\Delta i_{L(P-P)} = D_{MAX} \cdot \frac{V_{IN\_MIN}}{L \cdot f_{sw}} = 0.79 \cdot \frac{8\ V}{33\ \mu H \cdot 400\ kHz} = 0.48\ A$$

Then the maximum peak current into inductor is calculated as:

$$I_{L-MAX} = < I_{IN\_MAX} > + \frac{\Delta i_{L(P-P)}}{2} = 1.90\ A + \frac{0.48}{2}\ A = 2.14\ A$$

The important key parameters to select an inductor are then:

- Inductance > 33 µH
- Saturation current > 2.14 A

An inductor that fulfill the above requirements (nominal inductor value and saturation current) is the TDK CLF12577NIT-680M-D.

2.2 Output capacitor selection

Output capacitor acts as an energy tank when the diode is in reverse polarity and for this reason it is a victim of high ripple current. This component affects the bandwidth of the system and also the current ripple performance at the output. Usually, for this kind of application MLCCs with low ESR are preferred to the electrolytic capacitors.

Figure 4 depicts how the system manages the current into reactive components and LED string.

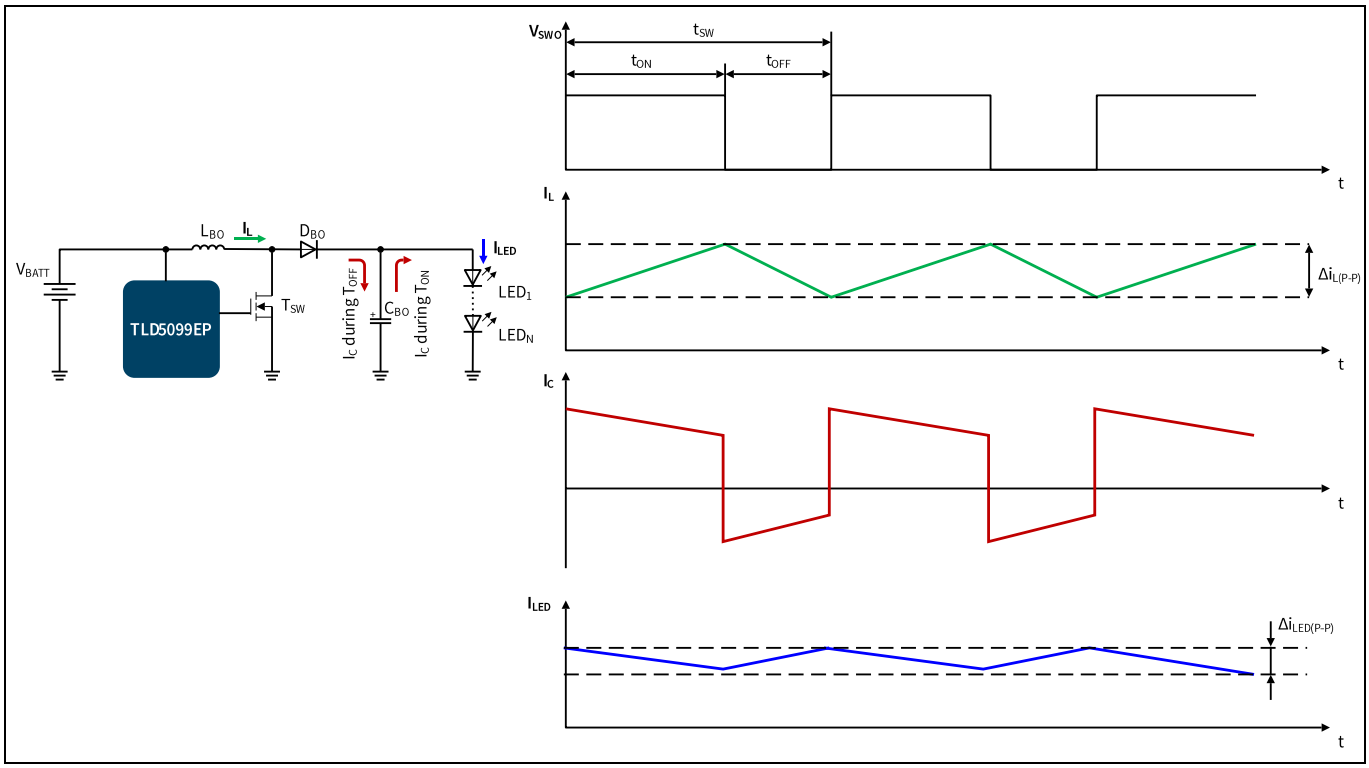


Figure 4 Waveform of current in reactive components and LED string

The output voltage ripple can be approximated by:

$$\Delta V_{OUT} \cong \Delta I_{OUT} \cdot R_{LOAD} = I_{OUT} \cdot ripple_{OUT} \cdot R_{LOAD} = 350\ mA \cdot 0.02 \cdot 12\ \Omega = 0.084\ V$$

Assuming the capacitor is discharged by a constant current (equal to average output current) for a time equal to t_{ON}, its value can be calculate in worst condition when duty cycle is maximum by:

$$C \geq \frac{I_{OUT}}{\Delta V_{OUT}} \cdot \frac{D_{MAX}}{f_{sw}} = \frac{0.35\ A}{0.084\ V} \cdot \frac{0.79}{400\ kHz} = 8.2\ \mu F$$

Also the equivalent series resistor (ESR) of the capacitor affects the ripple of the output voltage.

Its effect can be calculated during two phases:

- During capacitor discharging it can be described by

$$\Delta V_{ESR} = R_{ESR} \cdot I_{OUT}$$

- During the charging phase it can be described by

$$\Delta V_{ESR} = R_{ESR} \cdot (I_L - I_{OUT})$$

To make it negligible (for example less than 10% of the ripple imposed by capacitor), its contribution has to be lower than ΔV_{OUT} on both cases. From the equations above, it is possible to calculate the maximum ERS acceptable by the application.

$$R_{ESR} \leq \frac{\Delta V_{ESR}}{I_{OUT}} = \frac{0.1 \cdot \Delta V_{OUT}}{I_{OUT}} = \frac{0.1 \cdot 0.084\ V}{0.35\ A} = 24\ m\Omega$$

$$R_{ESR} \leq \frac{\Delta V_{ESR}}{I_{L-MAX} - I_{OUT}} = \frac{0.1 \cdot \Delta V_{OUT}}{I_{L-MAX} - I_{OUT}} = \frac{0.1 \cdot 0.084\ V}{2.38\ A - 0.35\ A} = 4\ m\Omega$$

To fulfil both equations, ESR of capacitor bank has to be lower than 4 mΩ that is a reasonable value for a ceramic capacitor. In case, to reduce the value of the ESR resistor, it is common practice to put some capacitors in parallel.

Just a reminder: MLCC capacitors show quite good value of capacitance related to small package and also very good performances related to ESR, but they suffer a dramatic variation of the capacitance as a function of the applied voltage. During the selection take into account this degradation and in such a case, use an adequate parallel of capacitors to overcome this drawback. As an example, in Figure 5 the behavior of TDK CGA9N2X7R2A475K230KA is shown.

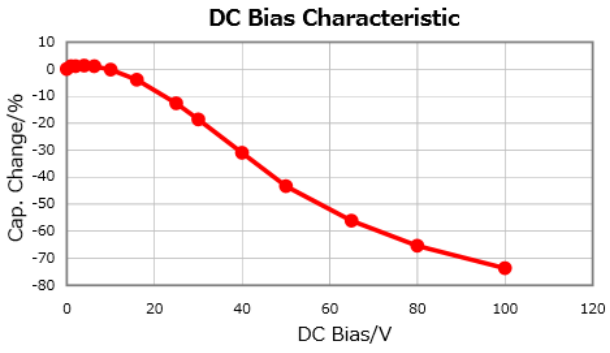


Figure 5 DC bias characteristic of TDK CGA9N2X7R2A475K230KA

The capacitor is rated 100 V to work properly at maximum of V_{OUT} = 39.0 V, but it shows 30% drop of its nominal value.

For the application described into this document, a good choice is n of 4 capacitors in parallel and that means the actual output value at maximum output voltage is 4.7µ * 4 * 0.7 = 13.16 µF

2.3 Input PI filter

PI filter is a common choice to filter out the undesired frequency components that affect the spectrum in the standardize bands.

As reported in application example chapter, this board fulfills the requirement of CISPR 25 class V standard.

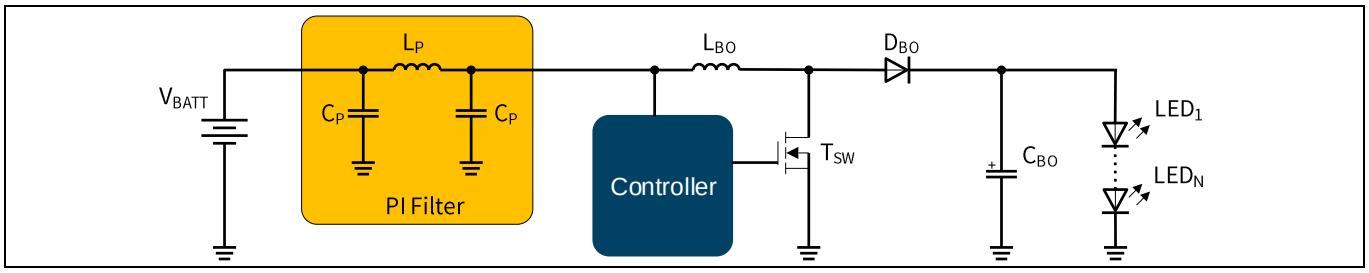


Figure 6 PI filter schematic simplified

Parasitic effects on capacitors and inductor shape the frequency response of PI filter and for this reason, it works fine up to 5-10 MHz; above this frequency, good PCB layout helps a lot on EMI emission. To achieve good results, damping zone of the filter has to be put where harmonics of switching frequency could exceed the limits related to the standard; usually harmonics of switching frequency causes problems in AM band.

To design the PI filter, the following rules of thumb can be used:

- Select L_p equal 1/10 * L_{BO} = 3.3 µH
- Put the corner frequency of PI filter 1/10 of the switching frequency of DC/DC than f_{PI} = 0.1 * f_{SW} = 40 kHz
- Have equal capacitance distribution on both sides of PI-Filter and value

$$C_P = \frac{1}{4 \cdot \pi^2 \cdot L_P \cdot f_P^2} = \frac{1}{4 \cdot \pi^2 \cdot 3.3\ \mu H \cdot (40\ kHz)^2} = 4.8\ \mu F$$

Then, for each side of PI filter at least 4.8 µF is needed; a possible choice is to have 2 capacitor of 3.3 µF (due to reduction of value at nominal battery value) that minimize parasitic effects.

For this purpose CGA5L3X7R1H475K160AB is a good candidate for the capacitors while the inductor could be SPM4015T-3R3M-LR.

2.4 Transistor selection

NMOS type device is used as switching element of the proposed DC/DC. The switching behavior is depicted in the Figure 7.

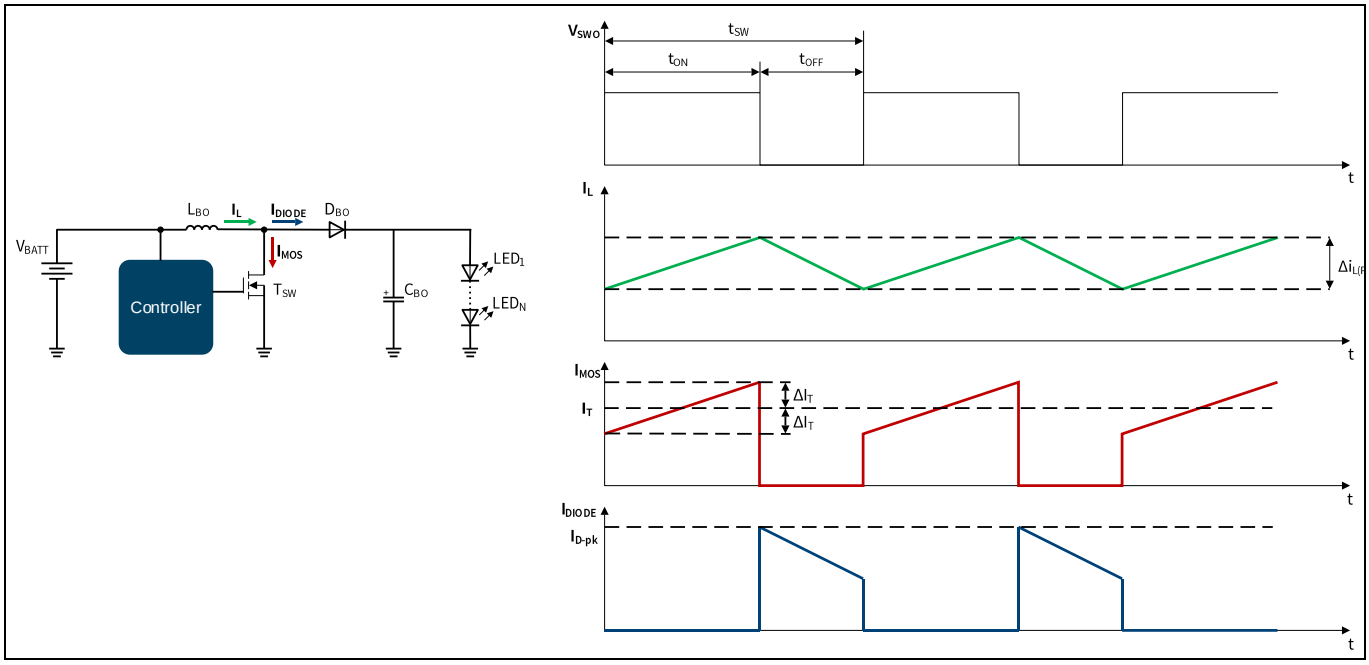


Figure 7 Waveform of current in power devices and inductor

With this shape, the RMS value of the current that flows into the transistor can be calculated as:

$$I_{T\_rms} = \sqrt[2]{\frac{1}{T}\int_0^T i_{MOS}(t)^2 dt} = \sqrt[2]{\frac{1}{T}\int_0^T \left(\frac{(I_T + \Delta I_T - I_T + \Delta I_T)\cdot t}{T_{ON}} + (I_T - \Delta I_T)\right)^2 dt}$$

$$= \sqrt{\frac{T_{ON}}{3T}\left(I_{MOS\_min}^2 + I_{MOS\_min}\cdot I_{MOS\_max} + I_{MOS\_max}^2\right)}$$

$$= \sqrt{\frac{D}{3}\left(I_{MOS\_min}^2 + I_{MOS\_min}\cdot I_{MOS\_max} + I_{MOS\_max}^2\right)}$$

Considering the current flowing into the MOSFET during the ON state is the same of the inductor current, the equation above has a maximum when V_{IN} is minimal (it means also duty cycle is maximum) and it can be calculated as:

$$I_{T\_rms,max}\sqrt{\frac{D_{MAX}}{3}\left(\left(I_{L-MAX} - \Delta i_{L(P-P)}\right)^2 + \left(I_{L-MAX} - \Delta i_{L(P-P)}\right)\cdot I_{L-MAX} + I_{L-MAX}^2\right)}$$

$$= \sqrt{\frac{0.79}{3}\left((2.14\,A - 0.48\,A)^2 + (2.14\,A - 0.48\,A)\cdot 2.14\,A + (2.14\,A)^2\right)} = 1.69\,A$$

Moreover, during the switching, it is stressed by the voltage equal to output voltage (voltage drop on diode is not take into account).

For EMI reason, it is common practice to put in series an R_{gate} resistor of approximately 10 to 20 Ω. This helps in reducing the current spikes into the gate and also having smooth transition from the OFF state to ON state. On the other hand, this lowers the overall efficiency of the converter.

Infineon offers a wide variety of MOSFET suitable for this purpose; IPD25N06S4L-30 is a good compromise of gate charge and R_{ds_on}.

2.5 Diode selection

The diode is the rectification device of the DC/DC. The current that flows into the device is depicted in blue in Figure 7 and it has a trapezoidal waveform as the current into the transistor and a similar equation can be used. Changing the limits in the integral on the equation of transistor current, the current into the diode can be described by the following equation.

$$I_{D\_rms,max} = \sqrt{\frac{T_{OFF}}{3T}\left(\left(I_{L-MAX} - \Delta i_{L(P-P)}\right)^2 + \left(I_{L-MAX} - \Delta i_{L(P-P)}\right) \cdot I_{L-MAX} + I_{L-MAX}^2\right)}$$
$$= \sqrt{\frac{0.21}{3}\left((2.14\ A - 0.48\ A)^2 + (2.14\ A - 0.48\ A) \cdot 2.14\ A + (2.14\ A)^2\right)} = 0.87\ A$$

During the ON state of the transistor, the voltage across the diode is V_{OUT} = 39.0 V (voltage drop on the transistor and sensing resistor is not take into account). To take same margin, 60 V Schottky diode has to be selected.

A good choice for this kind application could be the Vishay VSS8D2M6 that provides quite low forward voltage.

2.6 Current sense resistors selection

There are still few components that are needed to be chosen for a proper behavior of the main regulation loop. Two of these are resistors needed to sense the current into the switching transistor, and the output current.

The first resistor limits the current into the switching NMOS and inductor; it is placed below the transistor (refer to Figure 8) and it is useful for better control of the current at output (current mode control loop). This resistor converts the current flowing into the transistor in a voltage sensed by SWCS pin. The maximum voltage across the resistor must not reach the V_{SWCS} threshold of 150 mV. This has to be true not only during the steady state but also during the transition phase.

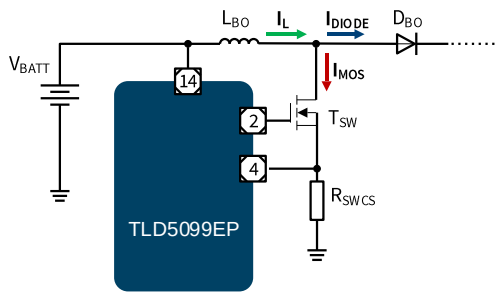


Figure 8 Peak current sensing resistor

For example, if the system has a phase margin of 46° (the minimum bandwidth for a stable system), the output has an overshoot about 50%; this means you can see the same effect also on the inductor current and switching current too. Taking into account the corner case with lower V_{IN}, the maximum current in the R_{SWCS} can be calculated, and then the resistor has to be lower than

$$R_{SWCS} < \frac{V_{SWCS}}{1.5 \cdot I_{L-MAX}} = \frac{150\ mV}{1.5 \cdot 2.14\ A} = 47\ m\Omega$$

On other hand, this resistor is also involved in stability of current control loop. To achieve a good behavior slope of the inductor current (sensed by resistor R_{SWCS}) must not to be too high in respect of internal reference.

To take a margin, 22 mΩ is a good choice (this choice influences also the stability of DC/DC, that is evaluated in Chapter 3).The RMS current that flows into the resistor is equal to the current flowing into power NMOS, then the power dissipated by the resistor is

$$P = R_{SWCS} \cdot I_{NMOS}^2 = 22\ m\Omega \cdot (1.69\ A)^2 = 62.8\ mW$$

To avoid overheating of the resistor it is a common practice to use resistors with 4-5 times power rating needed; for this application low inductive component has to be chosen, and the RCWL2010R022JQ from Vishay satisfies the requirements.

The second component involved into the regulation loop is the output current sensor (please refer to Figure 9). It can be easily calculated by the imposing the feedback voltage V_{REF} regulated by the device with the required output current.

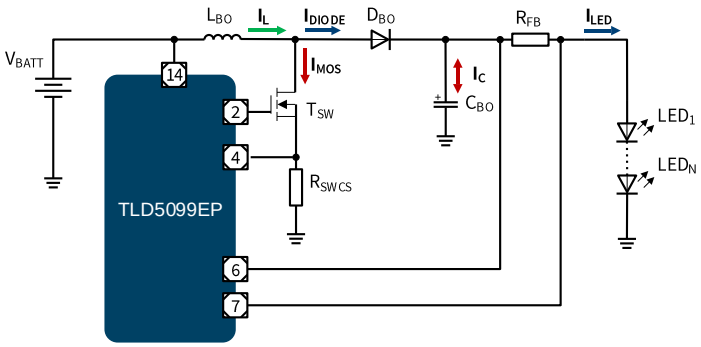


Figure 9 Output current sensing resistor

For this application, without analog dimming, the resistor can be calculated as follow:

$$R_{FB} = \frac{V_{REF}}{I_{OUT}} = \frac{0.3\ V}{0.35\ mA} = 0.857\ \Omega$$

This value is not available in the standard E24 series; the lower closest value in this series is 0.82 Ω;

With this value, the settled current is

$$I_{OUT} = \frac{V_{REF}}{R_{FB}} = \frac{0.3\ V}{0.82\ \Omega} = 365\ mA$$

This is higher than required, the output current has to be trimmed by analog dimming (the solution will be presented into Chapter 3)

The power rating of this device can be calculated as

$$P = R_{FB} \cdot I_{OUT}^2 = 0.82\ \Omega \cdot (0.35\ A)^2 = 0.1\ W$$

To avoid overheating of the resistor it is a common practice to use resistors with 4-5 times power rating needed; for this application RCWL2010R820JQ from Vishay is a good candidate.

3 Features design

TLD5099EP embeds many features to help the designer to realize a fully working system without the use of a microcontroller or lowering the complexity of the software/firmware (if microcontroller is used).

3.1 Embedded PWM engine

Embedded PWM engine is the feature that is common used to dim the daytime running light (DRL) from full power down to a position light (example 10% of full power) when low beam or high beam is activated. The frequency of PWM can be adjusted by using a capacitor, while the duty cycle is adjusted by a voltage divider from IVCC. The schematic to enable is feature is proposed on Figure 10.

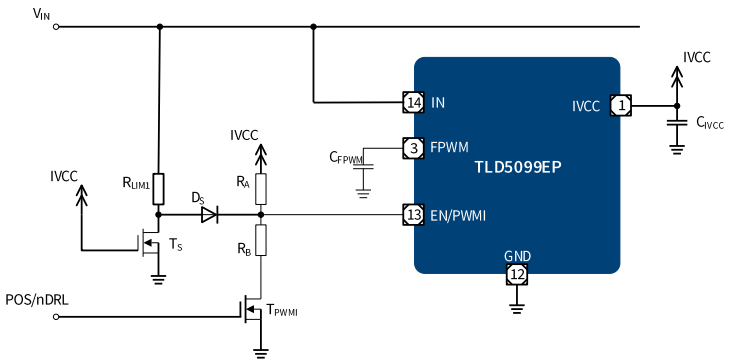


Figure 10 Embedded PWM engine schematic

From application assumption in Chapter 1.1, the capacitor C_{FPWM} has to be 560 pF to impose 400 Hz PWM signal when required (have a look at Table 10 of datasheet), while having 10% of DC, two resistors R_A and R_B are selected by following the formula 7.4 of the datasheet. The change on light function is performed by changing the voltage on the gate of T_{PWMI}. This transistor is a small signal NMOS and IRLML0100TRPBF-1 is a good candidate to be used ad T_S and T_{PWMI} too.

As reported into the datasheet of TLD5099EP, the device needs a startup circuit if embedded PWM engine is used. Purpose of startup circuit is to correctly bias the enable pin EN/PWMI when battery voltage is applied to the device. Following the steps reported in the datasheet, R_{LIM1} is fixed at 10 kΩ and R_B is calculated by the following formula:

$$R_B > \frac{V_{EN/PWMI,ON}}{(V_{IN\_MIN} - V_{D1} - V_{EN/PWMI,ON})} = \frac{3\ V}{(8\ V - 0.7\ V - 3\ V)} = 6.98\ k\Omega$$

To fix the value of duty cycle at 10%, the voltage on EN/PWMI pin has to be equal to

$$V_{EN/PWMI} = \frac{DC[\%] \cdot 0.24 \cdot V_{IVCC}}{100} + 0.32 \cdot V_{IVCC} = \frac{10 \cdot 0.24 \cdot 5\ V}{100} + 0.32 \cdot 5\ V = 1.72\ V$$

The current on RB that fix VEN/PWMI to 1.72 V is 246 µA and then the value of RA can be calculated as:

$$R_A = \frac{V_{IVCC} - V_{EN/PWMI}}{I_{R_B}} = \frac{5\ V - 1.72\ V}{246\ \mu A} = 13.3\ k\Omega$$

3.2 Dimming

TLD5099 has a dedicated gate driver for a NMOS transistor to support current PWM dimming at output. This gate driver is addressed with digital signal on EN/PWMI pin or with the PWM engine.

The NMOS connected to PWMO pin can be used to open the LED string on negative side or to enable a high side PMOS transistor as depicted on Figure 11. The level shifter (needed for properly biasing the PMOS) is made up with the transistor T_{DIM1}, the resistors R_{DIM1} and R_{DIM2} bias the gate of transistor T_{DIM2} while the 10 V Zener diode protects the gate of PMOS.

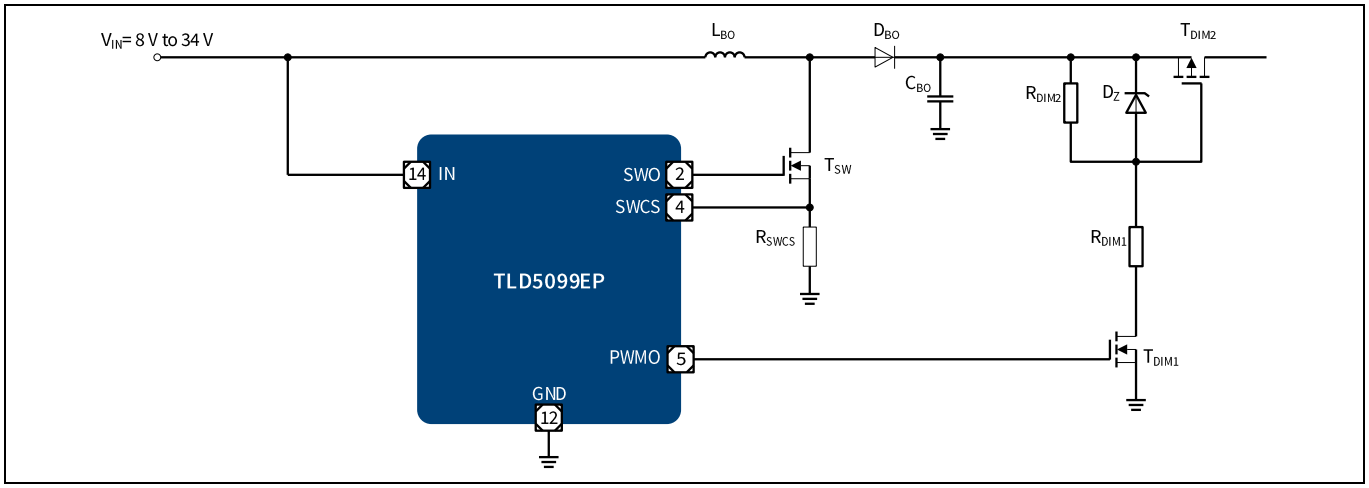


Figure 11 Dimming PMOS setup

T_{DIM2} manages the load current then the rating current of transistor is 350 mA, while when the transistor is in open state, its V_{GS} can reach 60 V. An Infineon component suitable for this application is BSO615CG; this device has in the same package a PMOS and a NMOS can be used as T_{DIM1}.

The threshold voltage of PMOS is 2V, but to have a low resistance a gate to source voltage of 10V can be applied. Fixing the current on the NMOS to 1 mA, R_{DIM2} can easily calculate as ratio between the desired V_{GS} of PMOS transistor and the current

$$R_{DIM2} = \frac{V_{GS-PMOS}}{I_R} = \frac{10\ V}{1\ mA} = 10\ k\Omega$$

While R_{DIM1} can be calculated as follows:

$$R_{DIM1} = \frac{V_{OUT\_min} - V_{GS-PMOS}}{I_R} = \frac{31.2\ V - 10\ V}{1\ mA} = 21.2\ k\Omega$$

The closest value on E24 series is 22 kΩ.

3.3 Spread Spectrum

The spread spectrum modulator helps the designer to solve the EMI issues by moving the power from the narrow peaks of the spectrum into a broad band signal. It is easily activated by selecting the correct resistor set.

To switch at 400 kHz with spread spectrum activated, a resistor can be selected by equation:

$$R_{FREQ-SSMon} = \frac{1}{(600 \cdot 10^{-12} \cdot f_{FREQ})^{0.943}} - 600 = \frac{1}{(600 \cdot 10^{-12} \cdot 400\ kHz)^{0.943}} - 600 = 1.99\ k\Omega$$

Than 2.0 kΩ (E96 series) has to be selected and connected between pin 11 and ground.

3.4 Analog dimming

LED string need accurate output current to produce the total amount of light required by the application. The output current is defined by a resistor placed between FBH and FBL pins. Due to the E24 series has a limited number of values, it is impossible to set every output current conditions. By means of the 0.82 Ω resistor, the DC/DC should drive out 366 mA instead 350 mA, this means the system needs 95.6% of dimming and the reference voltage will be set to 300 mV * 0.956 = 287 mV.

By using the formula in the datasheet, it is possible to calculate the correct value to put at SET pin

$$V_{SET} = 5 \cdot R_{FB} \cdot I_{OUT} + 0.1\ V = 5 \cdot 0.82\ \Omega \cdot 0.35\ mA + 0.1\ V = 1.535\ V$$

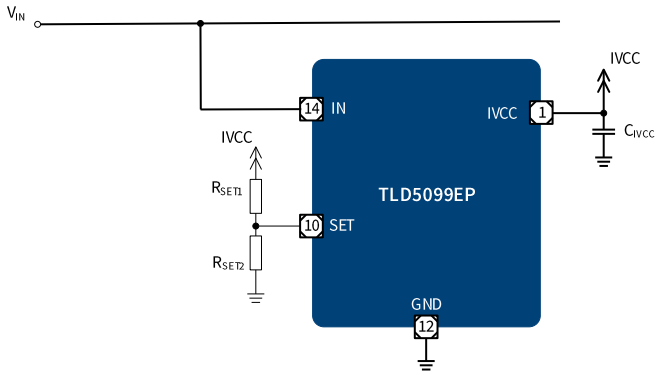


Figure 12 Analog dimming schematic

This voltage on the SET pin can be realized by means a voltage divider from IVCC. Imposing the maximum current consumption from IVCC of 1 mA, it easy to calculate R_{SET2} 1.54 kΩ, while R_{SET1} can be calculated as

$$R_{REST1} = \frac{V_{IVCC} - V_{SET}}{1\ mA} = \frac{5\ V - 1.535\ V}{1\ mA} = 3.465\ k\Omega$$

The closest commercial value in E96 series is 3.48 kΩ.

3.5 Overvoltage protection

This feature helps to avoid too high voltage during open fails of the load (for example if the load is disconnected). This voltage has to be set higher than the maximum voltage of the load; 48 V is a good value to take into account also spread variations.

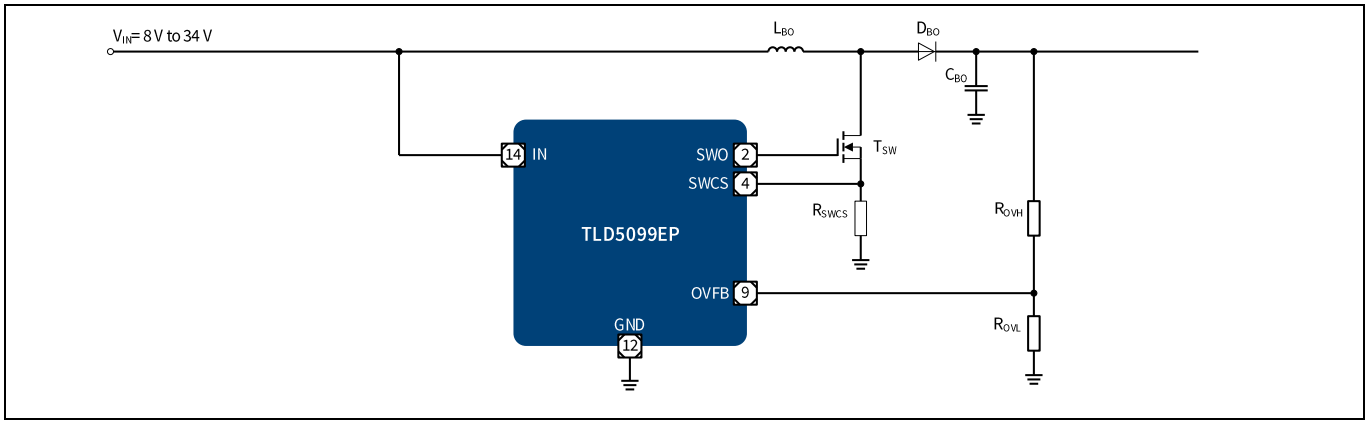


Figure 13 Overvoltage protection schematic

Overvoltage is triggered when the voltage on OVFB pin reaches 1.25 V. Fixing R_{OVL} at 1 kΩ, this threshold is reached when the current on R_{OVH} and R_{OVL} is 1.25 mA; then, R_{OVH} can be calculated as:

$$R_{OVH} = \frac{V_{OUT\_MAX} - V_{OVFB,TH}}{I_{R-OVFB}} = \frac{48\ V - 1.25\ V}{1.25\ mA} = 37.4\ k\Omega$$

This value is present on E96 series.

4 Compensation network

The TLD5099EP has a dedicated pin where a compensation network can be applied. It is possible to apply a proportional and integral (PI) compensation or only integral compensation.

As well known, in small signal approximation, the open loop transfer function of a DC/DC is the product of modulator transfer function and the feedback network transfer function.

The modulator transfer function can be expressed as product of two main parts: the gain of the error amplifier and the gain of the current mode modulator.

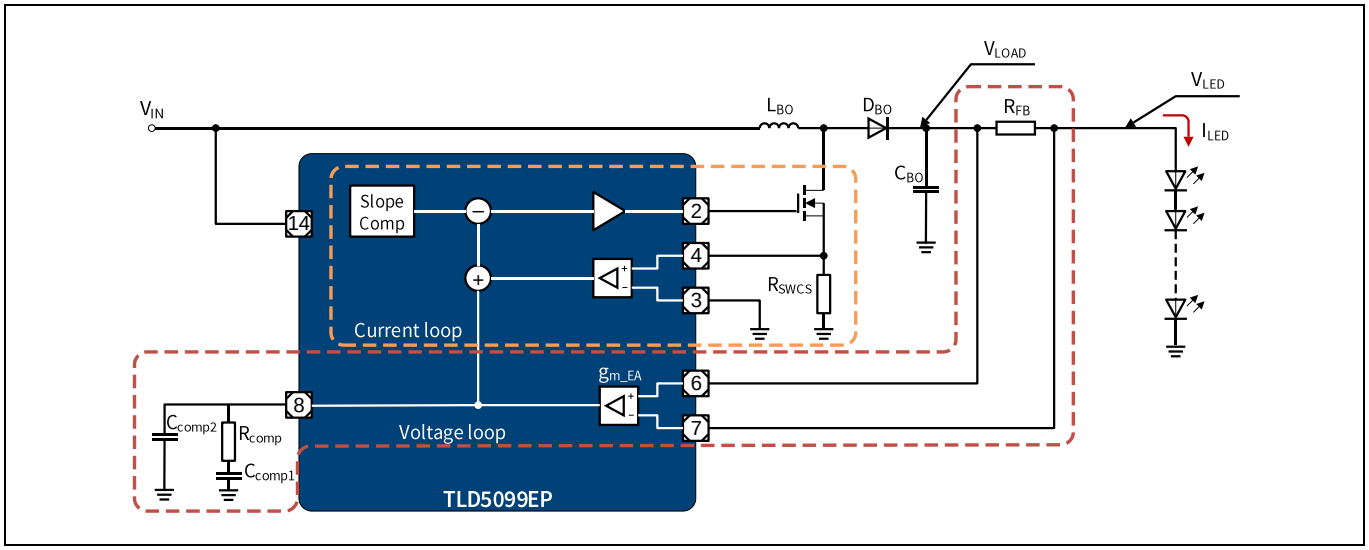


Figure 14 Compensation network schematic

The gain of the error amplifier can de described with the following formula:

$$A_{EA}(s) = g_{m\_EA} \cdot R_{EA} \cdot \frac{(1 + s \cdot \tau_{z1})}{(1 + s \cdot \tau_{p1}) \cdot (1 + s \cdot \tau_{p2})}$$

Where

- g_{m_EA} is the trans-conductance of the error amplifier (typical 600 µS)
- R_{EA} is the output resistance of the error amplifier (typical 2.5 MΩ)
- $\tau_{z1} = C_{comp1} \cdot R_{comp}$ is the zero of compensation network
- $\tau_{p1} = (C_{comp1} + C_{comp2}) \cdot R_{EA}$ is the pole associated to compensation network and the resistor of error amplifier
- $\tau_{p2} = C_{comp2} \cdot R_{comp}$ is a pole associated to compensation network

The gain of the current mode modulator can be described following the model presented by R.B Ridley (*Reference: Ridley, R. B.; "A new Continuous Time Model for Current Mode Control"; IEEE Transaction on Power Electronics; Vol. 6; Issue 2; pp. 271-280; 1991*). It can be mathematically described as:

$$A_{CM}(s) = \frac{0.2 \cdot (1 - D) \cdot R_{load}}{\left(1 + \frac{V_{ref}}{V_{LOAD} + V_{ref}}\right) \cdot R_{swcs}} \cdot \frac{(1 + s \cdot \tau_{z2})}{(1 + s \cdot \tau_{p3}) \cdot \left(1 + \frac{s}{\omega_n \cdot Q} + \frac{s^2}{\omega_n^2}\right)}$$

Where:

- R_{load} is the total resistor at the output of DC/DC and it is the sum of R_{FB} and R_{LED}
- V_{REF} is the voltage reference and it is modulated by the voltage on SET pin; in this application, with V_{SET} = 1,565 V it is 0.287 V
- V_{LOAD} is the voltage on LED string (Voltage across PMOS has been neglected) plus V_{REF}
- $\tau_{z2} = -\frac{L_{BO}}{(1-D)^2} \cdot \frac{(I_{OUT})}{(V_{LOAD}+V_{ref})}$ is the zero (RHP) of the boost DC/DC
- $\tau_{p3} = \frac{C_{OUT} \cdot R_{LED}}{1+\frac{V_{ref}}{V_{LOAD}+V_{ref}}}$ is the pole associated to boost converter
- ω_n is the natural pulsation of the system
- $Q = \frac{1}{\pi \cdot \left(\left(1+\frac{S_e}{S_n}\right) \cdot (1-D) - 0.5\right)}$ is the quality factor of a second order system, where:
  - $S_e = 50 \cdot 10^{-6} \cdot f_{sw}$ is the slope of integrated current compensation circuit (fixed by internal references)
  - $S_n = \frac{V_{in} \cdot R_{SWCS}}{L_{BO}} \cdot 10^{-3}$ is the slope of the current sensed by R_{swcs}.

Using the data previously calculated, it is possible calculate the gain in DC and cross over frequency f_c and the phase margin.

The transfer function of the feedback network is the ratio between R_{FB} and the R_{LED}

$$\beta = \frac{R_{FB}}{R_{LED} + R_{FB}}$$

For the gain calculation in typical conditions, the three part to be calculated are:

$$A_{EA}(0) = g_{m\_EA} \cdot R_{EA} = 600\ \mu S \cdot 2.5\ M\Omega = 1500$$

$$A_{CM}(0) = \frac{0.2 \cdot (1-D) \cdot R_{load}}{\left(1 + \frac{V_{ref}}{V_{LOAD}+V_{ref}}\right) \cdot R_{SWCS}} = \frac{0.2 \cdot (1-0.65) \cdot 12.82\ \Omega}{\left(1 + \frac{0.287\ V}{39.0\ V + 0.287\ V}\right) \cdot 0.022\ \Omega} = 40.16$$

$$\beta = \frac{R_{FB}}{R_{LED}} = \frac{0.82\ \Omega}{12\ \Omega + 0.82\ \Omega} = 0.064$$

And then the gain in DC can be calculated as:

$$T(0)|_{dB} = 20 \cdot \log(A_{EA}(0) \cdot A_{CM}(0) \cdot \beta) = 20 \cdot \log(1500 \cdot 40.16 \cdot 0.064) = 71.72\ dB$$

Using just a proportional and integrative compensation with R_{comp} = 6600 kΩ and C_{comp} = 22 nF, the constant time elements are:

$$\tau_{p1} = \left(C_{comp1} + C_{comp2}\right) \cdot R_{EA} = (22\ nF + 0) \cdot 2.5\ M\Omega = \ 0.055\ s$$

$$\tau_{p2} = C_{comp2} \cdot R_{comp} = 0\ F \cdot 6600\ \Omega = 0\ s$$

$$\tau_{p3} = \frac{C_{OUT} \cdot R_{LED}}{1 + \frac{V_{ref}}{V_{LOAD} + V_{ref}}} = \frac{13.16\,\mu F \cdot 12\,\Omega}{1 + \frac{0.287\,V}{39.0\,V + 0.287\,V}} = 156.77 \cdot 10^{-6}\,s$$

$$\tau_{z1} = C_{comp1} \cdot R_{comp} = 22\,nF \cdot 6600\,\Omega = 145.2 \cdot 10^{-6}\,s$$

$$\tau_{z2} = -\frac{L_{BO}}{(1-D)^2} \cdot \frac{(I_{OUT})}{(V_{LOAD} + V_{ref})} = -\frac{33\,\mu H}{(1-0.65)^2} \cdot \frac{0.35\,A}{39.0\,V + 0.287\,V} = -2.40 \cdot 10^{-6}\,s$$

$$\omega_n = \pi \cdot \frac{f_{sw}}{2} = 628 \cdot 10^3\ rad/s$$

$$Q = \frac{1}{\pi \cdot \left(\left(1 + \frac{S_e}{S_n}\right) \cdot (1-D) - 0.5\right)} = \frac{1}{\pi \cdot \left(\left(1 + \frac{50\mu \cdot 400\,kHz}{0.001 \cdot \frac{13.5\,V}{33\,\mu H} \cdot 0.022\,\Omega}\right) \cdot (1-0.65) - 0.5\right)} = 0.51$$

For stability reasons, quality factor Q has to be lower than 1. If Q is too high, it is necessary to increase the value of inductor or/and increase the switching frequency and/or reduce R_{SWCS}.

By using a mathematical analysis tool, it is possible to extract the cutoff frequency and phase margin of the system.

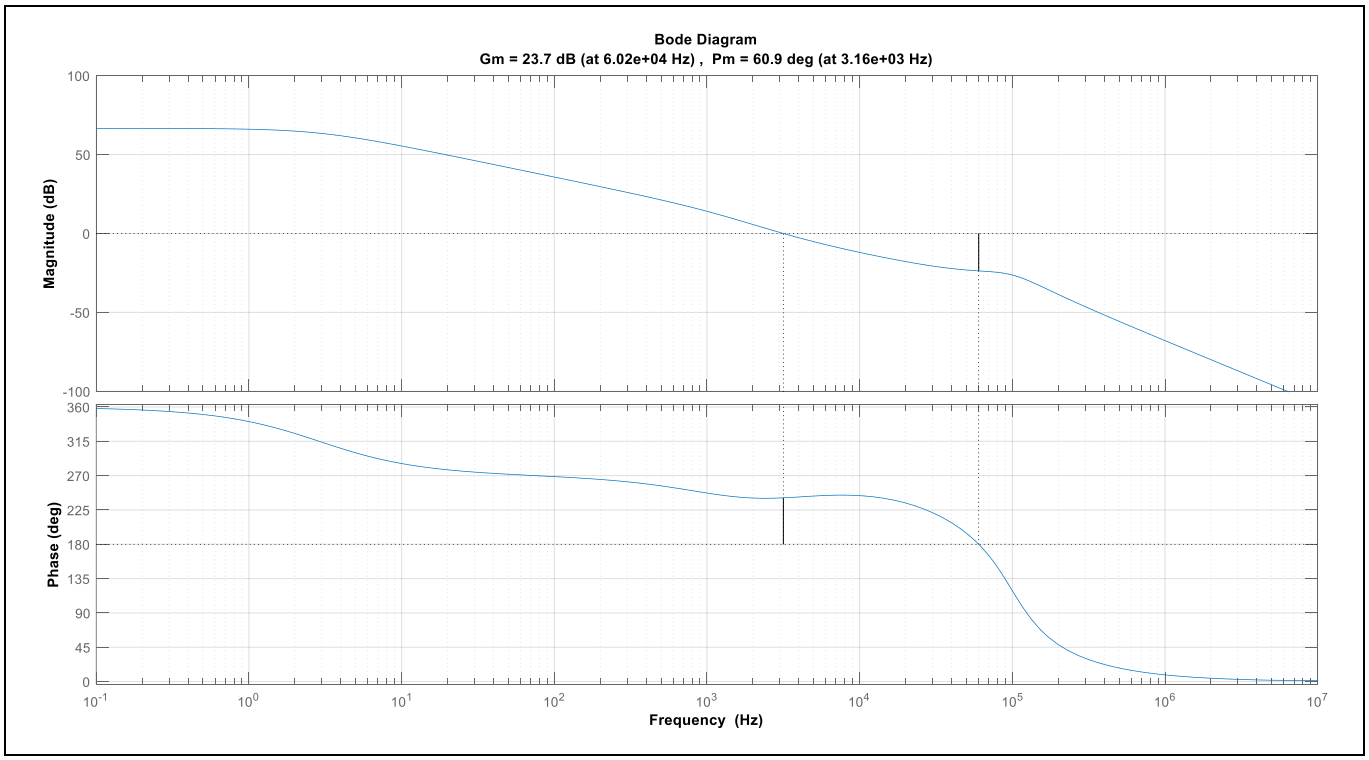


Figure 15 Cutoff frequency and phase margin calculated

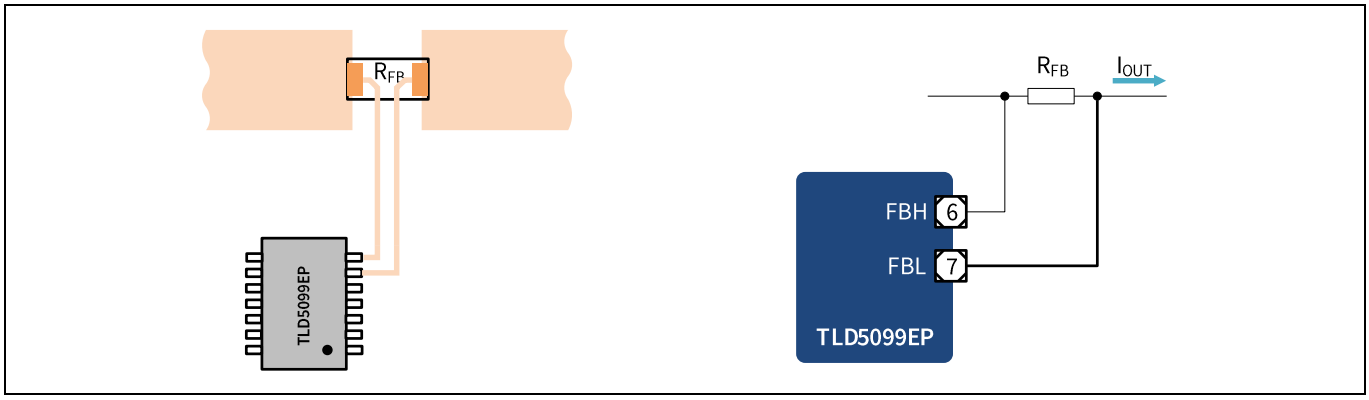
As a rule of thumb, τ_{p1} is the dominant pole and changing the value of C_{comp1} it is possible to tailor the bandwidth of the system. The zero produced by C_{comp1} and R_{comp} is needed to compensate the pole τ_{p3}. If needed, C_{comp2} can be used to reduce the secondary order effects.

Infineon can also provide SPICE models of the device to perform electrical simulation to double check performances.

5 Layout considerations

For a DC/DC converter, PCB design is a critical task as the component selection. Even if the circuit topology and components selection are reasonable, if the PCB layout is not good enough, the performances of the whole system will be lower than expected. Due to parasitic (capacitance and inductance) and coupling between traces, high ripple and poor regulation could appear. Even EMC problems can be mitigated with a proper layout.

The regulation is directly related on the voltage across FBH and FBL pins. To avoid poor regulation use a Kevin connection (4 wires measure approach) from the sensing resistor (R_{FB}) to TLD5099EP; if possible, route these traces as a differential pair and avoid coupling with noisy lines.

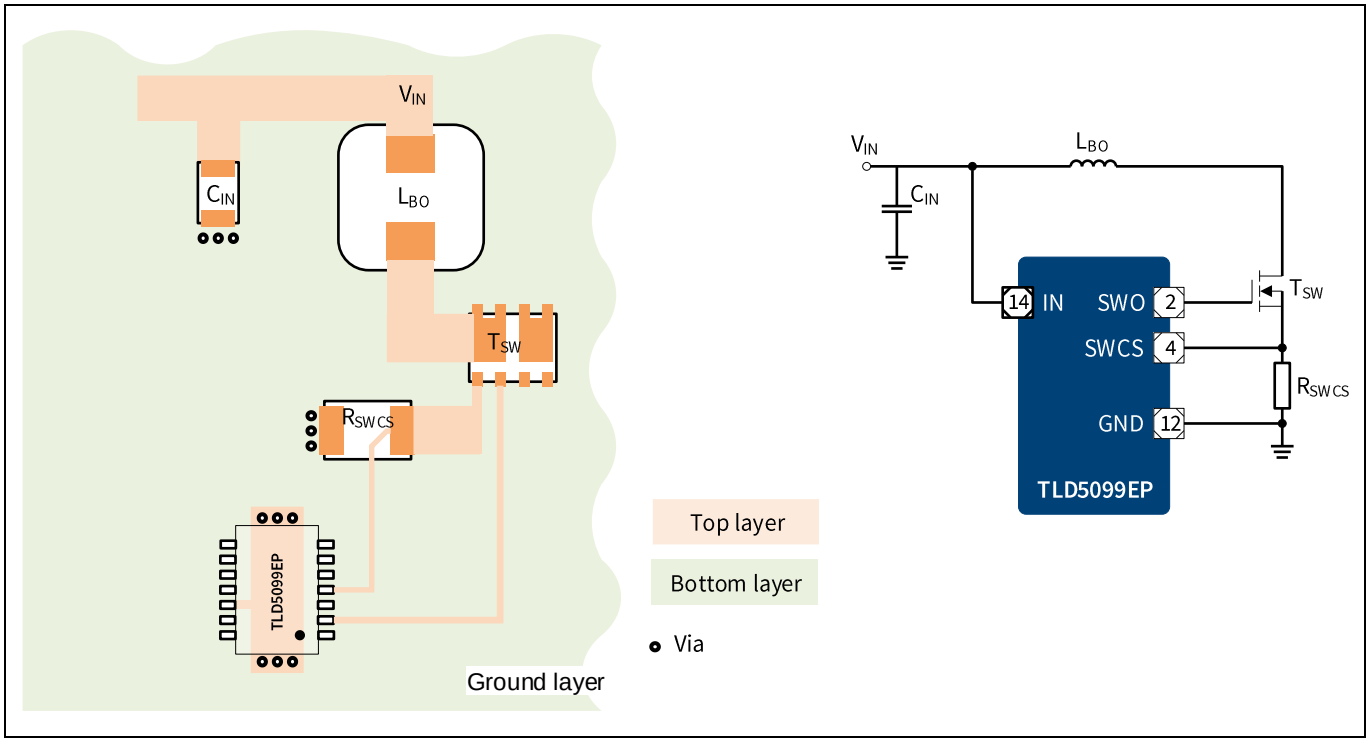


Path of high impedance pins has to be as short as possible or shielded by ground plane. High impedance pins sensitive to the noise are:

- FPWM
- FBH and FBL
- OVP

The exposed pad aids to dissipate the power through the PCB. Adding several vias under the device to connect the bottom of the package to bottom layer improves the thermal resistance. The diameter of the vias has to be carefully selected with the PCB manufacturer: holes too big suck the tin paste during the welding process and produce voids under the device, lowering the expected thermal performances; holes too small are not completely filled during welding process, lowering also in this case the expected thermal performances.

A good grounding of the device and of current loop sensing resistor (R_{SWCW}) helps to reduce the noise on the references and improves the regulation and the stability performances. A good grounding means having very low ohmic path (also at high frequency) between the GND pin of the TLD5099EP and the returning pad of R_{SWCW}.



Discontinuous currents are critical for the generation of electromagnetic interference. Particular attention has to be paid when routing these paths. Inductor, switching transistor and rectifier diode has to be placed as close as possible. This junction node (also called switching node) has to be just large enough to connect the devices; this acts as a plate of capacitor and radiates interferences at high frequency, lowering the EMC performance. A possible layout solution with switching transistor in TDSON-8 package is proposed in Figure 16

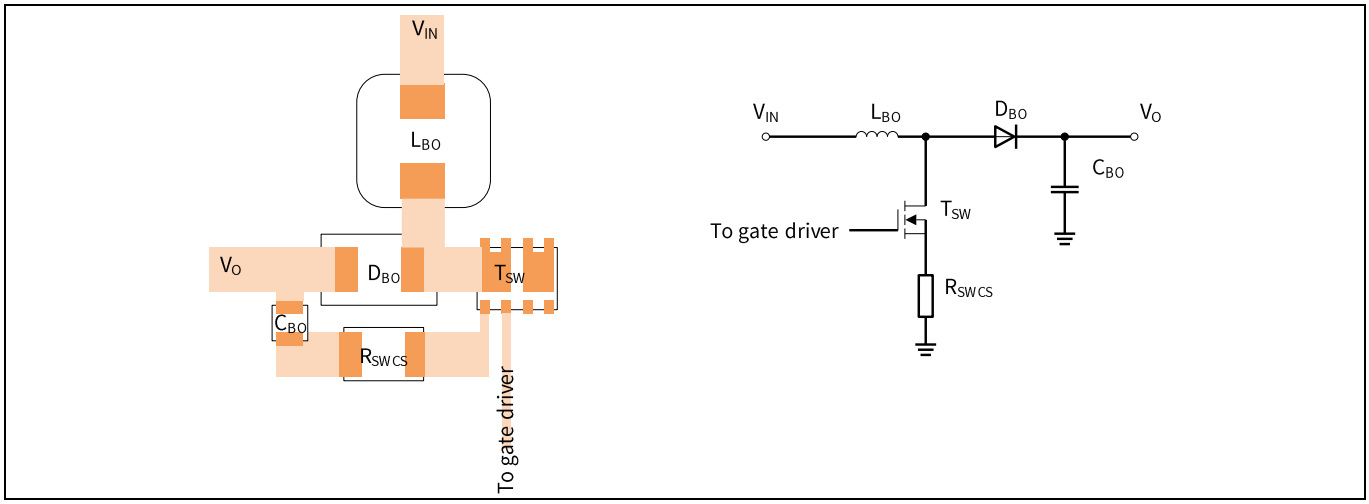


Figure 16 Possible layout solution with transistor in TSDON-8

All traces with unstable current have to be as short as possible.

Revision history

Major changes since the last revision

Page or Reference	Description of change
2019-12-18	Initial release

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